

[Notes]

R20TS0656EJ0100

Rev.1.00

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## e<sup>2</sup> studio Code Generator Plug-in and AP4 Coding Assistance Tool for RZ

### Overview

When using any of the products in the title, note the following point.

- Notes on counter clear setting for multi-function timer pulse unit 3 in complementary PWM mode

### 1. Notes on counter clear setting for multi-function timer pulse unit 3 in complementary PWM mode

#### 1.1 Applicable Products

e<sup>2</sup> studio V4.0.0.26 (V2.0.0 and later versions of the Code Generator Plug-in)

V1.00.00 and later versions of the AP4 coding assistance tool for RZ

#### 1.2 Applicable MCUs

RZ family: RZ/T1 group

#### 1.3 Description

Counter clear control for multi-function timer pulse unit 3 in complementary PWM mode has an error. If [Counter clear on another channel performing synchronous operation] is set, a malfunction occurs after the first synchronous clearing.

#### 1.4 Conditions

The problem arises when settings (1) and (2) are used.

- In the [General Setting] tab for multi-function timer pulse unit 3, [MTU3] or [MTU6] is set to complementary PWM mode.

MTU3	Complementary PWM mode 1
MTU4	Unused
MTU5	Unused
MTU6	Complementary PWM mode 1

- In the [MTU3] tab or [MTU6] tab for multi-function timer pulse unit 3, the following are set:

- Under [Synchronous mode setting], the [Include this channel in the synchronous operation] check box is selected.
- Under [TCNT3(or 6) counter setting], [Counter clear source] is set to [Counter clear on another channel performing synchronous operation].

The screenshot shows a configuration window for MTU3 with the following sections:

- Synchronous mode setting**: A checkbox labeled "Include this channel in the synchronous operation" is checked and circled in red.
- Count source setting**: A dropdown menu for "Counter clock selection" is set to "PCLK".
- Clock edge setting**: Three radio buttons are present: "Rising edge" (selected), "Falling edge", and "Both edges".
- TCNT3 counter setting**: A dropdown menu for "Counter clear source" is set to "Counter clear on another channel performing synchronous operation" and is circled in red.

## 1.5 Workaround

Add a code to specify synchronous clearing to the CCLR[2:0] bit of the timer control register (TCR) for MTU4<sup>\*1</sup> and MTU7<sup>\*2</sup> in the generated code (r\_cg\_mtu3.c), as shown below.

This modification is required every time code is generated.

\*1: When MTU3 is used

\*2: When MTU6 is used

- Function in the source file r\_cg\_mtu3.c: R\_MTU3\_Create(void)

Before modification

```

/*****
* Function Name: R_MTU3_Create
* Description  : This function initializes the MTU3 Unit0 module.
* Arguments    : None
* Return Value : None
*****/
void R_MTU3_Create(void)
{
    Omitted

    MTU3.TCR.BYTE = _MTU_PCLK_1 | _MTU_CKCL_SYN;
    MTU4.TCR.BYTE = _MTU_PCLK_1;

    Omitted

    MTU6.TCR.BYTE = _MTU_PCLK_1 | _MTU_CKCL_SYN;
    MTU7.TCR.BYTE = _MTU_PCLK_1;
}

```

#### After modification

```

/*****
* Function Name: R_MTU3_Create
* Description  : This function initializes the MTU3 Unit0 module.
* Arguments    : None
* Return Value : None
*****/
void R_MTU3_Create(void)
{
    Omitted

    MTU3.TCR.BYTE = _MTU_PCLK_1 | _MTU_CKCL_SYN;
    MTU4.TCR.BYTE = _MTU_PCLK_1 | _MTU_CKCL_SYN;
                                     Add

    Omitted

    MTU6.TCR.BYTE = _MTU_PCLK_1 | _MTU_CKCL_SYN;
    MTU7.TCR.BYTE = _MTU_PCLK_1 | _MTU_CKCL_SYN;
                                     Add

```

### 1.6 Permanent Measure

This problem will be fixed in the next version.

## Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Feb.16.21	-	First edition issued

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