To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

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GRADE A

RENESAS TECHNICAL NEWS

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Precautions Regarding the PWM Output Disable Function in the 32172 and 32173 Groups

Classification	Concerned Products
Corrections and supplementary explanation of document √ Notes Knowhow Others	32172 and 32173 groups

Content

If all of the conditions described below are met when the TOM output pin is set as a general-purpose port, one of the following register bits may inadvertently be cleared to 0:

- PWMOFF1S (Selects port P100-P105 output disable) bit in the PWM Output Disable Register 1 (PWMOFF1)
- PWMOFF0S (Selects port P110-P115 output disable) bit in the PWM Output Disable Register 0 (PWMOFF0)

(These bits basically are designed to be cleared by only writing a 0 in software.)

Occurrence conditions

The above problem occurs when all of the following conditions are met:

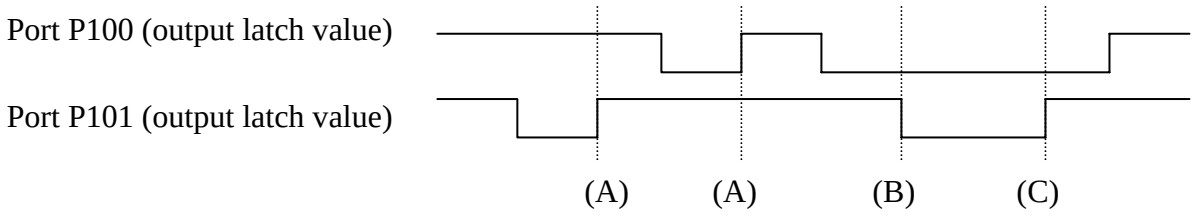
- The TOM output pin is set as a general-purpose port.[Note 1]
- The PLVDISx (Invalidates/validates output disable selection) bits in the respective control registers are set to 1 (output disable selection validated):
  - PLVDIS1 bit in the PWM Output Disable Control Register 1 (PLVCNT1)
  - PLVDIS0 bit in the PWM Output Disable Control Register 0 (PLVCNT0)
- The output latch levels on ports P100–P105 and P110–P115 change in state simultaneously from where the PWM output disable condition is met to where it is not or vice versa.[Note 2]

Note 1: This also applies when either one of the control pins that disable PWM output is set for use as a general-purpose port. (For example, port P100 is used as timer output TO8 and port P101 as a general-purpose port.)

Note 2: For example, this applies to the case where the output latch level on port P100 and that on port P101 simultaneously change from high to low and low to high respectively.

Note: The pin level-triggered PWM output disable function is controlled by the output latch level on each port. Therefore, even while the port is being used in input mode, the above phenomenon may occur depending on the value written to the port data register.

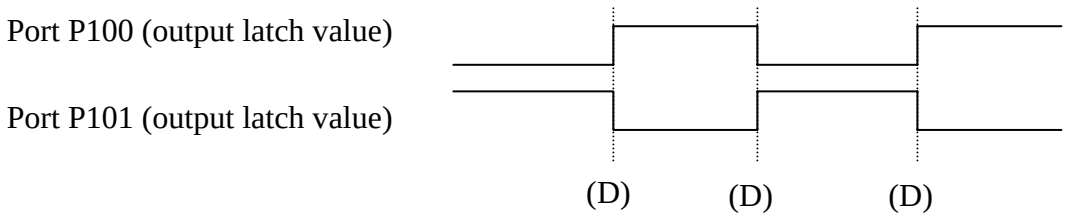
Example: When PWM output is disabled on condition that ports P100 and P101 are detected low at the same time.



(A): The anticipated phenomenon does not occur because the PWM output disable condition is not met.

(B): The PWMOFF1S (Selects port P100-P105 output disable) bit is set to 1 because the PWM output disable condition is met.

(C): The PWMOFF1S (Selects port P100-P105 output disable) bit may inadvertently be cleared to 0 by a change of states from where the PWM output disable condition is met to where it is not.



(D): The PWM output disable condition happens to be met due to a difference in output timing delays, causing the anticipated phenomenon to occur.

Countermeasures

- When using the pin level-triggered PWM output disable function, be sure to use the TOM output for control.
- When the TOM output pin is used as a general-purpose port and the PLVDISx (Invalidates/ validates output disable selection)bit has output disable validated, make sure to forbid the output latch levels on ports P100–P105 or P110–P115 to change in state from where the PWM output disable condition is met to where it is not. Or, if allowing such a change, check the status of the PWMOFFxS (Selects port P100–P105 or P110–P115 output disable) bit in software.