Date: May 30, 2022

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A0073A/E	Rev.	1.00
Title	S5D5 MCU Group, S5D9 MCU Group, S7G2 MCU Group, correction of EXENB bit in the CSnCR register		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S5D5 MCU Group Renesas Synergy™ S5D9 MCU Group Renesas Synergy™ S7G2 MCU Group	Lot No. All	Reference Document	S5D5 Microcontroller Group User's Manual Rev.1.30 S5D9 Microcontroller Group User's Manual Rev.1.30 S7G2 Microcontroller Group User's Manual Rev.1.40		

The descriptions of CSnCR.EXENB bit is corrected.

15. Buses

15.3 Register Descriptions

15.3.1 CSn Control Register (CSnCR) (n = 0 to 7)

[Before]

EXENB bit (Operation Enable)

The EXENB bit enables operation of the associated CS area. On MCU reset, operation is enabled (EXENB = 1) only for area 0. Operation in other areas is disabled (EXENB = 0). Attempts to access disabled areas have no effect.

When the CSC and SDRAMC are in use at the same time, BCLK and SDCLK must operate at the same frequency.

[After]

EXENB bit (Operation Enable)

The EXENB bit enables operation of the associated CS area. On MCU reset, operation is enabled (EXENB = 1) only for area 0. Operation in other areas is disabled (EXENB = 0). Attempts to access disabled areas have no effect.

When the CSC and SDRAMC are in use at the same time, BCLK and SDCLK must operate at the same frequency.

When using the CS0 to CS3 pin function and the EBCLK pin function, set the SDCKOCR.SDCKOEN bit to 0 to stop the output of the SDRAM clock (SDCLK).