

RENESAS TECHNICAL UPDATE

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| Product Category | MPU/MCU | Document No. | TN-RZ*-A053A/E | Rev. | 1.00 |
|--------------------|--|----------------------|------------------------|--|------|
| Title | RZ/T1 Group User's Manual: Hardware Restriction on Input capture function of MTU3a channel 1 | Information Category | Technical Notification | | |
| Applicable Product | RZ/T1 Group | Lot No. | Reference Document | RZ/T1 Group User's Manual: Hardware Rev1.40 R01UH0483EJ0140 Rev.1.40 | |
| | | All lots | | | |

There is a restriction on Input capture function of MTU3a channel 1 (MTU1). The following describes restriction and correction of User's Manual Hardware.

1. Condition:

When the IOB[3:0] bits of the Timer I/O Control Register (TIOR) of MTU1 are set to "111xb" as shown in the following table 19.15 and used Input capture function of MTU1 triggered by "occurrence of input capture in the MTU8.TGRC register".

2. Phenomenon

MTU1 Input capture does not occur.

3. Correction

| Page | Description | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|-------------|--|------|------|------------------------|--|-------------|--|------|------|------|------|--------------------|----------------------|-----|-----|-----|-----|-----|-----|---|---|---|---|------------------------|---|------|------|------|------|-------------|--|------|------|------|------|--------------------|----------------------|-----|-----|-----|-----|-----|-----|---|---|---|---|------------------------|--|
| 715 of 2635 | <p>[Current description] Table 19.15 TIOR (MTU1)</p> <table border="1"> <thead> <tr> <th>Bit7</th> <th>Bit6</th> <th>Bit5</th> <th>Bit4</th> <th>Description</th> <th></th> </tr> <tr> <th>IOB3</th> <th>IOB2</th> <th>IOB1</th> <th>IOB0</th> <th>MTU1.TGRB Function</th> <th>MTIOC1B Pin Function</th> </tr> </thead> <tbody> <tr> <td>...</td> <td>...</td> <td>...</td> <td>...</td> <td>...</td> <td>...</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>x</td> <td>Input capture register</td> <td>Input capture at occurrence of compare match or input capture in the MTU8.TGRC register</td> </tr> </tbody> </table> <p>[Correct description] Table 19.15 TIOR (MTU1)</p> <table border="1"> <thead> <tr> <th>Bit7</th> <th>Bit6</th> <th>Bit5</th> <th>Bit4</th> <th>Description</th> <th></th> </tr> <tr> <th>IOB3</th> <th>IOB2</th> <th>IOB1</th> <th>IOB0</th> <th>MTU1.TGRB Function</th> <th>MTIOC1B Pin Function</th> </tr> </thead> <tbody> <tr> <td>...</td> <td>...</td> <td>...</td> <td>...</td> <td>...</td> <td>...</td> </tr> <tr> <td>1</td> <td>1</td> <td>1</td> <td>x</td> <td>Input capture register</td> <td>Input capture at occurrence of compare match or input capture in the MTU8.TGRC register</td> </tr> </tbody> </table> | Bit7 | Bit6 | Bit5 | Bit4 | Description | | IOB3 | IOB2 | IOB1 | IOB0 | MTU1.TGRB Function | MTIOC1B Pin Function | ... | ... | ... | ... | ... | ... | 1 | 1 | 1 | x | Input capture register | Input capture at occurrence of compare match or input capture in the MTU8.TGRC register | Bit7 | Bit6 | Bit5 | Bit4 | Description | | IOB3 | IOB2 | IOB1 | IOB0 | MTU1.TGRB Function | MTIOC1B Pin Function | ... | ... | ... | ... | ... | ... | 1 | 1 | 1 | x | Input capture register | Input capture at occurrence of compare match or input capture in the MTU8.TGRC register |
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