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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU	Document No.	TN-RZ*-A050A/E	Rev.	1.00	
Title	RZ/T1 Group User's Manual: Hardware Collection for frequency of Trace clock output	Information Category	Technical Notification			
	RZ/T1 Group	Lot No.				
Applicable Product		All lots	Reference Document	RZ/T1 Group User's Manual: Hardware Rev1.40 R01UH0483EJ0140 Rev.1.40		

Incorrect description regarding frequency of trace clock output have been found.

This document describes corrections for the incorrect description.

1.Detail of a correction

No.	Page	Description							
1	224	[Current descrip 7.1 Overview							
		Table 7.2 Specif	2)						
		Item		Clock Source		Supplied to	Frequency		
		Trace interface	e clock (TCLK)	Selected from fr clocks for PLL0 or		CoreSight TPIU	150 MHz, 75 MHz		
		[Correct description] 7.1 Overview Table 7.2 Specifications of Clock Generation Circuit (Internal Clock) (2/2)							
		Item		Clock Source	, , ,	Supplied to	Frequency		
		Trace interface	e clock (TCLK)	Selected from fr		CoreSight TPIU	150 MHz, 75 MHz		
2	229	9 [Current description] 7.2.1 System Clock Control Register (SCKCR) b20							
		Bit Symb			Description		R/W		
		b20 TCLK		erface clock (TCLK)	0: 150 MHz 1: 75 MHz		R/W		
		[Correct description] 7.2.1 System Clock Control Register (SCKCR) b20							
		Bit Symb			Description		R/W		
		b20 TCLK		erface clock (TCLK)	0: Setting pro 1: 75 MHz	hibited	R/W		

3	268	[Current description] 10.1 Overview Table 10.1 CoreSight Specifications		
		Item Specifications		
		Trace function Trace port interface 8 bit x 150 Mbps (75 MHz or 37.5 MHz, DDR) trace data pin output Embedded Trace Buffer (ETB) 4KB SWV (Serial Wire Viewer) interface		
		[Correct description] 10.1 Overview Table 10.1 CoreSight Specifications		
		<u>Item</u> Specifications		
		Trace function Trace port interface 8 bit x 75 Mbps (75 MHz or 37.5 MHz, DDR) trace data pin output Embedded Trace Buffer (ETB) 4KB SWV (Serial Wire Viewer) interface		
4	277	[Current description] 10.3.3 Trace Port Interface As the output frequency of the TRACECLK pin, 75 MHz and 37.5 MHz (obtained by dividing the trace I/F clock (TCLK) by 2) can be set. For details, see section 7, Clock Generation Circuit.		
		[Correct description] 10.3.3 Trace Port Interface As the output frequency of the TRACECLK pin, 75 MHz and 37.5 MHz (obtained by dividing the trace I/F clock (TCLK) by 2) can be set. For details, see section 7, Clock Generation Circuit.		