Date: Nov. 24, 2021

RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0100B/E	Rev.	2.00
Title	Correction for Incorrect Description Notice RL78/G23 Descriptions in the User's Manual: Hardware Rev. 1.00 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G23 Group	Lot No. All lots	Reference Document	RL78/G23 User's Manual: Hardware Rev. 1.00 R01UH0896EJ0100 (Apr. 2021)		

This document describes misstatements found in the RL78/G23 User's Manual: Hardware Rev. 1.00 (R01UH0896EJ0100).

Corrections (1/3)

Applicable Item	Applicable Page	Contents
1.1 Features, Middle-speed on-chip oscillator	Page 17	Incorrect descriptions revised
1.6 Outline of Functions, Capacitive sensing unit	Page 18, Page 19	Incorrect descriptions revised
2.2.2 Description of pin functions, TS00-TS15, TS20-TS35, TSCAP	Page 20	Incorrect descriptions revised
Table 2 - 3 Connections of Unused Pins, P123, P124	Page 21	Caution added
Figure 2 - 25 Pin Block Diagram for Pin Type 8-31-1	Page 22	Incorrect descriptions revised
Figure 2 - 33 Pin Block Diagram for Pin Type 12-38-3	Page 23	Caution changed
Table 3 - 8 List of Extended Special Function Registers (2nd SFRs) (2/15), PFCMD register	Page 24	Incorrect descriptions revised
Table 3 - 8 List of Extended Special Function Registers (2nd SFRs) (7/15), MIOTRM register	Page 25	Incorrect descriptions revised
4.3.7 Port mode control A registers (PMCAxx)	Page 26	Caution added
4.5.4 Examples of register settings for port and alternate functions	Page 27	Caution added
Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (4/17)	Page 28	Incorrect descriptions revised
Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (1/21)	Page 29	Incorrect descriptions revised
Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (4/21)	Page 30	Incorrect descriptions revised
Figure 6 - 9 Format of Subsystem Clock Supply Mode Control Register (OSMC)	Page 31	Incorrect descriptions revised
9.2.11 Interval timer status register (ITLS0)	Page 32	Caution added
Table 12 - 3 A/D Conversion Time Selection (3/8)	Page 33	Incorrect descriptions revised
12.3.6 12-bit/10-bit A/D conversion result register (ADCRn)	Page 34	Caution added
Figure 12 - 12 Format of Analog Input Channel Specification Register (ADS)	Page 35, Page 36	Caution added and incorrect descriptions revised
12.6.2 Software trigger no-wait mode (select mode, one-shot conversion mode)	Page 37	Incorrect descriptions revised

Corrections (2/3)

Applicable Item	Applicable Page	Contents
12.6.4 Software trigger no-wait mode (scan mode, one-shot conversion mode)	Page 38	Incorrect descriptions revised
12.6.6 Software trigger wait mode (select mode, one-shot conversion mode)	Page 39	Incorrect descriptions revised
12.6.8 Software trigger wait mode (scan mode, one-shot conversion mode)	Page 40	Incorrect descriptions revised
12.6.9 Hardware trigger no-wait mode (select mode, sequential conversion mode)	Page 41	Incorrect descriptions revised
12.6.10 Hardware trigger no-wait mode (select mode, one-shot conversion mode)	Page 42	Incorrect descriptions revised
12.6.11 Hardware trigger no-wait mode (scan mode, sequential conversion mode)	Page 43	Incorrect descriptions revised
12.6.12 Hardware trigger no-wait mode (scan mode, one-shot conversion mode)	Page 44	Incorrect descriptions revised
12.6.14 Hardware trigger wait mode (select mode, one-shot conversion mode)	Page 45	Caution added and incorrect descriptions revised
12.6.16 Hardware trigger wait mode (scan mode, one-shot conversion mode)	Page 46	Incorrect descriptions revised
Figure 15 - 35 Example of Contents of Registers for Master Reception of 3-Wire Serial SPI (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21, CSI30, CSI31)	Page 47	Incorrect descriptions revised
Table 15 - 3 Baud Rate Setting for UART Reception in SNOOZE Mode	Page 48	Description changed
17.3.2 UART Mode, (5) Continuous transmission	Page 49	Description added
Figure 23 - 4 Procedure for Settings to Switch from Shutdown Mode to Normal Mode	Page 50	Caution added
Table 23 - 1 Operating Statuses in HALT Mode (1) (2/2)	Page 51	Description added
Table 23 - 2 Operating Statuses in HALT Mode (2) (2/2)	Page 52	Description added
Table 23 - 3 Operating Statuses in STOP Mode (2/2)	Page 53	Description added
Table 23 - 4 Operating Statuses in SNOOZE Mode (2/2)	Page 53	Description added
Figure 26 - 11 Delays from the Time an LVD0 or LVD1 Reset Source Condition is Satisfied until an LVD0 or LVD1 Reset has been Generated and Deasserted	Page 54	Incorrect descriptions revised
Figure 28 - 3 Procedure for Using the True Random Number Generator to Generate a Random Number Seed	Page 55	Description added
28.2.2 Setting of flash read protection	Page 56	Caution changed
CHAPTER 30 CAPACITIVE SENSING UNIT (CTSU2L), Number of the CTSU2L output channels	Page 57	Incorrect descriptions revised
Table 30 - 1 CTSU Functions, Transmission power switching of mutual capacitance method	Page 58	Incorrect descriptions revised
Table 30 - 2 External Pins Used in CTSU	Page 59	Incorrect descriptions revised
Figure 30 - 7 Format of CTSU Control Registers AL and AH (CTSUCRAL, CTSUCRAH)	Page 60, Page 61	Description changed
Figure 30 - 15 Format of CTSU Calibration Registers L and H (CTSUDBGR0, CTSUDBGR1)	Page 62	Incorrect descriptions revised
CHAPTER 30 CAPACITIVE SENSING UNIT (CTSU2L), Cautions when using capacitive sensing unit	Page 63	Description added
31.1 Overview	Page 64	Description added
Figure 32 - 5 Format of User Option Byte (000C2H or 040C2H)	Page 65	Incorrect descriptions revised
Figure 33 - 8 Flow of Self-Programming (Rewriting Flash Memory)	Page 66	Description changed
33.6.2.1 Flash address pointer registers H and L (FLAPH, FLAPL)	Page 67	Caution changed
33.6.2.2 Flash end address pointer registers H and L (FLSEDH, FLSEDL)	Page 68	Caution changed
33.6.2.3 Flash write buffer registers H and L (FLWH, FLWL)	Page 69, Page 70	Caution changed
33.6.2.6 Flash programming mode control register (FLPMC)	Page 71	Caution added
33.6.2.8 Flash memory sequencer initial setting register (FSSET)	Page 72, Page 73	Caution added and description changed

Corrections (3/3)

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33.6.2.9 Flash memory sequencer control register (FSSQ)	Page 74 to Page 76	Caution added and description changed
33.6.2.10 Flash extra sequencer control register (FSSE)	Page 77, Page 78	Caution added and description changed
33.6.2.11 Flash registers initialization register (FLRST)	Page 79	Caution changed
33.6.2.12 Flash memory sequencer status registers H and L (FSASTH, FSASTL)	Page 80	Incorrect descriptions revised
33.6.2.13 Flash security flag monitoring register (FLSEC)	Page 81	Description added and incorrect descriptions revised
33.6.2.14 Flash FSW monitoring register E (FLFSWE)	Page 82	Caution changed and description changed
33.6.2.16 Data flash control register (DFLCTL)	Page 83	Description changed
33.6.3 Setting the flash memory control mode	Page 84	Description changed
33.6.3.1 Procedure for executing the specific sequence	Page 85	Description changed
33.6.6.4 Operations for rewriting the code flash memory area	Page 86, Page 87	Caution added and description changed
33.6.6.5 Operations for rewriting the data flash memory area	Page 88, Page 89	Caution added and description changed
33.6.6.7 Operations for rewriting the extra area	Page 90, Page 91	Description changed
33.6.6.8 Data to be set for the commands for use with the extra area sequencer	Page 92 to Page 96	Caution changed and description changed
33.6.8 Flash shield window function	Page 97, Page 98	Caution changed and description changed
33.6.10.3 Example of executing the commands to rewrite the extra area	Page 99	Description changed
33.6.11 Notes on self-programming	Page 100	Caution changed and caution added
33.7 Security Settings	Page 101 to Page 104	Caution added and description changed
34.2 Connection between the External Device that Incorporates UART and RL78/G23	Page 105	Caution changed
37.1 Absolute Maximum Ratings	Page 106	Incorrect descriptions revised
37.2.1 Characteristics of the X1 and XT1 oscillators	Page 107	Incorrect descriptions revised
37.3.1 Pin characteristics	Page 108 to Page 111	Incorrect descriptions revised
37.3.2 Supply current characteristics	Page 112 to Page 122	Specifications changed and Specifications added
37.5.2 Serial interface UARTA	Page 123	Specifications changed
37.6.1 A/D converter characteristics, (1) Normal modes 1 and 2	Page 124	Description changed
37.6.1 A/D converter characteristics, (2) Low-voltage modes 1 and 2	Page 125	Description changed
37.6.4 Comparator characteristics	Page 126	Specifications changed
37.8 Flash Memory Programming Characteristics	Page 127	Incorrect descriptions revised
38.4 40-Pin Products	Page 128	Specifications added
38.6 48-Pin Products	Page 129	Specifications added

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware (1/3)

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10	Figure 32 - 4 Format of User Option Byte (000C1H or 040C1H) (3/3)		Page 1278	Page 16
11	1.1 Features, Middle-speed on-chip oscillator		Page 1	Page 17
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13	1.6 Outline of Functions, 52- to 128-pin products, Capacitive sensing unit		Page 29	Page 19
14	2.2.2 Description of pin functions, TS00-TS15, TS20-TS35, TSCAP		Page 68	Page 20
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20	4.3.7 Port mode control A registers (PMCAxx)		Page 191	Page 26
21	4.5.4 Examples of register settings for port and alternate functions		Page 211	Page 27
22	Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (4/17)		Page 215	Page 28
23	Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (1/21)		Page 228	Page 29
24	Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (4/21)		Page 231	Page 30
25	Figure 6 - 9 Format of Subsystem Clock Supply Mode Control Register (OSMC)		Page 282	Page 31
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29	Figure 12 - 12 Format of Analog Input Channel Specification Register (ADS)		Page 546	Page 35, Page 36
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35	12.6.10 Hardware trigger no-wait mode (select mode, one-shot conversion mode)		Page 563	Page 42
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37	12.6.12 Hardware trigger no-wait mode (scan mode, one-shot conversion mode)		Page 566	Page 44
38	12.6.14 Hardware trigger wait mode (select mode, one-shot conversion mode)		Page 568	Page 45
39	12.6.16 Hardware trigger wait mode (scan mode, one-shot conversion mode)		Page 570	Page 46
40	Figure 15 - 35 Example of Contents of Registers for Master Reception of 3-Wire Serial SPI (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21, CSI30, CSI31)		Page 676	Page 47
41	Table 15 - 3 Baud Rate Setting for UART Reception in SNOOZE Mode		Page 752	Page 48
42	17.3.2 UART Mode, (5) Continuous transmission		Page 911	Page 49
43	Figure 23 - 4 Procedure for Settings to Switch from Shutdown Mode to Normal Mode		Page 1108	Page 50
44	Table 23 - 1 Operating Statuses in HALT Mode (1) (2/2)		Page 1110	Page 51
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46	Table 23 - 3 Operating Statuses in STOP Mode (2/2)		Page 1117	Page 53
47	Table 23 - 4 Operating Statuses in SNOOZE Mode (2/2)		Page 1124	Page 53
48	Figure 26 - 11 Delays from the Time an LVD0 or LVD1 Reset Source Condition is Satisfied until an LVD0 or LVD1 Reset has been Generated and Deasserted		Page 1155	Page 54
49	Figure 28 - 3 Procedure for Using the True Random Number Generator to Generate a Random Number Seed		Page 1188	Page 55
50	28.2.2 Setting of flash read protection		Page 1190	Page 56
51	CHAPTER 30 CAPACITIVE SENSING UNIT (CTSU2L), Number of the CTSU2L output channels		Page 1236	Page 57
52	Table 30 - 1 CTSU Functions, Transmission power switching of mutual capacitance method		Page 1238	Page 58
53	Table 30 - 2 External Pins Used in CTSU		Page 1239	Page 59
54	Figure 30 - 7 Format of CTSU Control Registers AL and AH (CTSUCRAL, CTSUCRAH)		Page 1245, Page 1246, Page 1247	Page 60, Page 61
55	Figure 30 - 15 Format of CTSU Calibration Registers L and H (CTSUDBGR0, CTSUDBGR1)		Page 1264, Page 1266	Page 62
56	CHAPTER 30 CAPACITIVE SENSING UNIT (CTSU2L), Cautions when using capacitive sensing unit		Page 1271	Page 63
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58	Figure 32 - 5 Format of User Option Byte (000C2H or 040C2H)		Page 1279	Page 65
59	Figure 33 - 8 Flow of Self-Programming (Rewriting Flash Memory)		Page 1297	Page 66
60	33.6.2.1 Flash address pointer registers H and L (FLAPH, FLAPL)		Page 1300	Page 67
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62	33.6.2.3 Flash write buffer registers H and L (FLWH, FLWL)		Page 1303	Page 69, Page 70
63	33.6.2.6 Flash programming mode control register (FLPMC)		Page 1306	Page 71
64	33.6.2.8 Flash memory sequencer initial setting register (FSSET)		Page 1308	Page 72, Page 73
65	33.6.2.9 Flash memory sequencer control register (FSSQ)		Page 1310, Page 1311	Page 74 to Page 76
66	33.6.2.10 Flash extra sequencer control register (FSSE)		Page 1312	Page 77, Page 78
67	33.6.2.11 Flash registers initialization register (FLRST)		Page 1313	Page 79
68	33.6.2.12 Flash memory sequencer status registers H and L (FSASTH, FSASTL)		Page 1314	Page 80
69	33.6.2.13 Flash security flag monitoring register (FLSEC)		Page 1316	Page 81
70	33.6.2.14 Flash FSW monitoring register E (FLFSWE)		Page 1317	Page 82
71	33.6.2.16 Data flash control register (DFLCTL)		Page 1319	Page 83

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0896EJ0100	
72	33.6.3 Setting the flash memory control mode		Page 1322	Page 84
73	33.6.3.1 Procedure for executing the specific sequence		Page 1322	Page 85
74	33.6.6.4 Operations for rewriting the code flash memory area		Page 1326	Page 86, Page 87
75	33.6.6.5 Operations for rewriting the data flash memory area		Page 1327	Page 88, Page 89
76	33.6.6.7 Operations for rewriting the extra area		Page 1328	Page 90, Page 91
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78	33.6.8 Flash shield window function		Page 1335	Page 97, Page 98
79	33.6.10.3 Example of executing the commands to rewrite the extra area		Page 1340	Page 99
80	33.6.11 Notes on self-programming		Page 1341	Page 100
81	33.7 Security Settings		Page 1342, Page 1343	Page 101 to Page 104
82	34.2 Connection between the External Device that Incorporates UART and RL78/G23		Page 1347	Page 105
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84	37.2.1 Characteristics of the X1 and XT1 oscillators		Page 1376	Page 107
85	37.3.1 Pin characteristics		Page 1378 to Page 1381	Page 108 to Page 111
86	37.3.2 Supply current characteristics		Page 1387 to Page 1394	Page 112 to Page 122
87	37.5.2 Serial interface UARTA		Page 1430	Page 123
88	37.6.1 A/D converter characteristics, (1) Normal modes 1 and 2		Page 1434	Page 124
89	37.6.1 A/D converter characteristics, (2) Low-voltage modes 1 and 2		Page 1435	Page 125
90	37.6.4 Comparator characteristics		Page 1438	Page 126
91	37.8 Flash Memory Programming Characteristics		Page 1444	Page 127
92	38.4 40-Pin Products		Page 1450	Page 128
93	38.6 48-Pin Products		Page 1453	Page 129

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

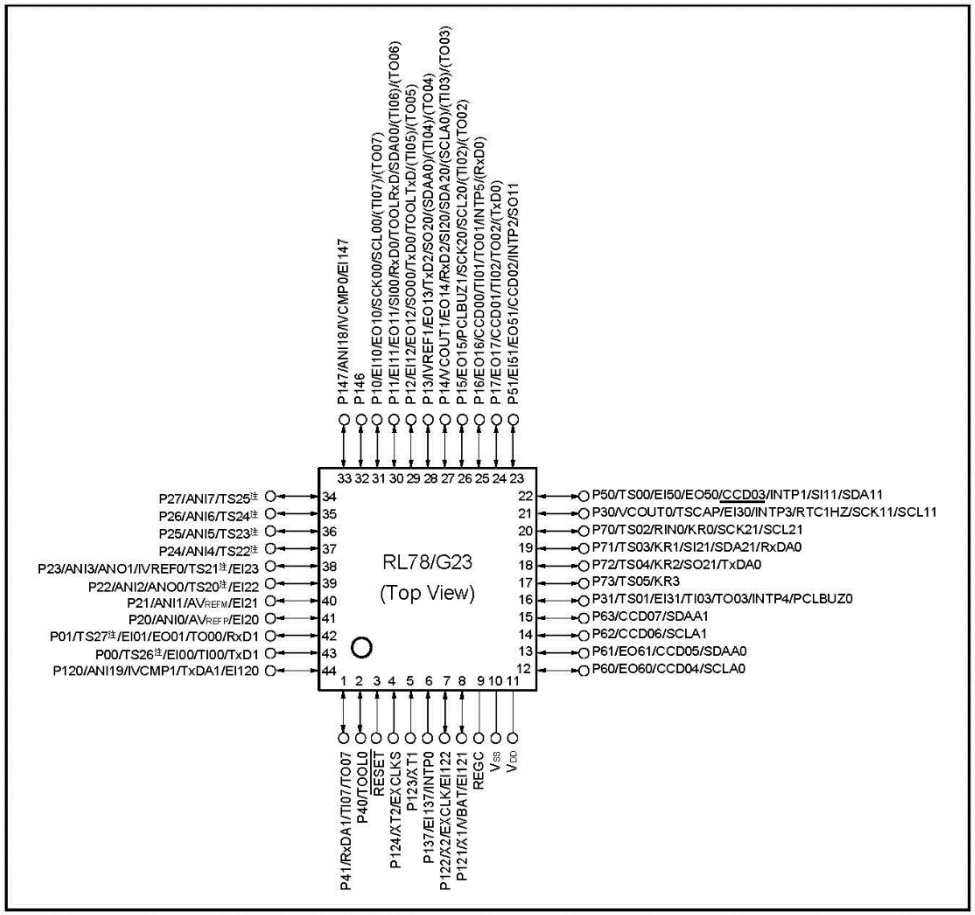
RL78/G23 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0100A/E	Jun. 29, 2021	First edition issued Corrections No.1 to No.10 revised (this document)
TN-RL*-A0100B/E	Nov. 24, 2021	Corrections No.11 to No.93 revised

1. Pin Configuration, 44-pin products (Page 13)

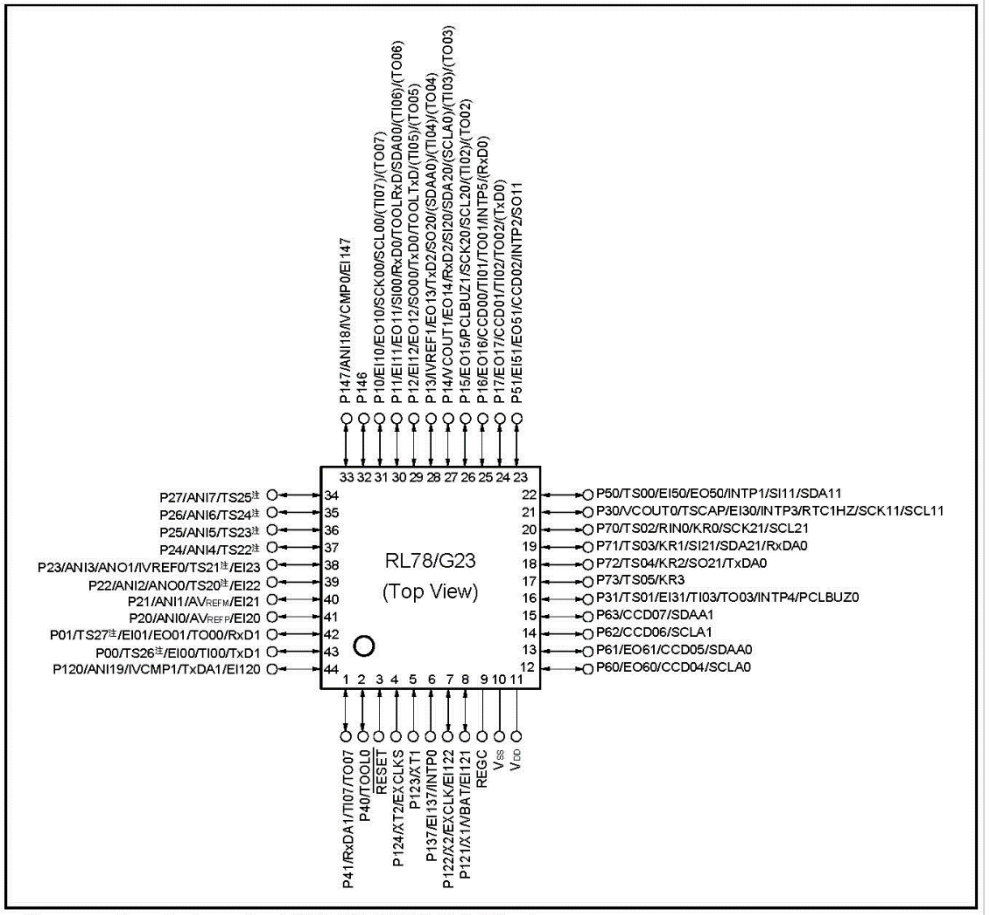
Incorrect:

• 44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)



Correct:

• 44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)



2. Outline of Functions, 44-pin products (Page 25)

Incorrect:

[30-, 32-, 36-, 40-, 44-, and 48-pin products]

Item		30-pin R7F100GAx		44-pin R7F100GFx	48-pin R7F100GGx
I/O port	Total number of pins	26		40	44
	CMOS I/O	23 (N-ch open drain I/O [V_{DD} withstand voltage]: 10)		33 (N-ch open drain I/O [V_{DD} withstand voltage]: 12)	36 (N-ch open drain I/O [V_{DD} withstand voltage]: 13)
	CMOS input	1		3	3
	CMOS output	-		-	1
	N-ch open drain I/O (withstand voltage: 6 V)	2		4	4
	Output current control port	6		8	8

Correct:

[30-, 32-, 36-, 40-, 44-, and 48-pin products]

Item		30-pin R7F100GAx		44-pin R7F100GFx	48-pin R7F100GGx
I/O port	Total number of pins	26		40	44
	CMOS I/O	23 (N-ch open drain I/O [V_{DD} withstand voltage]: 10)		33 (N-ch open drain I/O [V_{DD} withstand voltage]: 12)	36 (N-ch open drain I/O [V_{DD} withstand voltage]: 13)
	CMOS input	1		3	3
	CMOS output	-		-	1
	N-ch open drain I/O (withstand voltage: 6 V)	2		4	4
	Output current control port	6		7	8

3. Functions of Port Pins, 44-pin products (Page 41)

Incorrect:

2.1.5 44-pin products

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
P50	7-39-1	I/O	Input port	TS00/EI50/EO50/CCD03/ INTP1/SI11/SDA11	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (V**DD** tolerance). Input or output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P50 and P51 can be set as output current control port pins.
P51	7-38-1			EI51/EO51/CCD02/INTP2/ SO11	

Correct:

2.1.5 44-pin products

Function Name	Pin Type	I/O	After Reset Release	Alternate Function	Function
P50	7-39-1	I/O	Input port	TS00/EI50/EO50/ INTP1/SI11/SDA11	Port 5. 2-bit I/O port. Output of P50 can be set to N-ch open-drain output (V**DD** tolerance). Input or output can be specified in 1-bit units. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P51 can be set as output current control port pins.
P51	7-38-1			EI51/EO51/CCD02/INTP2/ SO11	

4. Functions for each product, 44-pin products (Page 62)

Incorrect:

2.2.1 Functions for each product

Function Name	128-pin	100-pin	80-pin	64-pin	52-pin	48-pin	44-pin	40-pin	36-pin	32-pin	30-pin
CCD00	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD01	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD02	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD03	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓

Correct:

2.2.1 Functions for each product

Function Name	128-pin	100-pin	80-pin	64-pin	52-pin	48-pin	44-pin	40-pin	36-pin	32-pin	30-pin
CCD00	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD01	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD02	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓	✓
CCD03	✓	✓	✓	✓	✓	✓	—	✓	✓	✓	✓

5. Table 4 - 1 Port Configuration (1/2) (Page 169)

Incorrect:

Table 4 - 1 Port Configuration (1/2)

Item	Configuration
Port	• 30-pin products Total: 26 (CMOS I/O: 23 (N-ch open drain I/O [VDD tolerance]: 10, output current control port: 6), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 2) • 32-pin products Total: 28 (CMOS I/O: 24 (N-ch open drain I/O [VDD tolerance]: 10, output current control port: 7), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 3) • 36-pin products Total: 32 (CMOS I/O: 28 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 7), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 3) • 40-pin products Total: 36 (CMOS I/O: 30 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 7), CMOS input: 3, N-ch open drain I/O [6-V tolerance]: 3) • 44-pin products Total: 40 (CMOS I/O: 33 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 8), CMOSinput: 3, N-ch open drain I/O [6-V tolerance]: 4)

Correct:

Table 4 - 1 Port Configuration (1/2)

Item	Configuration
Port	• 30-pin products Total: 26 (CMOS I/O: 23 (N-ch open drain I/O [VDD tolerance]: 10, output current control port: 6), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 2) • 32-pin products Total: 28 (CMOS I/O: 24 (N-ch open drain I/O [VDD tolerance]: 10, output current control port: 7), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 3) • 36-pin products Total: 32 (CMOS I/O: 28 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 7), CMOS input: 1, N-ch open drain I/O [6-V tolerance]: 3) • 40-pin products Total: 36 (CMOS I/O: 30 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 7), CMOS input: 3, N-ch open drain I/O [6-V tolerance]: 3) • 44-pin products Total: 40 (CMOS I/O: 33 (N-ch open drain I/O [VDD tolerance]: 12, output current control port: 7), CMOSinput: 3, N-ch open drain I/O [6-V tolerance]: 4)

6. Port Configuration, Port5 (Page 173)

Incorrect:

4.2.6 Port 5

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units by port mode register 5 (PM5). When the P50 to P57 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 5 (PU5).

Input to the P53 to P55 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units by port input mode register 5 (PIM5).

Output from the P50 and P52 to P55 pins can be specified as N-ch open-drain output (V_{DD} tolerance Note 1/EV_{DD} tolerance Note 2) in 1-bit units by port output mode register 5 (POM5).

Output from the P50 and P51 pins can be specified as output current control port pins in 1-bit units by the output current control enable register (CCDE).

This port can also be used for external interrupt request input, serial interface data I/O and clock I/O, capacitance measurement, and logic and event link controller I/O. Use the registers shown in **4.3 Registers to Control the Port Function** to specify the states of each of the pins. For the correspondence between register settings and pin state, see **Table 4 - 6**.

Port 5 is set to input mode following a reset.

Note 1. For 30- to 52-pin products

Note 2. For 64- to 128-pin products

Correct:

4.2.6 Port 5

Port 5 is an I/O port with an output latch. Port 5 can be set to the input mode or output mode in 1-bit units by port mode register 5 (PM5). When the P50 to P57 pins are used as an input port, use of an on-chip pull-up resistor can be specified in 1-bit units by pull-up resistor option register 5 (PU5).

Input to the P53 to P55 pins can be specified through a normal input buffer or a TTL input buffer in 1-bit units by port input mode register 5 (PIM5).

Output from the P50 Note 3 and P52 to P55 pins can be specified as N-ch open-drain output (V_{DD} tolerance Note 1/EV_{DD} tolerance Note 2) in 1-bit units by port output mode register 5 (POM5).

Output from the P50 and P51 pins can be specified as output current control port pins in 1-bit units by the output current control enable register (CCDE).

This port can also be used for external interrupt request input, serial interface data I/O and clock I/O, capacitance measurement, and logic and event link controller I/O. Use the registers shown in **4.3 Registers to Control the Port Function** to specify the states of each of the pins. For the correspondence between register settings and pin state, see **Table 4 - 6**.

Port 5 is set to input mode following a reset.

Note 1. For 30- to 52-pin products

Note 2. For 64- to 128-pin products

Note 3. Excluding 44-pin products

7. Figure 4 - 12 Format of Output Current Control Enable Register (CCDE) (Page 197)

Incorrect:

Figure 4 - 12 Format of Output Current Control Enable Register (CCDE)

CCDE03	Selection of digital I/O or output current control function for CCD03 (P50) pin
0	Digital I/O (alternate function other than current control function)
1	Current control function

Caution 1. When a port pin is to be used with output current control, make the setting for the output current control function and then set the corresponding bit in the PMxx register for output mode.

Caution 2. The state of a pin takes 10 μs to become stable after 1 having been written to the corresponding bit of the CCDE register.

Correct:

Figure 4 - 12 Format of Output Current Control Enable Register (CCDE)

CCDE03	Selection of digital I/O or output current control function for CCD03 (P50Note) pin
0	Digital I/O (alternate function other than current control function)
1	Current control function

Caution 1. When a port pin is to be used with output current control, make the setting for the output current control function and then set the corresponding bit in the PMxx register for output mode.

Caution 2. The state of a pin takes 10 μs to become stable after 1 having been written to the corresponding bit of the CCDE register.

Note. Excluding 44-pin products

8. **Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (9/17) (Page 220)**

Incorrect:

Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (9/17)

Pin Name	Function Used		PIOR	POMxx	PMCTxx	PMCEx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)								
P50	P50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
		Output	—	0	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1	SDA11 = 1	—								
		N-ch open drain output	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1										
	TS00	I/O	—	×	1	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	EI50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	EO50	Output	—	0/1	0	1	CCDE03 = 0	CCS0x = xxx	0	×	×	—	√	√	√	√	√	√	√	√
	CCD03	Output	—	0/1	0	0	CCDE03 = 1	CCS0x = 001 to 011	0	0	×	—	√	√	√	√	—	√	√	√
	INTP1	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	SI11	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	SDA11	I/O	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	1	×	—	√	√	√	√	√	√	√	√

Correct:

Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (9/17)

Pin Name	Function Used		PIOR	POMxx	PMCTxx	PMCEx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)								
P50	P50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
		Output	—	0	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1	SDA11 = 1	—								
		N-ch open drain output	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1										
	TS00	I/O	—	×	1	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	EI50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	EO50	Output	—	0/1	0	1	CCDE03 = 0	CCS0x = xxx	0	×	×	—	√	√	√	√	√	√	√	√
	CCD03	Output	—	0/1	0	0	CCDE03 = 1	CCS0x = 001 to 011	0	0	×	—	√	√	√	√	—	√	√	√
	INTP1	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	SI11	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√
	SDA11	I/O	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	1	×	—	√	√	√	√	√	√	√	√

9. **Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (9/21) (Page 236)**

Incorrect:

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (9/21)

Pin Name	Function Used		PIOR	POMxx	PMCTxx	PMCEx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)											
P50	P50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
		Output	—	0	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1	SDA11 = 1 Note 1	—											
		N-ch open drain output	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1													
	TS00	I/O	—	×	1	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	EI50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	EO50	Output	—	0/1	0	1	CCDE03 = 0	CCS0x = xxx	0	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	CCD03	Output	—	0/1	0	0	CCDE03 = 1	CCS0x = 001 to 011	0	0	×	—	√	√	√	√	√	√	√	√	√	√	√
	INTP1	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	—	—
	SI11	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	—
	SDA11	I/O	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	1	×	—	√	√	√	√	√	√	√	√	√	√	—

Correct:

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (9/21)

Pin Name	Function Used		PIOR	POMxx	PMCTxx	PMCEx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)											
P50	P50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
		Output	—	0	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1	SDA11 = 1 Note 1	—											
		N-ch open drain output	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	0/1													
	TS00	I/O	—	×	1	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	EI50	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	EO50	Output	—	0/1	0	1	CCDE03 = 0	CCS0x = xxx	0	×	×	—	√	√	√	√	√	√	√	√	√	√	√
	CCD03	Output	—	0/1	0	0	CCDE03 = 1	CCS0x = 001 to 011	0	0	×	—	√	√	√	√	—	√	√	√	√	√	√
	INTP1	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×		√	√	√	√	√	√	√	√	√	—	—
	SI11	Input	—	×	0	0	CCDE03 = 0	CCS0x = xxx	1	×	×	—	√	√	√	√	√	√	√	√	√	√	—
	SDA11	I/O	—	1	0	0	CCDE03 = 0	CCS0x = xxx	0	1	×	—	√	√	√	√	√	√	√	√	√	√	—

10. Figure 32 - 4 Format of User Option Byte (000C1H or 040C1H) (3/3) (Page 1278)

Incorrect:

・LVD0 off setting (external reset input from the $\overline{\text{RESET}}$ pin is used)

Detection Voltage		Option Byte Setting Value				
V_{LVD0}		LVD0EN	Mode setting	LVD0V2	LVD0V1	LVD0V0
Rising edge	Falling edge		LVD0SEL			
—	—	0	x	x	x	x
—		Settings other than the above are prohibited.				

Correct:

・LVD0 off setting (external reset input from the $\overline{\text{RESET}}$ pin is used)

Detection Voltage		Option Byte Setting Value				
V_{LVD0}		LVD0EN	Mode setting	LVD0V2	LVD0V1	LVD0V0
Rising edge	Falling edge		LVD0SEL			
—	—	0	x	0	1	0
—		Settings other than the above are prohibited.				

11. 1.1 Features, Middle-speed on-chip oscillator (Page 1)

Incorrect:

High-speed on-chip oscillator
- Select from 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, or 1 MHz
- High accuracy: ±1.0% (VDD = 1.8 to 5.5 V, TA = -20 to +85°C)

Middle-speed on-chip oscillator
- Select from 4 MHz, 3 MHz, 2 MHz, or 1 MHz (with adjustability)

Low-speed on-chip oscillator
- 32.768 kHz (typ.) (with adjustability)

Correct:

High-speed on-chip oscillator
- Select from 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, or 1 MHz
- High accuracy: ±1.0% (VDD = 1.8 to 5.5 V, TA = -20 to +85°C)

Middle-speed on-chip oscillator
- Select from 4 MHz, 2 MHz, or 1 MHz (with adjustability)

Low-speed on-chip oscillator
- 32.768 kHz (typ.) (with adjustability)

12. 1.6 Outline of Functions, 30- to 48-pin products, Capacitive sensing unit (Page 26)

Incorrect:

Item		30-pin R7F100GAx	32-pin R7F100GBx	36-pin R7F100GCx	40-pin R7F100GEx	44-pin R7F100GFx	48-pin R7F100GGx
Timers	16-bit timer	8 channels					
	Watchdog timer	1 channel					
	Realtime clock (RTC)	1 channel					
	32-bit interval timer (TML32)	1 channel in 32-bit mode, 2 channels in 16-bit mode, 4 channels in 8-bit mode					
	Timer output	4 channels (PWM outputs: 3Note 3), 8 channels (PWM outputs: 7Note 3)Note 4				5 channels (PWM outputs: 4Note 3), 8 channels (PWM outputs: 7Note 3)Note 4	
	RTC output	1 channel					
Clock output/buzzer output		2					
		• 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (at the 32-MHz operation with the main system clock (fMAIN)) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (at the 32.768-kHz operation with the low-speed peripheral clock (fSXP))					
8-/10-/12-bit resolution A/D converter		8 channels	8 channels	8 channels	9 channels	10 channels	10 channels
D/A converter		2 channels	2 channels	2 channels	2 channels	2 channels	2 channels
Comparator		2 channels	2 channels	2 channels	2 channels	2 channels	2 channels
Serial interface		[30- and 32-pin products] • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-, 40-, and 44-pin products] • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART (UART supporting LIN-bus): 1 channel [48-pin products] • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART (UART supporting LIN-bus): 1 channel					
	UARTA	—		1 channel	1 channel	2 channels	2 channels
	I2C bus	1 channel	1 channel	1 channel	1 channel	2 channels	2 channels
Remote control signal receiver		—	1 channel	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		30 sources	30 sources	32 sources	33 sources	35 sources	36 sources
Logic and event link controller (ELCL)		1					
SNOOZE mode sequencer (SMS)		1					
Capacitive sensing unit		6	7	11	13	14	16
Vectored interrupt sources	Internal	31	32	35	35	39	39
	External	6	6	6	7	7	10

Correct:

Item		30-pin R7F100GAx	32-pin R7F100GBx	36-pin R7F100GCx	40-pin R7F100GEx	44-pin R7F100GFx	48-pin R7F100GGx
Timers	16-bit timer	8 channels					
	Watchdog timer	1 channel					
	Realtime clock (RTC)	1 channel					
	32-bit interval timer (TML32)	1 channel in 32-bit mode, 2 channels in 16-bit mode, 4 channels in 8-bit mode					
	Timer output	4 channels (PWM outputs: 3Note 3), 8 channels (PWM outputs: 7Note 3)Note 4				5 channels (PWM outputs: 4Note 3), 8 channels (PWM outputs: 7Note 3)Note 4	
	RTC output	1 channel					
Clock output/buzzer output		2					
		• 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (at the 32-MHz operation with the main system clock (fMAIN)) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (at the 32.768-kHz operation with the low-speed peripheral clock (fSXP))					
8-/10-/12-bit resolution A/D converter		8 channels	8 channels	8 channels	9 channels	10 channels	10 channels
D/A converter		2 channels	2 channels	2 channels	2 channels	2 channels	2 channels
Comparator		2 channels	2 channels	2 channels	2 channels	2 channels	2 channels
Serial interface		[30- and 32-pin products] • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART (UART supporting LIN-bus): 1 channel [36-, 40-, and 44-pin products] • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART (UART supporting LIN-bus): 1 channel [48-pin products] • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART (UART supporting LIN-bus): 1 channel					
	UARTA	—		1 channel	1 channel	2 channels	2 channels
	I2C bus	1 channel	1 channel	1 channel	1 channel	2 channels	2 channels
Remote control signal receiver		—	1 channel	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		30 sources	30 sources	32 sources	33 sources	35 sources	36 sources
Logic and event link controller (ELCL)		1					
SNOOZE mode sequencer (SMS)		1					
Capacitive sensing unit	ROM size 96 to 128KB	2	3	5	6	6	8
	ROM size 192 to 768KB	6	7	11	13	14	16
Vectored interrupt sources	Internal	31	32	35	35	39	39
	External	6	6	6	7	7	10

13. 1.6 Outline of Functions, 52- to 128-pin products, Capacitive sensing unit (Page 29)

Incorrect:

Item		52-pin R7F100GJx	64-pin R7F100GLx	80-pin R7F100GMx	100-pin R7F100GPx	128-pin R7F100GSx
Timers	16-bit timer	8 channels		12 channels		16 channels
	Watchdog timer	1 channel				
	Realtime clock (RTC)	1 channel				
	32-bit interval timer (TML32)	1 channel in 32-bit mode, 2 channels in 16-bit mode, 4 channels in 8-bit mode				
	Timer output	5 channels (PWM outputs: 4Note 3), 8 channels (PWM outputs: 7Note 3Note 4	8 channels (PWMoutputs: 7Note 3)	12 channels (PWM outputs: 10Note 3)		16 channels (PWM outputs: 14Note 3)
	RTC output	1 channel				
Clock output/buzzer output		2	2	2	2	2
		• 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (at the 32-MHz operation with the main system clock (fMAIN)) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (at the 32.768-kHz operation with the low-speed peripheral clock (fSXP))				
8-/10-/12-bit resolution A/D converter		12 channels	12 channels	17 channels	20 channels	26 channels
D/A converter		2 channels	2 channels	2 channels	2 channels	2 channels
Comparator		2 channels	2 channels	2 channels	2 channels	2 channels
Serial interface		[52-pin products] • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART (UART supporting LIN-bus): 1 channel [80-, 100-, and 128-pin products] • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART (UART supporting LIN-bus): 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel				
	UARTA	2 channels	2 channels	2 channels	2 channels	2 channels
	I2C bus	2 channels	2 channels	2 channels	2 channels	2 channels
Remote control signal receiver		1 channel	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		36 sources	37 sources	39 sources		
Logic and event link controller (ELCL)		1				
SNOOZE mode sequencer (SMS)		1				
Capacitive sensing unit		20	22	30	32	32

Correct:

Item		52-pin R7F100GJx	64-pin R7F100GLx	80-pin R7F100GMx	100-pin R7F100GPx	128-pin R7F100GSx
Timers	16-bit timer	8 channels		12 channels		16 channels
	Watchdog timer	1 channel				
	Realtime clock (RTC)	1 channel				
	32-bit interval timer (TML32)	1 channel in 32-bit mode, 2 channels in 16-bit mode, 4 channels in 8-bit mode				
	Timer output	5 channels (PWM outputs: 4Note 3), 8 channels (PWM outputs: 7Note 3Note 4	8 channels (PWMoutputs: 7Note 3)	12 channels (PWM outputs: 10Note 3)		16 channels (PWM outputs: 14Note 3)
	RTC output	1 channel				
Clock output/buzzer output		2	2	2	2	2
		• 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (at the 32-MHz operation with the main system clock (fMAIN)) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (at the 32.768-kHz operation with the low-speed peripheral clock (fSXP))				
8-/10-/12-bit resolution A/D converter		12 channels	12 channels	17 channels	20 channels	26 channels
D/A converter		2 channels	2 channels	2 channels	2 channels	2 channels
Comparator		2 channels	2 channels	2 channels	2 channels	2 channels
Serial interface		[52-pin products] • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 1 channel/simplified I2C: 1 channel/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART (UART supporting LIN-bus): 1 channel [64-pin products] • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART (UART supporting LIN-bus): 1 channel [80-, 100-, and 128-pin products] • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART (UART supporting LIN-bus): 1 channel • SPI (CSI): 2 channels/simplified I2C: 2 channels/UART: 1 channel				
	UARTA	2 channels	2 channels	2 channels	2 channels	2 channels
	I2C bus	2 channels	2 channels	2 channels	2 channels	2 channels
Remote control signal receiver		1 channel	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)		36 sources	37 sources	39 sources		
Logic and event link controller (ELCL)		1				
SNOOZE mode sequencer (SMS)		1				
Capacitive sensing unit	ROM size 96 to 128KB	10	12	30	32	32
	ROM size 192 to 768KB	20	22	30	32	32

14. 2.2.2 Description of pin functions, TS00-TS15, TS20-TS35, TSCAP (Page 68)

Incorrect:

Function Name	I/O	Function
ANI0 to ANI14, ANI16 to ANI26	Input	Analog voltage inputs of the A/D converter (see **Figure 12 - 52 Connections of VDD, AVREFP, and Analog Input Pins**)
ANO0, ANO1	Output	D/A converter outputs
IVCMP0, IVCMP1	Input	Analog voltage inputs of the comparator
IVREF0, IVREF1	Input	Reference voltage inputs of the comparator
VCOUT0, VCOUT1	Output	Comparator outputs
TS00 to TS15, TS20 to TS35	Output	Electrostatic capacitance measurement pins (touch sensor)
TSCAP	Output	Pin for connecting a power supply stabilization capacitor for the touch sensor interface. Connect this pin to Vss via a capacitor (10 nF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.
CCD00 to CCD07	Output	Output current control port

Correct:

Function Name	I/O	Function
ANI0 to ANI14, ANI16 to ANI26	Input	Analog voltage inputs of the A/D converter (see **Figure 12 - 52 Connections of VDD, AVREFP, and Analog Input Pins**)
ANO0, ANO1	Output	D/A converter outputs
IVCMP0, IVCMP1	Input	Analog voltage inputs of the comparator
IVREF0, IVREF1	Input	Reference voltage inputs of the comparator
VCOUT0, VCOUT1	Output	Comparator outputs
TS00 to TS15, TS20 to TS35	I/O	Electrostatic capacitance measurement pins (touch sensor)
TSCAP	I/O	Pin for connecting a power supply stabilization capacitor for the touch sensor interface. Connect this pin to Vss via a capacitor (10 nF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.
CCD00 to CCD07	Output	Output current control port

15. Table 2 - 3 Connections of Unused Pins, P123, P124 (Page 70)

Incorrect:

Pin Name	I/O	Recommended Connection of Unused Pins
P00 to P07	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P10 to P17		
P20 to P27		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P30 to P37		Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P40/TOOL0		Input: Independently connect to EV_{DD0}, EV_{DD1} or leave open. Output: Leave open.
P41 to P47		Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P50 to P57		
P60 to P63		Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Set the port's output latch to 0 and leave the pins open, or set the port's output latch to 1 and independently connect the pins to EV_{DD0} and EV_{DD1} or EV_{SS0} and EV_{SS1} via a resistor.
P64 to P67		Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P70 to P77		
P80 to P87		
P90 to P97		
P100 to P106		
P110 to P117		
P120		
P121, P122		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P123, P124	Input	Set the EXCLKS bit in the clock operation mode control register (CMC) to 0, set the XTSTOP bit in the clock operation status control register (CSC) to 1, and leave the pin open-circuit. Alternatively, provide the pin with an independent connection to V_{DD} or V_{SS} via a resistor.
P125 to P127	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.

Correct:

Table 2 - 3 Connections of Unused Pins

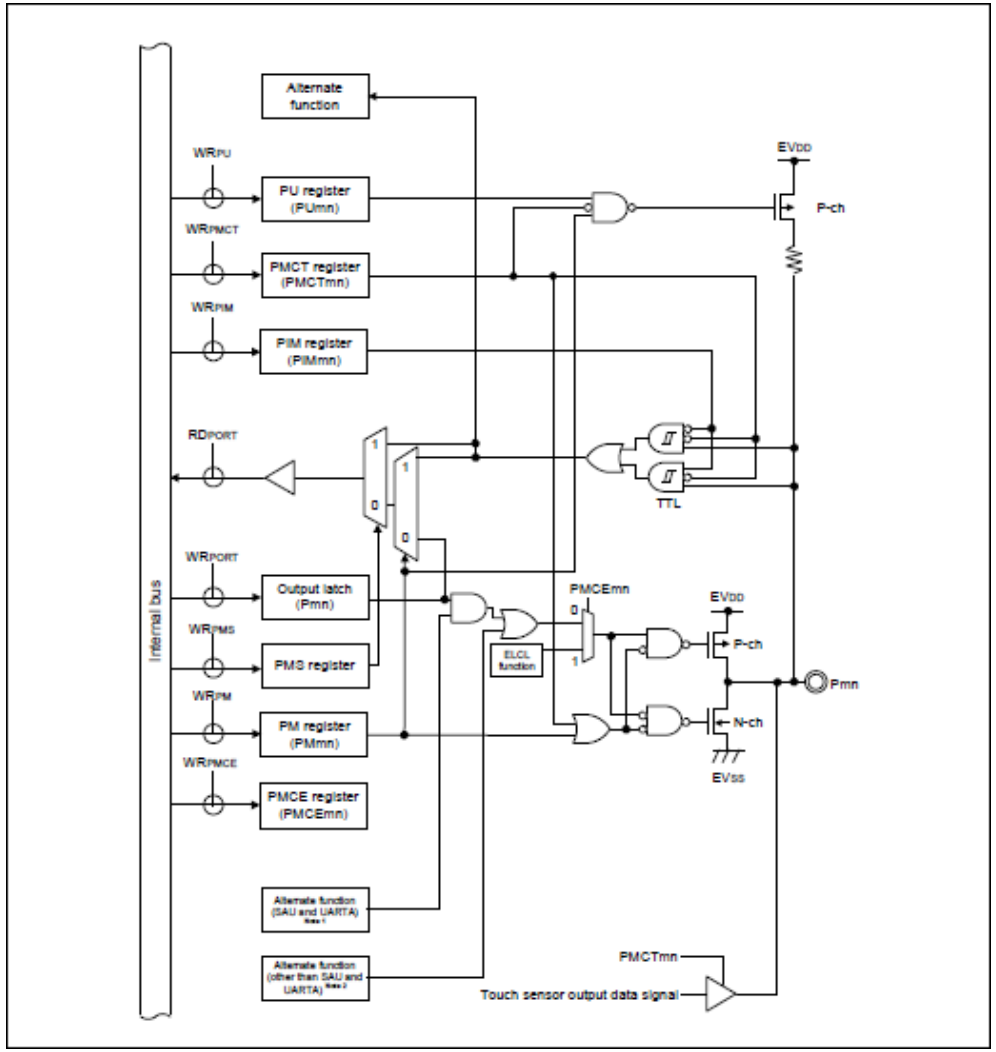
Pin Name	I/O	Recommended Connection of Unused Pins
P00 to P07	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P10 to P17		
P20 to P27		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P30 to P37		Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P40/TOOL0		Input: Independently connect to EV_{DD0}, EV_{DD1} or leave open. Output: Leave open.
P41 to P47		Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P50 to P57		
P60 to P63		Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Set the port's output latch to 0 and leave the pins open, or set the port's output latch to 1 and independently connect the pins to EV_{DD0} and EV_{DD1} or EV_{SS0} and EV_{SS1} via a resistor.
P64 to P67		Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.
P70 to P77		
P80 to P87		
P90 to P97		
P100 to P106		
P110 to P117		
P120		
P121, P122		Input: Independently connect to V_{DD} or V_{SS} via a resistor. Output: Leave open.
P123, P124	Input	Set the EXCLKS bit in the clock operation mode control register (CMC) to 0, set the XTSTOP bit in the clock operation status control register (CSC) to 1, and leave the pin open-circuit Note. Alternatively, provide the pin with an independent connection to V_{DD} or V_{SS} via a resistor.
P125 to P127	I/O	Input: Independently connect to EV_{DD0}, EV_{DD1} or EV_{SS0}, EV_{SS1} via a resistor. Output: Leave open.

Note When the low-speed on-chip oscillator clock (f_{IL}) is selected for the CPU/peripheral hardware clock frequency (f_{CLK}), the current may increase approximately by 1 μA.

16. Figure 2 - 25 Pin Block Diagram for Pin Type 8-31-1 (Page 96)

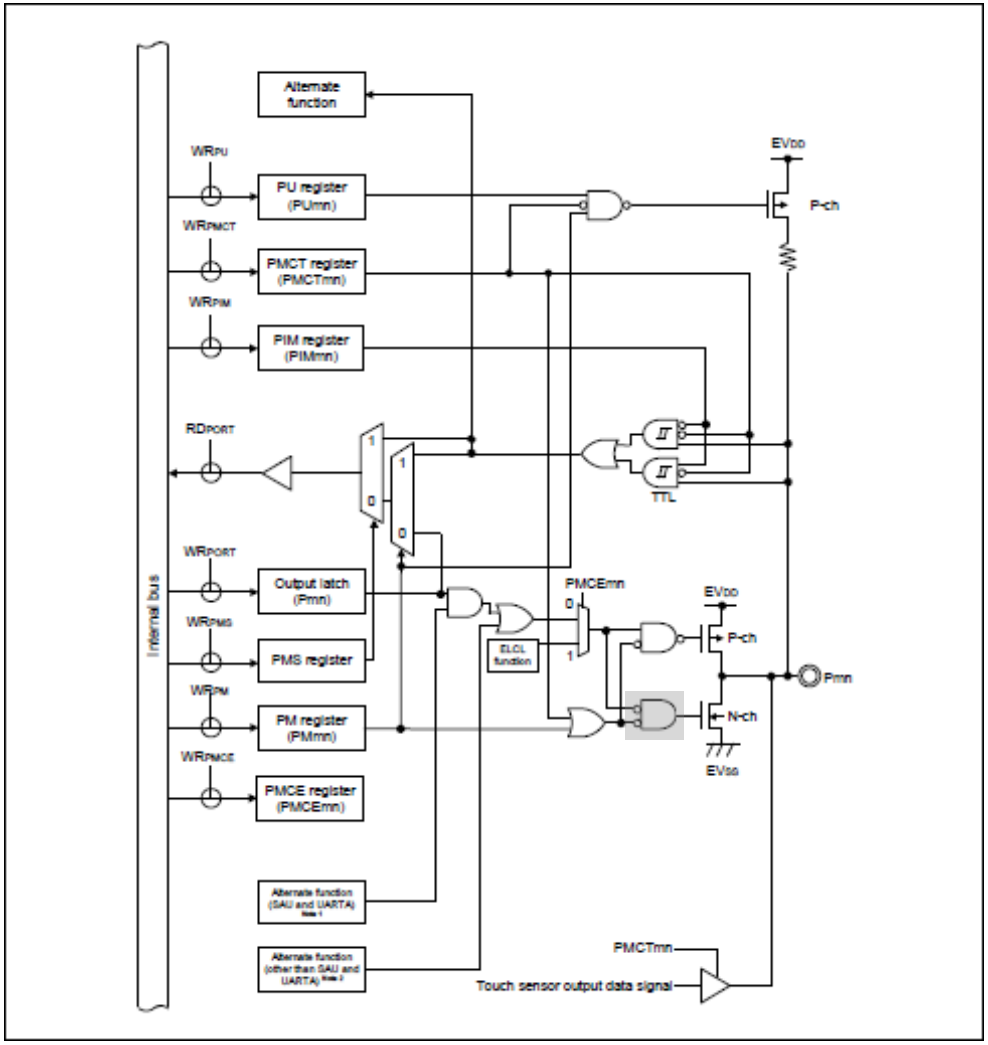
Incorrect:

Figure 2 - 25 Pin Block Diagram for Pin Type 8-31-1



Correct:

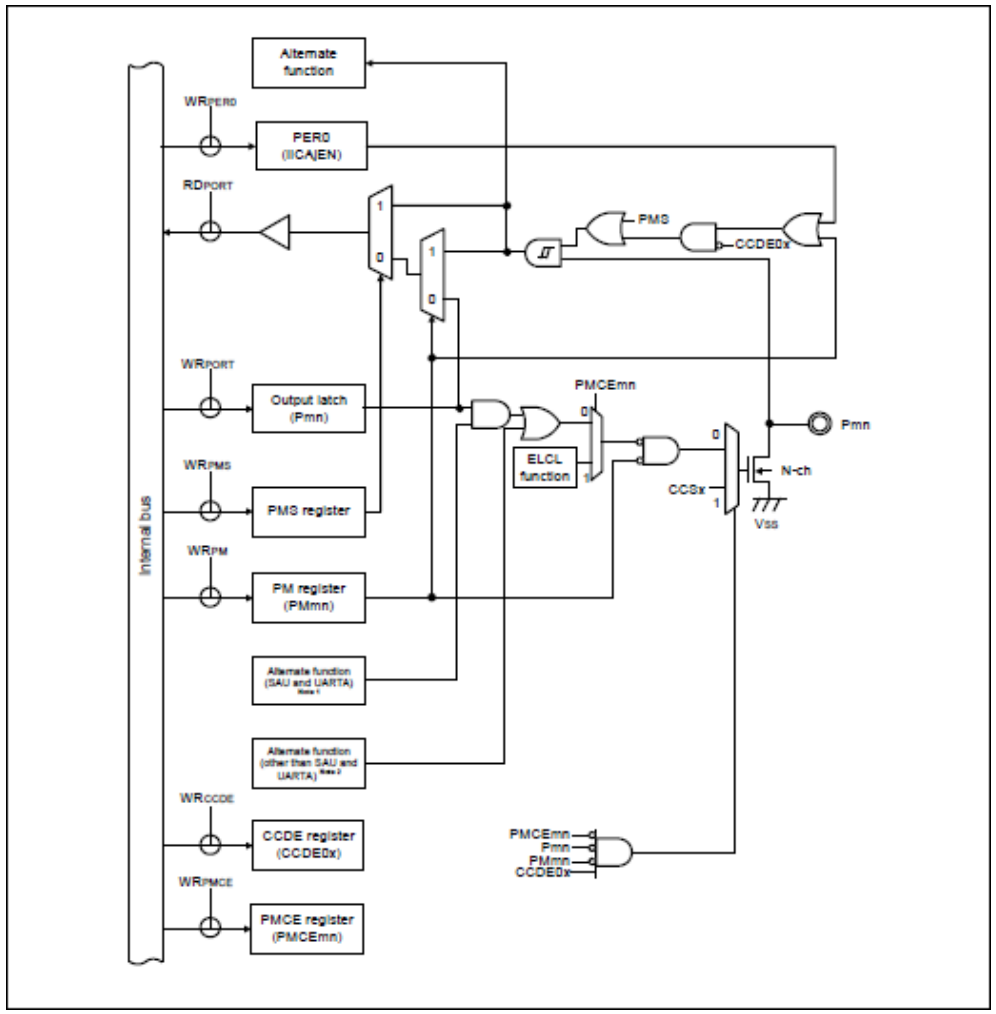
Figure 2 - 25 Pin Block Diagram for Pin Type 8-31-1



17. Figure 2 - 33 Pin Block Diagram for Pin Type 12-38-3 (Page 107)

Incorrect:

Figure 2 - 33 Pin Block Diagram for Pin Type 12-38-3



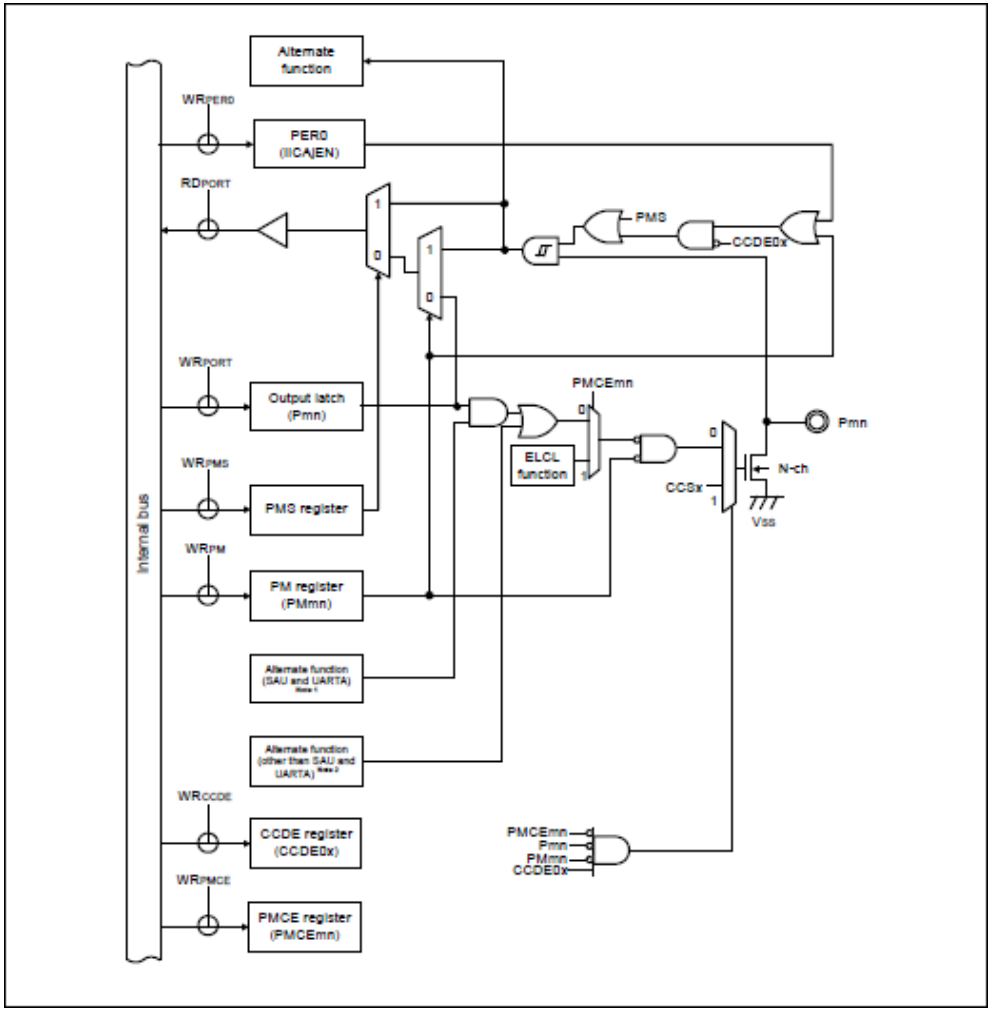
Note 1. This excludes the clock output from UARTA.

Note 2. This includes the clock output from UARTA.

Caution The input buffer is enabled even if the type 12-38-3 pin is operating as an output. This may lead to a through current flowing through the type 12-38-3 pin when the voltage level on this pin is intermediate.

Correct:

Figure 2 - 33 Pin Block Diagram for Pin Type 12-38-3



Note 1. This excludes the clock output from UARTA.

Note 2. This includes the clock output from UARTA.

Caution The input buffer is enabled when using the IICA with the IICAjEN bit in the PER0 register being set to 1. This may lead to a through current flowing through the type 12-38-3 pin when the voltage level on this pin is intermediate.

18. Table 3 - 8 List of Extended Special Function Registers (2nd SFRs) (2/15), PFCMD register (Page 139)

Incorrect:

Table 3 - 8 List of Extended Special Function Registers (2nd SFRs) (2/15)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F0063H	Port mode control A register 3	PMCA3	R/W	√	√	—	FFH
F006AH	Port mode control A register 10	PMCA10	R/W	√	√	—	FFH
F006BH	Port mode control A register 11	PMCA11	R/W	√	√	—	FFH
F006CH	Port mode control A register 12	PMCA12	R/W	√	√	—	FFH
F006EH	Port mode control A register 14	PMCA14	R/W	√	√	—	FFH
F006FH	Port mode control A register 15	PMCA15	R/W	√	√	—	FFH
F0070H	Noise filter enable register 0	NFEN0	R/W	√	√	—	00H
F0071H	Noise filter enable register 1	NFEN1	R/W	√	√	—	00H
F0072H	Noise filter enable register 2	NFEN2	R/W	√	√	—	00H
F0073H	Input switch control register	ISC	R/W	√	√	—	00H
F0074H	Timer input select register 0	TIS0	R/W	—	√	—	00H
F0075H	Timer input select register 1	TIS1	R/W	—	√	—	00H
F0077H	Peripheral I/O redirection register	PIOR	R/W	—	√	—	00H
F0078H	Invalid memory access detection control register	IAWCTL	R/W	—	√	—	00H
F0079H	UART loop back select register	ULBS	R/W	√	√	—	00H
F007BH	Port mode select register	PMS	R/W	√	√	—	00H
F007DH	Global digital input disable register	GDIDIS	R/W	√	√	—	00H
F0090H	Data flash control register	DFLCTL	R/W	√	√	—	00H
F00A0H	High-speed on-chip oscillator trimming register	HIOTRM	R/W	—	√	—	Undefined Note 1
F00A8H	High-speed on-chip oscillator frequency select register	HOCODIV	R/W	—	√	—	Undefined Note 2
F00AAH	Flash operating mode select register	FLMODE	R/W	√	√	—	40H/80H/C0H Note 3
F00ABH	Flash operating mode protect register	FLMWRP	R/W	√	√	—	00H
F00B0H	Flash security flag monitor register	FLSEC	R	—	—	√	Undefined
F00B2H	Flash FSW monitor register S	FLFSWS	R	—	—	√	Undefined
F00B4H	Flash FSW monitor register E	FLFSWE	R	—	—	√	Undefined
F00B6H	Flash memory sequencer initial setting register	FSSET	R/W	—	√	—	00H
F00B7H	Flash extra sequencer control register	FSSE	R/W	√	√	—	00H
F00C0H	Flash protect command register	PFCMD	R/W	—	√	—	—
F00C1H	Flash status register	PFS	R	√	√	—	00H

Correct:

Table 3 - 6 List of Extended Special Function Registers (2nd SFRs) (2/15)

Address	Special Function Register (SFR) Name	Symbol	R/W	Manipulable Bit Range			After Reset
				1-bit	8-bit	16-bit	
F0063H	Port mode control A register 3	PMCA3	R/W	√	√	—	FFH
F006AH	Port mode control A register 10	PMCA10	R/W	√	√	—	FFH
F006BH	Port mode control A register 11	PMCA11	R/W	√	√	—	FFH
F006CH	Port mode control A register 12	PMCA12	R/W	√	√	—	FFH
F006EH	Port mode control A register 14	PMCA14	R/W	√	√	—	FFH
F006FH	Port mode control A register 15	PMCA15	R/W	√	√	—	FFH
F0070H	Noise filter enable register 0	NFEN0	R/W	√	√	—	00H
F0071H	Noise filter enable register 1	NFEN1	R/W	√	√	—	00H
F0072H	Noise filter enable register 2	NFEN2	R/W	√	√	—	00H
F0073H	Input switch control register	ISC	R/W	√	√	—	00H
F0074H	Timer input select register 0	TIS0	R/W	—	√	—	00H
F0075H	Timer input select register 1	TIS1	R/W	—	√	—	00H
F0077H	Peripheral I/O redirection register	PIOR	R/W	—	√	—	00H
F0078H	Invalid memory access detection control register	IAWCTL	R/W	—	√	—	00H
F0079H	UART loop back select register	ULBS	R/W	√	√	—	00H
F007BH	Port mode select register	PMS	R/W	√	√	—	00H
F007DH	Global digital input disable register	GDIDIS	R/W	√	√	—	00H
F0090H	Data flash control register	DFLCTL	R/W	√	√	—	00H
F00A0H	High-speed on-chip oscillator trimming register	HIOTRM	R/W	—	√	—	Undefined Note 1
F00A8H	High-speed on-chip oscillator frequency select register	HOCODIV	R/W	—	√	—	Undefined Note 2
F00AAH	Flash operating mode select register	FLMODE	R/W	√	√	—	40H/80H/C0H Note 3
F00ABH	Flash operating mode protect register	FLMWRP	R/W	√	√	—	00H
F00B0H	Flash security flag monitor register	FLSEC	R	—	—	√	Undefined
F00B2H	Flash FSW monitor register S	FLFSWS	R	—	—	√	Undefined
F00B4H	Flash FSW monitor register E	FLFSWE	R	—	—	√	Undefined
F00B6H	Flash memory sequencer initial setting register	FSSET	R/W	—	√	—	00H
F00B7H	Flash extra are sequencer control register	FSSE	R/W	√	√	—	00H
F00C0H	Flash protect command register	PFCMD	W	—	√	—	Undefined
F00C1H	Flash status register	PFS	R	√	√	—	00H

19. Table 3 - 8 List of Extended Special Function Registers (2nd SFRs) (7/15), MIOTRM register (Page 144)

Incorrect:

Table 3 - 8 List of Extended Special Function Registers (2nd SFRs) (7/15)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F01E6H	Timer status register 13	TSR13L	TSR13	R	—	√	√	0000H
F01E7H		—			—	—		
F01E8H	Timer status register 14	TSR14L	TSR14	R	—	√	√	0000H
F01E9H		—			—	—		
F01EAH	Timer status register 15	TSR15L	TSR15	R	—	√	√	0000H
F01EBH		—			—	—		
F01ECH	Timer status register 16	TSR16L	TSR16	R	—	√	√	0000H
F01EDH		—			—	—		
F01EEH	Timer status register 17	TSR17L	TSR17	R	—	√	√	0000H
F01EFH		—			—	—		
F01F0H	Timer channel enable status register 1	TE1L	TE1	R	√	√	√	0000H
F01F1H		—			—	—		
F01F2H	Timer channel start register 1	TS1L	TS1	R/W	√	√	√	0000H
F01F3H		—			—	—		
F01F4H	Timer channel stop register 1	TT1L	TT1	R/W	√	√	√	0000H
F01F5H		—			—	—		
F01F6H	Timer clock select register 1	TPS1		R/W	—	—	√	0000H
F01F7H					—	—		
F01F8H	Timer output register 1	TO1L	TO1	R/W	—	√	√	0000H
F01F9H		—			—	—		
F01FAH	Timer output enable register 1	TOE1L	TOE1	R/W	√	√	√	0000H
F01FBH		—			—	—		
F01FCH	Timer output level register 1	TOL1L	TOL1	R/W	—	√	√	0000H
F01FDH		—			—	—		
F01FEH	Timer output mode register 1	TOM1L	TOM1	R/W	—	√	√	0000H
F01FFH		—			—	—		
F0212H	Middle-speed on-chip oscillator trimming register	MIOTRM		R/W	—	√	—	80H
F0213H	Low-speed on-chip oscillator trimming register	LIOTRM		R/W	—	√	—	80H

Correct:

Table 3 - 6 List of Extended Special Function Registers (2nd SFRs) (7/15)

Address	Special Function Register (SFR) Name	Symbol		R/W	Manipulable Bit Range			After Reset
					1-bit	8-bit	16-bit	
F01E6H	Timer status register 13	TSR13L	TSR13	R	—	√	√	0000H
F01E7H		—			—	—		
F01E8H	Timer status register 14	TSR14L	TSR14	R	—	√	√	0000H
F01E9H		—			—	—		
F01EAH	Timer status register 15	TSR15L	TSR15	R	—	√	√	0000H
F01EBH		—			—	—		
F01ECH	Timer status register 16	TSR16L	TSR16	R	—	√	√	0000H
F01EDH		—			—	—		
F01EEH	Timer status register 17	TSR17L	TSR17	R	—	√	√	0000H
F01EFH		—			—	—		
F01F0H	Timer channel enable status register 1	TE1L	TE1	R	√	√	√	0000H
F01F1H		—			—	—		
F01F2H	Timer channel start register 1	TS1L	TS1	R/W	√	√	√	0000H
F01F3H		—			—	—		
F01F4H	Timer channel stop register 1	TT1L	TT1	R/W	√	√	√	0000H
F01F5H		—			—	—		
F01F6H	Timer clock select register 1	TPS1		R/W	—	—	√	0000H
F01F7H					—	—		
F01F8H	Timer output register 1	TO1L	TO1	R/W	—	√	√	0000H
F01F9H		—			—	—		
F01FAH	Timer output enable register 1	TOE1L	TOE1	R/W	√	√	√	0000H
F01FBH		—			—	—		
F01FCH	Timer output level register 1	TOL1L	TOL1	R/W	—	√	√	0000H
F01FDH		—			—	—		
F01FEH	Timer output mode register 1	TOM1L	TOM1	R/W	—	√	√	0000H
F01FFH		—			—	—		
F0212H	Middle-speed on-chip oscillator trimming register	MIOTRM		R/W	—	√	—	90H
F0213H	Low-speed on-chip oscillator trimming register	LIOTRM		R/W	—	√	—	80H

20. 4.3.7 Port mode control A registers (PMCAxx) (Page 191)

Incorrect:

Figure 4 - 7 Format of Port Mode Control A Registers

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMCA0	1	1	1	1	PMCA03	PMCA02	PMCA01	PMCA00	F0060H	FFH	R/W
PMCA1	1	1	1	1	PMCA13	1	1	1	F0061H	FFH	R/W
PMCA2	PMCA27	PMCA26	PMCA25	PMCA24	PMCA23	PMCA22	PMCA21	PMCA20	F0062H	FFH	R/W
PMCA3	PMCA37	PMCA36	PMCA35	1	1	1	1	1	F0063H	FFH	R/W
PMCA10	1	1	1	1	1	1	1	PMCA100	F006AH	FFH	R/W
PMCA11	PMCA117	PMCA116	PMCA115	1	1	1	1	1	F006BH	FFH	R/W
PMCA12	1	1	1	1	1	1	1	PMCA120	F006CH	FFH	R/W
PMCA14	PMCA147	1	1	1	1	1	1	1	F006EH	FFH	R/W
PMCA15	1	PMCA156	PMCA155	PMCA154	PMCA153	PMCA152	PMCA151	PMCA150	F006FH	FFH	R/W

PMCAmn	Selection of digital I/O or analog input function for Pmn pin (m = 0 to 3, 10 to 12, 14, 15; n = 0 to 7)
0	Digital I/O
1	Analog input function

Caution 1. Select input mode by using port mode register 0 to 3, 10 to 12, 14, or 15 (PM0 to PM3, PM10 to PM12,
PM14, or PM15) for the port which is set to the analog input function by the PMCAxx register.

Caution 2. Do not set the pin that is specified as digital I/O by the PMCAxx register to the analog function by the
analog input channel specification register (ADS).

Caution 3. Be sure to set bits that are not implemented to their initial values.

Correct:

Figure 4 - 7 Format of Port Mode Control A Registers (PMCAxx)

Symbol	7	6	5	4	3	2	1	0	Address	After reset	R/W
PMCA0	1	1	1	1	PMCA03	PMCA02	PMCA01	PMCA00	F0060H	FFH	R/W
PMCA1	1	1	1	1	PMCA13	1	1	1	F0061H	FFH	R/W
PMCA2	PMCA27	PMCA26	PMCA25	PMCA24	PMCA23	PMCA22	PMCA21	PMCA20	F0062H	FFH	R/W
PMCA3	PMCA37	PMCA36	PMCA35	1	1	1	1	1	F0063H	FFH	R/W
PMCA10	1	1	1	1	1	1	1	PMCA100	F006AH	FFH	R/W
PMCA11	PMCA117	PMCA116	PMCA115	1	1	1	1	1	F006BH	FFH	R/W
PMCA12	1	1	1	1	1	1	1	PMCA120	F006CH	FFH	R/W
PMCA14	PMCA147	1	1	1	1	1	1	1	F006EH	FFH	R/W
PMCA15	1	PMCA156	PMCA155	PMCA154	PMCA153	PMCA152	PMCA151	PMCA150	F006FH	FFH	R/W

PMCAmn	Selection of digital I/O or analog input function for Pmn pin (m = 0 to 3, 10 to 12, 14, 15; n = 0 to 7)
0	Digital I/O
1	Analog input function

Caution 1. Select input mode by using port mode register 0 to 3, 10 to 12, 14, or 15 (PM0 to PM3, PM10 to PM12,
PM14, or PM15) for the port which is set to the analog input function by the PMCAxx register.

Caution 2. Do not set the pin that is specified as digital I/O by the PMCAxx register to the analog function by the
analog input channel specification register (ADS).

Caution 3. Be sure to set bits that are not implemented to their initial values.

Caution 4. The PMCA3, PMCA10, PMCA11, and PMCA15 registers in the 30- to 64-pin package products with 96 or 128 Kbytes of flash memory return 00H when read.

21. 4.5.4 Examples of register settings for port and alternate functions (Page 211)

Incorrect:

4.5.4 Examples of register settings for port and alternate functions

Examples of register settings for port and alternate functions are shown in Table 4 - 7 and Table 4 - 8. The registers used to control the port functions should be set as shown in Table 4 - 7 and Table 4 - 8. See the following remark for legends used in Table 4 - 7 and Table 4 - 8.

Remark —: Not supported
×: Don't care
PIOR: Peripheral I/O redirection register
POMxx: Port output mode registers
PMCAxx: Port mode control A registers
PMCTxx: Port mode control T registers
PMCEx: Port mode control E registers
CCDE: Output current control enable register
CCSx: Output current select registers
PMxx: Port mode registers
Pxx: Port output latch
Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR).

Correct:

4.5.4 Examples of register settings for port and alternate functions

Examples of register settings for port and alternate functions are shown in Table 4 - 7 and Table 4 - 8. The registers used to control the port functions should be set as shown in Table 4 - 7 and Table 4 - 8. See the following remark for legends used in Table 4 - 7 and Table 4 - 8.

Remark —: Not supported
×: Don't care
PIOR: Peripheral I/O redirection register
POMxx: Port output mode registers
PMCAxx: Port mode control A registers
PMCTxx: Port mode control T registers
PMCEx: Port mode control E registers
CCDE: Output current control enable register
CCSx: Output current select registers
PMxx: Port mode registers
Pxx: Port output latch
Functions in parentheses can be assigned via settings in the peripheral I/O redirection register (PIOR).

Caution In examples of register settings, the port digital input disable register (PDIDISxx) is set for input to the input buffer being enabled.

22. Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (4/17) (Page 215)

Incorrect:

Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (4/17)

Pin Name	Function Used		PIOR	POMxx	PMCAxx	PMCExx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)								
P13	P13	Input	—	x	0	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√
		Output	—	0	0	0	—	—	0	0/1	TxD2/ SO20 = 1	(TO04) = 0 (SDAA0) = 0								
		N-ch open drain output	—	1	0	0	—	—	0	0/1										
	EO13	Output	—	0/1	0	1	—	—	0	x	x	x	√	√	√	√	√	√	√	√
	TxD2	Output	PIOR1 = 0	0/1	0	0	—	—	0	1	x	(TO04) = 0 (SDAA0) = 0	√	√	√	√	√	√	√	√
	SO20	Output	PIOR1 = 0	0/1	0	0	—	—	0	1	x	(TO04)= 0 (SDAA0)= 0	√	√	√	√	√	√	√	√
	(SDAA0)	I/O	PIOR2 = 1	1	0	0	—	—	0	0	x	(TO04) = 0	√	√	√	√	√	√	√	√
	(TI04)	Input	PIOR0 = 1	x	0	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√
	(TO04)	Output	PIOR0 = 1	0	0	0	—	—	0	0	x	(SDAA0) = 0	√	√	√	√	√	√	√	√
	IVREF0	Analog input	—	x	1	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√

Correct:

Table 4 - 7 Examples of Register and Output Latch Settings for Alternate Functions (30-Pin to 64-Pin Products with 96-Kbyte or 128-Kbyte Flash Memory) (4/17)

Pin Name	Function Used		PIOR	POMxx	PMCAxx	PMCExx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)								
P13	P13	Input	—	x	0	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√
		Output	—	0	0	0	—	—	0	0/1	TxD2/ SO20 = 1	(TO04) = 0 (SDAA0) = 0								
		N-ch open drain output	—	1	0	0	—	—	0	0/1										
	EO13	Output	—	0/1	0	1	—	—	0	x	x	x	√	√	√	√	√	√	√	√
	TxD2	Output	PIOR1 = 0	0/1	0	0	—	—	0	1	x	(TO04) = 0 (SDAA0) = 0	√	√	√	√	√	√	√	√
	SO20	Output	PIOR1 = 0	0/1	0	0	—	—	0	1	x	(TO04)= 0 (SDAA0)= 0	√	√	√	√	√	√	√	√
	(SDAA0)	I/O	PIOR2 = 1	1	0	0	—	—	0	0	x	(TO04) = 0	√	√	√	√	√	√	√	√
	(TI04)	Input	PIOR0 = 1	x	0	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√
	(TO04)	Output	PIOR0 = 1	0	0	0	—	—	0	0	x	(SDAA0) = 0	√	√	√	√	√	√	√	√
	IVREF1	Analog input	—	x	1	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√

23. Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (1/21) (Page 228)

Incorrect:

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (1/21)

Pin Name	Function Used		PIOR	POMxx	PMCAxx	PMCTxx	PMCExx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin
	Function Name	I/O								SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)											
P00	P00	Input	—	X	0Note 1	0	—	1	X	X	—	√	√	√	√	√	√	√	√	√	√	√
		Output	—	0	0Note 1	0	—	0	0/1	TxD1 = 1 Note 2	—											
		N-ch open drain output	—	1	0Note 1	0	—	0	0/1													
	ANI17	Analog input	—	X	1	0	—	1	X	X	—	√	√	—	—	—	—	—	—	—	—	—
	TS26	I/O	—	X	0Note 1	1	—	1	X	X	—	√	√	√	√	√	√	√	√	√	√	√
	EI00	Input	—	X	0Note 1	0	—	1	X	X	—	√	√	√	√	√	√	√	√	√	√	√
	TI00	Input	—	X	0Note 1	0	—	1	X	X	—	√	√	√	√	√	√	√	√	√	√	√
	TxD1	Output	—	0/1	0Note 1	0	—	0	1	X	—	√	√	√	√	√	√	—	—	—	—	—
P01	P01	Input	—	—	0Note 1	0	0	1	X	—	X	√	√	√	√	√	√	√	√	√	√	√
		Output	—	—	0Note 1	0	0	0	0/1	—	TO00 = 0											
	ANI16	Analog input	—	—	1	0	0	1	X	—	X	√	√	—	—	—	—	—	—	—	—	—
	TS27	I/O	—	—	0Note 1	1	0	1	X	—	X	√	√	√	√	√	√	√	√	√	√	√
	EI01	Input	—	—	0Note 1	0	0	1	X	—	X	√	√	√	√	√	√	√	√	√	√	√
	EO01	Output	—	—	0Note 1	0	1	0	X	—	X	√	√	√	√	√	√	√	√	√	√	√
	TO00	Output	—	—	0Note 1	0	0	0	0	—	X	√	√	√	√	√	√	√	√	√	√	√
	RxD1	Input	—	—	0Note 1	0	0	1	X	—	X	√	√	√	√	√	√	—	—	—	—	—
P02	P02	Input	—	X	0	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
		Output	—	0	0	0	—	0	0/1	TxD1 = 1 SO10 = 1 Note 4	—											
		N-ch open drain output	—	1	0	0	—	0	0/1													
	ANI17	Analog input	—	X	1	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	TS28	Output	—	X	0	1	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	TxD1	Output	PIORS = 0 Note 3	0/1	0	0	—	0	1	X	—	—	—	—	—	—	—	√	√	√	√	√
	SO10	Output	PIORS = 0 Note 3	0/1	0	0	—	0	1	X	—	—	—	—	—	—	—	√	√	√	√	√
P03	P03	Input	—	X	0	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
		Output	—	0	0	0	—	0	0/1	SDA10 = 1 Note 4	—											
		N-ch open drain output	—	1	0	0	—	0	0/1													
	ANI16	Analog input	—	X	1	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	TS29	Output	—	X	0	1	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	SI10	Input	PIORS = 0 Note 3	X	0	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	RxD1	Input	PIORS = 0 Note 3	X	0	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	SDA10	I/O	PIORS = 0 Note 3	1	0	0	—	0	1	X	—	—	—	—	—	—	—	√	√	√	√	√

Correct:

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (1/21)

Pin Name	Function Used		PIOR	POMxx	PMCAxx	PMCTxx	PMCExx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin
	Function Name	I/O								SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)											
P00	P00	Input	—	X	0Note 1	0	—	1	X	X	—	√	√	√	√	√	√	√	√	√	√	√
		Output	—	0	0Note 1	0	—	0	0/1	TxD1 = 1 Note 2	—											
		N-ch open drain output	—	1	0Note 1	0	—	0	0/1													
	ANI17	Analog input	—	X	1	0	—	1	X	X	—	√	√	—	—	—	—	—	—	—	—	—
	TS26	I/O	—	X	0Note 1	1	—	1	X	X	—	√	√	√	√	√	√	√	√	√	√	√
	EI00	Input	—	X	0Note 1	0	—	1	X	X	—	√	√	√	√	√	√	√	√	√	√	√
	TI00	Input	—	X	0Note 1	0	—	1	X	X	—	√	√	√	√	√	√	√	√	√	√	√
	TxD1	Output	—	0/1	0Note 1	0	—	0	1	X	—	√	√	√	√	√	√	—	—	—	—	—
P01	P01	Input	—	—	0Note 1	0	0	1	X	—	X	√	√	√	√	√	√	√	√	√	√	√
		Output	—	—	0Note 1	0	0	0	0/1	—	TO00 = 0											
	ANI16	Analog input	—	—	1	0	0	1	X	—	X	√	√	—	—	—	—	—	—	—	—	—
	TS27	I/O	—	—	0Note 1	1	0	1	X	—	X	√	√	√	√	√	√	√	√	√	√	√
	EI01	Input	—	—	0Note 1	0	0	1	X	—	X	√	√	√	√	√	√	√	√	√	√	√
	EO01	Output	—	—	0Note 1	0	1	0	X	—	X	√	√	√	√	√	√	√	√	√	√	√
	TO00	Output	—	—	0Note 1	0	0	0	0	—	X	√	√	√	√	√	√	√	√	√	√	√
	RxD1	Input	—	—	0Note 1	0	0	1	X	—	X	√	√	√	√	√	√	—	—	—	—	—
P02	P02	Input	—	X	0	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
		Output	—	0	0	0	—	0	0/1	TxD1 = 1 SO10 = 1 Note 4	—											
		N-ch open drain output	—	1	0	0	—	0	0/1													
	ANI17	Analog input	—	X	1	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	TS28	I/O	—	X	0	1	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	TxD1	Output	PIORS = 0 Note 3	0/1	0	0	—	0	1	X	—	—	—	—	—	—	—	√	√	√	√	√
	SO10	Output	PIORS = 0 Note 3	0/1	0	0	—	0	1	X	—	—	—	—	—	—	—	√	√	√	√	√
P03	P03	Input	—	X	0	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
		Output	—	0	0	0	—	0	0/1	SDA10 = 1 Note 4	—											
		N-ch open drain output	—	1	0	0	—	0	0/1													
	ANI16	Analog input	—	X	1	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	TS29	I/O	—	X	0	1	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	SI10	Input	PIORS = 0 Note 3	X	0	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	RxD1	Input	PIORS = 0 Note 3	X	0	0	—	1	X	X	—	—	—	—	—	—	—	√	√	√	√	√
	SDA10	I/O	PIORS = 0 Note 3	1	0	0	—	0	1	X	—	—	—	—	—	—	—	√	√	√	√	√

24. Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (4/21) (Page 231)

Incorrect:

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (4/21)

Pin Name	Function Used		PIOR	POMxx	PMCAxx	PMCBx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)											
P13	P13	Input	—	x	0	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√	√	√	√
		Output	—	0	0	0	—	—	0	0/1	TxD2/ SO20 = 1	(TO04) = 0 (SDAA0) = 0											
		N-ch open drain output	—	1	0	0	—	—	0	0/1													
	EO13	Output	—	0/1	0	1	—	—	0	x	x	x	√	√	√	√	√	√	√	√	√	√	√
	TxD2	Output	PIOR1 = 0	0/1	0	0	—	—	0	1	x	(TO04) = 0 (SDAA0) = 0	√	√	√	√	√	√	√	√	√	√	√
	SO20	Output	PIOR1 = 0	0/1	0	0	—	—	0	1	x	(TO04) = 0 (SDAA0) = 0	√	√	√	√	√	√	√	√	√	√	√
	(SDAA0)	I/O	PIOR2 = 1	1	0	0	—	—	0	0	x	(TO04) = 0	√	√	√	√	√	√	√	√	√	√	√
	(TI04)	Input	PIOR0 = 1	x	0	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√	√	√	√
	(TO04)	Output	PIOR0 = 1	0	0	0	—	—	0	0	x	(SDAA0) = 0	√	√	√	√	√	√	√	√	√	√	√
	IVREF0	Analog input	—	x	1	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√	√	√	√

Correct:

Table 4 - 8 Examples of Register and Output Latch Settings for Alternate Functions (Products with 192-Kbyte to 768-Kbyte Flash Memory and 80-Pin and 100-Pin Products with 128-Kbyte Flash Memory) (4/21)

Pin Name	Function Used		PIOR	POMxx	PMCAxx	PMCBx	CCDE	CCSx	PMxx	Pxx	Alternate Function Output		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin	52-pin	64-pin	80-pin	100-pin	128-pin
	Function Name	I/O									SAU and UARTA (excluding clock output from the UARTA)	Other than SAU and UARTA (including clock output from the UARTA)											
P13	P13	Input	—	x	0	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√	√	√	√
		Output	—	0	0	0	—	—	0	0/1	TxD2/ SO20 = 1	(TO04) = 0 (SDAA0) = 0											
		N-ch open drain output	—	1	0	0	—	—	0	0/1													
	EO13	Output	—	0/1	0	1	—	—	0	x	x	x	√	√	√	√	√	√	√	√	√	√	√
	TxD2	Output	PIOR1 = 0	0/1	0	0	—	—	0	1	x	(TO04) = 0 (SDAA0) = 0	√	√	√	√	√	√	√	√	√	√	√
	SO20	Output	PIOR1 = 0	0/1	0	0	—	—	0	1	x	(TO04) = 0 (SDAA0) = 0	√	√	√	√	√	√	√	√	√	√	√
	(SDAA0)	I/O	PIOR2 = 1	1	0	0	—	—	0	0	x	(TO04) = 0	√	√	√	√	√	√	√	√	√	√	√
	(TI04)	Input	PIOR0 = 1	x	0	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√	√	√	√
	(TO04)	Output	PIOR0 = 1	0	0	0	—	—	0	0	x	(SDAA0) = 0	√	√	√	√	√	√	√	√	√	√	√
	IVREF1	Analog input	—	x	1	0	—	—	1	x	x	x	√	√	√	√	√	√	√	√	√	√	√

25. Figure 6 - 9 Format of Subsystem Clock Supply Mode Control Register (OSMC) (Page 282)

Incorrect:

Figure 6 - 9 Format of Subsystem Clock Supply Mode Control Register (OSMC)

Address: F00F3H
After reset: Undefined
R/W: R/W Note 1

Symbol	<7>	6	5	<4>	3	2	1	<0>
OSMC	RTCLPC	0	0	WUTMMCK 0	x	x	0	HIPREC

RTCLPC Note 4	Setting in STOP mode or in HALT mode while the CPU is operating with the subsystem clock.
0	Enables supply of the subsystem clock to peripheral functions (See **Table 23 - 1** to **Table 23 - 4** for peripheral functions whose operations are enabled.)
1	Stops supply of the subsystem clock to peripheral functions other than the realtime clock.

WUTMMCK0	Selection of the operating clock for the realtime clock, 32-bit interval timer, serial interfaces UARTA0 and UARTA1, remote control signal receiver, and clock output/buzzer output controller
0	Subsystem clock X
1	Low-speed on-chip oscillator clock Notes 2, 3

HIPREC	State of the high-speed on-chip oscillator clock Notes 6, 8
0	The high-speed on-chip oscillator clock is being started at high speed and waiting for the precision of its oscillation to become stable is in progress. Note 7
1	The high-speed on-chip oscillator clock is operating with high precision.

Correct:

Figure 6 - 9 Format of Subsystem Clock Supply Mode Control Register (OSMC)

Address: F00F3H
After reset: Undefined
R/W: R/W Note 1

Symbol	<7>	6	5	<4>	3	2	1	<0>
OSMC	RTCLPC	0	0	WUTMMCK 0	x	x	0	HIPREC

RTCLPC Note 4	Setting in STOP mode or in HALT mode while the CPU is operating with the subsystem clock X
0	Enables supply of the subsystem clock X to peripheral functions (See **Table 23 - 1** to **Table 23 - 4** for peripheral functions whose operations are enabled.)
1	Stops supply of the subsystem clock to peripheral functions other than the realtime clock.

WUTMMCK0	Selection of the operating clock for the realtime clock, 32-bit interval timer, serial interfaces UARTA0 and UARTA1, remote control signal receiver, and clock output/buzzer output controller
0	Subsystem clock X
1	Low-speed on-chip oscillator clock Notes 2, 3

HIPREC	State of the high-speed on-chip oscillator clock Notes 5, 6
0	The high-speed on-chip oscillator clock is being started at high speed and waiting for the precision of its oscillation to become stable is in progress. Note 7
1	The high-speed on-chip oscillator clock is operating with high precision.

26. 9.2.11 Interval timer status register (ITLS0) (Page 483)

Incorrect:

Figure 9 - 12 Format of Interval Timer Status Register (ITLS0)

Address: F036BH
After reset: 00H
R/W: R/W Note

Symbol	7	6	5	4	3	2	1	0
ITLS0	0	0	0	ITF0C	ITF03	ITF02	ITF01	ITF00

ITF0C	Capture detection flag
0	Completion of capturing has not been detected.
1	Completion of capturing has been detected.

ITF03	Compare match detection flag for channel 3
0	A compare match signal has not been detected in channel 3.
1	A compare match signal has been detected in channel 3.

ITF02	Compare match detection flag for channel 2
0	A compare match signal has not been detected in channel 2.
1	A compare match signal has been detected in channel 2.

ITF01	Compare match detection flag for channel 1
0	A compare match signal has not been detected in channel 1.
1	A compare match signal has been detected in channel 1.

ITF00	Compare match detection flag for channel 0
0	A compare match signal has not been detected in channel 0.
1	A compare match signal has been detected in channel 0.

Note Writing 1 to each bit is ignored. To clear the ITF0C or ITF0i bit, write 0 to the desired bit and 1 to the other bits by using an 8-bit memory manipulation instruction.

Caution If the value of the ITLS0 register is other than 00H, the interrupt request flag (ITLIF bit) is not set even when a compare match for the channel currently having that event or completion of capture is detected. That is, an interrupt is not generated in such cases. For this reason, when clearing the detection flags, check all channels that are in use and set the ITLS0 register to 00H.

Correct:

Figure 9 - 12 Format of Interval Timer Status Register (ITLS0)

Address: F036BH
After reset: 00H
R/W: R/W Note

Symbol	7	6	5	4	3	2	1	0
ITLS0	0	0	0	ITF0C	ITF03	ITF02	ITF01	ITF00

ITF0C	Capture detection flag
0	Completion of capturing has not been detected.
1	Completion of capturing has been detected.

ITF03	Compare match detection flag for channel 3
0	A compare match signal has not been detected in channel 3.
1	A compare match signal has been detected in channel 3.

ITF02	Compare match detection flag for channel 2
0	A compare match signal has not been detected in channel 2.
1	A compare match signal has been detected in channel 2.

ITF01	Compare match detection flag for channel 1
0	A compare match signal has not been detected in channel 1.
1	A compare match signal has been detected in channel 1.

ITF00	Compare match detection flag for channel 0
0	A compare match signal has not been detected in channel 0.
1	A compare match signal has been detected in channel 0.

Note Writing 1 to each bit is ignored. To clear the ITF0C or ITF0i bit (i = 0, 1, 2, 3), write 0 to the desired bit and 1 to the other bits by using an 8-bit memory manipulation instruction.

Caution 1. If clearing any of the ITF0C, ITF03, ITF02, ITF01, ITF00 flag bits to 0 does not lead to the value of the ITLS0 register becoming 00H, an interrupt request (INTITL) is generated and the interrupt request flag (ITLIF) is set to 1.

Caution 2. To clear a flag bit in the ITLS0 register to 0, only write 0 to a bit that has the setting 1. This is because writing 0 to a bit that has the setting 0 may make detecting a compare match signal or capture detection signal generated at the same time as the writing of 0 impossible. For example, when the ITF01 flag bit is set to 1, write 00011101B to the ITLS0 register to clear the ITF01 flag bit.

27. Table 12 - 3 A/D Conversion Time Selection (3/8) (Page 527)

Incorrect:

Table 12 - 3 A/D Conversion Time Selection (3/8)

(3) When there is A/D power supply stabilization wait time

Normal mode 1 and 2 (for software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay Note 2	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V			
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	4 f_{AD}	64 f_{AD}	4 f_{AD}	2304/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	72 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	64 f_{AD}	4 f_{AD}	1152/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	72 µs	36 µs
0	0	1	0				f_{CLK}/8	6 f_{AD}	64 f_{AD}	4 f_{AD}	592/f_{CLK}	Setting prohibited	Setting prohibited	74 µs	37 µs	18.5 µs
0	0	1	1				f_{CLK}/4	10 f_{AD}	64 f_{AD}	4 f_{AD}	312/f_{CLK}	Setting prohibited	Setting prohibited	39 µs	19.5 µs	9.75 µs
0	1	0	0				f_{CLK}/2	18 f_{AD}	64 f_{AD}	4 f_{AD}	172/f_{CLK}	Setting prohibited	Setting prohibited	21.5 µs	10.75 µs	5.375 µs
0	1	0	1				f_{CLK}	34 f_{AD}	64 f_{AD}	4 f_{AD}	102/f_{CLK}	Setting prohibited	Setting prohibited	12.75 µs	6.375 µs	3.1875 µs
1	0	1	1				f_{CLK}/4	4 f_{AD}	64 f_{AD}	4 f_{AD}	288/f_{CLK}	288 µs	72 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	0				f_{CLK}/2	4 f_{AD}	64 f_{AD}	4 f_{AD}	144/f_{CLK}	144 µs	36 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	64 f_{AD}	4 f_{AD}	74/f_{CLK}	74 µs	18.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above						Setting prohibited										

Correct:

Table 12 - 3 A/D Conversion Time Selection (3/8)

(3) When there is A/D power supply stabilization wait time

Normal mode 1 and 2 (for software trigger wait select mode and hardware trigger wait select mode[Note 1])

A/D Converter Mode Register 0 A/D Converter Mode Register 1						Mode	Conversion Clock (f_{AD})	Number of Clock Cycles for A/D Power Supply Stabilization Wait	Number of Clock Cycles for Conversion	Number of Clock Cycles for Interrupt Output Delay Note 2	A/D Conversion Time (A/D Power Supply Stabilization Wait Time + Conversion Time + Interrupt Output Delay Time)				
(ADM1)	(ADM0)											2.4 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V			
ADLSP	FR2	FR1	FR0	LV1	LV0							f_{CLK} = 1 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz
0	0	0	0	0	0	Normal 1	f_{CLK}/32	4 f_{AD}	64 f_{AD}	4 f_{AD}	2304/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	72 µs
0	0	0	1				f_{CLK}/16	4 f_{AD}	64 f_{AD}	4 f_{AD}	1152/f_{CLK}	Setting prohibited	Setting prohibited	Setting prohibited	72 µs	36 µs
0	0	1	0				f_{CLK}/8	6 f_{AD}	64 f_{AD}	4 f_{AD}	592/f_{CLK}	Setting prohibited	Setting prohibited	74 µs	37 µs	18.5 µs
0	0	1	1				f_{CLK}/4	10 f_{AD}	64 f_{AD}	4 f_{AD}	312/f_{CLK}	Setting prohibited	Setting prohibited	39 µs	19.5 µs	9.75 µs
0	1	0	0				f_{CLK}/2	18 f_{AD}	64 f_{AD}	4 f_{AD}	172/f_{CLK}	Setting prohibited	Setting prohibited	21.5 µs	10.75 µs	5.375 µs
0	1	0	1				f_{CLK}	34 f_{AD}	64 f_{AD}	4 f_{AD}	102/f_{CLK}	Setting prohibited	Setting prohibited	12.75 µs	6.375 µs	3.1875 µs
1	0	1	1				f_{CLK}/4	4 f_{AD}	64 f_{AD}	4 f_{AD}	288/f_{CLK}	Setting prohibited	72 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	0				f_{CLK}/2	4 f_{AD}	64 f_{AD}	4 f_{AD}	144/f_{CLK}	Setting prohibited	36 µs	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	1				f_{CLK}	6 f_{AD}	64 f_{AD}	4 f_{AD}	74/f_{CLK}	74 µs	18.5 µs	Setting prohibited	Setting prohibited	Setting prohibited
Other than the above						Setting prohibited										

28. 12.3.6 12-bit/10-bit A/D conversion result register (ADCRn) (Page 543)

Incorrect:

Figure 12 - 10 Format of 12-bit/10-bit A/D Conversion Result Register (ADCRn)

Address: FFF1FH, FFF1EH (ADCR)Note, F0021H, F0020H (ADCR0)Note, F0023H, F0022H (ADCR1), F0025H, F0024H (ADCR2), F0027H, F0026H (ADCR3)
After reset: 0000H
R/W: R

When A/D conversion with 12-bit resolution is selected

	FFF1FH (for ADCR)								FFF1EH (for ADCR)							
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCRn (n = 0 to 3)	0	0	0	0												

When A/D conversion with 10-bit resolution is selected

	FFF1FH (for ADCR)								FFF1EH (for ADCR)							
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCRn (n = 0 to 3)											0	0	0	0	0	0

Note The contents of the ADCR register are stored in the ADCR0 register.

Caution 1. When 8-bit resolution A/D conversion is selected (when the ADTYP1 and ADTYP0 bits of A/D converter mode register 2 (ADM2) are respectively set to 01) and the ADCRn register is read, 0 is read from the bits other than the higher 8 bits.

Caution 2. When the ADCRn register is accessed in 16-bit units, and A/D conversion with 10-bit resolution is selected, the higher 10 bits of the conversion result are read in order starting at bit 15 of the ADCRn register. When A/D conversion with 12-bit resolution is selected, the higher 12 bits of the conversion result are read in order starting at bit 11 of the ADCRn register.

Correct:

Figure 12 - 10 Format of 12-bit/10-bit A/D Conversion Result Register (ADCRn)

Address: FFF1FH, FFF1EH (ADCR)Note, F0021H, F0020H (ADCR0)Note, F0023H, F0022H (ADCR1), F0025H, F0024H (ADCR2), F0027H, F0026H (ADCR3)
After reset: 0000H
R/W: R

When A/D conversion with 12-bit resolution is selected

	FFF1FH (for ADCR)								FFF1EH (for ADCR)							
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCRn (n = 0 to 3)	0	0	0	0												

When A/D conversion with 10-bit resolution is selected

	FFF1FH (for ADCR)								FFF1EH (for ADCR)							
Symbol	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCRn (n = 0 to 3)											0	0	0	0	0	0

Note The contents of the ADCR register are stored in the ADCR0 register.

Caution 1. When 8-bit resolution A/D conversion is selected (when the ADTYP1 and ADTYP0 bits of A/D converter mode register 2 (ADM2) are respectively set to 01) and the ADCRn register is read, 0 is read from the bits other than the higher 8 bits.

Caution 2. When the ADCRn register is accessed in 16-bit units, and A/D conversion with 10-bit resolution is selected, the higher 10 bits of the conversion result are read in order starting at bit 15 of the ADCRn register. When A/D conversion with 12-bit resolution is selected, the higher 12 bits of the conversion result are read in order starting at bit 11 of the ADCRn register.

Caution 3. When writing to any of the following registers, the contents of the ADCRnH register may become undefined:

A/D converter mode register 0 (ADM0), analog input channel specification register (ADS), port mode control A registers 0, 2, 3, 10, 11, 12, 14, and 15 (PMCA0, PMCA2, PMCA3, PMCA10, PMCA11, PMCA12, PMCA14, and PMCA15), port mode control T registers 0, 2, and 15 (PMCT0, PMCT2, and PMCT15), and port mode control E register 0 (PMCE0)

Read the conversion result following conversion completion before writing to the ADM0, ADS, PMCAxx, PMCTxx, or PMCEx register. Using timing other than the above may cause an incorrect conversion result to be read.

29. Figure 12 - 12 Format of Analog Input Channel Specification Register (ADS) (Page 546)

Incorrect:

Figure 12 - 12 Format of Analog Input Channel Specification Register (ADS)
<Select mode (ADMD = 0)> (2/2)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	1	1	0	1	1	Setting prohibited	
1	0	0	0	0	0	—	Temperature sensor output voltage
1	0	0	0	0	1	—	Internal reference voltage Note 3
Other than the above						Setting prohibited	

Caution 1. Be sure to clear bits 6 and 5 to 0.

Caution 2. Set the channel that is specified as the analog input by a PMCAxx, PMCTxx, or PMCEx register to the input mode by using port mode registers 0, 2, 3, 10 to 12, 14, or 15 (PM0, PM2, PM3, PM10 to PM12, PM14, PM15).

Caution 3. When specifying an input channel by the ADS register, do not select the pin that is specified as digital I/O by port mode control A register 0, 2, 3, 10, 11, 12, 14, or 15 (PMCA0, PMCA2, PMCA3, PMCA10, PMCA11, PMCA12, PMCA14, or PMCA15), port mode control T register 0, 2, or 15 (PMCT0, PMCT2, or PMCT15), or port mode control E register 0 (PMCE0).

Caution 4. Rewrite the value of the ADISS bit while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 5. If using AVREFP as the + side reference voltage of the A/D converter, do not select ANI0 as an A/D conversion channel.

Caution 6. If using AVREFM as the – side reference voltage of the A/D converter, do not select ANI1 as an A/D conversion channel.

Caution 7. If the ADISS bit is set to 1, the internal reference voltage cannot be used for the + side reference voltage. After the ADISS bit is set to 1, the initial conversion result cannot be used. For the setting flow, see 12.7.5 Example of using the ADC when selecting the temperature sensor output voltage or internal reference voltage, and software trigger no-wait mode and one-shot conversion mode. For details about the internal reference voltage, see CHAPTER 37 ELECTRICAL CHARACTERISTICS TA = -40 to +105°C.

Correct:

Figure 12 - 12 Format of Analog Input Channel Specification Register (ADS)
<Select mode (ADMD = 0)> (2/2)

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog input channel	Input source
0	1	1	0	1	1	Setting prohibited	
0	1	1	1	1	0	—	Voltage on the TSCAP pin of the CTSU
0	1	1	1	1	1	Setting prohibited	
1	0	0	0	0	0	—	Temperature sensor output voltage
1	0	0	0	0	1	—	Internal reference voltage Note 3
Other than the above						Setting prohibited	

Caution 1. Be sure to clear bits 6 and 5 to 0.

Caution 2. Set the channel that is specified as the analog input by a PMCAxx, PMCTxx, or PMCEx register to the input mode by using port mode registers 0, 2, 3, 10 to 12, 14, or 15 (PM0, PM2, PM3, PM10 to PM12, PM14, PM15).

Caution 3. When specifying an input channel by the ADS register, do not select the pin that is specified as digital I/O by port mode control A register 0, 2, 3, 10, 11, 12, 14, or 15 (PMCA0, PMCA2, PMCA3, PMCA10, PMCA11, PMCA12, PMCA14, or PMCA15), port mode control T register 0, 2, or 15 (PMCT0, PMCT2, or PMCT15), or port mode control E register 0 (PMCE0).

Caution 4. Rewrite the value of the ADISS bit while conversion is stopped (ADCS = 0, ADCE = 0).

Caution 5. If using AVREFP as the + side reference voltage of the A/D converter, do not select ANI0 as an A/D conversion channel.

Caution 6. If using AVREFM as the – side reference voltage of the A/D converter, do not select ANI1 as an A/D conversion channel.

Caution 7. If the ADISS bit is set to 1, the internal reference voltage cannot be used for the + side reference voltage. After the ADISS bit is set to 1, the initial conversion result cannot be used. For the setting flow, see 12.7.5 Example of using the ADC when selecting the temperature sensor output voltage or internal reference voltage, and software trigger no-wait mode and one-shot conversion mode. For details about the internal reference voltage, see CHAPTER 37 ELECTRICAL CHARACTERISTICS TA = -40 to +105°C.

Caution 8. Do not set the ADISS bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock. When the ADISS bit is set to 1, the A/D converter reference voltage current (IADREF) indicated in 37.3.2 Supply current characteristics will be added.

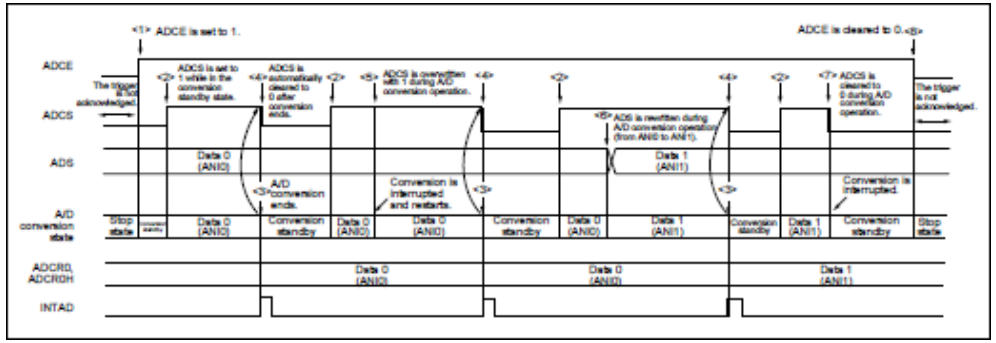
Caution 8. Do not set the ADISS bit to 1 when shifting to STOP mode, or to HALT mode while the CPU is operating on the subsystem clock. When the ADISS bit is set to 1, the A/D converter reference voltage current (IADREF) indicated in 37.3.2 Supply current characteristics will be added.

Caution9. When the setting of the ADISS bit is 1, the hardware trigger wait mode and one-shot conversion mode cannot be used.

30. 12.6.2 Software trigger no-wait mode (select mode, one-shot conversion mode) (Page 555)

Incorrect:

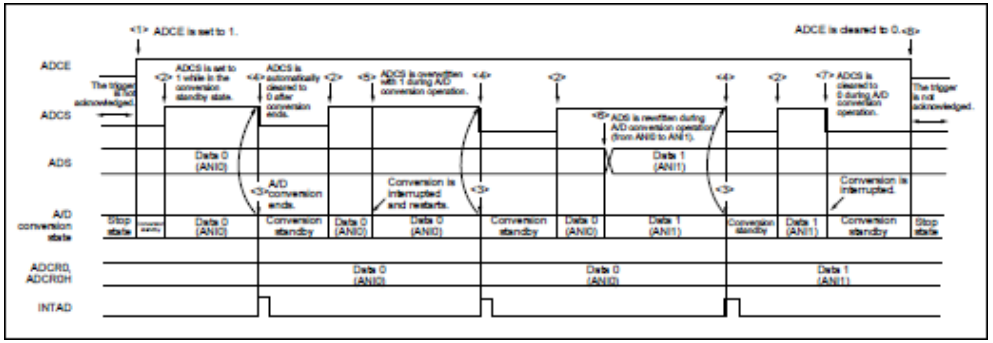
Figure 12 - 19 Example of Software Select No-Wait Mode (Select Mode, One-Shot Conversion Mode) Operation Timing



Caution When <4>, <5>, or <6> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

Figure 12 - 19 Example of Software Select No-Wait Mode (Select Mode, One-Shot Conversion Mode) Operation Timing

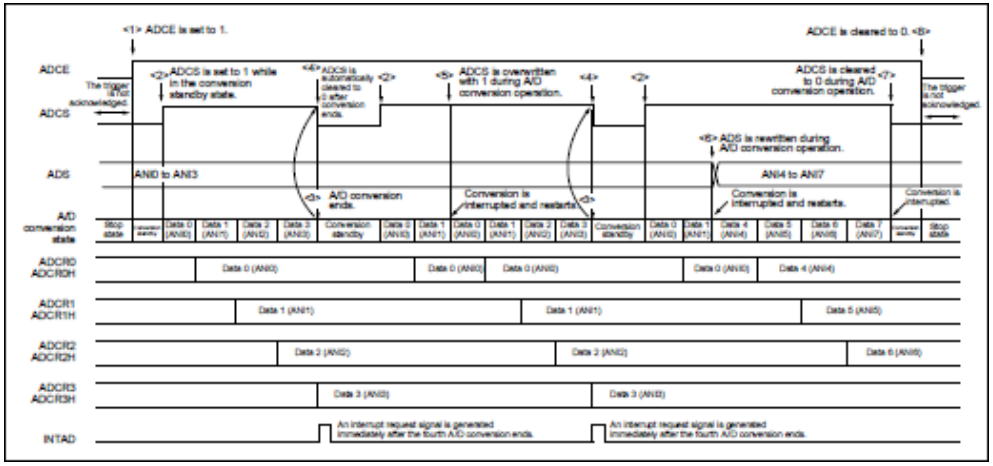


Caution When <5>, or <6> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

31. 12.6.4 Software trigger no-wait mode (scan mode, one-shot conversion mode) (Page 557)

Incorrect:

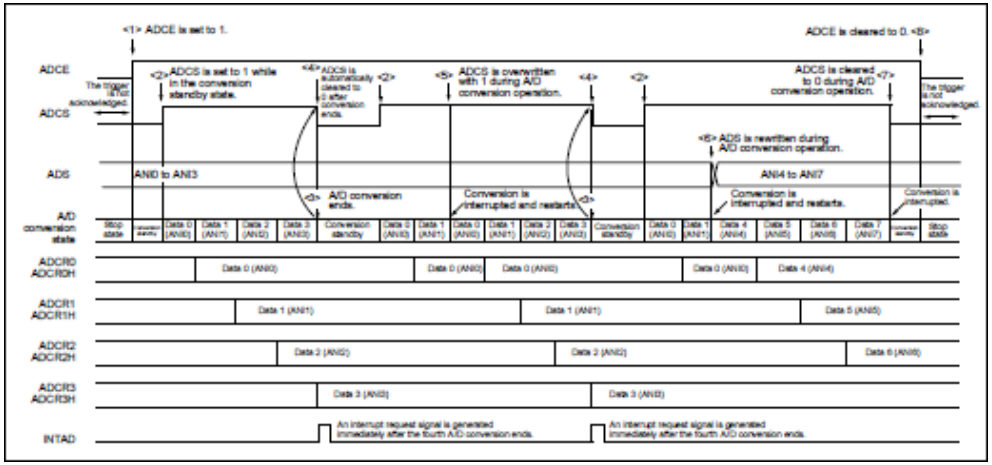
Figure 12 - 21 Example of Software Trigger No-Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing



Caution When <4>, <5>, or <6> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

Figure 12 - 21 Example of Software Trigger No-Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing

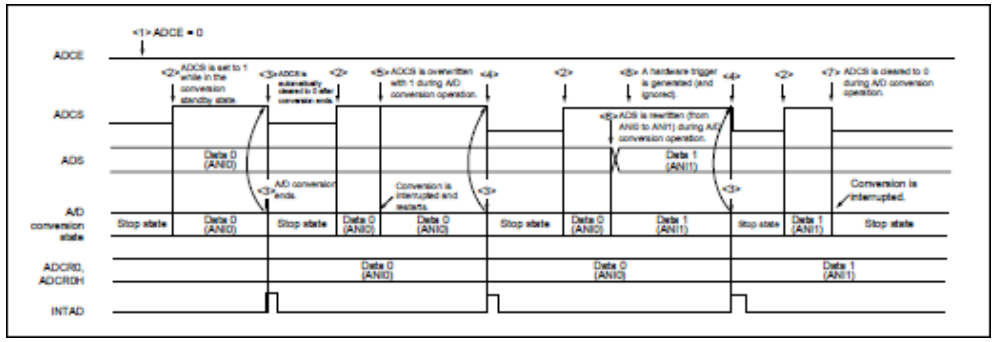


Caution When <5>, or <6> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

32. 12.6.6 Software trigger wait mode (select mode, one-shot conversion mode) (Page 559)

Incorrect:

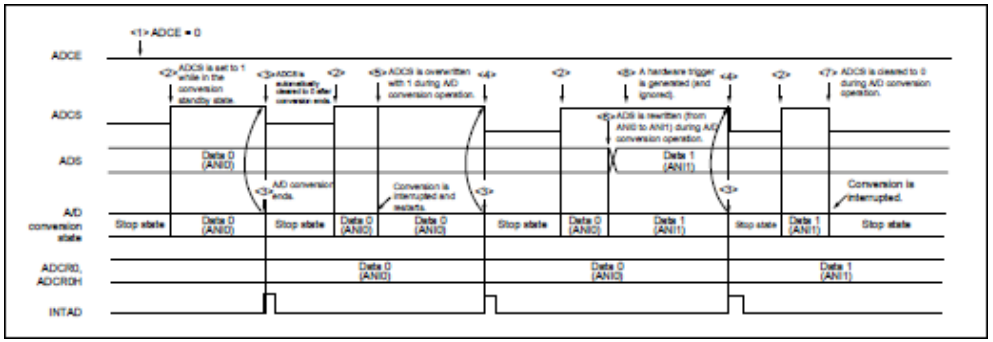
Figure 12 - 23 Example of Software Trigger Wait Mode (Select Mode, One-Shot Conversion Mode) Operation Timing



Caution When <4>, <5>, or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

Figure 12 - 23 Example of Software Trigger Wait Mode (Select Mode, One-Shot Conversion Mode) Operation Timing

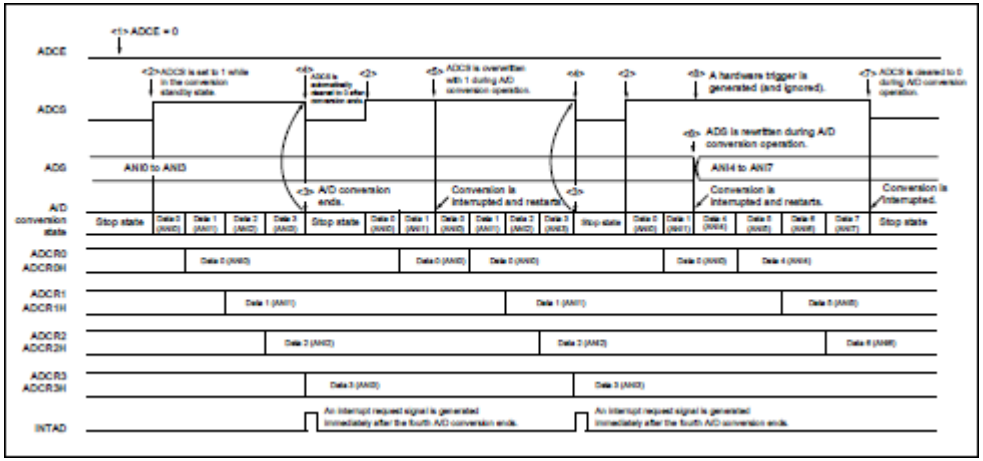


Caution When <5>, or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

33. 12.6.8 Software trigger wait mode (scan mode, one-shot conversion mode) (Page 561)

Incorrect:

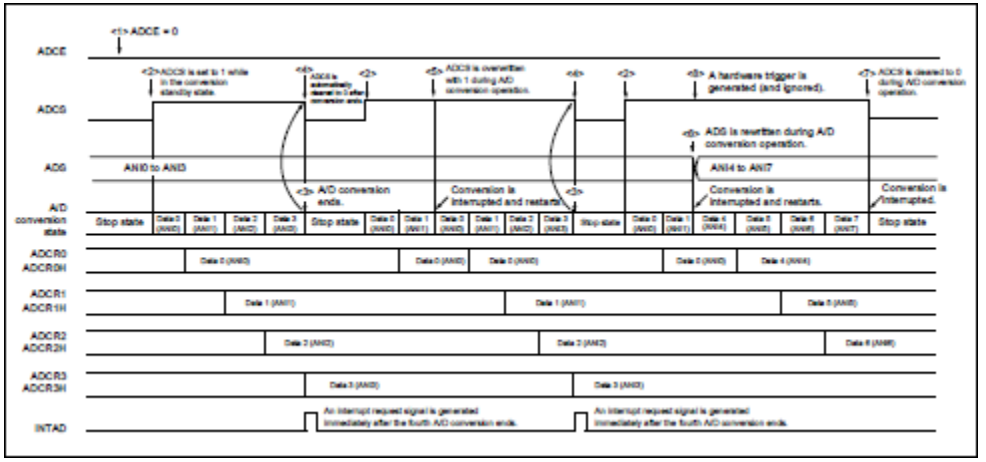
Figure 12 - 25 Example of Software Trigger Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing



Caution When <4>, <5>, or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

Figure 12 - 25 Example of Software Trigger Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing

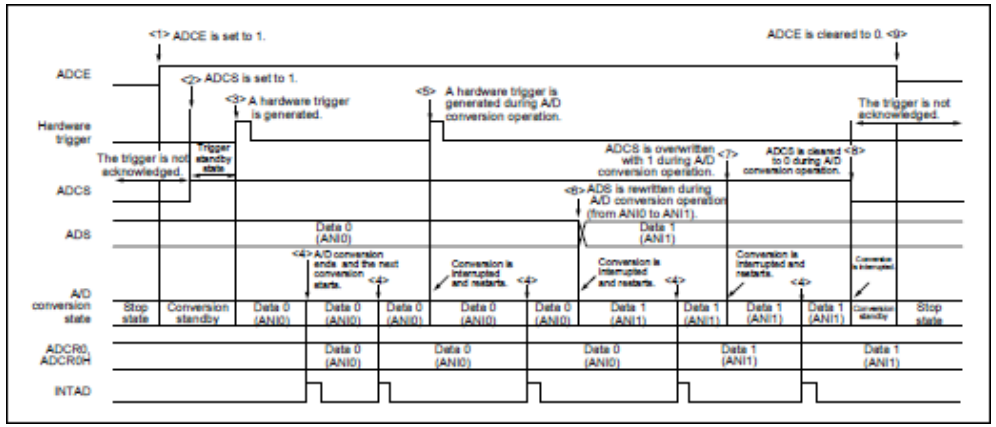


Caution When <5>, or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

34. 12.6.9 Hardware trigger no-wait mode (select mode, sequential conversion mode) (Page 562)

Incorrect:

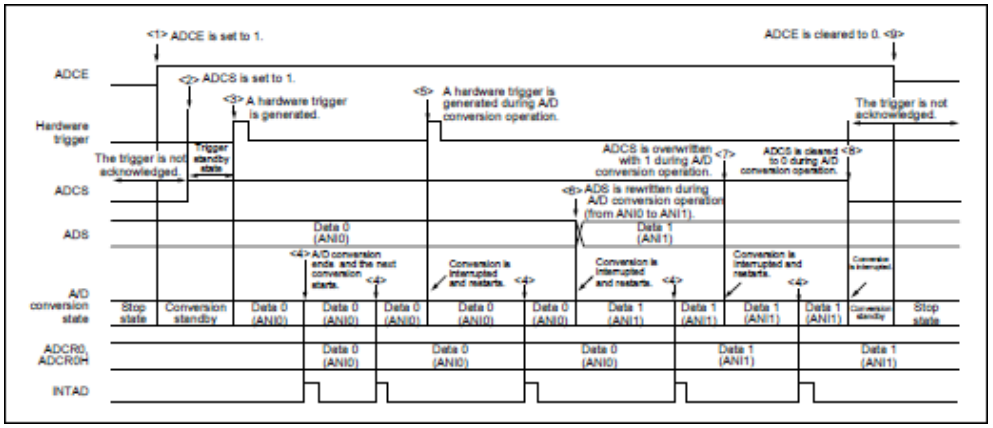
Figure 12 - 26 Example of Hardware Trigger No-Wait Mode (Select Mode, Sequential Conversion Mode) Operation Timing



Caution When <4>, <5>, or <6> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

Figure 12 - 26 Example of Hardware Trigger No-Wait Mode (Select Mode, Sequential Conversion Mode) Operation Timing

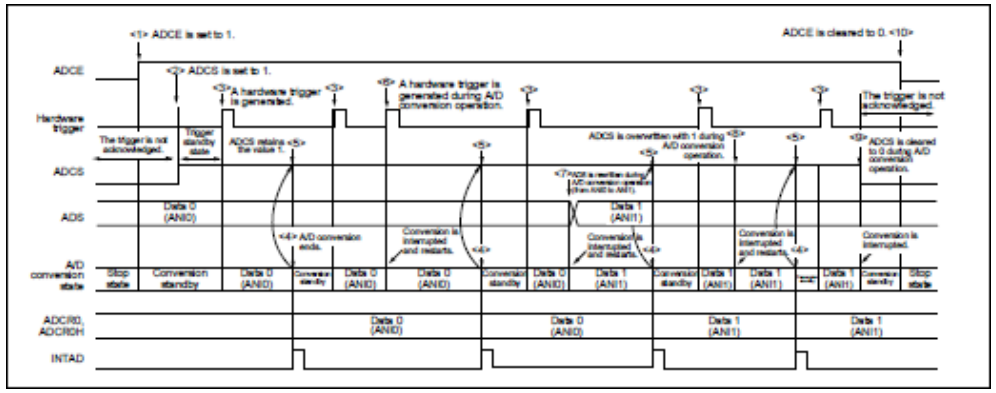


Caution When <5>, <6>, or <7> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

35. 12.6.10 Hardware trigger no-wait mode (select mode, one-shot conversion mode) (Page 563)

Incorrect:

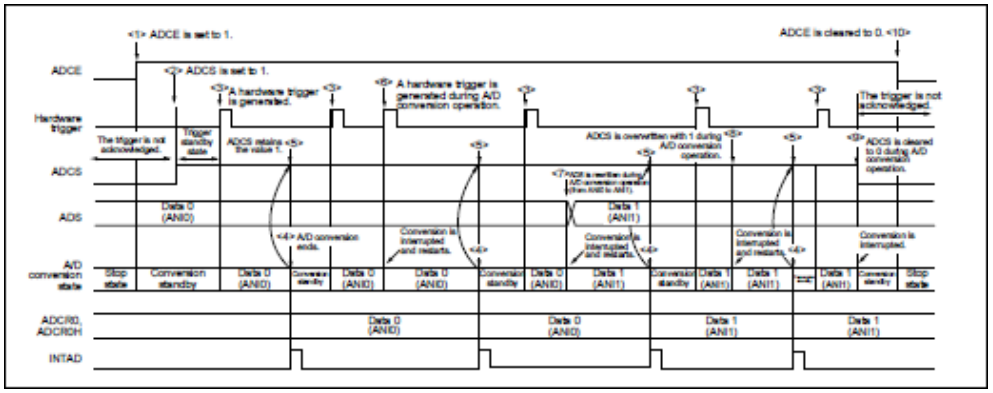
Figure 12 - 27 Example of Hardware Trigger No-Wait Mode (Select Mode, One-Shot Conversion Mode) Operation Timing



Caution When <4>, <5>, or <6> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

Figure 12 - 27 Example of Hardware Trigger No-Wait Mode (Select Mode, One-Shot Conversion Mode) Operation Timing

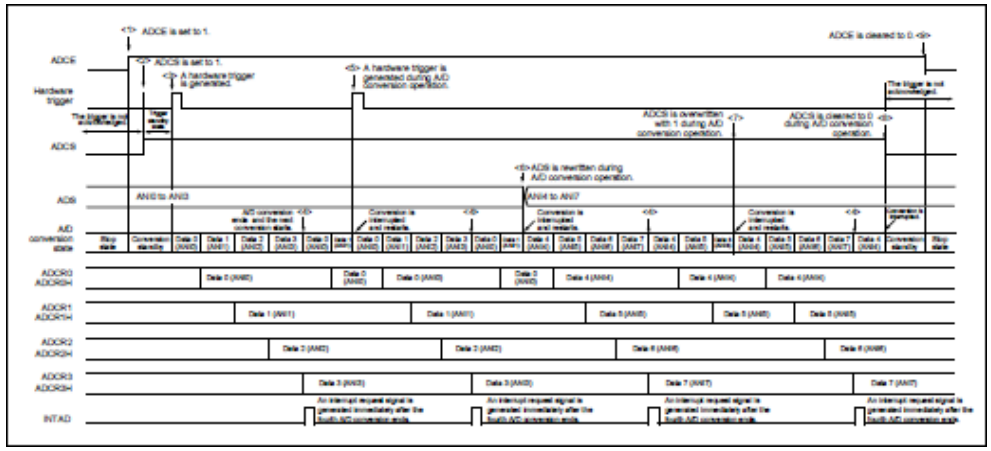


Caution When <6>, <7>, or <8> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

36. 12.6.11 Hardware trigger no-wait mode (scan mode, sequential conversion mode) (Page 564)

Incorrect:

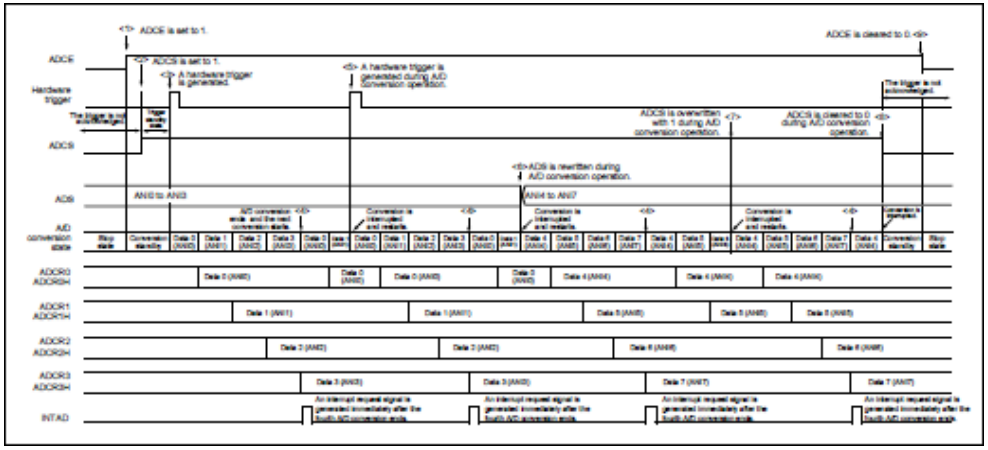
Figure 12 - 28 Example of Hardware Trigger No-Wait Mode (Scan Mode, Sequential Conversion Mode) Operation Timing



Caution When <4>, <5>, or <6> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

Figure 12 - 28 Example of Hardware Trigger No-Wait Mode (Scan Mode, Sequential Conversion Mode) Operation Timing

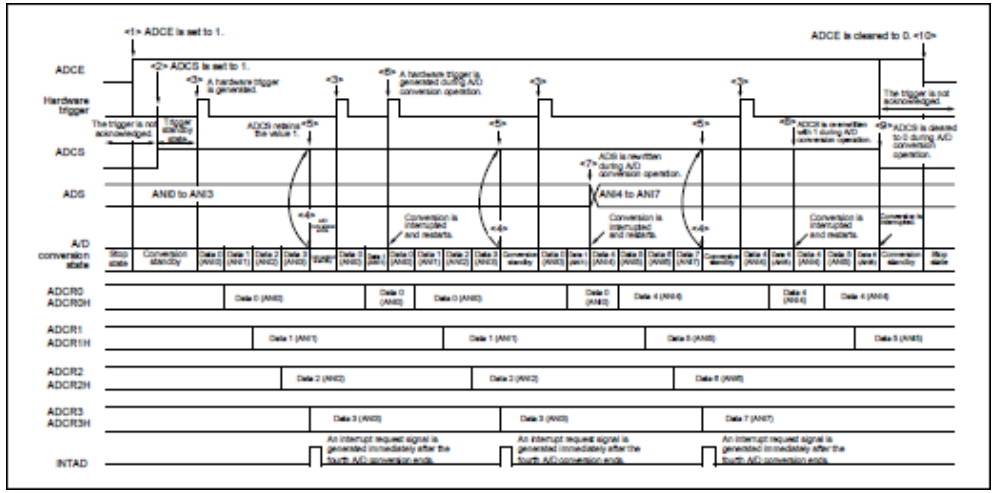


Caution When <5>, <6>, or <7> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

37. 12.6.12 Hardware trigger no-wait mode (scan mode, one-shot conversion mode) (Page 566)

Incorrect:

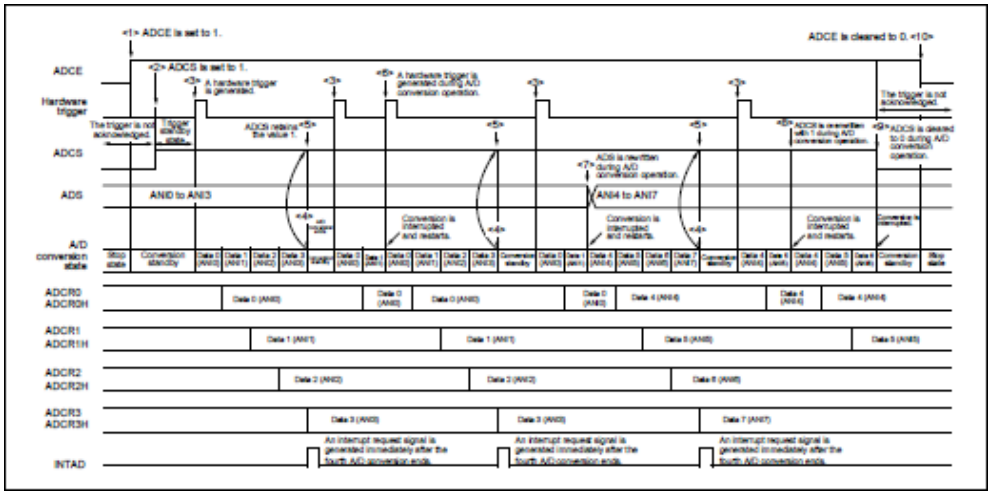
Figure 12 - 29 Example of Hardware Trigger No-Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing



Caution When <4>, <5>, or <6> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

Figure 12 - 29 Example of Hardware Trigger No-Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing

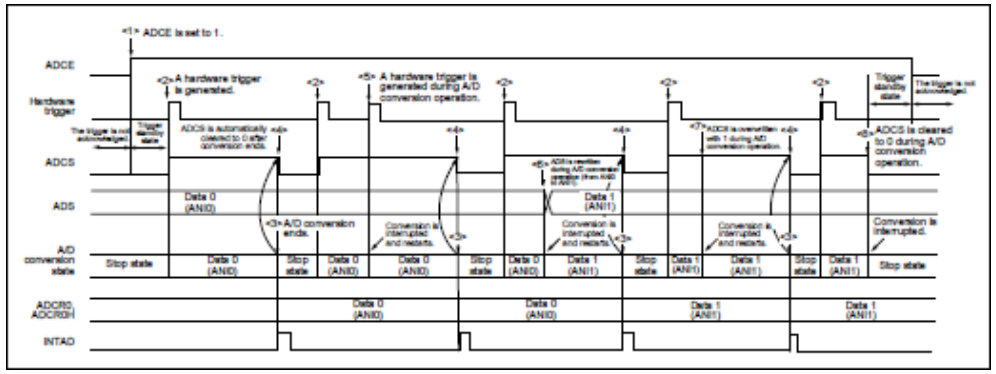


Caution When <6>, <7>, or <8> is detected while conversion is in progress, conversion is automatically restarted from the rising edge of the next cycle of the conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

38. 12.6.14 Hardware trigger wait mode (select mode, one-shot conversion mode) (Page 568)

Incorrect:

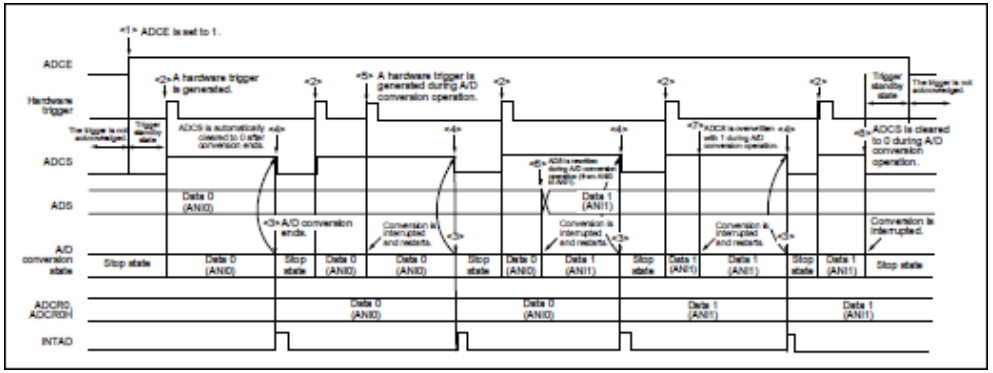
Figure 12 - 31 Example of Hardware Trigger Wait Mode (Select Mode, One-Shot Conversion Mode) Operation Timing



Caution When <4>, <5>, or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

Figure 12 - 31 Example of Hardware Trigger Wait Mode (Select Mode, One-Shot Conversion Mode) Operation Timing



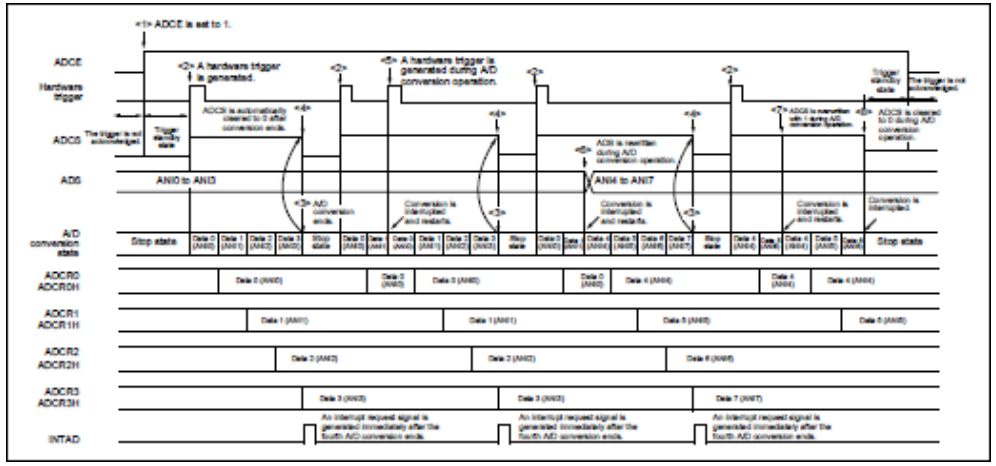
Caution1. When <5>, <6>, or <7> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Caction2. The setting of ADISS being 1 (the input source is temperature sensor output voltage and internal reference voltage) cannot be used in the hardware trigger wait mode (select mode and one-shot conversion mode).

39. 12.6.16 Hardware trigger wait mode (scan mode, one-shot conversion mode) (Page 570)

Incorrect:

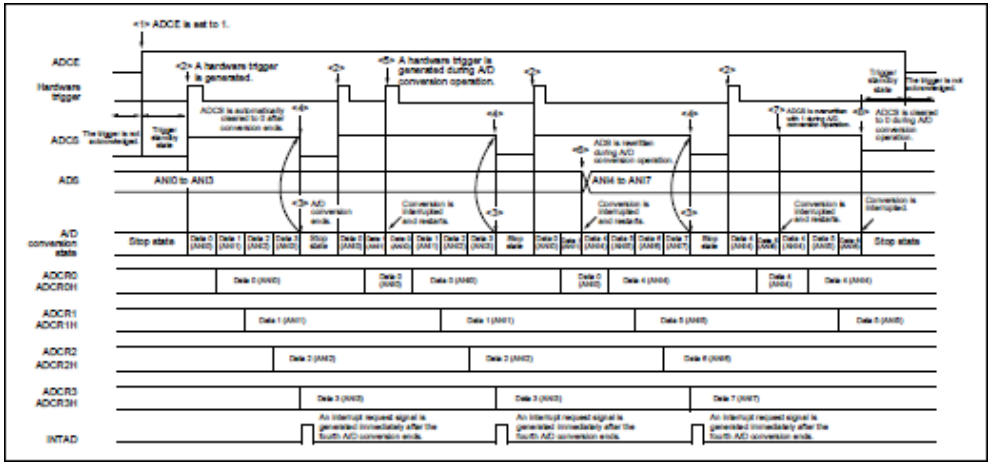
Figure 12 - 33 Example of Hardware Trigger Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing



Caution When <4>, <5>, or <6> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

Correct:

Figure 12 - 33 Example of Hardware Trigger Wait Mode (Scan Mode, One-Shot Conversion Mode) Operation Timing



Caution When <5>, <6>, or <7> is detected during conversion operation, conversion is restarted automatically after the stabilization wait time has passed since the rising edge of the next conversion clock (fAD). The conversion time at the first conversion operation restarted is the same as that when there is A/D power supply stabilization wait time in software trigger wait mode or hardware trigger wait mode. (See Table 12 - 3 A/D Conversion Time Selection (3/8) and Table 12 - 3 A/D Conversion Time Selection (4/8).)

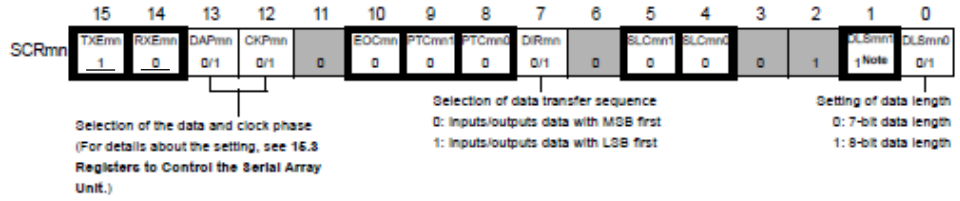
40. Figure 15 - 35 Example of Contents of Registers for Master Reception of 3-Wire Serial SPI (CSI00, CSI01, CSI10,CSI11, CSI20, CSI21, CSI30, CSI31) (Page 676)

Incorrect:

Figure 15 - 35 Example of Contents of Registers for Master Reception of 3-Wire Serial SPI (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21, CSI30, CSI31)

(a) Serial mode register mn (SMRmn)

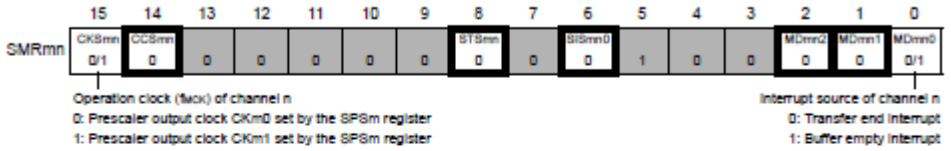
(b) Serial communication operation setting register mn (SCRmn)



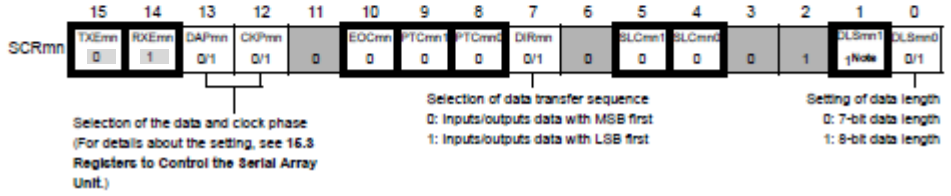
Correct:

Figure 15 - 35 Example of Contents of Registers for Master Reception of 3-Wire Serial SPI (CSI00, CSI01, CSI10, CSI11, CSI20, CSI21, CSI30, CSI31)

(a) Serial mode register mn (SMRmn)



(b) Serial communication operation setting register mn (SCRmn)



41. Table 15 - 3 Baud Rate Setting for UART Reception in SNOOZE Mode (Page 752)

Incorrect:

Table 15 - 3 Baud Rate Setting for UART Reception in SNOOZE Mode

High-speed On-chip Oscillator (f_{IH})	Baud Rate for UART Reception in SNOOZE Mode			
	Baud Rate of 4800 bps			
	Operation Clock (f_{MCK})	SDRmn [15:9]	Maximum Permissible Value	Minimum Permissible Value
32 MHz±1.0%Note	$f_{CLK}/2^5$	105	2.27%	-1.53%
24 MHz±1.0%Note	$f_{CLK}/2^5$	79	1.60%	-2.18%
16 MHz±1.0%Note	$f_{CLK}/2^4$	105	2.27%	-1.53%
12 MHz±1.0%Note	$f_{CLK}/2^4$	79	1.60%	-2.19%
8 MHz±1.0%Note	$f_{CLK}/2^3$	105	2.27%	-1.53%
6 MHz±1.0%Note	$f_{CLK}/2^3$	79	1.60%	-2.19%
4 MHz±1.0%Note	$f_{CLK}/2^2$	105	2.27%	-1.53%
3 MHz±1.0%Note	$f_{CLK}/2^2$	79	1.60%	-2.19%
2 MHz±1.0%Note	$f_{CLK}/2$	105	2.27%	-1.54%
1 MHz±1.0%Note	f_{CLK}	105	2.27%	-1.57%

Correct:

Table 15 - 3 Baud Rate Setting for UART Reception in SNOOZE Mode when Starting of the High-Speed On-Chip Oscillator is at Normal Speed (FWKUP = 0)

Baud Rate	High-Speed On-Chip Oscillator (f_{IH})	Operating Clock (f_{MCK})	SDRmn [15:9]	Maximum Permissible Value	Minimum Permissible Value
4800 bps	32 MHz ± 1%Note	$f_{CLK}/2^5$	106	1.45%	-1.67%
	24 MHz ± 1%Note	$f_{CLK}/2^5$	79	1.77%	-1.37%
9600 bps	32 MHz ± 1%Note	$f_{CLK}/2^4$	106	1.45%	-1.67%
	24 MHz ± 1%Note	$f_{CLK}/2^4$	79	1.77%	-1.37%

Table 15 - 4 Baud Rate Setting for UART Reception in SNOOZE Mode when Starting of the High-Speed On-Chip Oscillator is at High Speed (FWKUP = 1)

Baud Rate	High-Speed On-Chip Oscillator (f_{IH})	Operating Clock (f_{MCK})	SDRmn [15:9]	Maximum Permissible Value	Minimum Permissible Value
4800 bps	32 MHz ± 1%Note	$f_{CLK}/2^5$	106	1.45%	-1.67%
9600 bps		$f_{CLK}/2^4$	106	1.45%	-1.67%
19200 bps		$f_{CLK}/2^3$	106	1.45%	-1.67%
31250 bps		$f_{CLK}/2^3$	65	1.05%	-2.06%
38400 bps		$f_{CLK}/2^2$	106	1.45%	-1.67%
76800 bps		$f_{CLK}/2$	106	1.45%	-1.67%
115200 bps		$f_{CLK}/2$	70	1.93%	-1.21%

42. 17.3.2 UART Mode, (5) Continuous transmission (Page 911)

Incorrect:

(5) Continuous transmission

UARTAn has two separate registers for continuous transmission: the transmit buffer register
(TXBAn) and the transmit shift register.
At the moment the transmit shift register starts a shift operation, the next transmit data can be written to the transmit buffer register (TXBAn). This operation enables continuous transmission, thereby improving communication rate.
Note that continuous transmission is not achieved when writing to the TXBAn register is not completed within the maximum number of clock cycles defined below from generation of the transmit buffer register (TXBAn) empty interrupt.

Maximum number of clock cycles = Data transfer length × 2k - (2k + 3)
k: the value set with the BRGCAn bits (k = 2, 3, 4, 5, 6, …, 255)

An example of calculating the maximum number of clock cycles is described below.
When the BRGCAn register = 02H (k = 2),
start bit = 1 bit, character length = 8 bits, parity used, and stop bit = 1 bit:
The maximum number of clock cycles = Transfer length × 2k - (2k + 3) = 11 × 2 × 2 - (2 × 2 + 3) = 37 (Writing must be completed within 37 clock cycles.)

Continuous transmission is achieved by the following two methods.

Correct:

(5) Continuous transmission

UARTAn has two separate registers for continuous transmission: the transmit buffer register
(TXBAn) and the transmit shift register.
At the moment the transmit shift register starts a shift operation, the next transmit data can be written to the transmit buffer register (TXBAn). This operation enables continuous transmission, thereby improving communication rate.
Note that continuous transmission is not achieved when writing to the TXBAn register is not completed within the maximum number of clock cycles defined below from generation of the buffer empty interrupt.

Maximum number of clock cycles = Data transfer length × 2k - (2k + 3)
k: the value set with the BRGCAn bits (k = 2, 3, 4, 5, 6, …, 255)

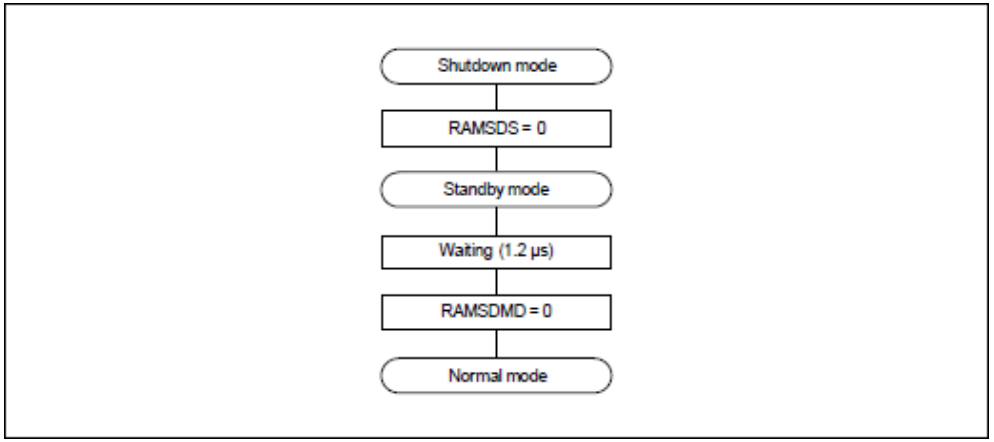
An example of calculating the maximum number of clock cycles is described below.
When the BRGCAn register = 02H (k = 2),
start bit = 1 bit, character length = 8 bits, parity used, and stop bit = 1 bit:
The maximum number of clock cycles = Transfer length × 2k - (2k + 3) = 11 × 2 × 2 - (2 × 2 + 3) = 37 (Writing must be completed within 37 clock cycles of the UARTAn operating clock (fUTAn).)

Continuous transmission is achieved by the following two methods.

43. Figure 23 - 4 Procedure for Settings to Switch from Shutdown Mode to Normal Mode (Page 1108)

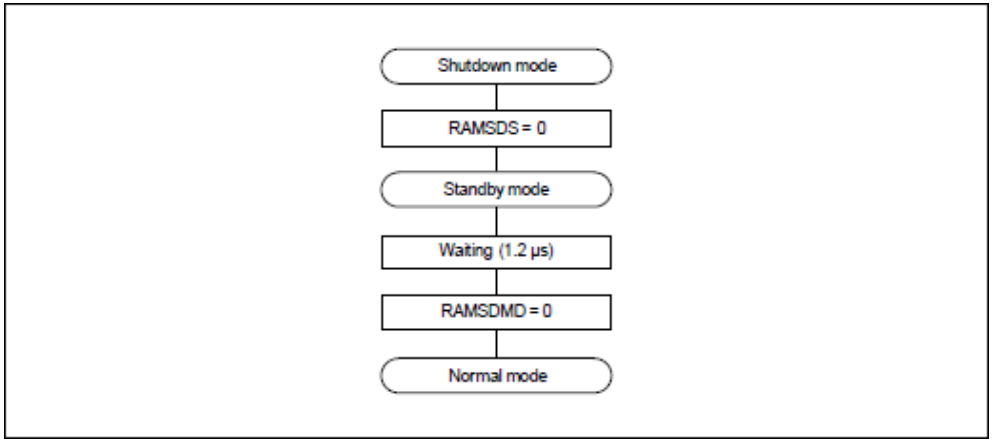
Incorrect:

Figure 23 - 4 Procedure for Settings to Switch from hutdown Mode to Normal Mode



Correct:

Figure 23 - 4 Procedure for Settings to Switch from Shutdown Mode to Normal Mode



Caution When the RAM returns to normal mode from shutdown mode, the contents of the RAM other than in the range from FF000H to FFEFFH are undefined. Initialize the RAM area to be used.

44. Table 23 - 1 Operating Statuses in HALT Mode (1) (2/2) (Page 1110)

Incorrect:

Table 23 - 1 Operating Statuses in HALT Mode (1) (2/2)

HALT Mode Setting / Item		When HALT Instruction Is Executed While CPU Is Operating on Main System Clock			
		When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU Is Operating on Middle-speed On-chip Oscillator Clock (f_{IM})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
Clock output/buzzer output		Operation enabled			
A/D converter					
D/A converter					
Comparator					
Serial array unit					
Serial interface IICA					
Serial interface UARTA					
Remote control signal receiver					
Data transfer controller (DTC)					
SNOOZE mode sequencer					
Logic and event link controller (ELCL)		Operation-enabled function blocks can be linked			
Power-on-reset function		Operation enabled			
Voltage detection function					
External interrupt					
Key interrupt function					
Capacitive sensing unit (CTSU)					
CRC operation function	High-speed CRC				
	General-purpose CRC	Capable of operations in response to access by the DTC or SMS to obtain data for calculations from the RAM area			
Illegal-memory access detection function		Capable of operations in response to access by the DTC or SMS			
RAM parity error detection function					
RAM guard function					
SFR guard function					

Correct:

Table 23 - 1 Operating Statuses in HALT Mode (1) (2/2)

HALT Mode Setting / Item		When HALT Instruction Is Executed While CPU Is Operating on Main System Clock			
		When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU Is Operating on Middle-speed On-chip Oscillator Clock (f_{IM})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
Clock output/buzzer output		Operation enabled			
A/D converter					
D/A converter					
Comparator					
Serial array unit					
Serial interface IICA					
Serial interface UARTA					
Remote control signal receiver					
Data transfer controller (DTC)					
SNOOZE mode sequencer					
Logic and event link controller (ELCL)		Operation-enabled function blocks can be linked			
Power-on-reset function		Operation enabled			
Voltage detection function					
External interrupt					
Key interrupt function					
Capacitive sensing unit (CTSU)					
CRC operation function	High-speed CRC				
	General-purpose CRC	Capable of operations in response to access by the DTC or SMS to obtain data for calculations from the RAM area			
Illegal-memory access detection function		Capable of operations in response to access by the DTC or SMS			
RAM parity error detection function					
RAM guard function					
SFR guard function					
True random number generator		Operation enabled			

45. Table 23 - 2 Operating Statuses in HALT Mode (2) (2/2) (Page 1112)

Incorrect:

Table 23 - 2 Operating Statuses in HALT Mode (2) (2/2)

Item \ HALT Mode Setting		When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock		
		When CPU Is Operating on XT1 Clock (f_{XT})	When CPU Is Operating on External Subsystem Clock (f_{EXS})	When CPU Is Operating on Low-speed on-chip oscillator clock (f_{IL})
SNOOZE mode sequencer		Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).		Operation enabled
Logic and event link controller (ELCL)		Operation-enabled function blocks can be linked		
Power-on-reset function		Operation enabled		
Voltage detection function				
External interrupt				
Key interrupt function				
Capacitive sensing unit (CTSU)		Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).		Operation enabled
CRC operation function	High-speed CRC	Operation disabled		
	General-purpose CRC	Capable of operations in response to access by the DTC or SMS to obtain data for calculations from the RAM area		
Illegal-memory access detection function		Capable of operations in response to access by the DTC or SMS		
RAM parity error detection function				
RAM guard function				
SFR guard function				

Correct:

Table 23 - 2 Operating Statuses in HALT Mode (2) (2/2)

Item \ HALT Mode Setting		When HALT Instruction Is Executed While CPU Is Operating on Subsystem Clock		
		When CPU Is Operating on XT1 Clock (f_{XT})	When CPU Is Operating on External Subsystem Clock (f_{EXS})	When CPU Is Operating on Low-speed on-chip oscillator clock (f_{IL})
SNOOZE mode sequencer		Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).		Operation enabled
Logic and event link controller (ELCL)		Operation-enabled function blocks can be linked		
Power-on-reset function		Operation enabled		
Voltage detection function				
External interrupt				
Key interrupt function				
Capacitive sensing unit (CTSU)		Operates when the RTCLPC bit is 0 (operation is disabled when the RTCLPC bit is not 0).		Operation enabled
CRC operation function	High-speed CRC	Operation disabled		
	General-purpose CRC	Capable of operations in response to access by the DTC or SMS to obtain data for calculations from the RAM area		
Illegal-memory access detection function		Capable of operations in response to access by the DTC or SMS		
RAM parity error detection function				
RAM guard function				
SFR guard function				
True random number generator		Operation enabled		

46. Table 23 - 3 Operating Statuses in STOP Mode (2/2) (Page 1117)

Incorrect:

Table 23 - 3 Operating Statuses in STOP Mode (2/2)

Item \ STOP Mode Setting		When STOP Instruction Is Executed While CPU Is Operating on Main System Clock			
		When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU Is Operating on Middle-speed On-chip Oscillator Clock (f_{IM})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
CRC operation function	High-speed CRC	Operation stopped			
	General-purpose CRC				
Illegal-memory access detection function					
RAM parity error detection function					
RAM guard function					
SFR guard function					

Correct:

Table 23 - 3 Operating Statuses in STOP Mode (2/2)

Item \ STOP Mode Setting		When STOP Instruction Is Executed While CPU Is Operating on Main System Clock			
		When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU Is Operating on Middle-speed On-chip Oscillator Clock (f_{IM})	When CPU Is Operating on X1 Clock (f_X)	When CPU Is Operating on External Main System Clock (f_{EX})
CRC operation function	High-speed CRC	Operation stopped			
	General-purpose CRC				
Illegal-memory access detection function					
RAM parity error detection function					
RAM guard function					
SFR guard function					
True random number generator					

47. Table 23 - 4 Operating Statuses in SNOOZE Mode (2/2) (Page 1124)

Incorrect:

Table 23 - 4 Operating Statuses in SNOOZE Mode (2/2)

Item \ STOP Mode Setting	Generation of source conditions which lead to transitions to SNOOZE mode during STOP mode	
	When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU Is Operating on Middle-speed On-chip Oscillator Clock (f_{IM})
Illegal-memory access detection function	Capable of operations in response to access by the DTC or SMS	
RAM parity error detection function		
RAM guard function		
SFR guard function		

Correct:

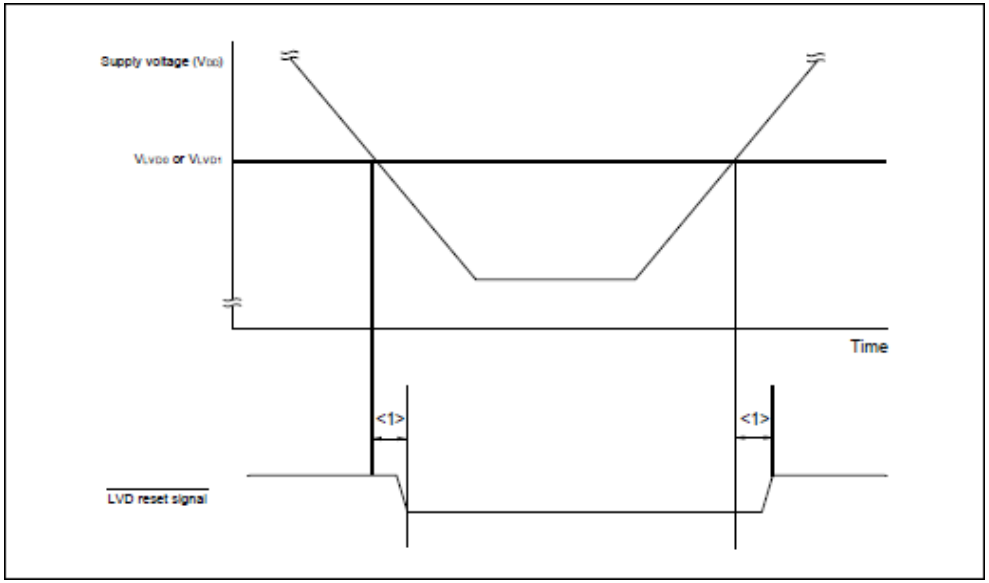
Table 23 - 4 Operating Statuses in SNOOZE Mode (2/2)

Item \ STOP Mode Setting	Generation of source conditions which lead to transitions to SNOOZE mode during STOP mode	
	When CPU Is Operating on High-speed On-chip Oscillator Clock (f_{IH})	When CPU Is Operating on Middle-speed On-chip Oscillator Clock (f_{IM})
Illegal-memory access detection function	Capable of operations in response to access by the DTC or SMS	
RAM parity error detection function		
RAM guard function		
SFR guard function		
True random number generator		

48. Figure 26 - 11 Delays from the Time an LVD0 or LVD1 Reset Source Condition is Satisfied until an LVD0 or LVD1 Reset has been Generated and Deasserted (Page 1155)

Incorrect:

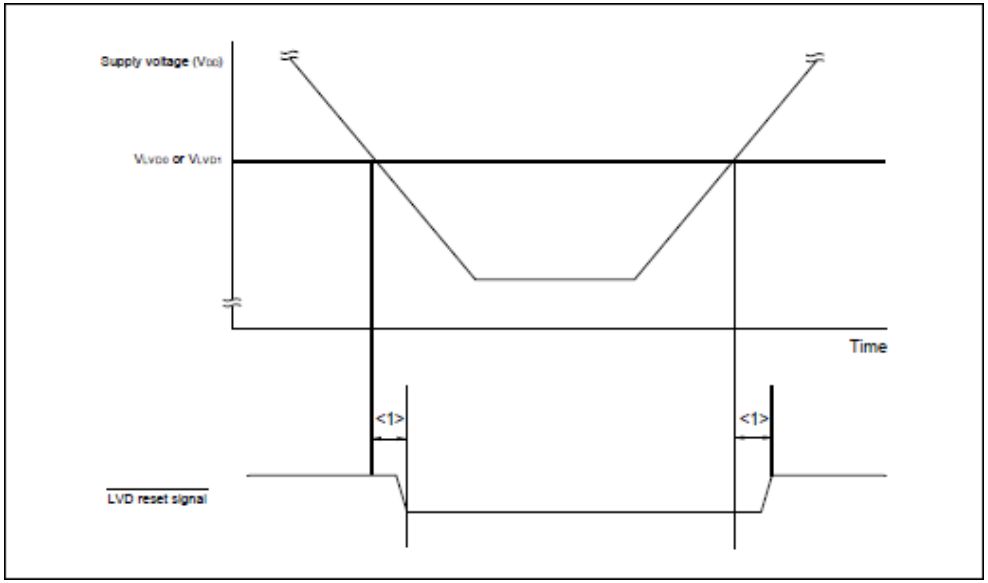
Figure 26 - 11 Delays from the Time an LVD0 or LVD1 Reset Source Condition is Satisfied until an LVD0 or LVD1 Reset has been Generated and Deasserted



<1>: Delay for detection (300 µs (max.))

Correct:

Figure 26 - 11 Delays from the Time an LVD0 or LVD1 Reset Source Condition is Satisfied until an LVD0 or LVD1 Reset has been Generated and Deasserted

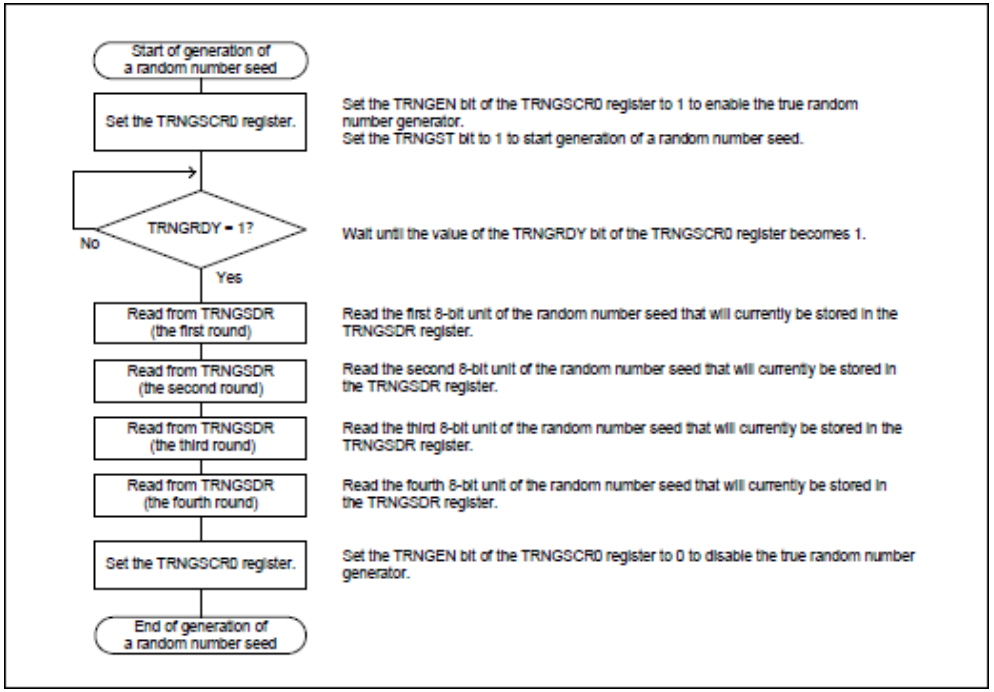


<1>: Delay for detection (500 µs (max.))

49. Figure 28 - 3 Procedure for Using the True Random Number Generator to Generate a Random Number Seed (Page 1188)

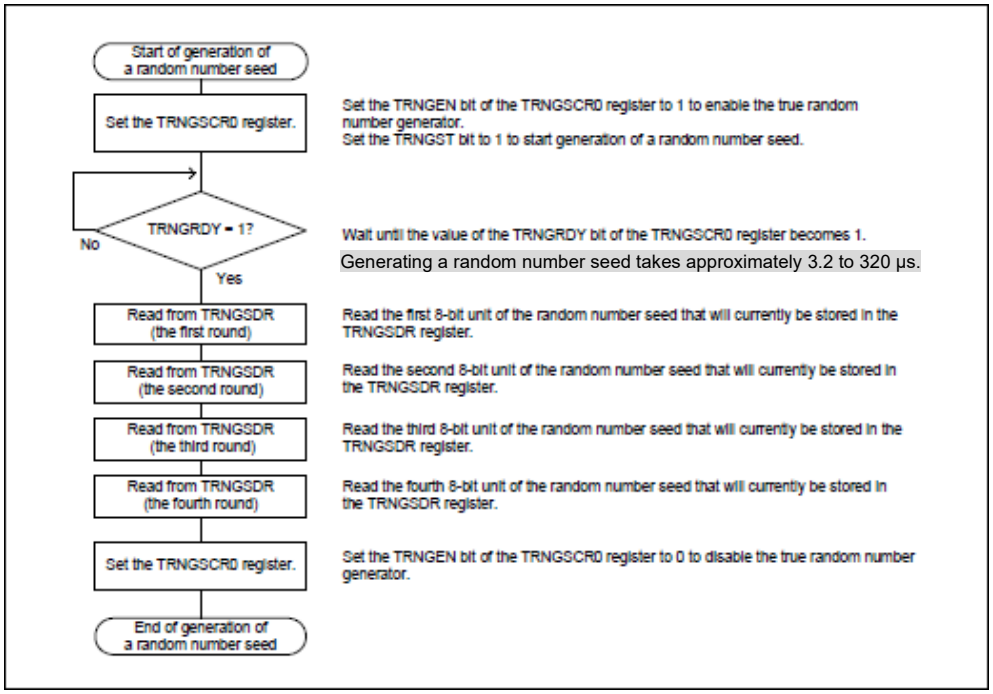
Incorrect:

Figure 28 - 3 Procedure for Using the True Random Number Generator to Generate a Random Number Seed



Correct:

Figure 28 - 3 Procedure for Using the True Random Number Generator to Generate a Random Number Seed



50. 28.2.2 Setting of flash read protection (Page 1190)

Incorrect:

Table 28 - 2 Method of Setting Flash Read Protection

Item to Be Set	Method of Setting	Method of Changing
Block where flash read protection starts	Using a flash memory programmer or self-programming.	Using a flash memory programmer or self-programming. Note that the block where protection starts is not adjustable while fixing of the flash read protection settings is enabled.
Block where flash read protection ends	Using a flash memory programmer or self-programming.	Using a flash memory programmer or self-programming. Note that the block where protection ends is not adjustable while fixing of the flash read protection settings is enabled.
Fixing the flash read protection settings	Using a flash memory programmer or self-programming.	Fixing of the flash read protection settings can be released by using a flash memory programmer.Note If you do so, the values for the start and end blocks are initialized.

Note Release from the fixed setting is only possible when erasure of blocks is not prohibited, rewriting of boot cluster 0 is not prohibited, and the code and data flash memory areas are blank.

Caution 1. The settings for flash read protection in the extra area are not readable. To confirm that the settings for flash read protection are in place, read from the read-access disabled area and confirm that FFH is returned.

Caution 2. To specify the read-access disabled area for flash read protection, be sure to specify the numbers of both the block where protection starts and the block where it ends.

Caution 3. Reading from the read-access disabled area by using an on-chip debugger is also impossible. This means that program code allocated to the read access-disabled area cannot be debugged by using the on-chip debugger. Therefore, only make the settings for flash read protection after having debugged the program code in the protected areas.

Caution 4. When a part of boot cluster 0 or boot cluster 1 is to be set as a part of the read-access disabled area, boot swapping may cause data in the read-access disabled area to be swapped with data in the read access-enabled area. To prevent this, when setting a part of boot cluster 0 or boot cluster 1 as part of the read-access disabled area, make the setting for prohibiting the rewriting of boot cluster 0 so as to prohibit boot swapping itself.

Correct:

Table 28 - 2 Method of Setting Flash Read Protection

Item to Be Set	Method of Setting	Method of Changing
Block where flash read protection starts	Using a flash memory programmer or self-programming.	Using a flash memory programmer or self-programming. Note that the block where protection starts is not adjustable while fixing of the flash read protection settings is enabled.
Block where flash read protection ends	Using a flash memory programmer or self-programming.	Using a flash memory programmer or self-programming. Note that the block where protection ends is not adjustable while fixing of the flash read protection settings is enabled.
Fixing the flash read protection settings	Using a flash memory programmer or self-programming.	Fixing of the flash read protection settings can be released by using a flash memory programmer.Note If you do so, the values for the start and end blocks are initialized.

Note Release from the fixed setting is only possible when erasure of blocks is not prohibited, rewriting of boot area is not prohibited, and the code and data flash memory areas are blank.

Caution 1. The settings for flash read protection in the extra area are not readable. To confirm that the settings for flash read protection are in place, read from the read-access disabled area and confirm that FFH is returned.

Caution 2. To specify the read-access disabled area for flash read protection, be sure to specify the numbers of both the block where protection starts and the block where it ends.

Caution 3. Reading from the read-access disabled area by using an on-chip debugger is also impossible. This means that program code allocated to the read access-disabled area cannot be debugged by using the on-chip debugger. Therefore, only make the settings for flash read protection after having debugged the program code in the protected areas.

Caution 4. When a part of boot clust 0 or boot cluster 1 is to be set as a part of the read-access disabled area, boot swapping may cause data in the read-access disabled area to be swapped with data in the read access-enabled area. To prevent this, when setting a part of boot cluster 0 or boot cluster 1 as part of the read-access disabled area, make the setting for prohibiting the rewriting of boot area so as to prohibit boot swapping itself.

51. CHAPTER 30 CAPACITIVE SENSING UNIT (CTSU2L), Number of the CTSU2L output channels (Page 1236)

Incorrect:

ROM size	64 to 128 Kbytes								
Pin count	30	32	36	40, 44	48	52	64	80	100
Number of the CTSU2L output channels	2 (TS00, TS01)	3 (TS00 to TS02)	5 (TS00 to TS04)	6 (TS00 to TS05)	8 (TS00 to TS07)	10 (TS00 to TS09)	12 (TS00 to TS11)	30 (TS00 to TS15, TS20 to TS33)	32 (TS00 to TS15, TS20 to TS35)

ROM size	192 to 768 Kbytes									
Pin count	30	32	36	40	44	48	52	64	80	100, 128
Number of the CTSU2L output channels	6 (TS00, TS01, TS20, TS21, TS26, TS27)	7 (TS00 to TS02, TS20, TS21, TS26, TS27)	11 (TS00 to TS04, TS20 to TS23, TS26, TS27)	13 (TS00 to TS05, TS20 to TS24, TS26, TS27)	14 (TS00 to TS05, TS20 to TS27)	16 (TS00 to TS07, TS20 to TS27)	20 (TS00 to TS09, TS20 to TS29)	22 (TS00 to TS11, TS20 to TS29)	30 (TS00 to TS15, TS20 to TS33)	32 (TS00 to TS15, TS20 to TS35)

Correct:

ROM size	96 to 128 Kbytes							128 Kbytes	
Pin count	30	32	36	40, 44	48	52	64	80	100
Number of the CTSU2L output channels	2 (TS00, TS01)	3 (TS00 to TS02)	5 (TS00 to TS04)	6 (TS00 to TS05)	8 (TS00 to TS07)	10 (TS00 to TS09)	12 (TS00 to TS11)	30 (TS00 to TS15, TS20 to TS33)	32 (TS00 to TS15, TS20 to TS35)

ROM size	192 to 256 Kbytes				192 to 768 Kbytes					256 to 768 Kbytes
Pin count	30	32	36	40	44	48	52	64	80	100, 128
Number of the CTSU2L output channels	6 (TS00, TS01, TS20, TS21, TS26, TS27)	7 (TS00 to TS02, TS20, TS21, TS26, TS27)	11 (TS00 to TS04, TS20 to TS23, TS26, TS27)	13 (TS00 to TS05, TS20 to TS24, TS26, TS27)	14 (TS00 to TS05, TS20 to TS27)	16 (TS00 to TS07, TS20 to TS27)	20 (TS00 to TS09, TS20 to TS29)	22 (TS00 to TS11, TS20 to TS29)	30 (TS00 to TS15, TS20 to TS33)	32 (TS00 to TS15, TS20 to TS35)

52. Table 30 - 1 CTSU Functions, Transmission power switching of mutual capacitance method (Page 1238)

Incorrect:

Table 30 - 1 CTSU Functions

Item		Configuration
CTSU2L operating voltage condition		VDD = 1.8 to 5.5 V
Operating clock		fCLK, fCLK/2, fCLK/4, or fCLK/8
Pins	Electrostatic capacitance measurement	TSm (m = 00 to 15, 20 to 35) up to 32 channels
	Connection pin to capacitor for measurement secondary power	TSCAP (10 nF) We recommend connecting a 10-nF capacitor.
Measurement mode	Self-capacitance measurement mode	Electrostatic capacitance is measured from the charged current that flows toward the electrode used in the self-capacitance method.
	Mutual capacitance measurement mode	Electrostatic capacitance is measured from the charged current that flows toward the capacitance generated between the transmit and receive electrodes used in the mutual capacitance method.
	DC current measurement mode	Current from a measurement pin is measured.
Calibration mode		Characteristic correction of the current control oscillator for measurement
Noise prevention		Synchronous noise prevention, high-pass noise prevention Majority decision by multi-frequency measurement
Adjustment for each pin		Offset current adjustment function Sensor drive pulse frequency specification Measurement time specification
Measurement start conditions		Software trigger External trigger (ELCL)
Low-power function		SNOOZE function supported
Requests	Data transfer request	Channel measurement setting write request Measurement result read request
	Interrupt request	Measurement end interrupt request
Transmission power switching of mutual capacitance method		The power for transmission in the mutual capacitance method can be switched among VDD (VCL), VCC (I/O port), and VCC (dedicated).

Correct:

Table 30 - 1 CTSU Functions

Item		Configuration
CTSU operating voltage condition		VDD = 1.8 to 5.5 V
Operating clock		fCLK, fCLK/2, fCLK/4, or fCLK/8
Pins	Electrostatic capacitance measurement	TSm (m = 00 to 15, 20 to 35) up to 32 channels
	Connection pin to capacitor for measurement secondary power	TSCAP (10 nF) We recommend connecting a 10-nF capacitor.
Measurement mode	Self-capacitance measurement mode	Electrostatic capacitance is measured from the charged current that flows toward the electrode used in the self-capacitance method.
	Mutual capacitance measurement mode	Electrostatic capacitance is measured from the charged current that flows toward the capacitance generated between the transmit and receive electrodes used in the mutual capacitance method.
	Current measurement mode	Current from a measurement pin is measured.
Calibration mode		Characteristic correction of the current control oscillator for measurement
Noise prevention		Synchronous noise prevention, high-pass noise prevention Majority decision by multi-frequency measurement
Adjustment for each pin		Offset current adjustment function Sensor drive pulse frequency specification Measurement time specification
Measurement start conditions		Software trigger External trigger (ELCL)
Low-power function		SNOOZE function supported
Interrupt requests	DTC activation source/ DTC interrupt source	Request to write to a configuration register of an individual CTSU channel Request to transfer data measured by the CTSU
	Interrupt source	Measurement end interrupt
Transmission power switching of mutual capacitance method		The power for transmission in the mutual capacitance method is switchable.

53. Table 30 - 2 External Pins Used in CTSU (Page 1239)

Incorrect:

Table 30 - 2 External Pins Used in CTSU

Pin name	Input/output	Function
TSm (m = 00 to 15, 20 to 35)	Output	Electrostatic capacitance measurement pin, transmit pin in the mutual capacitance method, active shield control pin, or current measurement pin
TSCAP	—	Connection pin to capacitor for measurement secondary power

Correct:

Table 30 - 2 External Pins Used in CTSU

Pin name	Input/output	Function
TSm (m = 00 to 15, 20 to 35)	Input/output	Electrostatic capacitance measurement pin, transmit pin in the mutual capacitance method, active shield control pin, or current measurement pin
TSCAP	Input/output	Connection pin to capacitor for measurement secondary power

54. Figure 30 - 7 Format of CTSU Control Registers AL and AH (CTSUCRAL, CTSUCRAH) (Page 1245, Page 1246, Page 1247)

Incorrect:

Figure 30 - 7 Format of CTSU Control Registers AL and AH (CTSUCRAL, CTSUCRAH)

MD1	Measurement Mode Select 1
0	Self-capacitance method (single measurement) When CHTRCx is set to 1 (transmission), the transmit pin outputs the first (same phase) pulse. When multiple bits are set to 1, scan is performed. When CHTRCx is set to all 0, measurement is performed without transmission.
1	Mutual capacitance method (double-measurement requiring CHTRCx setting) When CHTRCx is set to all 0, scan fails without measurement.
The MD1 bit selects single measurement (assuming self-capacitance method) or double-measurement (assuming mutual capacitance method).	

TXVSEL	Transmission Power Supply Select
0	Vcc (I/O port)
1	VDD (VCL)

TXVSEL2	Transmission Power Supply Select 2
0	Follows the TXVSEL setting.
1	Vcc (dedicated)

Correct:

Figure 30 - 7 Format of CTSU Control Registers AL and AH (CTSUCRAL, CTSUCRAH)

MD1	Measurement Mode Select 1
0	Self-capacitance method (single measurement) When CHTRCx is set to 1 (transmission), the same phase pulse is output from the TSm pin for measurement. When multiple CHTRCx bits are set to 1, measurement is scanned.
1	Mutual capacitance method (double-measurement) Set the CHTRCx bit to 1 (transmission) to handle measurement. The same phase pulse is output from the TSm pin in the first measurement. The reverse phase pulse is output from the TSm pin in the second measurement.
Set the MD1 bit to select self-capacitance method. Set the MD1 bit to select mutual-capacitance method.	

TXVSEL	TXVSEL2	Transmission Power Supply Select
0	0	Not recommended
0	1	This setting is recommended when transmission power of mutual capacitance method transmission is used.Note
1	0	Use this setting when the active shield function is in use.
1	1	This setting is recommended when transmission power of mutual capacitance method transmission is used.Note

Note The same transmission power supply is selected when the setting of TXVSEL2 is 1.

SNZ	SNOOZE Enable
0	Disables the SNOOZE function.
1	Enables the SNOOZE function.

The SNZ bit enables or disables the SNOOZE function when an external trigger is selected (CAP = 1). Setting this bit to 1 drives the CTSU hardware macro into the suspended state to enable low-power operation in the standby state.

<CTSU hardware macro state control>

PON	SNZ	CAP	STRT	External trigger	Hardware macro(VDC) state
0	0	0	0	—	Stopped
1	0	—	—	—	Operating
1	1	1	0	—	Suspended
1	1	1	1	None (waiting)	Suspended
1	1	1	1	Provided (active)	Operating
1	1	0	0	—	Software suspended
Other than above					Setting prohibited

The SNZ bit enables SNOOZE operation. In the external trigger waiting state enabled by setting the STRT bit to 1, the CPU can enter STOP mode. When a falling edge of the external trigger is detected during STOP mode, the CTSU sends a clock request to the clock generating block and enters the SNOOZE state to start measurement. After the measurement end interrupt, clear this bit to 0 by software.
The software suspended state in this table is used when the software of a system without SNOOZE function suspends the CTSU hardware macro to enable low-power operation. In this case, set the SNZ bit to 0 after the CPU returns to the previous state by an external interrupt, and then set the STRT bit to 1 to start measurement upon a software trigger.

SNZ	SNOOZE Enable
0	Disables the SNOOZE function.
1	Enables the SNOOZE function.

The SNZ bit enables or disables the SNOOZE function when an external trigger is selected (CAP = 1). Setting this bit to 1 drives the CTSU hardware macro into the suspended state to enable low-power operation in the standby state.

<CTSU hardware state control>

PON	SNZ	CAP	STRT	Trigger	State of the CTSU
0	0	0	0	—	Stopped
1	0	0	0	—	State until measurement starts (VDC = ON)
1	0	0	1	—	Measurement in the normal mode (VDC = ON)
1	1	1	0	—	Prepared for measurement start by an external trigger (VDC = OFF)
1	1	1	1	Not present	Suspended (waiting for a trigger) (VDC = OFF)
1	1	1	1	Present	Measurement in the SNOOZE mode (VDC = ON)Note
1	1	0	0	—	Software suspended (VDC = OFF)
Other than above					Setting prohibited

Note When a trigger is generated in the STOP mode, measurement is handled in the SNOOZE mode.

The SNZ bit enables SNOOZE operation. In the external trigger waiting state enabled by setting the STRT bit to 1, the CPU can enter STOP mode. When a falling edge of the external trigger is detected during STOP mode, the CTSU sends a clock request to the clock generating block and enters the SNOOZE state to start measurement. After the measurement end interrupt, clear this bit to 0 by software.
The software suspended state in this table is used when the software of a system without SNOOZE function suspends the CTSU hardware macro to enable low-power operation. In this case, set the SNZ bit to 0 after the CPU returns to the previous state by an external interrupt, and then set the STRT bit to 1 to start measurement upon a software trigger.

55. Figure 30 - 15 Format of CTSU Calibration Registers L and H (CTSUDBGR0, CTSUDBGR1) (Page 1264, Page 1266)

Incorrect:

Figure 30 - 15 Format of CTSU Calibration Registers L and H (CTSUDBGR0, CTSUDBGR1)

Address: F0528H, F052AH
After reset: 0000H, 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
CTSUDBGR1	TXREV	CCOCALIB	CCOCLK	DACCLK	SUCARRY	SUMSEL	DACCARRY	DACMSEL
	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0

Symbol	15	14	13	12	11	10	9	8
CTSUDBGR0	0	0	0	0	DCOFF	0	IOC	CNTRDSEL
	7	6	5	4	3	2	1	0
	TSOC	SUCLKEN	CLKSEL0[1:0]		DRV	TSOD	TEST[1:0]	

TEST[1:0]		Test Mode
0	0	Normal operation mode
0	1	Setting prohibited
1	0	Setting prohibited. Burn-in mode 1 (STRESS)
1	1	Setting prohibited

The TEST[1:0] bits control operating mode of the CTSU hardware macro.

- Burn-in mode 1 (STRESS)
  This mode is used to increase the reference voltage to stress the V_{DD} system.

Correct:

Figure 30 - 15 Format of CTSU Calibration Registers L and H (CTSUDBGR0, CTSUDBGR1)

Address: F0528H, F052AH
After reset: 0000H, 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
CTSUDBGR1	TXREV	CCOCALIB	CCOCLK	DACCLK	SUCARRY	SUMSEL	DACCARRY	DACMSEL
	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0

Symbol	15	14	13	12	11	10	9	8
CTSUDBGR0	0	0	0	0	DCOFF	0	IOC	CNTRDSEL
	7	6	5	4	3	2	1	0
	TSOC	SUCLKEN	CLKSEL0[1:0]		DRV	TSOD	0	0

56. CHAPTER 30 CAPACITIVE SENSING UNIT (CTSU2L), Cautions when using capacitive sensing unit (Page 1271)

Correct:

30.3 Usage Notes of the Capacitive Sensing Unit

1. Evaluation of detection by the capacitive sensing unit (CTSU)

In the final stage of development, the user must judge whether or not detection by the touch sensor is reliable in the systems for customers. To do so, the user must run the systems in nearly completed products and use the QE for Capacitive Touch tool (development assistance tool for capacitive touch sensors) to thoroughly evaluate operation by monitoring the measurement of electrostatic capacitance.

If obtaining the desired results of detection is not possible, adjust the CapTouch parameters (mainly the touch threshold) through QE for Capacitive Touch and re-evaluate the system. Note that, if the CTSU is to be used with the mutual-capacitance method, the measured values for electrostatic capacitance (counted values) might fluctuate according to the state of the port output of the microcomputer due to fluctuations of the output voltage on the transmission pin. If such a phenomenon is observed, use QE for Capacitive Touch to set the touch threshold in consideration of the fluctuations in the counted values. Such fluctuations will not be seen with the self-capacitance method.

57. 31.1 Overview (Page 1272)

Incorrect:

31.1 Overview

The RL78/G23 incorporates a circuit for constant voltage operation. To stabilize the output voltage from the regulator, connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). Use a capacitor with good characteristics, since it is for stabilizing the internal voltage.

Correct:

31.1 Overview

The RL78/G23 incorporates a circuit for constant voltage operation. To stabilize the output voltage from the regulator, connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). Use a capacitor with good characteristics, since it is for stabilizing the internal voltage.

The REGC pin can be used as a reference voltage for an external circuit. An external circuit for connection to the REGC pin for this purpose must have an input impedance of at least 1.5 MΩ. The voltage on the REGC pin is in the range from 1.38 to 1.60 V, and the typical value is 1.5 V.

58. Figure 32 - 5 Format of User Option Byte (000C2H or 040C2H) (Page 1279)

Incorrect:

Figure 32 - 5 Format of User Option Byte (000C2H or 040C2H)

Address: 000C2H or 040C2H[Note]

Symbol	7	6	5	4	3	2	1	0
	CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

Value of the Option Byte (000C2H)		Flash Operation Mode	Operating Frequency Range	Operating Voltage Range
CMODE1	CMODE0			
0	1	LP (low-power main) mode	1 MHz to 2 MHz	1.6 V to 5.5 V
1	0	LS (low-speed main) mode	1 MHz to 2 MHz	1.6 V to 5.5 V
			1 MHz to 4 MHz (Rewriting of flash memory is not possible.)	
			1 MHz to 24 MHz	1.8 V to 5.5 V
1	1	HS (high-speed main) mode	1 MHz to 2 MHz	1.6 V to 5.5 V
			1 MHz to 4 MHz (Rewriting of flash memory is not possible.)	
			1 MHz to 32 MHz	1.8 V to 5.5 V
Other than above		Setting prohibited		

Correct:

Figure 32 - 5 Format of User Option Byte (000C2H or 040C2H)

Address: 000C2H or 040C2H[Note]

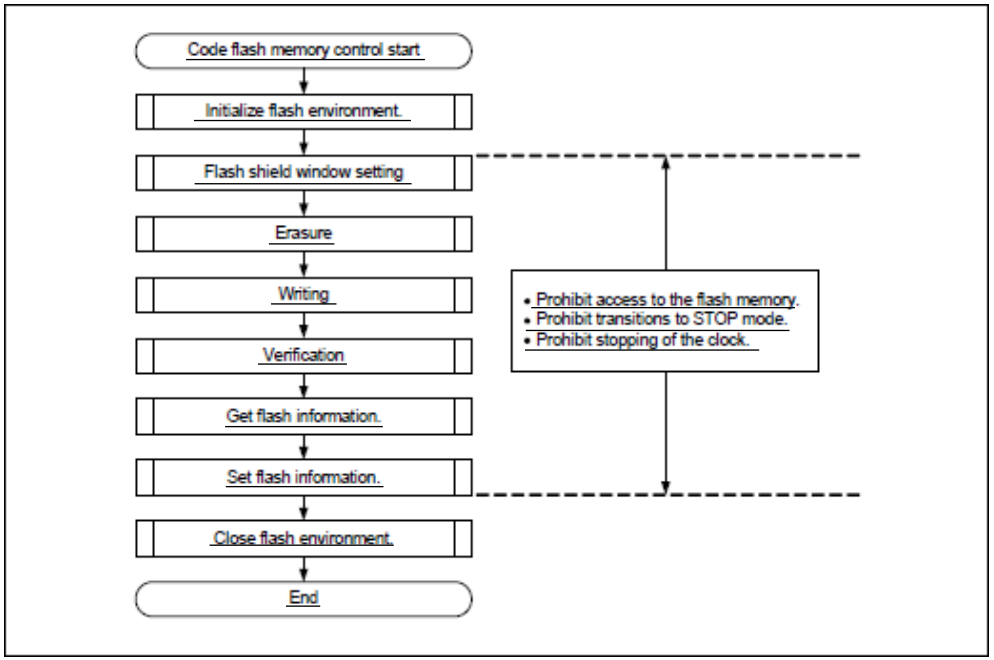
Symbol	7	6	5	4	3	2	1	0
	CMODE1	CMODE0	1	0	FRQSEL3	FRQSEL2	FRQSEL1	FRQSEL0

Value of the Option Byte (000C2H)		Flash Operation Mode	Operating Frequency Range	Operating Voltage Range
CMODE1	CMODE0			
0	1	LP (low-power main) mode	1 MHz to 2 MHz (Rewriting of flash memory is not possible.)	1.6 V to 5.5 V
1	0	LS (low-speed main) mode	1 MHz to 2 MHz	1.6 V to 5.5 V
			1 MHz to 4 MHz (Rewriting of flash memory is not possible.)	
			1 MHz to 24 MHz	1.8 V to 5.5 V
1	1	HS (high-speed main) mode	1 MHz to 2 MHz	1.6 V to 5.5 V
			1 MHz to 4 MHz (Rewriting of flash memory is not possible.)	
			1 MHz to 32 MHz	1.8 V to 5.5 V
Other than above		Setting prohibited		

59. Figure 33 - 8 Flow of Self-Programming (Rewriting Flash Memory) (Page 1297)

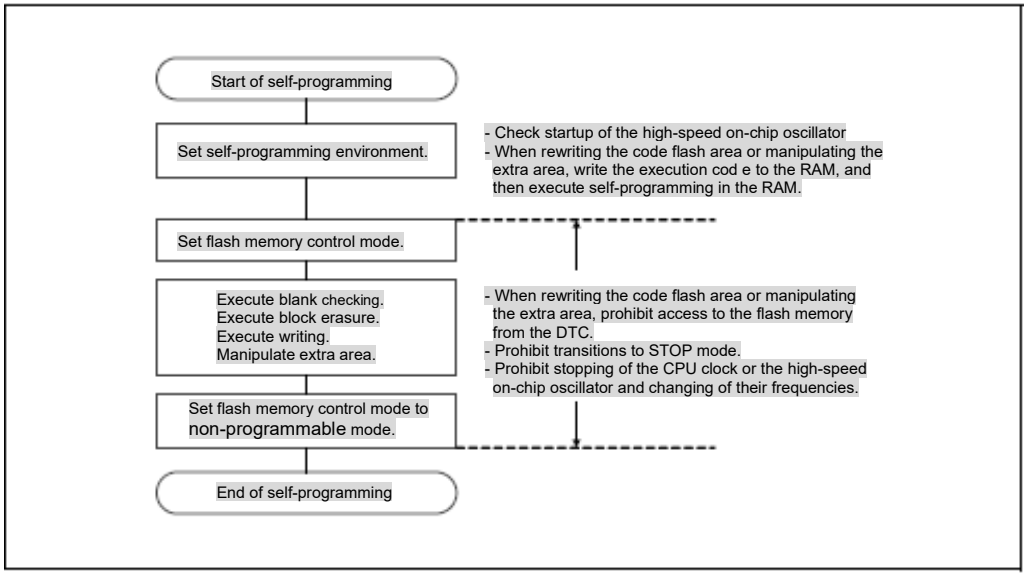
Incorrect:

Figure 33 - 8 Flow of Self-Programming (Rewriting Flash Memory)



Correct:

Figure 33 - 8 Flow of Self-Programming (Rewriting Flash Memory)



60. 33.6.2.1 Flash address pointer registers H and L (FLAPH, FLAPL) (Page 1300)

Incorrect:

Figure 33 - 9 Format of Flash Address Pointer Registers H and L (FLAPH, FLAPL)

Address: F02C4H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
FLAPH	0	0	0	0	FLAP19	FLAP18	FLAP17	FLAP16

Address: F02C2H
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
FLAPL	FLAP15	FLAP14	FLAP13	FLAP12	FLAP11	FLAP10	FLAP9	FLAP8

7	6	5	4	3	2	1	0
FLAP7	FLAP6	FLAP5	FLAP4	FLAP3	FLAP2	FLAP1	FLAP0

Caution 1. Values read during the execution of a command for the extra area sequencer are undefined.

Caution 2. The settings of the FLAP1 and FLAP0 bits are meaningless during programming of the code flash memory.

Caution 3. New values cannot be written to these registers while the flash memory sequencer is operating.

Correct:

Figure 33 - 9 Format of Flash Address Pointer Registers H and L (FLAPH, FLAPL)

Address: F02C4H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
FLAPH	0	0	0	0	FLAP19	FLAP18	FLAP17	FLAP16

Address: F02C2H
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
FLAPL	FLAP15	FLAP14	FLAP13	FLAP12	FLAP11	FLAP10	FLAP9	FLAP8

7	6	5	4	3	2	1	0
FLAP7	FLAP6	FLAP5	FLAP4	FLAP3	FLAP2	FLAP1	FLAP0

Caution 1. The FLAPH and FLAPL registers can be rewritten under either of the following conditions.
- The FLSPM bit in the FLPMC register is 1 (Code flash memory area: programming mode).
- The EEMD bit in the FLPMC register is 1 (Data flash memory area: programming mode).

Caution 2. Rewrite or read these registers when the extra area sequencer and the code/data flash memory area sequencer are stopped (the SQEND and ESQEND bits in FSASTH are 0).

61. 33.6.2.2 Flash end address pointer registers H and L (FLSEDH, FLSEDL) (Page 1301)

Incorrect:

Figure 33 - 10 Format of Flash End Address Pointer Registers H and L (FLSEDH, FLSEDL)

Address: F02C8H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
FLSEDH	0	0	0	0	EWA19	EWA18	EWA17	EWA16

Address: F02C8H
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
FLSEDL	EWA15	EWA14	EWA13	EWA12	EWA11	EWA10	EWA9	EWA8

7	6	5	4	3	2	1	0
EWA7	EWA6	EWA5	EWA4	EWA3	EWA2	EWA1	EWA0

Caution 1. Values read during the execution of a command for the extra area sequencer are undefined.

Caution 2. The settings of the EWA1 and EWA0 bits are meaningless during programming of the code flash memory.

Caution 3. New values cannot be written to these registers while the flash memory sequencer is operating.

Correct:

Figure 33 - 10 Format of Flash End Address Pointer Registers H and L (FLSEDH, FLSEDL)

Address: F02C8H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
FLSEDH	0	0	0	0	EWA19	EWA18	EWA17	EWA16

Address: F02C8H
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
FLSEDL	EWA15	EWA14	EWA13	EWA12	EWA11	EWA10	EWA9	EWA8

7	6	5	4	3	2	1	0
EWA7	EWA6	EWA5	EWA4	EWA3	EWA2	EWA1	EWA0

Caution 1. The FLSEDH and FLSEDL registers can be rewritten under either of the following conditions.
- The FLSPM bit in the FLPMC register is 1 (Code flash memory area: programming mode).
- The EEMD bit in the FLPMC register is 1 (Data flash memory area: programming mode).

Caution 2. Rewrite or read these registers when the extra area sequencer and the code/data flash memory area sequencer are stopped (the SQEND and ESQEND bits in FSASTH are 0).

Caution 3. The settings of the EWA1 and EWA0 bits are meaningless during programming of the code flash memory.

62. 33.6.2.3 Flash write buffer registers H and L (FLWH, FLWL) (Page 1303)

Incorrect:

33.6.2.3 Flash write buffer registers H and L (FLWH, FLWL)

The FLWH and FLWL registers hold data to be written during programming of the flash memory.

The FLWH and FLWL registers can be set by a 16-bit memory manipulation instruction.

The value of each of the FLWH and FLWL registers is 0000H under any of the following conditions.

• Following a reset

• The value of the FLRST bit of the FLRST register is 1.

• The flash memory sequencer has finished operating.

Writing to these registers is not possible while the value of the FLRST bit is 1.

Set data to be written to the data flash memory in the 8 lower-order bits of the FLWL register.

Figure 33 - 11 Format of Flash Write Buffer Registers H and L (FLWH, FLWL)

Address: F02CEH
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
FLWH	FLW31	FLW30	FLW29	FLW28	FLW27	FLW26	FLW25	FLW24

7	6	5	4	3	2	1	0
FLW23	FLW22	FLW21	FLW20	FLW19	FLW18	FLW17	FLW16

Address: F02CCH
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
FLWL	FLW15	FLW14	FLW13	FLW12	FLW11	FLW10	FLW9	FLW8

7	6	5	4	3	2	1	0
FLW7	FLW6	FLW5	FLW4	FLW3	FLW2	FLW1	FLW0

Correct:

33.6.2.3 Flash write buffer registers H and L (FLWH, FLWL)

The FLWH and FLWL registers hold data to be written during programming of the flash memory.

The FLWH and FLWL registers can be set by a 16-bit memory manipulation instruction.

The value of each of the FLWH and FLWL registers is 0000H under any of the following conditions.

• Following a reset

• The value of the FLRST bit of the FLRST register is 1.

• The flash memory sequencer has finished operating.

Set data to be written to the data flash memory in the 8 lower-order bits of the FLWL register.

Figure 33 - 11 Format of Flash Write Buffer Registers H and L (FLWH, FLWL)

Address: F02CEH
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
FLWH	FLW31	FLW30	FLW29	FLW28	FLW27	FLW26	FLW25	FLW24

7	6	5	4	3	2	1	0
FLW23	FLW22	FLW21	FLW20	FLW19	FLW18	FLW17	FLW16

Address: F02CCH
After reset: 0000H
R/W: R/W

Symbol	15	14	13	12	11	10	9	8
FLWL	FLW15	FLW14	FLW13	FLW12	FLW11	FLW10	FLW9	FLW8

7	6	5	4	3	2	1	0
FLW7	FLW6	FLW5	FLW4	FLW3	FLW2	FLW1	FLW0

Caution 1. Reading from these registers is not possible while a sequencer command is being executed.

Caution 2. When writing to the data flash memory, set 0s in the FLWH register and the bits of the FLWL register other than the 8 lower-order bits.

Caution 3. New values cannot be written to these registers while the flash memory sequencer is operating.

Caution 1. The FLWH and FLWL registers can be rewritten under either of the following conditions.
- The FLSPM bit in the FLPMC register is 1 (Code flash memory area: programming mode).
- The EEMD bit in the FLPMC register is 1 (Data flash memory area: programming mode).

Caution 2. Rewrite or read these registers when the extra area sequencer and the code/data flash memory area sequencer are stopped (the SQEND and ESQEND bits in FSASTH are 0).

Caution 3. When writing to the data flash memory, set write data in the 8 lower-order bits of the FLWL register. Set other bits to 0.

63. 33.6.2.6 Flash programming mode control register (FLPMC) (Page 1306)

Incorrect:

Figure 33 - 14 Format of Flash Programming Mode Control Register (FLPMC)

Address: F02C0H
After reset: 08H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
FLPMC	0	0	0	EEEMD	FWEDIS	0	FLSPM	0

EEEMD	Selection of the programming mode for the data flash memory
0	Rewrite-disabled mode
1	Programming mode

FWEDIS	Software control over enabling or disabling erasure and programming of the code flash memory Note
0	Enables erasure and programming.
1	Disables erasure and programming.

FLSPM	Selection of the programming mode for the code flash memory
0	Rewrite-disabled mode
1	Programming mode

Note Be sure to keep the value of this bit at 0 until erasure or programming of the code flash memory is completed.

Correct:

Figure 33 - 14 Format of Flash Programming Mode Control Register (FLPMC)

Address: F02C0H
After reset: 08H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
FLPMC	0	0	0	EEEMD	FWEDIS	0	FLSPM	0

EEEMD	Selection of the programming mode for the data flash memory
0	Non-programmable mode
1	Programming mode

FWEDIS	Software control over enabling or disabling erasure and programming of the code flash memory Note
0	Enables erasure and programming.
1	Disables erasure and programming.

FLSPM	Selection of the programming mode for the code flash memory
0	Non-programmable mode
1	Programming mode

Note Be sure to keep the value of this bit at 0 until erasure or programming of the code flash memory is completed.

Caution When the extra area sequencer and the code/data flash memory area sequencer are stopped (the SQEND and ESQEND bits in FSASTH are 0), rewriting to the FLPMC register is enabled.

64. 33.6.2.8 Flash memory sequencer initial setting register (FSSET) (Page 1308)

Incorrect:

Figure 33 - 16 Format of Flash Memory Sequencer Initial Setting Register (FSSET)

Address: F00B6H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
FSSET	TMSPMD	TMBTSEL	0	FSET4	FSET3	FSET2	FSET1	FSET0

TMSPMD	Specification for boot swapping[Note]
0	Follows the information in the extra area.
1	Follows the setting of the TMBTSEL bit.

TMBTSEL	Setting for temporary boot swapping[Note]
0	Specifies boot cluster 0 as the boot area (boot swapping does not proceed).
1	Specifies boot cluster 1 as the boot area (boot swapping proceeds).

FSET[4:0]	Setting of the operating frequency of the flash memory sequencer
—	Set the operating frequency of the flash memory sequencer. For the correspondence between the operating frequency of the flash memory sequencer and the setting of the FSET[4:0] bits, see **Table 33 - 12**.

Note Setting the TMSPMD and TMBTSEL bits is not possible while boot protection is set (BTPR = 0).

Caution Set the value corresponding to that obtained by rounding the CPU operating frequency up to the nearest whole number in the FSET[4:0] bits. For example, when the CPU operating frequency is 4.5 MHz, set the bits for 5 MHz.
Note that frequencies that are not whole numbers, such as 1.5 MHz, are not available as CPU operating frequencies below 4 MHz.

Correct:

Figure 33 - 16 Format of Flash Memory Sequencer Initial Setting Register (FSSET)

Address: F00B6H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
FSSET	TMSPMD	TMBTSEL	0	FSET4	FSET3	FSET2	FSET1	FSET0

TMSPMD	Selection of boot area setting [Note]
0	Specifies the boot area according to the setting of EX bit 8 (BTFLG) in the security flag and boot swap function setting area of the extra area. BTFLG = 0: Boot cluster 1 as the boot area BTFLG = 1: Boot cluster 0 as the boot area (default)
1	Specifies the boot area according to the setting of the TMBTSEL bit.

TMBTSEL	Specification of the boot area when TMPSMD = 1
0	Specifies boot cluster 0 as the boot area.
1	Specifies boot cluster 1 as the boot area.

FSET4 to FSET0	Setting of the operating frequency of the flash memory sequencer
—	Sets the operating frequency of the flash memory sequencer. For the correspondence between the operating frequency of the flash memory sequencer and the setting of the FSET4 to FSET0 bits, see **Table 33 - 11**.

Note Setting the TMSPMD and TMBTSEL bits is not possible while the BTPR bit in FLSEC is 0 (rewriting of the boot area disabled).

Caution 1. The FSSET register can be rewritten under either of the following conditions.
- The FLSPM bit in the FLPMC register is 1 (Code flash memory area: programming mode)
- The EEMD bit in the FLPMC register is 1 (Data flash memory area: programming mode)

Caution 2. The set values of the boot area are immediately reflected. To change the boot area after a reset is released, read the MBTSL bit in FSASTL while TMPSMD = 0 and set the same value to the TMBTSL bit. After that, set the TMPSMD bit to 1, and then specify the boot cluster to be set as the boot area after release from the reset state in the BTFLG bit using the extra area sequencer. The boot cluster set by the BTFLG bit is activated as a boot area at the next reset release.

Table 33 - 12 Correspondence between the Operating Frequency of the Flash Memory Sequencer and the Setting of the FSET[4:0] Bits

Operating Frequency (MHz)	Setting of the FSET[4:0] Bits	Operating Frequency (MHz)	Setting of the FSET[4:0] Bits	Operating Frequency (MHz)	Setting of the FSET[4:0] Bits
32	11111b	31	11110b	30	11101b
29	11100b	28	11011b	27	11010b
26	11001b	25	11000b	24	10111b
23	10110b	22	10101b	21	10100b
20	10011b	19	10010b	18	10001b
17	10000b	16	01111b	15	01110b
14	01101b	13	01100b	12	01011b
11	01010b	10	01001b	9	01000b
8	00111b	7	00110b	6	00101b
5	00100b	4	00011b	3	00010b
2	00001b	1	00000b	—	—

Table 33 - 12 Correspondence between the Operating Frequency of the Flash Memory Sequencer and the Setting of the FSET4 to FSET0 Bits

Operating Frequency (MHz)	Setting of the FSET4 to FSET0 Bits	Operating Frequency (MHz)	Setting of the FSET4 to FSET0 Bits	Operating Frequency (MHz)	Setting of the FSET4 to FSET0 Bits
32	11111b	31	11110b	30	11101b
29	11100b	28	11011b	27	11010b
26	11001b	25	11000b	24	10111b
23	10110b	22	10101b	21	10100b
20	10011b	19	10010b	18	10001b
17	10000b	16	01111b	15	01110b
14	01101b	13	01100b	12	01011b
11	01010b	10	01001b	9	01000b
8	00111b	7	00110b	6	00101b
5	00100b	4	00011b	3	00010b
2	00001b	1	00000b	—	—

Caution Set the value corresponding to that obtained by rounding the CPU operating frequency up to the nearest whole number in the FSET[4:0] bits.(For example, when the CPU operating frequency is 4.5 MHz, set the bits for 5 MHz.)Note that frequencies that are not whole numbers, such as 1.5 MHz, are not available as CPU operating frequencies below 4 MHz.

65. 33.6.2.9 Flash memory sequencer control register (FSSQ) (Page 1310, Page 1311)

Incorrect:

33.6.2.9 Flash memory sequencer control register (FSSQ)

The FSSQ register specifies the commands to be used when the code/data flash memory area sequencer is activated.

The FSSQ register can be set by a 1-bit or 8-bit memory manipulation instruction.

The value of the FSSQ register is 00H under either of the following conditions.

• Following a reset

• The value of the FLRST bit of the FLRST register is 1.

Figure 33 - 17 Format of Flash Memory Sequencer Control Register (FSSQ)

Address: F02C5H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
FSSQ	SQST	FSSTP	0	0	MDCH	SQMD2	SQMD1	SQMD0

SQST	Operation control of the code/data flash memory area sequencer
0	The code/data flash memory area sequencer is stopped.
1	The code/data flash memory area sequencer is started.

FSSTP	Forcible termination control of the code/data flash memory area sequencer
0	The code/data flash memory area sequencer is not forcibly terminated.
1	The code/data flash memory area sequencer is forcibly terminated.

Correct:

33.6.2.9 Flash memory sequencer control register (FSSQ)

The FSSQ register specifies operation control and commands for use with the code/data flash memory area sequencer.

When the SQST bit in this register is set to 1, the code/data flash memory area sequencer executes the command set in the MDCH, SQMD2, SQMD1, and SQMD0 bits.

The FSSQ register can be set by a 1-bit or 8-bit memory manipulation instruction.

The value of the FSSQ register is 00H under either of the following conditions.

• Following a reset

• The value of the FLRST bit of the FLRST register is 1.

Figure 33 - 17 Format of Flash Memory Sequencer Control Register (FSSQ) (1/2)

Address: F02C5H
After reset: 00H
R/W: R/W

Symbol	<7>	<6>	5	4	3	2	1	0
FSSQ	SQST	FSSTP	0	0	MDCH	SQMD2	SQMD1	SQMD0

SQST	Operation control of the code/data flash memory area sequencer
0	The code/data flash memory area sequencer is stopped. Note 1
1	The code/data flash memory area sequencer is started.

FSSTP	Forcible termination control of the code/data flash memory area sequencer
0	The code/data flash memory area sequencer is not forcibly terminated.
1	The code/data flash memory area sequencer is forcibly terminated.

SQMD[2:0]	MDCH setting	Control of the code/data flash memory area sequencer
01H	CF: 0 DF: 0	Write Writes data specified in the FLWH and FLWL registers to the address specified in the FLAPH and FLAPL registers. • Writing 1 word (4 bytes) of data to the code flash memory: Set the data in the FLWH and FLWL registers. • Writing 1 byte of data to the data flash memory: Set the data in the FLW[7:0] bits of the FLWL register.
03H	CF: 0 DF: 1	Blank check Executes blank checking of the range from the address specified in the FLAPH and FLAPL registers to the address specified in the FLSEDH and FLSEDL registers. The setting of the MDCH bit of the FSSQ register depends on the target flash memory area for blank checking. Blank checking of the code flash memory or data flash memory respectively requires setting the MDCH bit to 0 or 1 before running the check.
04H	CF: 0 DF: 0	Block erase Erases blocks in the range from the block start address specified in the FLAPL and FLAPH registers to the block end address specified in the FLSEDL and FLSEDH registers.
Other than above		Setting prohibited

Caution Initialization by setting the FLRST bit to 1 is only enabled while the sequencer is stopped (both the SQEND and ESQEND bits of the FSASTH register have the setting 0).

MDCH	SQMD2	SQMD1	SQMD0	Commands for Use with the Code/Data Flash Memory Area Sequencer
0	0	0	1	• Writing Writes data stored in the FLWH and FLWL registers to the address specified in the FLAPH and FLAPL registers. Note 2 Writes 4-byte data when the code flash memory area address is specified. Writes the 1-byte data stored in the eight lower-order bits (FLW7 to FLW0) in FLWL to the specified address when the data flash memory area address is specified.
0	0	1	1	• Blank checking of the code flash memory area Checks whether the value of the code flash memory area (from the address specified in the FLAPH and FLAPL registers to the address specified in the FLSEDH and FLSEDL registers) is 0. Note 3
1	0	1	1	• Blank checking of the data flash memory area Checks whether the value of the data flash memory area (from the address specified in the FLAPH and FLAPL registers to the address specified in the FLSEDH and FLSEDL registers) is 0.
0	1	0	0	• Block erasure Erases blocks in the range from the block start address specified in the FLAPH and FLAPL registers to the block end address specified in the FLSEDH and FLSEDL registers. Note 4
Other than above				Setting prohibited

Note 1. Check that the SQEND bit in the FSASTH register is 1 (the code/data flash memory area sequencer being stopped.), and then set the SQST bit to 0 to stop the code/data flash memory area sequencer.

Note 2. Four-byte data can be written to the code flash memory area. Set the two lower-order bits of the FLSEDL register to 00B to be a multiple of 4. For details, see 33.6.6.4 Operations for rewriting the code flash memory area.

Note 3. Specify a start address (at intervals of four bytes) for blank checking of the code flash memory area. Set the two lower-order bits of the FLSEDL register to 00B to be a multiple of 4. For details, see 33.6.6.4 Operations for rewriting the code flash memory area.

Note 4. The code flash memory area blocks can be erased in units of 2 Kbytes. The data flash memory blocks can be erased in units of 256 bytes. Specify the erase addresses (start address and end address) so that all blocks to be erased are included. For details, see 33.6.6.4 Operations for rewriting the code flash memory area and 33.6.6.5 Operations for rewriting the data flash memory area. For the relationship between the address and block number, see Table 3 - 1 Correspondence between Addresses and Block Numbers in Flash Memory (1/3).

Caution The FSSQ register can be rewritten under either of the following conditions.

- The FLSPM bit in the FLPMC register is 1 (code flash memory area: programming mode) and the FWEDIS bit is 0 (enabling erasure and programming of the code flash memory).
- The EEEMD bit in the FLPMC register is 1 (data flash memory area: programming mode).

66. 33.6.2.10 Flash extra sequencer control register (FSSE) (Page 1312)

Incorrect:

Figure 33 - 18 Format of Flash Extra Sequencer Control Register (FSSE)

ESQMD [3:0]	Control of the extra area sequencer
00H	Write to the extra area (programming of the FSW-related data) Writes data specified in the FLWH and FLWL registers. Sets up the FSW, FSW control, and FSW protection flag. When the FSW protection flag has been set (FSPR = 0), this action cannot be executed. Attempted execution leads to a sequencer error (setting the ESEQER bit of the FSASTL register to 1).
06H	Write to the extra area (programming of the read-prohibited area of software from a third party and the protection flag) Writes data specified in the FLWH and FLWL registers. Sets up the read-prohibited area of software from a third party and the protection flag. When the protection flag has been set (SWPR = 0), this action cannot be executed. Attempted execution leads to a sequencer error (setting the ESEQER bit of the FSASTL register to 1).
07H	Write to the extra area (programming of the security flags and boot area switching flag) Writes data specified in the FLWH and FLWL registers. Sets up the security flags and boot area switching flag. For the security flags, only changing the current state of each flag to "disabled" is possible. If boot protection has been set (BTPR = 0), setting the boot area switching flag is not possible.
Other than above	Setting prohibited

Correct:

Figure 33 - 18 Format of Flash Extra Area Sequencer Control Register (FSSE) (2/2)

ESQMD3	ESQMD2	ESQMD1	ESQMD0	Commands for Use with the extra area sequencer
0	0	0	1	• Write to the flash shield window setting area Writes the 4-byte data specified in the FLWH and FLWL registers to the flash shield window setting area of the extra area to control flash shield window mode and set the start block and end block. Also, if the setting of EX bit 15 (FSPR) in the flash shield window setting area is 0, no value can be written to the area. Attempted writing leads to setting of the extra area sequencer error flag (ESEQER) to 1.
0	1	1	0	• Write to the flash read protection setting area Writes the 4-byte data specified in the FLWH and FLWL registers to the flash read protection setting area of the extra area to disable changing of the flash read protection setting and set the start block and end block. Also, if the setting of EX bit 31 (SWPR) in the flash read protection setting area is 0, no value can be written to the area. Attempted writing leads to setting of the extra area sequencer error flag (ESEQER) to 1.
0	1	1	1	• Write to the security flag and boot swap function setting area Writes the 4-byte data specified in the FLWH and FLWL registers to the flash memory security flag and boot swap function setting area of the extra area to disable block erasure, writing, and rewriting of boot cluster 0 and set selection of the boot area. Also, if the setting of EX bit 9 (BTPR) in the security flag and boot swap function setting area is 0, no value can be written to the area. Attempted writing leads to setting of the extra area sequencer error flag (ESEQER) to 1.
Other than above				Setting prohibited

Caution 1. Initialization by setting the FLRST bit to 1 is only enabled while the sequencer is stopped (both the SQEND and ESQEND bits of the FSASTH register have the setting 0).

Caution 2. To write to the extra area, set the EXA bit of the FLARS register to 1 and set the data to be written in the FLWH and FLWL registers before activating the extra area sequencer.

Caution 3. Values read from the FLAPL, FLWH, FLWL, and FSSQ registers are undefined after activation of the extra area sequencer.

Note Check that the ESQEND bit in the FSASTH register is 1 (The extra area sequencer being stopped), and then set the ESQST bit to 0 to stop the extra area sequencer.

Caution 1. The FSSE register can be rewritten when the following condition is met.
- The FLSPM bit in the FLPMC register is 1 (code flash memory area: programming mode) and the FWEDIS bit is 0 (enabling erasure and programming of the code flash memory).

Caution 2. To write to the extra area, set the EXA bit of the FLARS register to 1 and set the data to be written in the FLWH and FLWL registers before activating the extra area sequencer.

Caution 3. Rewrite the ESQMD3 to ESQMD0 bits while the extra area sequencer and the code/data flash memory area sequencer are stopped (SQEND = 0, ESQEND = 0 in FSASTH).

67. 33.6.2.11 Flash registers initialization register (FLRST) (Page 1313)

Incorrect:

Figure 33 - 19 Format of Flash Registers Initialization Register (FLRST)

Address: F02C9H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
FLRST	0	0	0	0	0	0	0	FLRST

FLRST	Control of initializing the registers[Note]
0	The registers are not initialized.
1	The registers are initialized.

Note For details on how to handle the FLRST register, see 33.6.4 Clearing the registers for use with the flash memory sequencer.

Caution The registers below are initialized with the use of this register.
FLAPH, FLAPL, FLSEDH, FLSEDL, FLWH, FLWL, FLARS, FSSQ, FSSE

Correct:

Figure 33 - 19 Format of Flash Registers Initialization Register (FLRST)

Address: F02C9H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	0
FLRST	0	0	0	0	0	0	0	FLRST

FLRST	Control of initializing the registers[Note]
0	The registers are not initialized.
1	The registers are initialized.

Caution 1. Registers can be initialized by setting the FLRST bit to 1 only when the extra area sequencer and the code/data flash memory area sequencer are stopped (SQEND = 0, ESQEND = 0 in FSASTH).

Caution 2. When using the sequencer, be sure to set the FLRST bit to 0 before setting the FLAPH, FLAPL, FLSEDH, FLSEDL, FLWH, FLWL, FLARS, FSSQ, and FSSE registers. Do not set the FLRST bit to 1 during operation of the sequencer.

68. 33.6.2.12 Flash memory sequencer status registers H and L (FSASTH, FSASTL) (Page 1314)

Incorrect:

Figure 33 - 20 Format of Flash Memory Sequencer Status Registers H and L (FSASTH, FSASTL)

Address: F02CBH
After reset: 00H
R/W: R

Symbol	7	6	5	4	3	2	1	0
FSASTH	ESQEND	SQEND	0	0	0	0	0	0

Address: F02CAH
After reset: 00H Note
R/W: R

Symbol	7	6	5	4	3	2	1	0
FSASTL	MBTSEL	MOPEN	ESEQER	SEQER	BLER	0	WRER	ERER

Note The initial value of the MBTSEL bit is undefined because it depends on the value of the BTFLG bit (boot area switching flag) stored in the extra area.

Correct:

Figure 33 - 20 Format of Flash Memory Sequencer Status Registers H and L (FSASTH, FSASTL)

Address: F02CBH
After reset: 00H
R/W: R

Symbol	7	6	5	4	3	2	1	0
FSASTH	ESQEND	SQEND	0	0	0	0	0	0

Address: F02CAH
After reset: Undefined Note
R/W: R

Symbol	7	6	5	4	3	2	1	0
FSASTL	MBTSEL	MOPEN	ESEQER	SEQER	BLER	0	WRER	ERER

Note The initial value of the MBTSEL bit is undefined because it depends on the value of the BTFLG bit (boot area switching flag) stored in the extra area.

69. 33.6.2.13 Flash security flag monitoring register (FLSEC) (Page 1316)

Incorrect:

Figure 33 - 21 Format of Flash Security Flag Monitoring Register (FLSEC)

Address: F00B0H
After reset: Undefined
R/W: R

Symbol	15	14	13	12	11	10	9	8
FLSEC	0	0	0	WRPR	0	SEPR	BTPR	BTFLG

7	6	5	4	3	2	1	0
0	0	0	0	SWPR	0	1	0

WRPR	Write-prohibited flag
0	Writing is prohibited.
1	Writing is enabled.

SEPR	Block erase-prohibited flag
0	Block erasure is prohibited.
1	Block erasure is enabled.

BTPR	Boot area rewrite-prohibited flag
0	Rewriting of the boot area is prohibited.
1	Rewriting of the boot area is enabled.

BTFLG	Boot area switching flag
0	The boot area is boot cluster 0.
1	The boot area is boot cluster 1.

SWPR	Software from a third party read-prohibited flag
0	Reading software from a third party is prohibited.
1	Reading software from a third party is enabled.

Correct:

Figure 33 - 21 Format of Flash Security Flag Monitoring Register (FLSEC)

Address: F00B0H
After reset: Undefined
R/W: R

Symbol	15	14	13	12	11	10	9	8
FLSEC	0	0	0	WRPR	0	SEPR	BTPR	BTFLG

7	6	5	4	3	2	1	0
0	0	0	0	SWPR	0	IFPR	IDEN

WRPR	Write-disabled flag
0	Writing is disabled.
1	Writing is enabled.

SEPR	Block erase-disabled flag
0	Block erasure is disabled.
1	Block erasure is enabled.

BTPR	Boot area rewrite-disabled flag
0	Rewriting of the boot area is disabled.
1	Rewriting of the boot area is enabled.

BTFLG	Boot area switching flag
0	The boot area is boot cluster 1.
1	The boot area is boot cluster 0.

SWPR	Flag to indicate disabling changing of the flash memory read protection setting
0	Changing of the flash memory read protection setting is disabled.
1	Changing of the flash memory read protection setting is enabled.

IFPR	Flag to indicate disabling of connection to the programmer and on-chip debugger
0	Connection to the programmer and on-chip debugger is disabled.
1	Connection to the programmer and on-chip debugger is enabled.

IDEN	Flag to indicate enabling of programmer connection ID authentication
0	ID authentication is enabled.
1	ID authentication is disabled.

70. 33.6.2.14 Flash FSW monitoring register E (FLFSWE) (Page 1317)

Incorrect:

Figure 33 - 22 Format of Flash FSW Monitoring Register E (FLFSWE)

Address: F00B4H
After reset: Undefined
R/W: R

Symbol	15	14	13	12	11	10	9	8
FLFSWE	FSWC	0	0	0	0	0	0	FSWE8

7	6	5	4	3	2	1	0
FSWE7	FSWE6	FSWE5	FSWE4	FSWE3	FSWE2	FSWE1	FSWE0

FSWE[8:0]	End block number specified for the flash shield area
—	End block number (end block number in the window range + 1)Note

FSWC	Setting of the shield area
0	The shield area is set inside the window range.
1	The shield area is set outside the window range.

Note The setting during serial programming is different from this. For details, see Table 33 – 13.

Correct:

Figure 33 - 22 Format of Flash FSW Monitoring Register E (FLFSWE)

Address: F00B4H
After reset: Undefined
R/W: R

Symbol	15	14	13	12	11	10	9	8
FLFSWE	FSWC	0	0	0	0	0	0	FSWE8

7	6	5	4	3	2	1	0
FSWE7	FSWE6	FSWE5	FSWE4	FSWE3	FSWE2	FSWE1	FSWE0

FSWC	Setting of the flash memory shield area
0	Inside shield mode The flash memory shield area is set inside the window range.
1	Outside shield mode The flash memory shield area is set outside the window range.

FSWE8 to FSWE0	End block number of the flash memory shield area
—	End block number + 1 Note

Note These bits show the value set in the extra area. The actual end block number is (the value of the FSWE8 to FSWE0 bits - 1). Though the end block number is specified for serial programming, (end block number + 1) is set in the extra area. For details, see Table 33 - 12.

71. 33.6.2.16 Data flash control register (DFLCTL) (Page 1319)

Incorrect:

33.6.2.16 Data flash control register (DFLCTL)

The DFLCTL register enables or disables access to the data flash memory.

The DFLCTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

The value of this register is 00H following a reset.

Figure 33 - 24 Format of Data Flash Control Register (DFLCTL)

Address: F0090H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	<0>
DFLCTL	0	0	0	0	0	0	0	DFLEN

DFLEN	Data flash access control
0	Access to the data flash memory is disabled.
1	Access to the data flash memory is enabled.

Correct:

33.6.2.16 Data flash control register (DFLCTL)

The DFLCTL register enables or disables access to the data flash memory area and extra area.

The DFLCTL register can be set by a 1-bit or 8-bit memory manipulation instruction.

The value of this register is 00H following a reset.

Figure 33 - 24 Format of Data Flash Control Register (DFLCTL)

Address: F0090H
After reset: 00H
R/W: R/W

Symbol	7	6	5	4	3	2	1	<0>
DFLCTL	0	0	0	0	0	0	0	DFLEN

DFLEN	Data flash memory area/extra area access control
0	Access to the data flash memory area and extra area is disabled.
1	Access to the data flash memory area and extra area is enabled.

72. 33.6.3 Setting the flash memory control mode (Page 1322)

Incorrect:

33.6.3 Setting the flash memory control mode

Execution of the specific sequence for use with the flash memory sequencer enables setting the flash memory control mode to the states where the code or data flash memory area or neither of them can be rewritten.

– State where the code flash memory (and extra area) can be rewritten: Code flash programming mode
– State where the data flash memory can be rewritten: Data flash programming mode
– State where the flash memory (and extra area) cannot be rewritten: Rewrite-disabled mode

Caution For handling of the extra area or data flash memory area, follow the procedure while access to the data flash memory is enabled (the value of the DFLEN bit of the DFLCTL register is 1).

Correct:

33.6.3 Setting the flash memory control mode

The flash memory has the following flash memory control modes.

– Code flash programming mode
  The code flash memory area and the extra area can be rewritten.
– Data flash programming mode
  The data flash memory area and the extra area can be rewritten.
– Rewrite-disabled mode
  The flash memory (code flash memory area, data flash memory area, and extra area) cannot be rewritten.

To rewrite the flash memory, set the flash memory control mode to code flash programming mode or data flash programming mode. Setting each of the flash memory control modes requires executing the specific sequence for setting the flash protect command register (PFCMD) and flash programming mode control register (FLPMC).

Caution For handling of the extra area or data flash memory area, follow the procedure while access to the data flash memory is enabled (the value of the DFLEN bit of the DFLCTL register is 1).

73. 33.6.3.1 Procedure for executing the specific sequence (Page 1322)

Incorrect:

33.6.3.1 Procedure for executing the specific sequence

Writing the required values to the flash programming mode control register (FLPMC register) by following steps 1 to 4 below enables the transitions to each of the flash memory control modes.

<1> Write A5H to the PFCMD register.
<2> Write the value to be set to the FLPMC register.
<3> Write the inverse of the value to be set to the FLPMC register.
<4> Write the value to be set to the FLPMC register.

- The specific sequence can only be executed while the value of the FLRST bit of the FLRST register is 0 and the flash memory sequencer is stopped.
- If writing to any other memory area or register is attempted in the intervals between steps 1 to 4 during execution of the specific sequence, a protection error occurs, writing to the specified register does not proceed, and the FPRERR flag of the flash status register (PFS) is set to 1. The FPRERR flag is cleared following a reset or when execution of the specific sequence is re-started.

Correct:

33.6.3.1 Procedure for executing the specific sequence

Writing the required values to the flash protect command register (PFCMD) and the flash programming mode control register (FLPMC) by following steps 1 to 4 below enables the transitions to each of the flash memory control modes.

<1> Write A5H to the PFCMD register.
<2> Write the value to be set to the FLPMC register.
<3> Write the inverse of the value to be set to the FLPMC register.
<4> Write the value to be set to the FLPMC register.

- The specific sequence can only be executed while the value of the FLRST bit of the FLRST register is 0 and the flash memory sequencer is stopped.
- If writing to any other memory area or register is attempted in the intervals between steps 1 to 4 during execution of the specific sequence, a protection error occurs, writing to the specified register does not proceed, and the FPRERR flag of the flash status register (PFS) is set to 1. The FPRERR flag is cleared following a reset or when execution of the specific sequence is re-started.

74. 33.6.6.4 Operations for rewriting the code flash memory area (Page 1326)

Incorrect:

33.6.6.4 Operations for rewriting the code flash memory area

To rewrite the code flash memory area, enter the code flash programming mode and then execute commands for use with the code/data flash memory area sequencer. Before starting to execute a command, set the data required for execution, such as specifying an address, addresses, or data, in the corresponding registers.

Units for block erasure and for writing in rewriting of the code flash memory area
– Unit for blocks to be erased: 2 Kbytes
– Unit for writing: 1 word (4 bytes)

<Handling the commands>
The commands to be used are for writing to and for block erasure and blank checking of the code flash memory area.
• Enter the code flash programming mode. For the procedure for entry to the code flash programming mode, see 33.6.3.1 Procedure for executing the specific sequence and 33.6.3.2 Procedure for entry to the code flash programming mode.
• FLARS register = 00H (EXA bit = 0): Setting to select the user (not extra) area
• Set the specified data in the corresponding registers before executing the individual commands.

(1) Block erasure
FLAPH and FLAPL registers: Block start address in the code flash memory (example: 0x002000)
FLSEDH and FLSEDL registers: Block end address in the code flash memory (example: 0x0027FF)
(2) Writing: As writing proceeds in one-word (four-byte) units, set the address bits to a multiple of four; that is, set the two lower-order bits to 00B.
FLAPH and FLAPL registers: Start address in the target flash memory area (example: 0x002000)
FLSEDH and FLSEDL registers: Set all bits to 0 or do not set them (example: 0x000000).
FLWH and FLWL registers: One-word (four-byte) values to be written

Correct:

33.6.6.4 Operations for rewriting the code flash memory area

To rewrite the code flash memory area, execute commands for use with the code/data flash memory area sequencer. Before starting to execute a command, set the data required for execution, such as specifying an address, addresses, or data, in the corresponding registers. Allocate the processing software to rewrite the code flash memory area in the RAM and execute it from the RAM.

Units for block erasure and for writing in rewriting of the code flash memory area
– Unit for blocks to be erased: 2 Kbytes
– Unit for writing: 4 bytes

<Handling the commands>
<1> Enter the code flash programming mode. For the procedure for entry to the code flash programming mode, see 33.6.3.1 Procedure for executing the specific sequence and 33.6.3.2 Procedure for entry to the code flash programming mode.
<2> Set the EXA bit of the FLARS register to 0 (code/data flash memory areas).
<3> Before executing each command, set the address, data, write data, and command in the corresponding registers.

• Block erasure
Set the block start address Note 1 (example: 0x002000) of the code flash memory to be erased in the FLAPH and FLAPL registers.
Set the block end address Note 1 (example: 0x0027FF) of the code flash memory to be erased in the FLSEDH and FLSEDL registers.
• Writing
Set the start address Note 2 (example: 0x002000) of the flash memory to be written in the FLAPH and FLAPL registers.
Set 4-byte write data in the FLWH and FLWL registers.

(3) Blank checking: As blank checking proceeds in one-word (four-byte) units, set the address bits to a multiple of four; that is, set the two lower-order bits to 00B.
FLAPH and FLAPL registers: Start address in the target flash memory area (example: 0x002000)
FLSEDH and FLSEDL registers: End address in the target flash memory area (example: 0x0027FF)
* When blank checking is only to be applied to one word (four bytes), set the FLSEDH and FLSEDL registers to the same values as those in the FLAPH and FLAPL registers.

• After issuing a command for use with the code/data flash memory area sequencer, wait for the completion of its execution. For details on the procedure for waiting for the completion of command execution, see the section titled "Procedure for checking the completion of commands for use with the code/data flash memory area sequencer" in 33.6.6.9 Procedures for checking completion of the commands for use with the flash memory sequencer in the respective areas.
• Processing after executing a command
When command processing is to continue:
The same command with the target registers set to updated values or a rewrite command for any other area in the code flash memory can be executed with the state remaining in code flash programming mode.
When command processing has been completed:
Switch to the rewrite-disabled mode. For the procedure for switching to the rewrite-disabled mode, see 33.6.3.1
Procedure for executing the specific sequence and 33.6.3.4 Procedure for entry to the rewrite-disabled mode.

• Blank checking
Set the start address[Note 2] (example: 0x002000) of the flash memory to be blank-checked in the FLAPH and FLAPL registers.
Set the end address (example: 0x0027FF) of the flash memory to be blank-checked in the FLSEDH and FLSEDL registers.
When blank checking is only to be applied to one word (four bytes), set the FLSEDH and FLSEDL registers to the same values as those in the FLAPH and FLAPL registers.

<4> When the value of the command to be executed is set in the MDCH and SQMD2 to SQMD0 bits of the FSSQ register and the SQST bit is set to 1, the code/data flash memory area sequencer executes the specified command.
The MDCH, SQST, and SQMD2 to SQMD0 bits can be set simultaneously.
If these bits are set simultaneously, the FSSQ register is set to the following values.
• Block erasure: 84H
• Writing: 81H
• Blank checking of the code flash memory area: 83H

<5> Wait until the command for use with the code/data flash memory area sequencer is complete. For details on the procedure for waiting for the completion of command execution, see the section titled "Procedure for checking the completion of commands for use with the code/data flash memory area sequencer" in 33.6.6.9 Procedures for checking completion of the commands for use with the flash memory sequencer in the respective areas.

<6> Processing after executing a command
<Continuing command processing>
The same command or another command can be executed by continuously updating the address, data, and write data (in step 3) with the state remaining in code flash programming mode.
<Completing command processing>
Switch to the non-programmable mode. For the procedure for switching to the non-programmable mode, see 33.6.3.1 Procedure for executing the specific sequence and 33.6.3.4 Procedure for entry to the nonprogrammable mode.

Note 1. The code flash memory area blocks can be erased in units of 2 Kbytes. Specify the erase addresses (start address and end address) so that all blocks to be erased are included. For the relationship between addresses and block numbers, see Table 3 - 1 Correspondence between Addresses and Block Numbers in Flash Memory (1/3).

Note 2. The code flash memory area can be written and blank-checked in units of 4 bytes. Therefore, set the two lower-order bits of the FLAPL register for specifying the address to 00B (an integer of 4).

75. 33.6.6.5 Operations for rewriting the data flash memory area (Page 1327)

Incorrect:

33.6.6.5 Operations for rewriting the data flash memory area

To rewrite the data flash memory area, enter the data flash programming mode and then execute commands for use with the code/data flash memory area sequencer. Before starting to execute a command, set the data required for execution, such as specifying an address, addresses, or data, in the corresponding registers.

Units for block erasure and for writing in rewriting of the data flash memory area
– Unit for blocks to be erased: 256 bytes
– Unit for writing: 1 byte

<Handling the commands>
The commands to be used are for writing to and for block erasure and blank checking of the data flash memory area.
• Enter the data flash programming mode. For the procedure for entry to the data flash programming mode, see 33.6.3.1
Procedure for executing the specific sequence and 33.6.3.3 Procedure for entry to the data flash programming mode.
• FLARS register = 00H (EXA bit = 0): Setting to select the user (not extra) area
• Set the specified data in the corresponding registers before executing the individual commands.

(1) Block erasure
FLAPH and FLAPL registers: Block start address in the data flash memory (example: 0x0F1100)
FLSEDH and FLSEDL registers: Block end address in the data flash memory (example: 0x0F11FF)
(2) Writing: 1 byte
FLAPH and FLAPL registers: Start address in the target flash memory area (example: 0x0F1101)
FLSEDH and FLSEDL registers: Set all bits to 0 or do not set them (example: 0x000000).
FLWH and FLWL registers: Set a value to be written in the range from 0x00000000 to 0x000000FF, since only the FLW7 to FLW0 bits are valid.

Correct:

33.6.6.5 Operations for rewriting the data flash memory area

To rewrite the data flash memory area, execute commands for use with the code/data flash memory area sequencer. Before starting to execute a command, set the data required for execution, such as specifying an address, addresses, or data, in the corresponding registers.

Units for block erasure and for writing in rewriting of the data flash memory area
– Unit for blocks to be erased: 256 bytes
– Unit for writing: 1 byte

<Handling the commands>
<1> Enter the data flash programming mode. For the procedure for entry to the data flash programming mode, see 33.6.3.1 Procedure for executing the specific sequence and 33.6.3.3 Procedure for entry to the data flash programming mode.
<2> Set the EXA bit of the FLARS register to 0 (code/data flash memory areas).
<3> Before executing each command, set the address, data, write data, and command in the corresponding registers.
• Block erasure
Set the block start address**Note** (example: 0x0F1100) of the data flash memory to be erased in the FLAPH and FLAPL registers.
Set the block end address**Note** (example: 0x0F11FF) of the data flash memory to be erased in the FLSEDH and FLSEDL registers.
• Writing
Set the start address (example: 0x0F1101) of the flash memory to be written in the FLAPH and FLAPL registers.
Set the write data in the 8 lower-order bits of the FLWL register.
• Blank checking:
Set the start address (example: 0x0F1100) of the flash memory to be blank-checked in the FLAPH and FLAPL registers.
Set the end address (example: 0x0F11FF) of the flash memory to be blank-checked in the FLSEDH and FLSEDL registers.
When blank checking is only to be applied to one byte, set the FLSEDH and FLSEDL registers to the same values as those in the FLAPH and FLAPL registers.

(3) Blank checking:

FLAPH and FLAPL registers: Start address in the target flash memory area (example: 0x0F1100)

FLSEDH and FLSEDL registers: End address in the target flash memory area (example: 0x0F11FF)

* When blank checking is only to be applied to one byte, set the FLSEDH and FLSEDL registers to the same

values as those in the FLAPH and FLAPL registers.

• After issuing a command for use with the code/data flash memory area sequencer, wait for the completion of its execution. For details on the procedure for waiting for the completion of command execution, see the section titled "Procedure for checking the completion of commands for use with the code/data flash memory area sequencer" in 33.6.6.9 Procedures for checking completion of the commands for use with the flash memory sequencer in the respective areas.

• Processing after executing a command

When command processing is to continue:

The same command with the target registers set to updated values or a rewrite command for any other area in the data flash memory can be executed with the state remaining in data flash programming mode.

When command processing has been completed:

Switch to the rewrite-disabled mode. For the procedure for switching to the rewrite-disabled mode, see 33.6.3.1

Procedure for executing the specific sequence and 33.6.3.4 Procedure for entry to the rewrite-disabled mode.

<4> When the value of the command to be executed is set in the MDCH and SQMD2 to SQMD0 bits of the FSSQ register and the SQST bit is set to 1, the code/data flash memory area sequencer executes the specified command. The MDCH, SQST, and SQMD2 to SQMD0 bits can be set simultaneously. If these bits are set simultaneously, the FSSQ register is set to the following values.

• Block erasure: 84H

• Writing: 81H

• Blank checking of the data flash memory area: 8BH

<5> Wait until the command for use with the code/data flash memory area sequencer is complete. For details on the procedure for waiting for the completion of command execution, see the section titled "Procedure for checking the completion of commands for use with the code/data flash memory area sequencer" in 33.6.6.9 Procedures for checking completion of the commands for use with the flash memory sequencer in the respective areas.

<6> Processing after executing a command

<Continuing command processing>

The same command or another command can be executed by continuously updating the address, data, and write

data (in step 3) with the state remaining in data flash programming mode.

<Completing command processing>

Switch to the non-programmable mode. For the procedure for switching to the non-programmable mode, see 33.6.3.1 Procedure for executing the specific sequence and 33.6.3.4 Procedure for entry to the nonprogrammable mode.

Note The data flash memory area blocks can be erased in units of 256 bytes. Therefore, set the 8 lower-order bits of the FLAPL register for specifying the start address to 0000 0000B (an integer of 256). Also set the 8 lower-order bits of the FLSEDL register for specifying the end address to 1111 1111B.

76. 33.6.6.7 Operations for rewriting the extra area (Page 1328)

Incorrect:

33.6.6.7 Operations for rewriting the extra area

To rewrite the extra area, enter the code flash programming mode and then execute commands for use with the extra area sequencer. Before starting to execute a command, set the data required for execution in the corresponding registers.

Unit for writing in rewriting of the extra area
– Unit for writing: 1 word (4 bytes)
* No erasure command is available, so a unit is not specified.

<Handling the commands>
The target commands are for writing data to the extra area.
• Enter the code flash programming mode. For the procedure for entry to the code flash programming mode, see 33.6.3.1 Procedure for executing the specific sequence and 33.6.3.2 Procedure for entry to the code flash programming mode.
• FLARS register = 01H (EXA bit = 1): Setting to select the extra (not user) area
• Before executing a command, set a one-word (four-byte) value in the FLWH and FLWL registers. Specifically, set the value to be written to the target extra area data EX bits 31 to 0 in the FLW[31:0] bits of the FLWH and FLWL registers.
• Specifying a command determines the area to which data are to be written. Enter the target command number in the ESQMD[3:0] bits of the FSSE register and also set the ESQST bit of the same register to 1.

(1) For programming of the FSW-related data: 81H
(2) For programming of the read-prohibited area of software from a third party and the protection flag: 86H
(3) For programming of the security flags and boot area switching flag: 87H

• After issuing a command for use with the extra area sequencer, wait for the completion of its execution. For details on the procedure for waiting for the completion of command execution, see the section titled "Procedure for checking the completion of commands for use with the extra area sequencer" in 33.6.6.9 Procedures for checking completion of the commands for use with the flash memory sequencer in the respective areas.

Correct:

33.6.6.7 Operations for rewriting the extra area

To rewrite the extra area, enter the code flash programming mode and then execute commands for use with the extra area sequencer. Before starting to execute a command, set the data required for executing each command in the corresponding registers.

<Handling the commands>
<1> Enter the code flash programming mode. For the procedure for entry to the code flash programming mode, see 33.6.3.1 Procedure for executing the specific sequence and 33.6.3.2 Procedure for entry to the code flash programming mode.
<2> Set the EXA bit of the FLARS register to 1 (extra area).
<3> Before executing a command, set 4-byte data in the FLWH and FLWL registers. Each bit of the FLW31 to FLW0 bits corre-sponds to EX bits 31 to 0 of the target extra area data. For details of setting data for each command, see 33.6.6.8 Data to be set for the commands for use with the extra area sequencer.
<4> When the value of the command to be executed is set in the ESQMD3 to ESQMD0 bits of the FSSE register and the ESQST bit is set to 1, the extra area sequencer executes the specified command. The ESQMD3 to ESQMD0 bits and the ESQST bit can be set simultaneously. If these bits are set simultaneously, the FSSE register is set to the following values.
• Write data to the flash shield window setting area: 81H
• Write data to the flash read protection setting area: 86H
• Write data to the security flag and boot swap function setting area: 87H
<5> Wait until the command for use with the extra area sequencer is complete. For details on the procedure for waiting for the completion of command execution, see the section titled "Procedure for checking the completion of commands for use with the extra area sequencer" in 33.6.6.9 Procedures for checking completion of the commands for use with the flash memory sequencer in the respective areas.

• Processing after executing a command

When command processing is to continue:

The same command with the target registers set to updated values or a rewrite command for any other area in the extra area can be executed with the state remaining in code flash programming mode.

When command processing has been completed:

Switch to the rewrite-disabled mode. For the procedure for switching to the rewrite-disabled mode, see 33.6.3.1

Procedure for executing the specific sequence and 33.6.3.4 Procedure for entry to the rewrite-disabled mode.

<6> Processing after executing a command

<Continuing command processing>

The same command or another command can be executed by continuously updating the FLWH and FLWL register data to be set in the extra area (in step 3) with the state remaining in code flash programming mode.

<Completing command processing>

Switch to the non-programmable mode. For the procedure for switching to the non-programmable mode, see 33.6.3.1 Procedure for executing the specific sequence and 33.6.3.4 Procedure for entry to the nonprogrammable mode.

77. 33.6.6.8 Data to be set for the commands for use with the extra area sequencer (Page 1329 to Page 1331)

Incorrect:

33.6.6.8 Data to be set for the commands for use with the extra area sequencer

Writing to the extra area proceeds per word (four bytes), including values that are not to be changed.

Before executing a command, set the value to be set in the extra area data EX bits 31 to 0 for each target command to be executed in the FLW[31:0] bits of the FLWH and FLWL registers.

(1) Programming of the FSW-related data

Set the value to be set in the extra area data EX bits 31 to 0 shown below in the FLW31 to FLW0 bits of the FLWH and FLWL registers.

EX bit 31	EX bit 30	EX bit 29	EX bit 28	EX bit 27	EX bit 26	EX bit 25	EX bit 24
FSWC	0	0	0	0	0	0	FSWE8

EX bit 23	EX bit 22	EX bit 21	EX bit 20	EX bit 19	EX bit 18	EX bit 17	EX bit 16
FSWE7	FSWE6	FSWE5	FSWE4	FSWE3	FSWE2	FSWE1	FSWE0

EX bit 15	EX bit 14	EX bit 13	EX bit 12	EX bit 11	EX bit 10	EX bit 9	EX bit 8
FSPR	0	0	0	0	0	0	FSWS8

EX bit 7	EX bit 6	EX bit 5	EX bit 4	EX bit 3	EX bit 2	EX bit 1	EX bit 0
FSWS7	FSWS6	FSWS5	FSWS4	FSWS3	FSWS2	FSWS1	FSWS0

– The value to be set in the FSWE8 to FSWE0 bits (bits 24 to 16) is the end block number (end block number in the window range + 1).

– The value to be set in the FSWC bit (bit 31) is for FSW mode control.
FSWC = 0/1 (at shipment): Respectively select shielding of the area inside the window range or outside the window range

– The value to be set in FSWS8 to FSWS0 bits (bits 8 to 0) is the start block number (start block number in the window range).

– The value to be set in the FSPR bit (bit 15) is for making the FSW setting to prohibit rewriting.
FSPR = 0/1 (at shipment): FSW is set to prohibit rewriting/FSW is set to enable rewriting.

Correct:

33.6.6.8 Data to be set for the commands for use with the extra area sequencer

Writing to the extra area proceeds per 4 bytes.

Each command for use with the extra area sequencer writes the data set in the FLW31 to FLW0 bits of the FLWH and FSWL registers to EX bits 31 to 0 in the extra area corresponding to the given command.

(1) Write to the flash shield window setting area

Set the data in the FLWH and FLWL registers to the flash shield window setting area.

EX bit 31	EX bit 30	EX bit 29	EX bit 28	EX bit 27	EX bit 26	EX bit 25	EX bit 24
FSWC	1	1	1	1	1	1	FSWE8

EX bit 23	EX bit 22	EX bit 21	EX bit 20	EX bit 19	EX bit 18	EX bit 17	EX bit 16
FSWE7	FSWE6	FSWE5	FSWE4	FSWE3	FSWE2	FSWE1	FSWE0

EX bit 15	EX bit 14	EX bit 13	EX bit 12	EX bit 11	EX bit 10	EX bit 9	EX bit 8
FSPR	1	1	1	1	1	1	FSWS8

EX bit 7	EX bit 6	EX bit 5	EX bit 4	EX bit 3	EX bit 2	EX bit 1	EX bit 0
FSWS7	FSWS6	FSWS5	FSWS4	FSWS3	FSWS2	FSWS1	FSWS0

Bit Name	Setting
FSWC	Specifies the range of the flash memory shield area. 0 : Flash memory shield area: Inside the window range 1 : Flash memory shield area: Outside the window range (default)
FSPR	Specifies whether to enable or disable changing of the flash shield window setting area. 0 : Changing of the flash shield window setting area is disabled. 1 : Changing of the flash shield window setting area is enabled (default).
FSWE8 - FSWE0	Flash shield window end block setting area Specify the block number (end block number + 1).Note
FSWS8 - FSWS0	Flash shield window start block setting area Specify the start block number.Note

Note For the relationship between addresses and block numbers, see Table 3 - 1 Correspondence between Addresses and Block Numbers in Flash Memory (1/3).

Caution The value of the FSPR bit can be changed from 0 (disabling) to 1 (enabling) by executing the chip erase command of the dedicated flash memory programmer or the Security Release command for use in serial programming mode with the entire flash memory erased.
Note that if either of the disabling settings listed below is made, executing the chip erase command of the dedicated flash memory programmer or the Security Release command for use in serial programming mode is not possible.
- SEPR = 0 (block erasure is disabled)
- BTPR = 0 (rewriting of the boot area is disabled)

Moreover, setting the FSPR bit to 1 (enabling) is not possible because a command cannot be transmitted when connection in serial programming mode is not available due to the setting for disabling connection to the programmer and on-chip debugger or for enabling programmer connection ID authentication having been made.

(2) Programming of the read-prohibited area of software from a third party and the protection flag

Set the value to be set in the extra area data EX bits 31 to 0 shown below in the FLW31 to FLW0 bits of the FLWH and FLWL registers.

EX bit 31	EX bit 30	EX bit 29	EX bit 28	EX bit 27	EX bit 26	EX bit 25	EX bit 24
SWPR	—	—	—	—	—	—	UPAddr8

EX bit 23	EX bit 22	EX bit 21	EX bit 20	EX bit 19	EX bit 18	EX bit 17	EX bit 16
UPAddr7	UPAddr6	UPAddr5	UPAddr4	UPAddr3	UPAddr2	UPAddr1	UPAddr0

EX bit 15	EX bit 14	EX bit 13	EX bit 12	EX bit 11	EX bit 10	EX bit 9	EX bit 8
—	—	—	—	—	—	—	LOWAddr8

EX bit 7	EX bit 6	EX bit 5	EX bit 4	EX bit 3	EX bit 2	EX bit 1	EX bit 0
LOWAddr7	LOWAddr6	LOWAddr5	LOWAddr4	LOWAddr3	LOWAddr2	LOWAddr1	LOWAddr0

– The value to be set in the UPAddr8 to UPAddr0 (bits 24 to 16) is the number of the end block in the read-prohibited area of software from a third party.

– The value to be set in the LOWAddr8 to LOWAddr0 (bits 8 to 0) is the number of the start block in the read-prohibited area of software from a third party.

– The value to be set in the SWPR bit (bit 31) controls the prohibition of rewriting in the read-prohibited area of software from a third party.

SWPR = 0/1 (at shipment): Rewriting in the read-prohibited area is prohibited/rewriting in the read-prohibited area is enabled.

(2) Write to the flash read protection setting area

Set the data in the FLWH and FLWL registers to the flash read protection setting area.

EX bit 31	EX bit 30	EX bit 29	EX bit 28	EX bit 27	EX bit 26	EX bit 25	EX bit 24
SWPR	1	1	1	1	1	1	UPAddr8

EX bit 23	EX bit 22	EX bit 21	EX bit 20	EX bit 19	EX bit 18	EX bit 17	EX bit 16
UPAddr7	UPAddr6	UPAddr5	UPAddr4	UPAddr3	UPAddr2	UPAddr1	UPAddr0

EX bit 15	EX bit 14	EX bit 13	EX bit 12	EX bit 11	EX bit 10	EX bit 9	EX bit 8
1	1	1	1	1	1	1	LOWAddr8

EX bit 7	EX bit 6	EX bit 5	EX bit 4	EX bit 3	EX bit 2	EX bit 1	EX bit 0
LOWAddr7	LOWAddr6	LOWAddr5	LOWAddr4	LOWAddr3	LOWAddr2	LOWAddr1	LOWAddr0

Bit Name	Setting
SWPR	Specifies whether to enable or disable changing of the flash read protection setting area. 0: Changing of the flash read protection setting area is disabled. 1: Changing of the flash read protection setting area is enabled (default).
UPAddr8 to UPAddr0	Flash read protection end block setting area Specify the end block number.Note
LOWAddr8 to LOWAddr0	Flash read protection start block setting area Specify the start block number.Note

Note For the relationship between addresses and block numbers, see Table 3 - 1 Correspondence between Addresses and Block Numbers in Flash Memory (1/3). The flash read protection setting area cannot be read after a reset is released.

Caution The value of the SWPR bit can be changed from 0 (disabling) to 1 (enabling) by executing the chip erase command of the dedicated flash memory programmer or the Security Release command for use in serial programming mode with the entire flash memory erased.
Note that if either of the disabling settings listed below is made, executing the chip erase command of the dedicated flash memory programmer or the Security Release command for use in serial programming mode is not possible.
- SEPR = 0 (block erasure is disabled)
- BTPR = 0 (rewriting of the boot area is disabled)

Moreover, setting the SWPR bit to 1 (enabling) is not possible because a command cannot be transmitted when connection in serial programming mode is not available due to the setting for disabling connection to the programmer and on-chip debugger or for enabling programmer connection ID authentication having been made.

(3) Programming of the security flags and boot area switching flag

Set the value to be set in the extra area data EX bits 31 to 0 shown below in the FLW31 to FLW0 bits of the FLWH and FLWL registers.

EX bit 31	EX bit 30	EX bit 29	EX bit 28	EX bit 27	EX bit 26	EX bit 25	EX bit 24
1	1	1	1	1	1	1	1

EX bit 23	EX bit 22	EX bit 21	EX bit 20	EX bit 19	EX bit 18	EX bit 17	EX bit 16
1	1	1	1	1	1	1	1

EX bit 15	EX bit 14	EX bit 13	EX bit 12	EX bit 11	EX bit 10	EX bit 9	EX bit 8
1	1	1	WRPR	1	SEPR	BTPR	BTFLG

EX bit 7	EX bit 6	EX bit 5	EX bit 4	EX bit 3	EX bit 2	EX bit 1	EX bit 0
1	1	1	1	1	1	1	1

– The value to be set in the WRPR bit (bit 12) controls the prohibition of writing in serial programming mode.
WRPR = 0/1 (at shipment): Writing in serial programming mode is prohibited/writing in serial programming mode is enabled.

– The value to be set in the SEPR bit (bit 10) controls the prohibition of block erasure in serial programming mode.
SEPR = 0/1 (at shipment): Block erasure in serial programming mode is prohibited/block erasure in serial programming mode is enabled.

– The value to be set in the BTPR bit (bit 9) controls the prohibition of rewriting in the boot area through serial programming and self-programming.
BTPR = 0/1 (at shipment): Rewriting in the boot area is prohibited/rewriting in the boot area is enabled.

– The value to be set in the BTFLG bit (bit 8) is for control of the boot cluster to be set as the boot area when TMSPMD = 0; that is, boot swapping follows the information in the extra area (the BTFLG setting).
BTFLG = 0/1 (at shipment): The boot area is boot cluster 1/the boot area is boot cluster 0.

(3) Write to the security flag and boot swap function setting area

Set the data in the FLWH and FLWL registers to the security flag and boot swap function setting area. For details of the security settings, see 33.9 Security Settings.

EX bit 31	EX bit 30	EX bit 29	EX bit 28	EX bit 27	EX bit 26	EX bit 25	EX bit 24
1	1	1	1	1	1	1	1

EX bit 23	EX bit 22	EX bit 21	EX bit 20	EX bit 19	EX bit 18	EX bit 17	EX bit 16
1	1	1	1	1	1	1	1

EX bit 15	EX bit 14	EX bit 13	EX bit 12	EX bit 11	EX bit 10	EX bit 9	EX bit 8
1	1	1	WRPR	1	SEPR	BTPR	BTFLG

EX bit 7	EX bit 6	EX bit 5	EX bit 4	EX bit 3	EX bit 2	EX bit 1	EX bit 0
1	1	1	1	1	IFPR	1	IDEN

Bit Name	Setting
WRPR	Specifies whether to enable or disable writing in serial programming mode. 0: Writing in serial programming mode is disabled. 1: Writing in serial programming mode is enabled (default).
SEPR	Specifies whether to enable or disable block erasure in serial programming mode. 0: Block erasure in serial programming mode is disabled. 1: Block erasure in serial programming mode is enabled (default).
BTPR	Specifies whether to enable or disable rewriting of the boot area and boot swapping. 0: Rewriting of the boot area and boot swapping are disabled. 1: Rewriting of the boot area and boot swapping are enabled (default).
BTFLG	Specifies the boot area when the TMSPMD bit in the FSSET register is 0. 0: Boot area: Boot cluster 1 1: Boot area: Boot cluster 0 (default)
IFPR	Specifies whether to enable or disable serial programming mode and connection to the programmer and on-chip debugger. 0: Serial programming mode and connection to the on-chip debugger are disabled. 1: Serial programming mode and connection to the on-chip debugger are enabled (default).
IDEN	Specifies whether to enable or disable programmer connection ID authentication to be made in serial programming mode. 0: ID authentication for connection in serial programming mode is enabled. 1: ID authentication for connection in serial programming mode is disabled (default).

Caution 1. When changing the value of the BTFLG bit, set all other bits to 1.
Caution 2. When changing the values of security flags other than BTFLG to 0 (prohibition), read the register first and set the BTFLG bit to the same value as was read, and set the other bits to 1.
Caution 3. When setting the WRPR bit to 0 (prohibition), the WRPR bit can only be set to 1 (enabling) by executing the chip erase command in serial programming mode.
Note that if either of the prohibition settings listed below is made, executing the chip erase command in serial programming mode is not possible.
• SEPR = 0 (Block erasure is prohibited.)
• BTPR = 0 (Rewriting of the boot area is prohibited.)

Caution 1. When changing the value of the BTFLG bit, set all other bits to 1.
Caution 2. When changing the values of security flags other than BTFLG to 0 (disabling), read the register first and set the BTFLG bit to the same value as was read, and set the other bits to 1.
Caution 3. The value of the WRPR bit can be changed from 0 (disabling) to 1 (enabling) by executing the chip erase command of the dedicated flash memory programmer or the Security Release command for use in serial programming mode with the entire flash memory erased.
Note that if either of the disabling settings listed below is made, executing the chip erase command of the dedicated flash memory programmer or the Security Release command for use in serial programming mode is not possible.
- SEPR = 0 (block erasure is disabled)
- BTPR = 0 (rewriting of the boot area is disabled)
Moreover, setting the WRPR bit to 1 (enabling) is not possible because a command cannot be transmitted when connection in serial programming mode is not available due to the setting for disabling connection to the programmer and on-chip debugger or for enabling programmer connection ID authentication having been made.
Caution 4. Restoring the value of any among the SEPR, BTPR, IFPR, and IDEN bits to 1 after having set it to 0 is not possible.

78. 33.6.8 Flash shield window function (Page 1335)

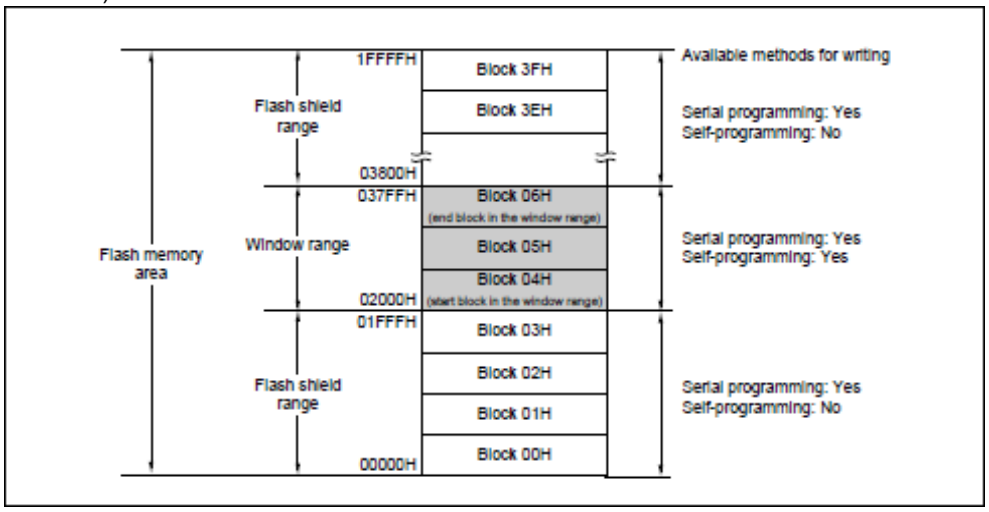
Incorrect:

33.6.8 Flash shield window function

The flash shield window function is provided as one of the security functions for use with self-programming. It disables writing to and erasing of areas selected as being either inside or outside the range specified as the window. This function is only effective for self-programming. The window range can be set by specifying the start and end blocks. The window range can be set or changed during both serial programming and self-programming.

Writing to and erasing of areas selected as being either inside or outside the range specified as the window are disabled during self-programming. During serial programming, however, areas selected as being both inside and outside the range specified as the window can be written and erased.

Figure 33 - 29 Flash Shield Window Setting Example (Target Devices: R7F100GLG, Start Block Number in the Window Range: 04H, End Block Number in the Window Range: 06H, FSWC: 1)



Caution 1. If the rewrite-prohibited area of the boot cluster 0 overlaps with the flash shield window range, prohibition to rewrite the boot cluster 0 takes priority.

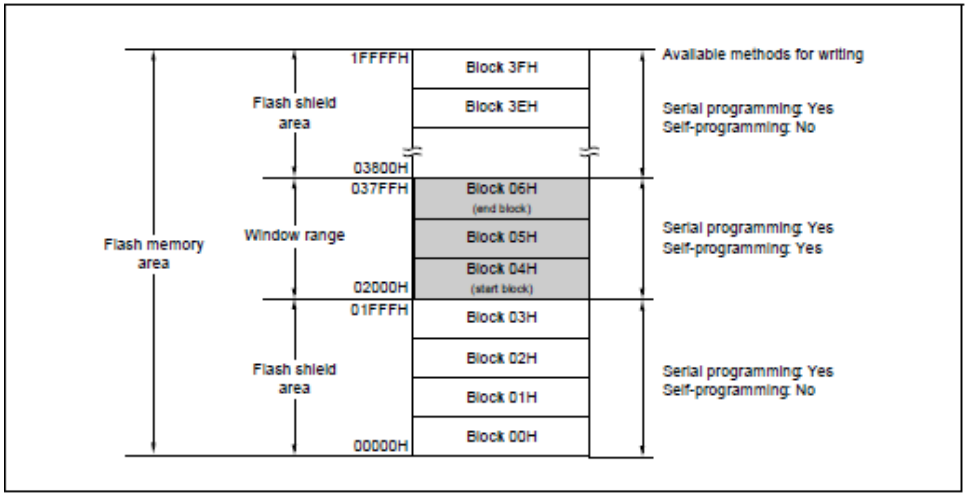
Caution 2. The flash shield window can only be used for the code flash memory (and is not supported for the data flash memory).

Correct:

33.8 Flash Shield Window Function

The flash shield window function is provided as a security function which disables writing to and erasing of the selected flash memory shield area. This function is only effective for self-programming. The flash memory shield area is selectable as either the area inside or areas outside the range specified as the window. The window range is set by specifying the blocks where it starts and ends. The flash memory shield area can be set or changed during both serial programming and self-programming. Writing to and erasing of the flash memory shield area are disabled during self-programming. During serial programming, however, the flash memory shield area can also be written and erased.

Figure 33 - 32 Flash Shield Window Setting Example (Target Devices: R7F100GLG, Start Block Number: 04H, End Block Number: 06H, FSWC: 1)



Caution 1. If the non-programmable area of the boot area overlaps with the flash shield window range, disabling of rewriting the boot area takes priority.

Caution 2. The flash shield window can only be used for the code flash memory (and is not supported for the data flash memory).

Table 33 - 13 Relationship between Flash Shield Window Function Setting/Change Methods and Commands

Programming Condition	Window Range Setting/Change Method	Command to be Executed	
		Block erase	Write
Self-programming	Specify the start block number (the start block number in the window range) and the end block number (the end block number in the window range + 1) by the flash self-programming code.	Block erasure is only possible either inside or outside the window range.	Writing is only possible either inside or outside the window range.
Serial programming	Specify the start block number (the start block number in the window range) and the end block number (the end block number in the window range) on GUI of dedicated flash memory programmer, etc.	Block erasure is possible both inside and outside the window range.	Writing is possible both inside and outside the window range.

Remark See 33.7 Security Settings to prohibit writing/erasure during serial programming.

Table 33 - 12 Relationship between Flash Shield Window Function Setting/Change Methods and Commands

Programming Condition	Window Range Setting/Change Method	Command to be Executed	
		Block erase	Write
Self-programming	Specify the window start block number and the (end block number + 1) block number (following the end block) in the flash shield window setting area using the self-programming.	Block erasure is not possible inside the flash memory shield area.	Writing is not possible inside the flash memory shield area.
Serial programming	Specify the start block number in the window range and the end block number in the window range on GUI of dedicated flash memory programmer, etc.	Block erasure is also possible inside the flash memory shield area.	Writing is also possible inside the flash memory shield area.

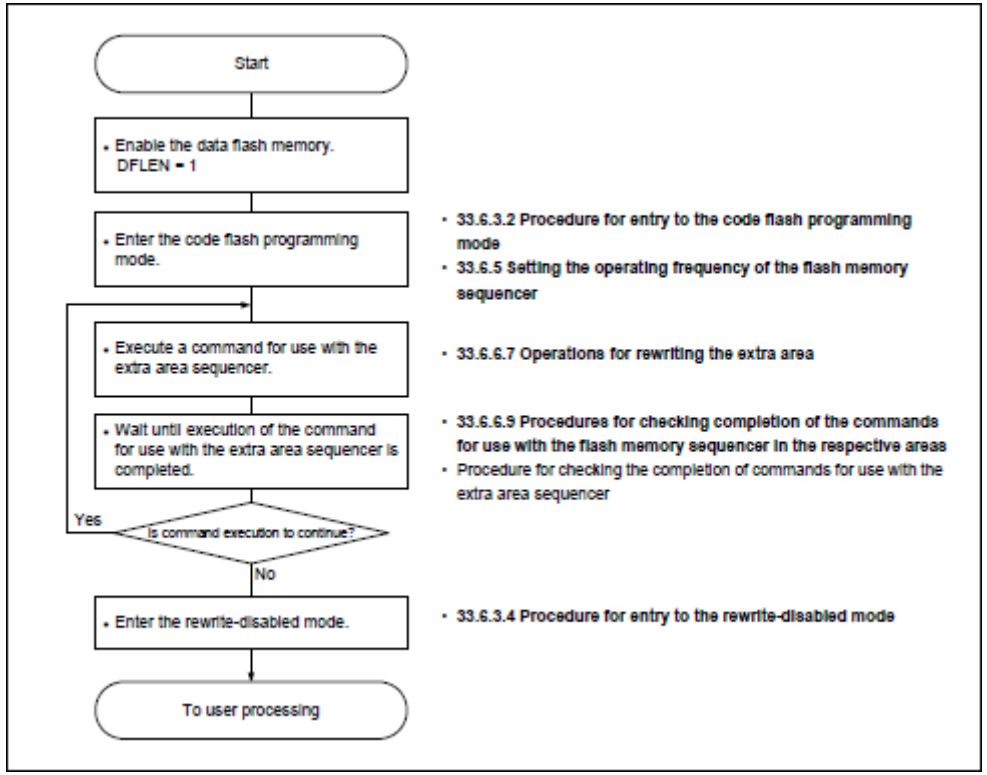
79. 33.6.10.3 Example of executing the commands to rewrite the extra area (Page 1340)

Incorrect:

33.6.10.3 Example of executing the commands to rewrite the extra area

Figure 33 - 32 shows the flow of executing the commands to rewrite the extra area.

Figure 33 - 32 Flow of Executing the Commands to Rewrite the Extra Area

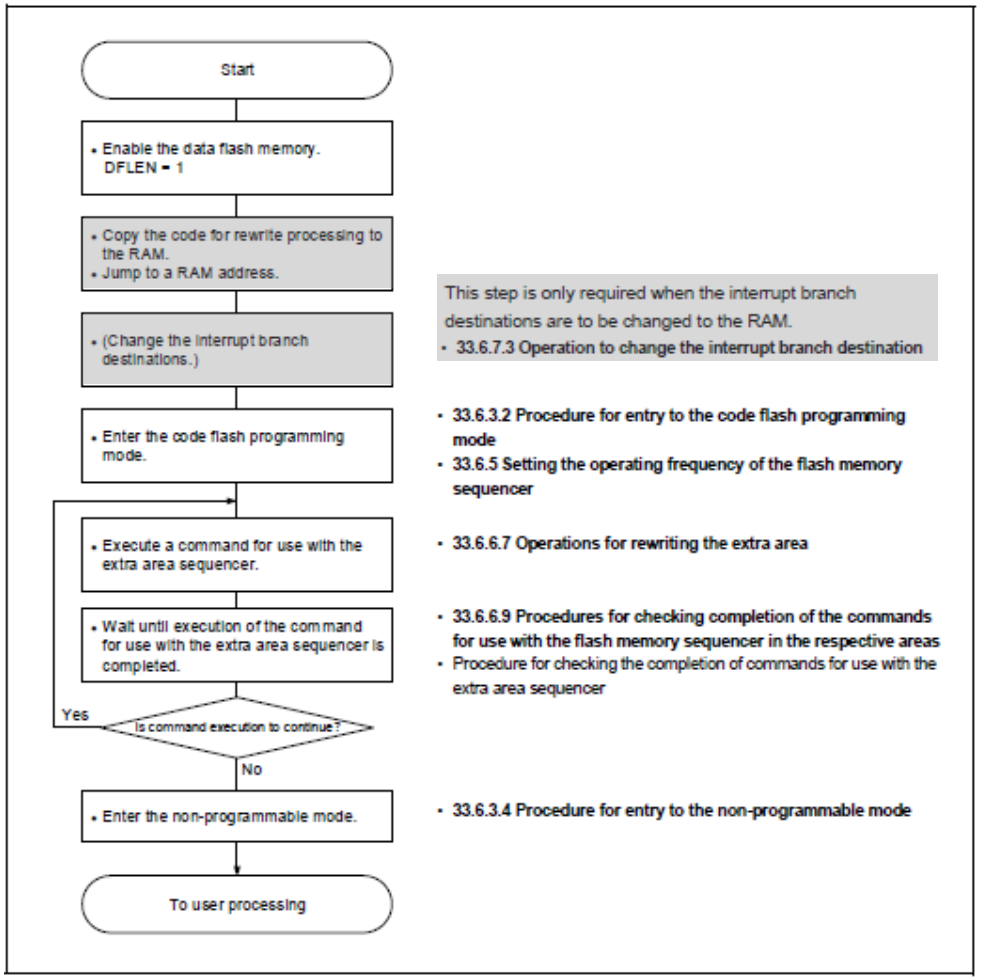


Correct:

33.6.8.3 Example of executing the commands to rewrite the extra area

Figure 33 - 29 shows the flow of executing the commands to rewrite the extra area.

Figure 33 - 29 Flow of Executing the Commands to Rewrite the Extra Area



80. 33.6.11 Notes on self-programming (Page 1341)

Incorrect:

33.6.11 Notes on self-programming

(1) Rewriting the code flash memory or extra area

To rewrite the code flash memory or extra area, place the code or values in the RAM.

(2) Precondition for manipulating the data flash memory area

Before manipulating the data flash memory area, set the DFLEN bit of the data flash control register (DFLCTL) to 1 (enabling access to the data flash memory).

(3) Execution of programs during rewriting of the flash memory

The flash memory sequencer is used to control rewriting of the flash memory during self-programming. In the flash memory control modes where rewriting of the flash memory is enabled, reference to the flash memory to be manipulated is not possible.

- In code flash programming mode, reference to the code flash memory is not possible. Accordingly, in code flash programming mode, copy the user program that is to be executed from the ROM (code flash memory) and its data for reference to the RAM in advance so that the program can be executed and reference to the data in the RAM is possible.
- In data flash programming mode, reference to the data flash memory is not possible. Accordingly, in data flash programming mode, copy data that are for reference to the RAM in advance so that reference to the data in the RAM is possible.

Correct:

33.6.9 Notes on self-programming

(1) Rewriting the code flash memory or extra area

To rewrite the code flash memory or extra area, place the code or values in the RAM.

(2) Precondition for manipulating the data flash memory area and extra area

Before manipulating the data flash memory area and extra area, set the DFLEN bit of the data flash control register (DFLCTL) to 1 (enabling access to the data flash memory).

(3) Execution of programs during rewriting of the flash memory

The flash memory sequencer is used to control rewriting of the flash memory during self-programming.

In the flash memory control modes where rewriting of the flash memory is enabled, reference to the flash memory to be manipulated is not possible.

- In code flash programming mode, reference to the code flash memory is not possible. Accordingly, in code flash programming mode, copy the user program that is to be executed from the ROM (code flash memory) and its data for reference to the RAM in advance so that the program can be executed and reference to the data in the RAM is possible.
- In data flash programming mode, reference to the data flash memory is not possible. Accordingly, in data flash programming mode, copy data that are for reference to the RAM in advance so that reference to the data in the RAM is possible.

(4) Specifying the range of unavailable area

Specify the range of blank checking and block erasure within the range of code flash memory area or data flash memory area. Do not specify any unavailable area or both the code flash memory area and data flash memory area including an unavailable area.

(5) Specifying the range of code flash memory area

For products that have a code flash memory area larger than 512 Kbytes, specifying a range that spans addresses or blocks across the 512-Kbyte boundary for blank checking or block erasure is not possible. Specify an address range of 000000H to 7FFFFFH or 800000H to BFFFFFH for blank checking. Specify a block range of 000H to 099H or 100H to 17FH for block erasure.

81. 33.7 Security Settings (Page 1342, Page 1343)

Incorrect:

33.7 Security Settings

The RL78 microcontroller supports a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person.

The operations shown below can be performed using the security set command.

• Disabling block erasure

Execution of the block erase command for a specific block in the code flash memory is prohibited during serial programming. However, blocks can be erased by means of self-programming.

• Disabling writing

Execution of the write command for entire blocks in the code flash memory is prohibited during serial programming.

However, blocks can be written by means of self-programming.

After the setting to prohibit writing has been made, releasing the setting by the security release command is enabled by a reset.

• Disabling rewriting boot cluster 0

Execution of the block erase command and write command on boot cluster 0 (00000H to 00FFFH) in the code flash memory is prohibited by this setting.

The block erase, write commands, and rewriting boot cluster 0 are enabled by the default setting when the flash memory is shipped. Security can be set by serial programming and self-programming. Each security setting can be used in combination.

Table 33 - 14 shows the relationship between the erase and write commands when the RL78 microcontroller security function is enabled.

Caution The security function of the dedicated flash programmer does not support self-programming.

Remark To prohibit writing and erasure during self-programming, use the flash shield window function (see 33.6.8 Flash shield window function for detail).

Correct:

33.9 Security Settings

The RL78 microcontroller supports a security function that prohibits rewriting the user program written to the internal flash memory, so that the program cannot be changed by an unauthorized person.

The operations shown below can be performed by serial programming or self-programming.

• Disabling block erasure

Execution of the block erase command for a specific block in the code flash memory is prohibited during serial programming. However, blocks can be erased by means of self-programming.

• Disabling writing

Execution of the write command for entire blocks in the code flash memory is prohibited during serial programming.

However, blocks can be written by means of self-programming.

After the setting to prohibit writing has been made, releasing the setting by the Security Release command is enabled by a reset.

• Disabling rewriting the boot area

Execution of the block erase command and write command on the boot area (00000H to 00FFFH) in the code flash memory is prohibited.

• Disabling connection to the programmer and on-chip debugger

Connection to a dedicated flash memory programmer and on-chip debugger is prohibited. A dedicated flash memory programmer and on-chip debugger cannot be used to manipulate the flash memory.

• Enabling programmer connection ID authentication

Authentication for an arbitrary 10-byte ID code is enabled when connecting to a dedicated flash memory programmer. The 10-byte ID area is 000C4H to 000CDH**Note**. If the ID does not match when using serial programming, the dedicated flash memory programmer cannot be used to manipulate the flash memory.

Block erasure, writing, and rewriting the boot area are enabled by the default setting when the flash memory is shipped.
Security can be set by serial programming and self-programming. Each security setting can be used in combination.
Table 33 - 13 shows the relationship between the erase and write commands when the RL78 microcontroller security function is enabled.

Note The 10-byte ID code area for the programmer connection ID is shared with the security ID code for on-chip debugging.

Caution The security function of the dedicated flash programmer does not support self-programming.

Remark To prohibit writing and erasure during self-programming, use the flash shield window function (see 33.8
Flash Shield Window Function for detail).

Table 33 - 14 Relationship between Enabling the Security Function and Commands

(1) During serial programming

Valid Security	Command to be Executed	
	Block Erase	Write
Prohibition of block erasure	Blocks cannot be erased.	Data can be written.Note
Prohibition of writing	Blocks can be erased.	Data cannot be written.
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Note Confirm that no data have been written to the write area. If data in the area has not been erased, do not attempt further writing of data because data cannot be erased after the setting to prohibit block erasure has been made.

(2) During self-programming

Valid Security	Command to be Executed	
	Block Erase	Write
Prohibition of block erasure	Blocks can be erased.	Data can be written.
Prohibition of writing		
Prohibition of rewriting boot cluster 0	Boot cluster 0 cannot be erased.	Boot cluster 0 cannot be written.

Remark To prohibit writing and erasure during self-programming, use the flash shield window function (see 33.6.8 Flash shield window function for detail).

Table 33 - 13 Relationship between Enabling the Security Function and Commands

(1) During serial programming

Valid Security	Command to be Executed	
	Block Erase	Write
Prohibition of block erasure	Blocks cannot be erased.	Data can be written.Note
Prohibition of writing	Blocks can be erased.	Data cannot be written.
Prohibition of rewriting the boot area	The boot area cannot be erased	The boot area cannot be written.
Prohibition of connection to the programmer and on-chip debugger	Blocks cannot be erased.	Data cannot be written.
Success in authentication with programmer connection ID authentication enabled	Blocks can be erased.	Data can be written.
Failure in authentication with programmer connection ID authentication enabled	Blocks cannot be erased.	Data cannot be written.

Note Confirm that no data have been written to the write area. If data in the area has not been erased, do not attempt further writing of data because data cannot be erased after the setting to prohibit block erasure has been made.

(2) During self-programming

Valid Security	Command to be Executed	
	Block Erase	Write
Prohibition of block erasure	Blocks can be erased.	Data can be written.
Prohibition of writing		
Prohibition of rewriting the boot area	The boot area cannot be erased.	The boot area cannot be written.
Prohibition of connection to the programmer and on-chip debugger	Blocks can be erased.	Data can be written.
Programmer connection ID authentication enabled	Blocks can be erased.	Data can be written.

Remark To prohibit writing and erasure during self-programming, use the flash shield window function (see 33.8 Flash Shield Window Function for detail).

Table 33 - 15 Setting Security in Each Programming Mode (1)
During serial programming

Security	Security Setting	Disabling the Security Setting
Prohibition of block erasure	Set via GUI of dedicated flash memory programmer, etc.	Disabling the setting is not possible.
Prohibition of writing		Set via GUI of dedicated flash memory programmer, etc.
Prohibition of rewriting boot cluster 0		Disabling the setting is not possible.

Caution The setting to prohibit writing can only be released when the settings to prohibit erasing blocks and rewriting boot cluster 0 are not made and the code and data flash memory areas are blank.

(2) During self-programming

Security	Security Setting	Disabling the Security Setting
Prohibition of block erasure	Set by using flash self-programming code.	Disabling the setting is not possible.
Prohibition of writing		Disabling the setting is not possible during self-programming (set via GUI of dedicated flash memory programmer, etc. during serial programming).
Prohibition of rewriting boot cluster 0		Disabling the setting is not possible.

Table 33 - 14 Setting Security in Each Programming Mode
(1) During serial programming

Security	Security Setting	Disabling the Security Setting
Prohibition of block erasure	Set via GUI of dedicated flash memory programmer, etc.	Disabling the setting is not possible.
Prohibition of writing		Set via GUI of dedicated flash memory programmer, etc.
Prohibition of rewriting the boot area		Disabling the setting is not possible.
Prohibition of connection to the programmer and on-chip debugger		
Enabling programmer connection ID authentication		

Caution The setting to prohibit writing can only be released when the settings to prohibit erasing blocks and rewriting the boot area are not made and the code and data flash memory areas are blank. However, if connection for serial programming is prohibited due to the setting to prohibit connection to the programmer and on-chip debugger or to enable programmer connection ID authentication, releasing the setting to prohibit writing is not possible because serial programming cannot be executed.

(2) During self-programming

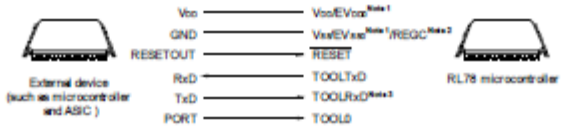
Security	Security Setting	Disabling the Security Setting
Prohibition of block erasure	Set by using self-programming.	Disabling the setting is not possible.
Prohibition of writing		Disabling the setting is not possible during self-programming. Set via GUI of dedicated flash memory programmer, etc.
Prohibition of rewriting the boot area		Disabling the setting is not possible.
Prohibition of connection to the programmer and on-chip debugger		
Enabling programmer connection ID authentication		

82. 34.2 Connection between the External Device that Incorporates UART and RL78/G23 (Page 1347)

Incorrect:

34.2 Connection between the External Device that Incorporates UART and RL78/G23

On-board communications between an external device (a microcontroller or ASIC) that is connected to the RL78 microcontroller via a UART and the host machine is possible. Pins VDD, $\overline{\text{RESET}}$, TOOL0, VSS, TOOLTxD, and TOOLRxD are used for the communications. Communications between the external device and the RL78 microcontroller is established by serial communication using the TOOLTxD and TOOLRxD pins via the dedicated UART of the RL78 microcontroller.



Note 1. This pin is only present in the 64-pin, 80-pin, 100-pin and 128-pin products.

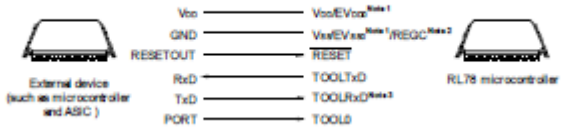
Note 2. Connect the REGC pin to the ground via a capacitor (0.47 to 1 μF).

Note 3. Set the port pin with which TOOLRxD is multiplexed as an input.

Correct:

34.2 Connection between the External Device that Incorporates UART and RL78/G23

On-board communications between an external device (a microcontroller or ASIC) that is connected to the RL78 microcontroller via a UART and the host machine is possible. Pins VDD, $\overline{\text{RESET}}$, TOOL0, VSS, TOOLTxD, and TOOLRxD are used for the communications. Communications between the external device and the RL78 microcontroller is established by serial communication using the TOOLTxD and TOOLRxD pins via the dedicated UART of the RL78 microcontroller. For details and usage notes on the circuit to make the connection, refer to RL78 Debugging Functions Using the Serial Port (R20AN0632EJ0100).



Note 1. This pin is only present in the 64-pin, 80-pin, 100-pin and 128-pin products.

Note 2. Connect the REGC pin to the ground via a capacitor (0.47 to 1 μF).

Note 3. Set the port pin with which TOOLRxD is multiplexed as an input. The input to the input buffer must also be enabled by using the PDIDISx register.

83. 37.1 Absolute Maximum Ratings (Page 1375)

Incorrect:

(2/2)

Absolute Maximum Ratings

Item	Symbols	Conditions		Ratings	Unit
High-level output current	I_{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	-100	mA
	I_{OH2}	Per pin	P20 to P27, P121 to P124, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Low-level output current	I_{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40Note	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P121 to P124, P150 to P156	1	mA
		Total of all pins		5	mA
Ambient operating temperature	T_A	In normal operation mode		-40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Note The rating for the following port pins is 80 mA when IOL1 = 40.0 mA is specified by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P110 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17, P51, and P70 of the 30- to 52-pin package products

Correct:

Absolute Maximum Ratings (2/2)

Item	Symbols	Conditions		Ratings	Unit
High-level output current	I_{OH1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	-100	mA
	I_{OH2}	Per pin	P20 to P27, P121 to P124, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
Low-level output current	I_{OL1}	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40Note	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	I_{OL2}	Per pin	P20 to P27, P121 to P124, P150 to P156	1	mA
		Total of all pins		5	mA
Ambient operating temperature	T_A	In normal operation mode		-40 to +105	°C
		In flash memory programming mode			
Storage temperature	T_{stg}			-65 to +150	°C

Note The rating for the following port pins is 80 mA when IOL1 = 40.0 mA is specified by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P110 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17 and P51 of the 30- to 52-pin package products
- Pin P70 of the 32- to 52-pin package products

84. 37.2.1 Characteristics of the X1 and XT1 oscillators (Page 1376)

Incorrect:

37.2.1 Characteristics of the X1 and XT1 oscillators

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time Note	Ceramic resonator/ crystal resonator		0.05		1	μs
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator			32.768		kHz

Correct:

37.2.1 Characteristics of the X1 and XT1 oscillators

(T_A = −40～+105°C, 2.4V ≦ V_{DD} ≦ 5.5 V (30- to 36-pin products), 1.6 V ≦ V_{DD} ≦ 5.5 V (40- to 128-pin products), V_{SS} = 0 V)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time Note	Ceramic resonator/ crystal resonator		0.05		1	μs
XT1 clock oscillation frequency (f_{XT}) Note	Crystal resonator			32.768		kHz

85. 37.3.1 Pin characteristics (Page 1378 to Page 1381)

Incorrect:

37.3.1 Pin characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable high-level output current Note 1	I_{OH1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV_{DD0} ≤ 5.5 V			-10.0 Note 2	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (when duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-55.0 Note 4	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-10.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			-5.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (when duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-80.0 Note 5	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-19.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			-10.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			-5.0	mA
		Total of all pins (when duty ≤ 70% Note 3)	1.6 V ≤ EV_{DD0} ≤ 5.5 V			-135.0 Note 6	mA
	I_{OH2}	Per pin for P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V			-3.0 Note 2	mA
			2.7 V ≤ V_{DD} < 4.0 V			-1.0 Note 2	mA
			1.8 V ≤ V_{DD} < 2.7 V			-1.0 Note 2	mA
			1.6 V ≤ V_{DD} < 1.8 V			-0.5 Note 2	mA
		Total of all pins (when duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			-5.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			-5.0	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the EVDD0, EVDD1, or VDD pin to an output pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Correct:

37.3.1 Pin characteristics

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable high-level output current Note 1	I_{OH1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	1.6 V ≤ EV_{DD0} ≤ 5.5 V			-10.0 Note 2	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (when duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-55.0 Note 4	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-10.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			-5.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (when duty ≤ 70% Note 3)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			-80.0 Note 5	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			-19.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			-10.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			-5.0	mA
		Total of all pins (when duty ≤ 70% Note 3)	1.6 V ≤ EV_{DD0} ≤ 5.5 V			-135.0 Note 6	mA
	I_{OH2}	Per pin for P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V			-3.0 Note 2	mA
			2.7 V ≤ V_{DD} < 4.0 V			-1.0 Note 2	mA
			1.8 V ≤ V_{DD} < 2.7 V			-1.0 Note 2	mA
			1.6 V ≤ V_{DD} < 1.8 V			-0.5 Note 2	mA
		Total of all pins (when duty ≤ 70% Note 3)	4.0 V ≤ V_{DD} ≤ 5.5 V			-20.0	mA
			2.7 V ≤ V_{DD} < 4.0 V			-10.0	mA
			1.8 V ≤ V_{DD} < 2.7 V			-5.0	mA
			1.6 V ≤ V_{DD} < 1.8 V			-5.0	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the EVDD0, EVDD1, or VDD pin to an output pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The listed currents apply when the duty cycle is no greater than 70%.
Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.
• Total output current from the listed pins = (IOH □ 0.7)/(n □ 0.01)
Example when n = 80% and IOH = -10.0 mA
Total output current from the listed pins = (-10.0 □ 0.7)/(80 □ 0.01) □ -8.7 mA
Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is -30 mA in the products for industrial applications (R7F100Gxx3xxxC) with an ambient operating temperature range of 85°C to 105°C.

Note 5. The maximum value is -50 mA in the products for industrial applications (R7F100Gxx3xxxC) with an ambient operating temperature range of 85°C to 105°C.

Note 6. The maximum values are respectively -100 mA and -60 mA in the products for industrial applications (R7F100Gxx3xxxC) with an ambient operating temperature range of -40°C to 85°C and of 85°C to 105°C.

Caution The following pins are not capable of the output of high-level signals in the N-ch open-drain mode.
P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Note 3. The listed currents apply when the duty cycle is no greater than 70%.
Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.
• Total output current from the listed pins = (IOH □ 0.7)/(n □ 0.01)
Example when n = 80% and IOH = -10.0 mA
Total output current from the listed pins = (-10.0 □ 0.7)/(80 □ 0.01) □ -8.7 mA
Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 4. The maximum value is -30 mA in the products for industrial applications (R7F100Gxx3xxxC) with an ambient operating temperature range of 85°C to 105°C.

Note 5. The maximum value is -50 mA in the products for industrial applications (R7F100Gxx3xxxC) with an ambient operating temperature range of 85°C to 105°C.

Note 6. The maximum values are respectively -100 mA and -60 mA in the products for industrial applications (R7F100Gxx3xxxC) with an ambient operating temperature range of -40°C to 85°C and of 85°C to 105°C.

Caution The following pins are not capable of the output of high-level signals in the N-ch open-drain mode.
P00, P02 to P04, P10 to P15, P17, P43 to P45, P50, P52 to P55, P71, P74, P80 to P82, P96, and P142 to P144

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable low-level output current Note 1	I_{OL1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				20.0 Notes 2, 3	mA
		Per pin for P60 to P63				15.0 Note 2	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (when duty ≤ 70% Note 4)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			70.0 Note 5	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			9.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (when duty ≤ 70% Note 4)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			80.0 Note 5	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			35.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			20.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			10.0	mA
		Total of all pins (when duty ≤ 70% Note 4)				150.0 Note 6	mA
	I_{OL2}	Per pin for P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5 Note 2	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.5 Note 2	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.6 Note 2	mA
			1.6 V ≤ V_{DD} < 1.8 V			0.4 Note 2	mA
		Total of all pins (when duty ≤ 70% Note 4)	4.0 V ≤ V_{DD} ≤ 5.5 V			20	mA
			2.7 V ≤ V_{DD} < 4.0 V			20	mA
			1.8 V ≤ V_{DD} < 2.7 V			15	mA
			1.6 V ≤ V_{DD} < 1.8 V			10	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the EVSS0, EVSS1, or VSS pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The maximum rating for the following port pins is 40 mA when IOL1 = 40.0 mA is specified by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P101 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17, P51, and P70 of the 30- to 52-pin package products

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (2/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Allowable low-level output current Note 1	I_{OL1}	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147				20.0 Notes 2, 3	mA
		Per pin for P60 to P63				15.0 Note 2	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (when duty ≤ 70% Note 4)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			70.0 Note 5	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			15.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			9.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (when duty ≤ 70% Note 4)	4.0 V ≤ EV_{DD0} ≤ 5.5 V			80.0 Note 5	mA
			2.7 V ≤ EV_{DD0} < 4.0 V			35.0	mA
			1.8 V ≤ EV_{DD0} < 2.7 V			20.0	mA
			1.6 V ≤ EV_{DD0} < 1.8 V			10.0	mA
		Total of all pins (when duty ≤ 70% Note 4)				150.0 Note 6	mA
	I_{OL2}	Per pin for P20 to P27, P121, P122, P150 to P156	4.0 V ≤ V_{DD} ≤ 5.5 V			8.5 Note 2	mA
			2.7 V ≤ V_{DD} < 4.0 V			1.5 Note 2	mA
			1.8 V ≤ V_{DD} < 2.7 V			0.6 Note 2	mA
			1.6 V ≤ V_{DD} < 1.8 V			0.4 Note 2	mA
		Total of all pins (when duty ≤ 70% Note 4)	4.0 V ≤ V_{DD} ≤ 5.5 V			20	mA
			2.7 V ≤ V_{DD} < 4.0 V			20	mA
			1.8 V ≤ V_{DD} < 2.7 V			15	mA
			1.6 V ≤ V_{DD} < 1.8 V			10	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the EVSS0, EVSS1, or VSS pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The maximum rating for the following port pins is 40 mA when IOL1 = 40.0 mA is specified by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P101 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17 and P51 of the 30- to 52-pin package products
- Pin P70 of the 32- to 52-pin package products

Note 4. The listed currents apply when the duty cycle is no greater than 70%.
Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.
• Total output current from the listed pins = (IOL □ 0.7)/(n □ 0.01)
Example when n = 80% and IOL = 10.0 mA
Total output current from the listed pins = (10.0 □ 0.7)/(80 □ 0.01) □ 8.7 mA
Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 5. The maximum value is 40 mA in the products for industrial applications (R7F100Gxx3xxxC) with an ambient operating temperature range of 85°C to 105°C.

Note 6. The maximum value is 80 mA in the products for industrial applications (R7F100Gxx3xxxC) with an ambient operating temperature range of 85°C to 105°C.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Note 4. The listed currents apply when the duty cycle is no greater than 70%.
Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.
• Total output current from the listed pins = (IOL □ 0.7)/(n □ 0.01)
Example when n = 80% and IOL = 10.0 mA
Total output current from the listed pins = (10.0 □ 0.7)/(80 □ 0.01) □ 8.7 mA
Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

Note 5. The maximum value is 40 mA in the products for industrial applications (R7F100Gxx3xxxC) with an ambient operating temperature range of 85°C to 105°C.

Note 6. The maximum value is 80 mA in the products for industrial applications (R7F100Gxx3xxxC) with an ambient operating temperature range of 85°C to 105°C.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

86. 37.3.2 Supply current characteristics (Page 1387 to Page 1394)

Incorrect:

37.3.2 Supply current characteristics

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions						Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V			1.4	—	mA
						V_{DD} = 1.8 V			1.4	—	
					Normal operation	V_{DD} = 5.0 V			3.1	5.1	mA
						V_{DD} = 1.8 V			3.1	5.1	
			LS (low-speed main) mode	f_{IH} = 24 MHz Note 2	Normal operation	V_{DD} = 5.0 V			2.3	3.9	mA
						V_{DD} = 1.8 V			2.3	3.9	
				f_{IH} = 16 MHz Note 2	Normal operation	V_{DD} = 5.0 V			1.7	2.8	mA
						V_{DD} = 1.8 V			1.7	2.8	
				f_{IM} = 4 MHz Note 3	Normal operation	V_{DD} = 5.0 V			0.4	0.7	mA
						V_{DD} = 1.6 V			0.4	0.7	
			LP (low-power main) mode	f_{IM} = 2 MHz Note 3	Normal operation	V_{DD} = 5.0 V			206	332	μA
						V_{DD} = 1.6 V			205	331	
				f_{IM} = 1 MHz Note 3	Normal operation	V_{DD} = 5.0 V			115	181	μA
						V_{DD} = 1.6 V			114	180	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V			1.9	3.2	mA
						V_{DD} = 1.8 V			1.9	3.2	
			LS (low-speed main) mode	f_{MX} = 20 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V			1.8	3.0	mA
						V_{DD} = 1.8 V			1.8	3.0	
				f_{MX} = 20 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V			2.0	3.3	mA
						V_{DD} = 1.8 V			2.0	3.2	
				f_{MX} = 10 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V			0.9	1.6	mA
						V_{DD} = 1.8 V			0.9	1.6	
				f_{MX} = 10 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V			1.0	1.7	mA
						V_{DD} = 1.8 V			1.0	1.7	
				f_{MX} = 8 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V			0.8	1.3	mA
						V_{DD} = 1.8 V			0.8	1.3	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V			0.9	1.4	mA
						V_{DD} = 1.8 V			0.9	1.4	

Correct:

37.3.2 Supply current characteristics

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (1/4)

Item	Symbol	Conditions						Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 2	Basic operation	V_{DD} = 5.0 V			1.3	—	mA
						V_{DD} = 1.8 V			1.3	—	
					Normal operation	V_{DD} = 5.0 V			3.0	5.0	mA
						V_{DD} = 1.8 V			3.0	5.0	
			LS (low-speed main) mode	f_{IH} = 24 MHz Note 2	Normal operation	V_{DD} = 5.0 V			2.3	3.8	mA
						V_{DD} = 1.8 V			2.3	3.8	
				f_{IH} = 16 MHz Note 2	Normal operation	V_{DD} = 5.0 V			1.7	2.7	mA
						V_{DD} = 1.8 V			1.7	2.7	
				f_{IM} = 4 MHz Note 3	Normal operation	V_{DD} = 5.0 V			0.4	0.7	mA
						V_{DD} = 1.6 V			0.4	0.7	
			LP (low-power main) mode	f_{IM} = 2 MHz Note 3	Normal operation	V_{DD} = 5.0 V			200	325	μA
						V_{DD} = 1.6 V			200	325	
				f_{IM} = 1 MHz Note 3	Normal operation	V_{DD} = 5.0 V			112	178	μA
						V_{DD} = 1.6 V			111	176	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V			1.9	3.2	mA
						V_{DD} = 1.8 V			1.9	3.2	
			LS (low-speed main) mode	f_{MX} = 20 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V			1.8	3.0	mA
						V_{DD} = 1.8 V			1.7	3.0	
				f_{MX} = 20 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V			1.9	3.2	mA
						V_{DD} = 1.8 V			1.9	3.2	
				f_{MX} = 10 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V			0.9	1.6	mA
						V_{DD} = 1.8 V			0.9	1.6	
				f_{MX} = 10 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V			1.0	1.7	mA
						V_{DD} = 1.8 V			1.0	1.7	
				f_{MX} = 8 MHz Note 4, Square wave input	Normal operation	V_{DD} = 5.0 V			0.8	1.3	mA
						V_{DD} = 1.8 V			0.7	1.3	
				f_{MX} = 8 MHz Note 4, Resonator connection	Normal operation	V_{DD} = 5.0 V			0.9	1.4	mA
						V_{DD} = 1.8 V			0.8	1.4	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pulldown resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pulldown resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 2, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.7	6.3	μA
						T_A = +25°C		4.1	6.8	
						T_A = +50°C		4.4	9.7	
						T_A = +70°C		5.1	15.0	
						T_A = +85°C		6.0	23.4	
						T_A = +105°C		8.7	42.5	
				f_{SUB} = 32.768 kHz Note 3, Square wave input	Normal operation	T_A = -40°C		3.3	5.6	μA
						T_A = +25°C		3.5	5.7	
						T_A = +50°C		3.7	8.4	
						T_A = +70°C		4.3	13.5	
						T_A = +85°C		5.2	21.3	
						T_A = +105°C		7.6	38.7	
				f_{SUB} = 32.768 kHz Note 3, Resonator connection	Normal operation	T_A = -40°C		3.3	5.2	μA
						T_A = +25°C		3.6	5.5	
						T_A = +50°C		3.8	7.9	
						T_A = +70°C		4.4	13.5	
						T_A = +85°C		5.3	21.1	
						T_A = +105°C		7.9	38.9	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pulldown resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (2/4)

Item	Symbol	Conditions					Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 2, Low-speed on-chip oscillator operation	Normal operation	T_A = -40°C		3.2	5.5	μA
						T_A = +25°C		3.5	5.8	
						T_A = +50°C		3.8	8.5	
						T_A = +70°C		4.4	13.8	
						T_A = +85°C		5.3	22.1	
						T_A = +105°C		7.7	40.9	
				f_{SUB} = 32.768 kHz Note 3, Square wave input	Normal operation	T_A = -40°C		3.2	5.6	μA
						T_A = +25°C		3.4	5.7	
						T_A = +50°C		3.7	8.5	
						T_A = +70°C		4.3	13.7	
						T_A = +85°C		5.2	21.4	
						T_A = +105°C		7.6	39.0	
				f_{SUB} = 32.768 kHz Note 3, Resonator connection	Normal operation	T_A = -40°C		3.2	5.2	μA
						T_A = +25°C		3.4	5.4	
						T_A = +50°C		3.7	7.7	
						T_A = +70°C		4.3	13.4	
						T_A = +85°C		5.2	20.9	
						T_A = +105°C		7.7	38.5	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pulldown resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.58	1.98	mA
					V_{DD} = 1.8 V		0.58	1.98	
			LS (low-speed main) mode	f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V		0.48	1.54	mA
					V_{DD} = 1.8 V		0.48	1.54	
				f_{IH} = 16 MHz Note 3	V_{DD} = 5.0 V		0.48	1.23	mA
					V_{DD} = 1.8 V		0.48	1.23	
				f_{IM} = 4 MHz Note 4	V_{DD} = 5.0 V		0.09	0.27	mA
					V_{DD} = 1.6 V		0.09	0.27	
			LP (low-power main) mode	f_{IM} = 2 MHz Note 4	V_{DD} = 5.0 V		34	121	µA
					V_{DD} = 1.6 V		34	121	
				f_{IM} = 1 MHz Note 4	V_{DD} = 5.0 V		29	75	µA
					V_{DD} = 1.6 V		29	75	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.23	1.07	mA
					V_{DD} = 1.8 V		0.20	1.04	
			LS (low-speed main) mode	f_{MX} = 20 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.23	1.07	mA
					V_{DD} = 1.8 V		0.20	1.04	
				f_{MX} = 20 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.41	1.29	mA
					V_{DD} = 1.8 V		0.41	1.29	
				f_{MX} = 10 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.14	0.57	mA
					V_{DD} = 1.8 V		0.12	0.55	
				f_{MX} = 10 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.24	0.69	mA
					V_{DD} = 1.8 V		0.24	0.69	
				f_{MX} = 8 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.12	0.47	mA
					V_{DD} = 1.8 V		0.10	0.45	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.21	0.58	mA
					V_{DD} = 1.8 V		0.21	0.58	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pulldown resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode	f_{IH} = 32 MHz Note 3	V_{DD} = 5.0 V		0.54	1.93	mA
					V_{DD} = 1.8 V		0.53	1.92	
			LS (low-speed main) mode	f_{IH} = 24 MHz Note 3	V_{DD} = 5.0 V		0.45	1.50	mA
					V_{DD} = 1.8 V		0.44	1.49	
				f_{IH} = 16 MHz Note 3	V_{DD} = 5.0 V		0.45	1.19	mA
					V_{DD} = 1.8 V		0.44	1.18	
				f_{IM} = 4 MHz Note 4	V_{DD} = 5.0 V		0.08	0.26	mA
					V_{DD} = 1.6 V		0.08	0.26	
			LP (low-power main) mode	f_{IM} = 2 MHz Note 4	V_{DD} = 5.0 V		33	120	µA
					V_{DD} = 1.6 V		33	120	
				f_{IM} = 1 MHz Note 4	V_{DD} = 5.0 V		29	76	µA
					V_{DD} = 1.6 V		28	74	
			HS (high-speed main) mode	f_{MX} = 20 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.22	1.07	mA
					V_{DD} = 1.8 V		0.19	1.03	
			LS (low-speed main) mode	f_{MX} = 20 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.22	1.07	mA
					V_{DD} = 1.8 V		0.19	1.03	
				f_{MX} = 20 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.40	1.28	mA
					V_{DD} = 1.8 V		0.39	1.27	
				f_{MX} = 10 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.14	0.57	mA
					V_{DD} = 1.8 V		0.12	0.54	
				f_{MX} = 10 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.24	0.69	mA
					V_{DD} = 1.8 V		0.23	0.68	
				f_{MX} = 8 MHz Note 5, Square wave input	V_{DD} = 5.0 V		0.12	0.47	mA
					V_{DD} = 1.8 V		0.10	0.44	
				f_{MX} = 8 MHz Note 5, Resonator connection	V_{DD} = 5.0 V		0.21	0.58	mA
					V_{DD} = 1.8 V		0.20	0.57	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pulldown resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_{IH}: High-speed on-chip oscillator clock frequency

Remark 2. f_{IM}: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM
(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 3, Low-speed on-chip oscillator operation	T_A = -40°C		0.85	2.94	µA
					T_A = +25°C		1.08	3.25	
					T_A = +50°C		1.30	5.95	
					T_A = +70°C		1.72	11.05	
					T_A = +85°C		2.40	19.17	
					T_A = +105°C		4.32	37.31	
				f_{SUB} = 32.768 kHz, Square wave input Note 4	T_A = -40°C		0.22	2.01	µA
					T_A = +25°C		0.29	1.90	
					T_A = +50°C		0.44	4.46	
					T_A = +70°C		0.80	9.36	
					T_A = +85°C		1.44	17.53	
					T_A = +105°C		3.24	35.11	
				f_{SUB} = 32.768 kHz, Resonator connection Note 5	T_A = -40°C		0.23	2.06	µA
					T_A = +25°C		0.34	2.24	
					T_A = +50°C		0.51	4.91	
					T_A = +70°C		0.88	9.93	
					T_A = +85°C		1.52	18.11	
					T_A = +105°C		3.37	36.04	
	I_{DD3}	STOP mode	RAMSDS = 0 Note 6		T_A = -40°C		0.15	1.45	µA
					T_A = +25°C		0.23	1.45	
					T_A = +50°C		0.45	4	
					T_A = +70°C		0.9	9	
					T_A = +85°C		1.6	17	
					T_A = +105°C		4	35	
			RAMSDS = 1 Note 7		T_A = -40°C		0.14	1.45	µA
					T_A = +25°C		0.21	1.45	
					T_A = +50°C		0.4	3.5	
					T_A = +70°C		0.8	8.5	
					T_A = +85°C		1.4	15	
					T_A = +105°C		3.2	30	
			RAMSDS = 1, 128-Hz realtime clock operation Note 8		T_A = -40°C		0.22	1.53	µA
					T_A = +25°C		0.32	1.56	
					T_A = +50°C		0.52	3.62	
					T_A = +70°C		0.93	8.63	
					T_A = +85°C		1.54	15.14	
					T_A = +105°C		3.34	30.14	

(1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM
(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = 0 V) (4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	Subsystem clock operation mode	f_{SUB} = 32.768 kHz Note 3, Low-speed on-chip oscillator operation	T_A = -40°C		0.53	2.31	µA
					T_A = +25°C		0.65	2.38	
					T_A = +50°C		0.80	4.95	
					T_A = +70°C		1.17	9.97	
					T_A = +85°C		1.78	17.96	
					T_A = +105°C		4.41	37.71	
				f_{SUB} = 32.768 kHz, Square wave input Note 4	T_A = -40°C		0.20	1.97	µA
					T_A = +25°C		0.29	2.00	
					T_A = +50°C		0.54	5.33	
					T_A = +70°C		0.99	10.94	
					T_A = +85°C		1.70	19.62	
					T_A = +105°C		4.10	41.82	
				f_{SUB} = 32.768 kHz, Resonator connection Note 5	T_A = -40°C		0.21	2.04	µA
					T_A = +25°C		0.33	2.28	
					T_A = +50°C		0.49	4.98	
					T_A = +70°C		1.05	11.36	
					T_A = +85°C		1.76	20.04	
					T_A = +105°C		4.20	42.52	
	I_{DD3}	STOP mode	RAMSDS = 0 Note 6		T_A = -40°C		0.15	1.45	µA
					T_A = +25°C		0.23	1.45	
					T_A = +50°C		0.45	4	
					T_A = +70°C		0.9	9	
					T_A = +85°C		1.6	17	
					T_A = +105°C		4	35	
			RAMSDS = 1 Note 7		T_A = -40°C		0.14	1.45	µA
					T_A = +25°C		0.21	1.45	
					T_A = +50°C		0.4	3.5	
					T_A = +70°C		0.8	8.5	
					T_A = +85°C		1.4	15	
					T_A = +105°C		3.2	30	
			RAMSDS = 1, 128-Hz realtime clock operation Note 8		T_A = -40°C		0.22	1.53	µA
					T_A = +25°C		0.32	1.56	
					T_A = +50°C		0.53	3.62	
					T_A = +70°C		0.94	8.64	
					T_A = +85°C		1.55	15.15	
					T_A = +105°C		3.40	30.20	

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pulldown resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped. They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The currents in the Max. column include the peripheral operation current, but do not include those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pulldown resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped. They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They include the currents flowing into the RTC, but do not include those into the 32-bit interval timer and watchdog timer.

Note 6. The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.

Note 7. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Note 8. The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

(2) Peripheral Functions (Common to all products)

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I_{FH} Note 1	HIPREC = 1			380	—	μA
		HIPREC = 0			240	—	μA
Middle-speed on-chip oscillator operating current	I_{FIM} Note 1				20	—	μA
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				03	—	μA
RTC operating current	I_{RTC} Notes 1, 2, 3	f_{RTCCLK} = 32.768 kHz			0.005	—	μA
		f_{RTCCLK} = 128 Hz			0.002	—	μA
32-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.04	—	μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 32.768 kHz (typ.)			0.32	—	μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		0.95	1.6	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.75	mA
AV_{REFP} current	I_{ADREF} Note 7	AV_{REFP} = 5.0 V			52	—	μA
A/D converter internal reference voltage current	I_{ADREF} Note 1				114	—	μA
Temperature sensor operating current	I_{TMPS} Note 1				110	—	μA
D/A converter operating current	I_{DAC} Notes 1, 8	Per channel			150	—	μA
Comparator operating current	I_{CMP} Notes 1, 9				6	—	μA
LVD operating current	I_{LVD0} Notes 1, 10				0.02	—	μA
	I_{LVD1} Notes 1, 10				0.02	—	μA
Self-programming operating current	I_{FSP} Notes 1, 11				2.5	12.2	mA
Data flash rewrite operating current	I_{BGO} Notes 1, 12				2.5	12.2	mA
Snooze mode sequencer operating current	I_{SMS} Notes 1, 13	f_{IH} = 32 MHz			1.1	—	mA
		f_{IL} = 32.768 kHz			1.2	—	μA
SNOOZE operating current	I_{SNOZ} Note 1	ADC to be in use	The ADC is shifting from the STOP mode to the SNOOZE mode. Note 14		0.6	0.81	mA
			The ADC is operating in the low-voltage mode. AV_{REFP} = V_{DD} = 3.0 V		1.2	1.56	
		SPI (CSI)/UART to be in use			0.7	0.92	
Remote control signal receiver operating current	I_{REM} Notes 1, 15				0.03	—	μA
Low-speed peripheral clock supply current	I_{SXP} Notes 1, 16	RTCLPC = 0			0.22	—	μA

(4) Peripheral Functions (Common to all products)

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V) (1/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	I_{FH} Note 1	HIPREC = 1			240	—	μA
		HIPREC = 0			380	—	μA
Middle-speed on-chip oscillator operating current	I_{FIM} Note 1				20	—	μA
Low-speed on-chip oscillator operating current	I_{FIL} Note 1				0.3	—	μA
RTC operating current	I_{RTC} Notes 1, 2, 3	f_{RTCCLK} = 32.768 kHz			0.005	—	μA
		f_{RTCCLK} = 128 Hz			0.002	—	μA
32-bit interval timer operating current	I_{IT} Notes 1, 2, 4				0.04	—	μA
Watchdog timer operating current	I_{WDT} Notes 1, 2, 5	f_{IL} = 32.768 kHz (typ.)			0.32	—	μA
A/D converter operating current	I_{ADC} Notes 1, 6	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V		0.95	1.6	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V		0.5	0.75	mA
AV_{REFP} current	I_{ADREF} Note 7	AV_{REFP} = 5.0 V			52	—	μA
A/D converter internal reference voltage current	I_{ADREF} Note 1				114	—	μA
Temperature sensor operating current	I_{TMPS} Note 1				110	—	μA
D/A converter operating current	I_{DAC} Notes 1, 8	Per channel			150	—	μA
Comparator operating current	I_{CMP} Notes 1, 9				6	—	μA
LVD operating current	I_{LVD0} Notes 1, 10				0.02	—	μA
	I_{LVD1} Notes 1, 10				0.02	—	μA
Self-programming operating current	I_{FSP} Notes 1, 11				2.5	12.2	mA
Data flash rewrite operating current	I_{BGO} Notes 1, 12				2.5	12.2	mA

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Output current control operating current	ICCDA Notes 1, 17	The setting of the CCDE register is not 00H.			100	—	μA
	ICCDP Notes 1, 18	Per single output current control port	Setting of the low-level output current: Hi-Z		30	—	μA
			Setting of the low-level output current: 2 to 15 mA		200	—	μA

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (2/2)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit
SNOOZE mode sequencer operating current	ISMS Notes 1, 13	fIH = 32 MHz		30- to 64-pin package products with 96- to 128-Kbyte flash ROM		1.1	—	mA
				30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM		1.1	—	
				44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products		1.4	—	
		fIL = 32.768 kHz		30- to 64-pin package products with 96- to 128-Kbyte flash ROM		1.2	—	μA
				30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM		1.2	—	
				44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products		1.6	—	
SNOOZE operating current	ISNOZ Note 1	fIH=32 MHz	ADC to be in use	The ADC is shifting from the STOP mode to the SNOOZE mode. Note 14		0.6	0.81	mA
				The ADC is operating in the low-voltage mode. AVREFP = VDD = 3.0 V		1.2	1.56	
			Simplified SPI (CSI)/UART to be in use			0.7	0.92	mA
			SMS Note 19	30- to 64-pin package products with 96- to 128-Kbyte flash ROM		1.6	—	mA
				30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM		1.7	—	
				44- to 80-pin package products with 384- to 768-Kbyte flash ROM, and 100- to 128-pin package products		2.0	—	
Remote control signal receiver operating current	IREM Notes 1, 15					0.03	—	μA
Low-speed peripheral clock supply current	ISXP Notes 1, 16	RTCLPC = 0				0.22	—	μA
Output current control operating current	ICCDA Notes 1, 17	The setting of the CCDE register is not 00H.				100	—	μA
	ICCDP Notes 1, 18	Per single output current control port		Setting of the low-level output current: HI-Z		30	—	μA
				Setting of the low-level output current: 2 to 15 mA		200	—	μA
Operating current of the true random number generator	ITRNG Note 1					1.1	—	mA

Note 1. This current flows into VDD.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

Note 3. This current flows into the realtime clock (RTC). It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and IRTC, when the realtime clock is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be included in the supply current. IDD2 in the subsystem clock operation mode includes the operating current of the realtime clock.

Note 4. This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and IIT, when the 32-bit interval timer is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be included in the supply current.

Note 5. This current only flows to the watchdog timer. It includes the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is operating.

Note 6. This current only flows to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter is operating or in the HALT mode.

Note 7. This current flows into AVREFP.

Note 8. This current only flows to the D/A converter. The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IDAC, when the D/A converter is operating or in the HALT mode.

Note 9. This current only flows to the comparator. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ICMP when the comparator is in operation.

Note 10. This current only flows to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.

Note 11. This current only flows during self programming.

Note 12. This current only flows while the data flash memory is being rewritten.

Note 13. This current only flows into the snooze mode sequencer. Note that the operating current of the low-speed on-chip oscillator and the XT1 oscillator are not included. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and ISMS, when the snooze mode sequencer is operating or in the HALT mode.

Note 1. This current flows into VDD.

Note 2. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.

Note 3. This current flows into the realtime clock (RTC). It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and IRTC, when the realtime clock is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be included in the supply current. IDD2 in the subsystem clock operation mode includes the operating current of the realtime clock.

Note 4. This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and IIT, when the 32-bit interval timer is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, IFIL

should be included in the supply current.

Note 5. This current only flows to the watchdog timer. It includes the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is operating.

Note 6. This current only flows to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter is operating or in the HALT mode.

Note 7. This current flows into AVREFP.

Note 8. This current only flows to the D/A converter.

The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IDAC, when the D/A converter is operating or in the HALT mode.

Note 9. This current only flows to the comparator. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ICMP when the comparator is in operation.

Note 10. This current only flows to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.

Note 11. This current only flows during self programming.

Note 12. This current only flows while the data flash memory is being rewritten.

Note 13. This current only flows into the SNOOZE mode sequencer. Note that the operating current of the low-speed on-chip oscillator and the XT1 oscillator are not included. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and ISMS, when the SNOOZE mode sequencer is operating or in the HALT mode.

Note 14. For shift time to the SNOOZE mode, see 18.3.13 SNOOZE Mode Function.

Note 15. This current flows into the remote control signal receiver. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2}, and I_{IT}, when the remote control signal receiver is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current.

Note 16. This current is added to the supply current in the HALT mode when the setting of RTCLPC is 0 in the STOP mode, or when the setting of RTCLPC is 0 with the sub-system clock (f_{SUB}) selected as the CPU clock.

Note 17. This current is added to the supply current when the output voltage control port is set.

Note 18. This current does not include the current flowing into the I/O port pins.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

Note 14. For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode**.

Note 15. This current flows into the remote control signal receiver. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either I_{DD1} or I_{DD2}, and I_{IT}, when the remote control signal receiver is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be included in the supply current.

Note 16. This current is added to the supply current in the HALT mode when the setting of RTCLPC is 0 in the STOP mode, or when the setting of RTCLPC is 0 with the sub-system clock X (f_{SX}) selected as the CPU clock, while the sub-system clock X (fsx) is oscillating.

Note 17. This current is added to the supply current when the output voltage control port is set.

Note 18. This current does not include the current flowing into the I/O port pins.

Note 19. The listed values apply when the SNOOZE mode sequencer is in normal operation equivalent to I_{DD1}. They do not include the current flowing into the peripheral functions other than the SNOOZE mode sequencer.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SX}: Subsystem clock X frequency

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. The typical value for the ambient operating temperature (T_A) is 25°C unless otherwise specified.

87. 37.5.2 Serial interface UARTA (Page 1430)

Incorrect:

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate			200	0	19200	bps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Correct:

(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate			200	0	153600	bps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

88. 37.6.1 A/D converter characteristics, (1) Normal modes 1 and 2 (Page 1434)

Incorrect:

(1) Normal modes 1 and 2

(TA = -40 to +105°C, 2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V,
reference voltage (+) = AVREFP (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM (ADREFM = 1), target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	f_{AD}		1		32	MHz
Overall error Notes 1, 3, 4, 6	AINL	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±7.5	LSB
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
Conversion time Note 6	t_{CONV}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
Zero-scale error Notes 1, 2, 3, 4, 6	E_{ZS}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Full-scale error Notes 1, 2, 3, 4, 6	E_{FS}	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Integral linearity error Notes 1, 4, 6	ILE	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
Differential linearity error Note 1	DLE	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
		2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
		2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
Analog input voltage	V_{AIN}		0		AV_{REFP}	V

Correct:

(1) Normal modes 1 and 2

(TA = -40 to +105°C, 2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V,
reference voltage (+) = AVREFP (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM (ADREFM = 1), target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	f_{AD}			1		32	MHz
Overall error Notes 1, 3, 4, 5	AINL	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±7.5	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±9.0	LSB
Conversion time Note 6	t_{CONV}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V	2.0			µs
Zero-scale error Notes 1, 2, 3, 4, 5	E_{ZS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Full-scale error Notes 1, 2, 3, 4, 5	E_{FS}	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.17	%FSR
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±0.21	%FSR
Integral linearity error Notes 1, 4, 5	ILE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V			±3.0	LSB
Differential linearity error Note 1	DLE	12-bit resolution	4.5 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.7 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
			2.4 V ≤ AV_{REFP} = V_{DD} ≤ 5.5 V		±1.0		LSB
Analog input voltage	V_{AIN}			0		AV_{REFP}	V

89. 37.6.1 A/D converter characteristics, (2) Low-voltage modes 1 and 2 (Page 1435)

Incorrect:

(2) Low-voltage modes 1 and 2

(TA = -40 to +105°C, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V,
reference voltage (+) = AVREFP (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM (ADREFM = 1), target pins ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8		12	Bit
Conversion clock	f_{AD}		1		24	MHz
Overall error Notes 1, 3, 4, 6	AINL	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±9	LSB
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±9	LSB
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±11.5	LSB
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±12.0	LSB
Conversion time Note 6	t_{CONV}	2.7 V ≤ AVREFP = VDD ≤ 5.5 V	3.33			µs
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V	5.0			µs
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V	10.0			µs
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V	20.0			µs
Zero-scale error Notes 1, 2, 3, 4, 6	E_{ZS}	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±0.27	%FSR
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±0.28	%FSR
Full-scale error Notes 1, 2, 3, 4, 6	E_{FS}	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±0.27	%FSR
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±0.28	%FSR
Integral linearity error Notes 1, 4, 6	ILE	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±4.0	LSB
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±4.0	LSB
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±4.5	LSB
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±4.5	LSB
Differential linearity error Note 1	DLE	2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±1.5		LSB
		2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±1.5		LSB
		1.8 V ≤ AVREFP = VDD ≤ 5.5 V		±2.0		LSB
		1.6 V ≤ AVREFP = VDD ≤ 5.5 V		±2.0		LSB
Analog input voltage	V_{AIN}		0		AVREFP	V

Correct:

(2) Low-voltage modes 1 and 2

(TA = -40 to +105°C, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V,
reference voltage (+) = AVREFP (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM (ADREFM = 1), target pins ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	f_{AD}			1		24	MHz
Overall error Notes 1, 3, 4, 5	AINL	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±9	LSB
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±9	LSB
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±11.5	LSB
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±12.0	LSB
Conversion time Note 6	t_{CONV}	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V	3.33			µs
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V	5.0			µs
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V	10.0			µs
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V	20.0			µs
Zero-scale error Notes 1, 2, 3, 4, 5	E_{ZS}	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±0.28	%FSR
Full-scale error Notes 1, 2, 3, 4, 5	E_{FS}	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±0.21	%FSR
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±0.27	%FSR
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±0.28	%FSR
Integral linearity error Notes 1, 4, 5	ILE	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V			±4.0	LSB
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V			±4.0	LSB
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V			±4.5	LSB
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V			±4.5	LSB
Differential linearity error Note 1	DLE	12-bit resolution	2.7 V ≤ AVREFP = VDD ≤ 5.5 V		±1.5		LSB
			2.4 V ≤ AVREFP = VDD ≤ 5.5 V		±1.5		LSB
			1.8 V ≤ AVREFP = VDD ≤ 5.5 V		±2.0		LSB
			1.6 V ≤ AVREFP = VDD ≤ 5.5 V		±2.0		LSB
Analog input voltage	V_{AIN}			0		AVREFP	V

90. 37.6.4 Comparator characteristics (Page 1438)

Incorrect:

(Ta = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage range	IVREF	Input to the IVREF0 and IVREF1 pins C0LVL = 0, C1LVL = 0		0		VDD - 1.4	V
		Input to the IVREF0 and IVREF1 pins C0LVL = 1, C1LVL = 1		1.4		VDD	V
	IVCMP	Input to the IVCMP0 and IVCMP1 pins		-0.3		VDD + 0.3	V
Output delay	td	VDD = 3.0 V, Input slew rate > 1 V/μs	High-speed mode			1.5	μs
			Low-speed mode		3.0		μs
Offset voltage	—	High-speed mode				50	mV
		Low-speed mode				40	mV
Operation stabilization wait time	tCMP			30			μs
Internal reference voltage	VBGR2			1.4		1.6	V

Correct:

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input voltage range	IVREF	Input to the IVREF0 and IVREF1 pins C0LVL = 0, C1LVL = 0		0		VDD – 1.4 and EVDD0	V
		Input to the IVREF0 and IVREF1 pins C0LVL = 1, C1LVL = 1		1.4		EVDD0	V
	IVCMP	Input to the IVCMP0 and IVCMP1 pins		-0.3		EVDD0 + 0.3	V
Output delay	td	VDD = 3.0 V, Input slew rate > 1 V/μs	High-speed mode			1.5	μs
			Low-speed mode		3.0		μs
Offset voltage	—	High-speed mode				50	mV
		Low-speed mode				40	mV
Operation stabilization wait time	tCMP			30			μs
Internal reference voltage	VBGR2			1.4		1.6	V

91. 37.8 Flash Memory Programming Characteristics (Page 1444)

Incorrect:

(2) Data flash memory

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		Symbol	f_{CLK} = 1 MHz			f_{CLK} = 2 MHz, 3 MHz			4 MHz ≤ f_{CLK} < 8 MHz			8 MHz ≤ f_{CLK} < 32 MHz			f_{CLK} = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	µs
Erasure time	256 bytes	t_{E2K}	—	7.8	259.2	—	6.4	232.0	—	5.8	218.5	—	5.5	211.8	—	5.4	209.7	ms
Blank checking time	1 byte	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	256 bytes	t_{BC2K}	—	—	1326.1	—	—	663.1	—	—	335.1	—	—	171.2	—	—	121.0	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs
Time until reading starts following setting DFLEN to 1		—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	ns

Correct:

(2) Data flash memory

(T_A = -40 to +105°C, 1.6 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Item		Symbol	f_{CLK} = 1 MHz			f_{CLK} = 2 MHz, 3 MHz			4 MHz ≤ f_{CLK} < 8 MHz			8 MHz ≤ f_{CLK} < 32 MHz			f_{CLK} = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	t_{P4}	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	µs
Erasure time	256 bytes	t_{E2K}	—	7.8	259.2	—	6.4	232.0	—	5.8	218.5	—	5.5	211.8	—	5.4	209.7	ms
Blank checking time	1 byte	t_{BC4}	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	µs
	256 bytes	t_{BC2K}	—	—	1326.1	—	—	663.1	—	—	335.1	—	—	171.2	—	—	121.0	µs
Time taken to forcibly stop the erasure		t_{SED}	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	µs
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	µs
Time until reading starts following setting DFLEN to 1		—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	µs

92. 38.4 40-Pin Products (Page 1450)

Incorrect:

R7F100GEF3CNP, R7F100GEG3CNP, R7F100GEH3CNP, R7F100GEJ3CNP
R7F100GEF2DNP, R7F100GEG2DNP, R7F100GEH2DNP, R7F100GEJ2DNP

Contact a Renesas Electronics sales office for details.

Correct:

R7F100GEF3CNP, R7F100GEG3CNP, R7F100GEH3CNP, R7F100GEJ3CNP
R7F100GEF2DNP, R7F100GEG2DNP, R7F100GEH2DNP, R7F100GEJ2DNP

JEITA Package code	RENESAS code	MASS(TYP.)[g]
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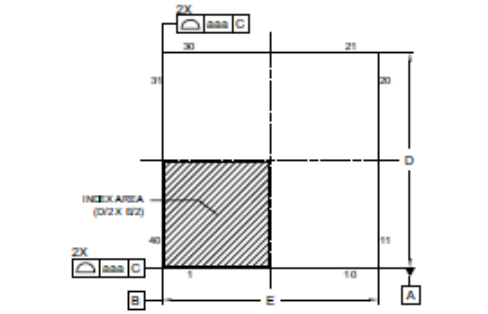
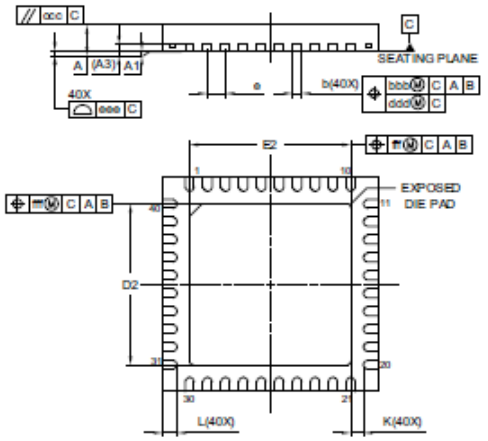




Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.18	0.25	0.30
D		6.00 BSC	
E		6.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	4.45	4.50	4.55
E_2	4.45	4.50	4.55
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	

93. 38.6 48-Pin Products (Page 1453)

Incorrect:

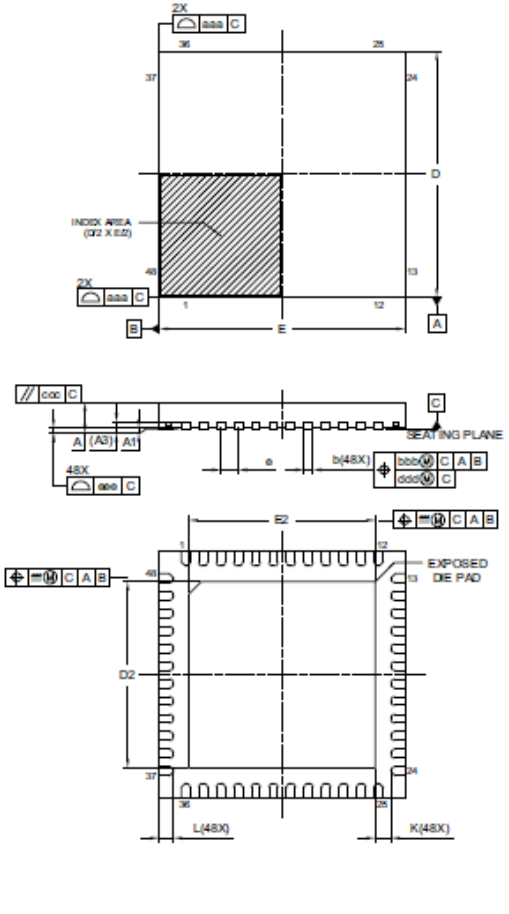
R7F100GGF3CNP, R7F100GGG3CNP, R7F100GGH3CNP, R7F100GGJ3CNP
R7F100GGK3CNP, R7F100GGL3CNP, R7F100GGN3CNP
R7F100GGF2DNP, R7F100GGG2DNP, R7F100GGH2DNP, R7F100GGJ2DNP
R7F100GGK2DNP, R7F100GGL2DNP, R7F100GGN2CNP

Contact a Renesas Electronics sales office for details.

Correct:

R7F100GGF3CNP, R7F100GGG3CNP, R7F100GGH3CNP, R7F100GGJ3CNP
R7F100GGK3CNP, R7F100GGL3CNP, R7F100GGN3CNP
R7F100GGF2DNP, R7F100GGG2DNP, R7F100GGH2DNP, R7F100GGJ2DNP
R7F100GGK2DNP, R7F100GGL2DNP, R7F100GGN2CNP

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A_1	0.00	0.02	0.05
A_3		0.203 REF.	
b	0.20	0.25	0.30
D		7.00 BSC	
E		7.00 BSC	
e		0.50 BSC	
L	0.30	0.40	0.50
K	0.20	—	—
D_2	5.25	5.30	5.35
E_2	5.25	5.30	5.35
aaa		0.15	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	
fff		0.10	