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RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RA*-A0031A/E	Rev.	1.00
Title	RA4M2 Group, RA4M3 Group, RA6M4 Group, RA6M5 Group, addition of CTSU register bit (CTSUERRS)		Information Category	Technical Notification		
Applicable Product	RA4M2 Group RA4M3 Group RA6M4 Group RA6M5 Group	Lot No. All	Reference Document	RA4M2 Group User's Manual Hardware Rev.1.10 RA4M3 Group User's Manual Hardware Rev.1.20 RA6M4 Group User's Manual Hardware Rev.1.10 RA6M5 Group User's Manual Hardware Rev.1.10		

The bit of CTSU Error Status Register (CTSUERRS) is added.

[before] example

CTSU Error Status Register(CTSUERRS)

Base address: CTSU = 0x400D_0000

Offset address: 0x1C

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUICOMP	-	-	-	-	-	-	-	CTSUTSOC	-	-	-	CTSUDRV	CTSUTSOD	CTSUSPMD[1:0]	
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Functions	R/W
1:0	CTSUSPMD[1:0]	Calibration Mode Bits	Calibration Mode 00: Capacitance measurement mode 10: Calibration mode Others: Setting prohibited	R/W
2	CTSUTSOD	TS Pins Fixed Output Bit	TS Pins Fixed Output 0: Capacitance measurement mode 1: Output High or Low from TS terminals	R/W
3	CTSUDRV	Calibration Setting 1 Bit	Calibration Setting 1 0: Capacitance measurement mode 1: Calibration setting 1	R/W
6:4	-	Reserved Bits	These bits are read as 0. The write value should be 0.	R/W
7	CTSUTSOC	Calibration Setting 2 Bit	Calibration Setting 2 0: Capacitance measurement mode 1: Calibration setting 2	R/W
14:8	-	Reserved Bits	These bits are read as 0. The write value should be 0.	R/W
15	CTSUICOMP	TSCAP Voltage Error Monitor Bit	This bit monitors the error status of the TSCAP voltage 0: Normal TSCAP voltage 1: Abnormal TSCAP voltage.	R

CTSUSPMD[1:0] bits (Calibration Mode)

The CTSUSPMD[1:0] bits are used to calibrate the CTSU. When measuring the capacitance, set these bits to 00b.

CTSUTSOD bit (TS Pin Fixed Output)

The CTSUTSOD bit is used to calibrate the CTSU. When setting this bit to 1, the TS pins are forced to the logic level specified by the CTSUCR0.CTSUIOC bit. When measuring the capacitance, set this bit to 0.

CTSUDRV bit (Calibration Setting 1)

The CTSUDRV bit is used to calibrate the CTSU. When measuring the capacitance, set this bit to 0.

CTSUTSOC bit (Calibration Setting 2)

The CTSUTSOC bit is used to calibrate the CTSU. When measuring capacitance, set this bit to 0.

CTSUICOMP bit (TSCAP Voltage Error Monitor)

If the offset current amount set in the CTSUSO1 register exceeds the sensor ICO input current during touch measurement, the TSCAP voltage becomes abnormal and touch measurement cannot be performed correctly. The CTSUICOMP bit monitors the TSCAP voltage and it sets to 1 if the voltage becomes abnormal.

If the TSCAP voltage becomes abnormal, the sensor ICO counter value becomes undefined, but touch measurement completes normally, so it is difficult to detect an abnormality by reading the sensor ICO counter value. If the CTSU reference ICO current adjustment bits (CTSURICOA[7:0]) in the CTSUSO1 register are set to any value other than 0, always check this bit when touch measurement completes.

[after]

CTSU Error Status Register(CTSUERRS)

Base address: CTSU = 0x400D_0000

Offset address: 0x1C

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUICOMP	-	-	-	-	-	-	-	CTSUTSOC	CTSUCLKSEL1	-	-	CTSUDRV	CTSUTSOD	CTSUSPMD[1:0]	
Reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Functions	R/W
1:0	CTSUSPMD[1:0]	Calibration Mode Bits	Calibration Mode 00: Capacitance measurement mode 10: Calibration mode Others: Setting prohibited	R/W
2	CTSUTSOD	TS Pins Fixed Output Bit	TS Pins Fixed Output 0: Capacitance measurement mode 1: Output High or Low from TS terminals	R/W
3	CTSUDRV	Calibration Setting 1 Bit	Calibration Setting 1 0: Capacitance measurement mode 1: Calibration setting 1	R/W
5:4	-	Reserved Bits	These bits are read as 0. The write value should be 0.	R/W
6	CTSUCLKSEL1	Calibration Setting 3 Bit	Calibration Setting 3 0: Capacitance measurement mode 1: Calibration setting 3	R/W
7	CTSUTSOC	Calibration Setting 2 Bit	Calibration Setting 2 0: Capacitance measurement mode 1: Calibration setting 2	R/W
14:8	-	Reserved Bits	These bits are read as 0. The write value should be 0.	R/W
15	CTSUICOMP	TSCAP Voltage Error Monitor Bit	This bit monitors the error status of the TSCAP voltage 0: Normal TSCAP voltage 1: Abnormal TSCAP voltage. *1	R

Note 1. When CTSUCR1.CTSUPON bit is 0, this bit is set to 1.

CTSUSPMD[1:0] bits (Calibration Mode)

The CTSUSPMD[1:0] bits are used to calibrate the CTSU. When measuring the capacitance, set these bits to 00b.

CTSUTSOD bit (TS Pins Fixed Output)

The CTSUTSOD bit is used to calibrate the CTSU. When setting this bit to 1, the TS pins are forced to the logic level specified by the CTSUCR0.CTSUIOC bit. When measuring the capacitance, set this bit to 0.

CTSUDRV bit (Calibration Setting 1)

The CTSUDRV bit is used to calibrate the CTSU. When measuring capacitance, set these bits to 0.

CTSUCLKSEL1 bit (Calibration Setting 3)

The CTSUCLKSEL1 bit is used to calibrate the CTSU. When measuring capacitance, set these bits to 0.

CTSUTSOC bit (Calibration Setting 2)

The CTSUTSOC bit is used to calibrate the CTSU. When measuring capacitance, set these bits to 0.

CTSUICOMP bit (TSCAP Voltage Error Monitor)

The CTSUICOMP bit monitors the TSCAP voltage and it is set to 1 if the voltage becomes abnormal.

If the offset current ~~amount set~~ specified in the CTSUSO0 register exceeds the sensor ICO input current during touch measurement, the TSCAP voltage becomes abnormal and touch measurement cannot be performed correctly. ~~The CTSUICOMP bit monitors the TSCAP voltage and it sets to 1 if the voltage becomes abnormal.~~

If the TSCAP voltage becomes abnormal, the sensor ICO counter value becomes undefined, but touch measurement completes normally, therefore it is difficult to detect an abnormality by reading the sensor ICO counter value. If the CTSU reference ICO current adjustment bits (CTSURICOA[7:0]) in the CTSUSO1 register are set to any value other than 0, always check this bit when touch measurement completes.

This bit is cleared by writing 0 to the CTSUCR1.CTSUPON bit and turning off the power supply.