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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-R8C-A030A/E	Rev.	1.00
Title	Note Regarding the RXD2 Pin of the Serial Interface (UART2)		Information Category	Technical Notification		
Applicable Product	See below	Lot No.	Reference Document			

Incorrect descriptions have been found in the port setting when using the RXD2 pin. The information in this Technical Update applies to the products below.

1. Applicable products

R8C/32A Group, R8C/32C Group, R8C/32D Group, R8C/32M Group,
R8C/33A Group, R8C/33C Group, R8C/33D Group, R8C/33M Group,
R8C/34C Group, R8C/34M Group,
R8C/35A Group, R8C/35C Group, R8C/35D Group, R8C/35M Group,
R8C/36A Group, R8C/36C Group, R8C/36M Group,
R8C/38A Group, R8C/38C Group, R8C/38M Group,
R8C/3GA Group, R8C/3GC Group, R8C/3GD Group, R8C/3GM Group,
R8C/3JA Group, R8C/3JC Group, R8C/3JM Group,
R8C/33T Group, R8C/3JT Group,
R8C/34K Group, R8C/34U Group, R8C/3MK Group, R8C/3MU Group,
R8C/32G Group, R8C/32H Group, R8C/33G Group, R8C/33H Group,
R8C/34P Group, R8C/34R Group,
R8C/34E Group, R8C/34F Group, R8C/34G Group, R8C/34H Group,
R8C/36E Group, R8C/36F Group, R8C/36G Group, R8C/36H Group,
R8C/38E Group, R8C/38F Group, R8C/38G Group, R8C/38H Group,
R8C/34W Group, R8C/34X Group, R8C/34Y Group, R8C/34Z Group,
R8C/36W Group, R8C/36X Group, R8C/36Y Group, R8C/36Z Group,
R8C/38W Group, R8C/38X Group, R8C/38Y Group, R8C/38Z Group,
R8C/LA6A Group, R8C/LA8A Group

2. Port setting when using the RXD2 pin

When using the RXD2 pin with UART2, set the IICM bit in the U2SMR register to 0.

Although the IICM bit is specified as either 1 or X (meaning 0 or 1) in port settings tables in I/O Ports Chapter in the User's Manual: Hardware, make sure to set the IICM bit to 0.

Example:

Table P8_6(/RXD0/RXD2/SCL2)

Register		PD8	U0SR		U2SR0		U2MR			U2SMR	Function
Bit		PD8_6	RXD0SEL		RXD2SEL		SMD			IICM	
			1	0	1	0	2	1	0		
Pin	P8_6	0	Other than 01b		Other than 11b		X	X	X	X	Input port (1)
		1	Other than 01b		Other than 11b		X	X	X	X	Output port (2)
	(RXD0)	0	0	1	Other than 11b		X	X	X	X	RXD0 input (2)
	(RXD2)	0	Other than 01b		1	1	X	X	X	1	RXD2 input (2)
	(SCL2)	0	Other than 01b		1	1	0	1	0	1	SCL2 input/output (3)

0

X: 0 or 1

Notes:

1. Pulled up by setting the PU86 bit in the P8PUR register to 1.
2. Output drive capacity high by setting the P8DRR6 bit in the P8DRR register to 1.
3. N-channel open-drain output by setting the NCH bit in the U2C0 register to 1. At this time, set the PD8_6 bit in the PD8 register to 0.