To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

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RENESAS TECHNICAL UPDATE

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Product Category	MPU&MCU		Document No.	TN-32R-A076A/E	Rev.	1.00
Title	Precautions to be taken when switching from flash E/W enable mode to normal mode		Information Category	Technical Notification		
Applicable Product	32170/32174 Group, 32171 Group, 32172/32173 Group, 32176 Group, 32180 Group, 32182 Group, 32185/32186 Group, 32192/32195/32196 Group	Lot No. -	Reference Document	Hardware Manual		

When switching from flash E/W enable mode to normal mode, the following precautions should be taken.

[Content]

When reading internal flash memory after switching from flash E/W enable mode to normal mode, it should be read after waiting for more than the following CPUCLK cycle when FENTRY bit in Flash Control Register 1 (FCNT1) is set from “1 ” to ”0”.

If internal flash memory is read before waiting for the following CPUCLK cycle, the undefined value may be read.

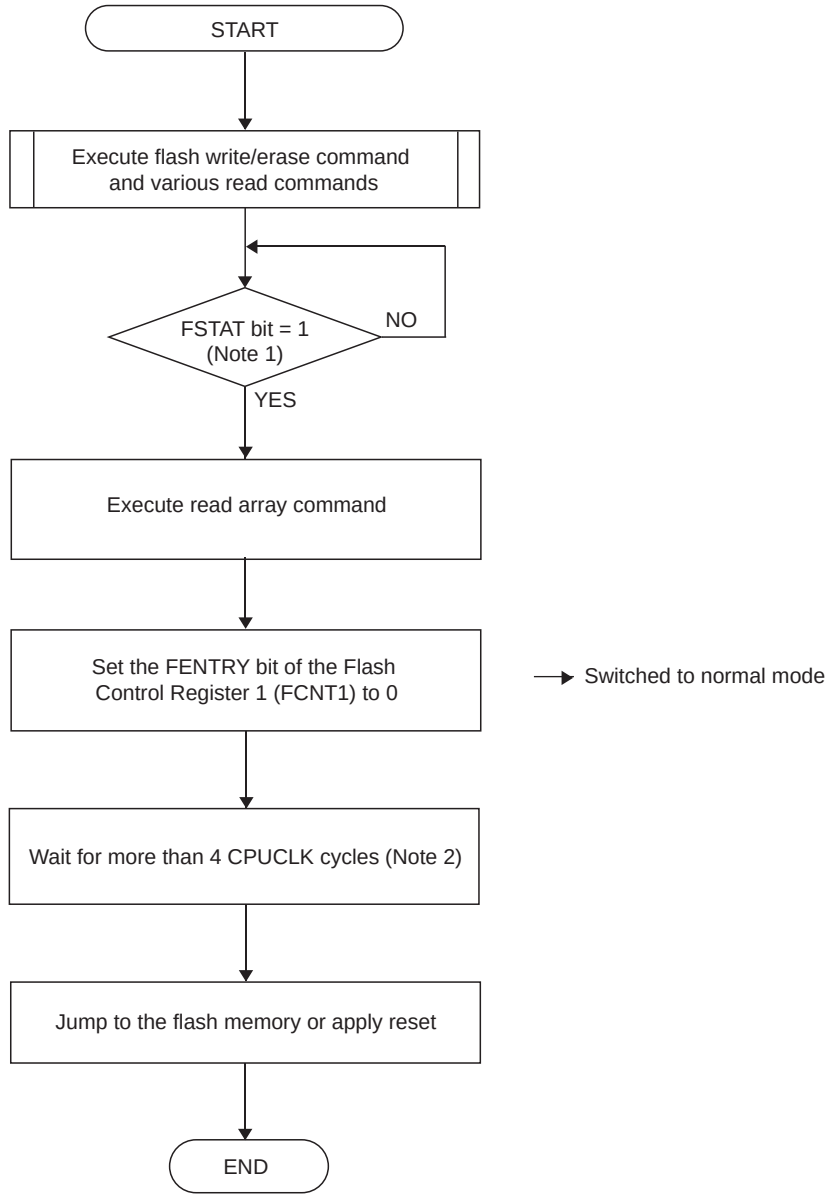
As the EI vector entry address is exchanged in the following CPUCLK cycle, disenable the External Interrupt (EI).

- When using 32170/32174 Group, 32171 Group or 32172/32173 Group
  CPUCLK cycle = 4 CPUCLK cycles
- When using 32176 Group
  CPUCLK cycle = 4 CPUCLK cycles
- When using 32180 Group or 32182 Group
  CPUCLK cycle = 8 CPUCLK cycles
- When using 32185/32186 Group, or 32192/32195/32196 Group
  CPUCLK cycle = 8 CPUCLK cycles

Procedures for switching from flash E/W enable mode to normal mode are shown on the following page.

Note: The instruction fetch and operand accesses are included in the reading process for internal flash memory.

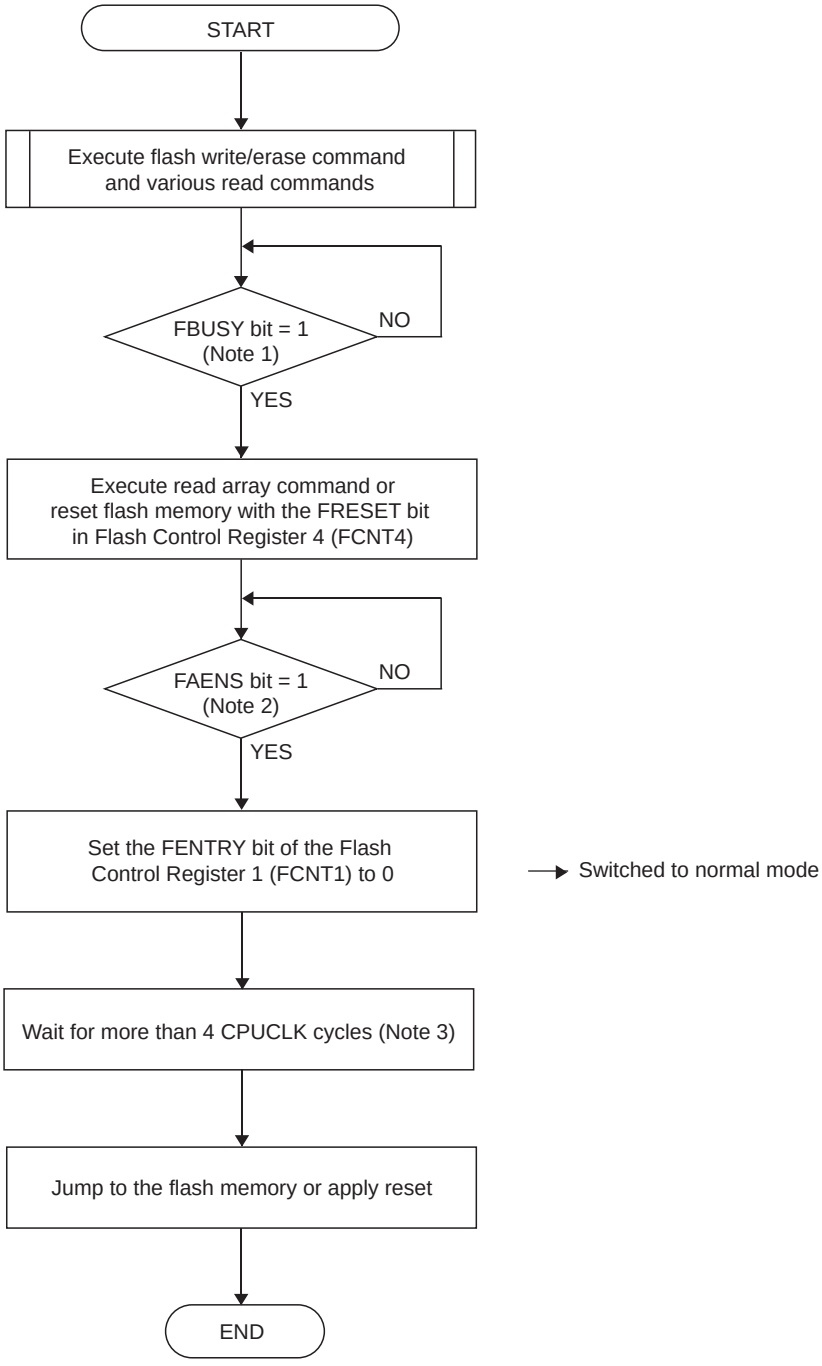
When using the 32170/32174 Group 32171 Group or 32172/32173 Group



Note1: If it is checked that the value of FSTAT bit in Flash Status Register 1 (FSTAT1) is "1" after executing the command in flash E/W enable mode, it is not necessary to check that the value of FSTAT bit is "1".
Note2: Insert any instructions for more than 4 CPUCLK waits other than NOP that do not require clock cycles (one that is automatically inserted by the assembler for alignment adjustment: instruction code H'F000). As the EI vector entry address is exchanged in the instructions for 4 CPUCLK waits, disenable the External Interrupt (EI).
Note: When switching to normal mode by entering a low-level signal to the RESET# pin in flash E/W enable mode, enter the signal to the RESET# pin after checking that the value of FSTAT bit is "1"(ready).

Figure 1 Procedure for switching from flash E/W enable mode to normal mode

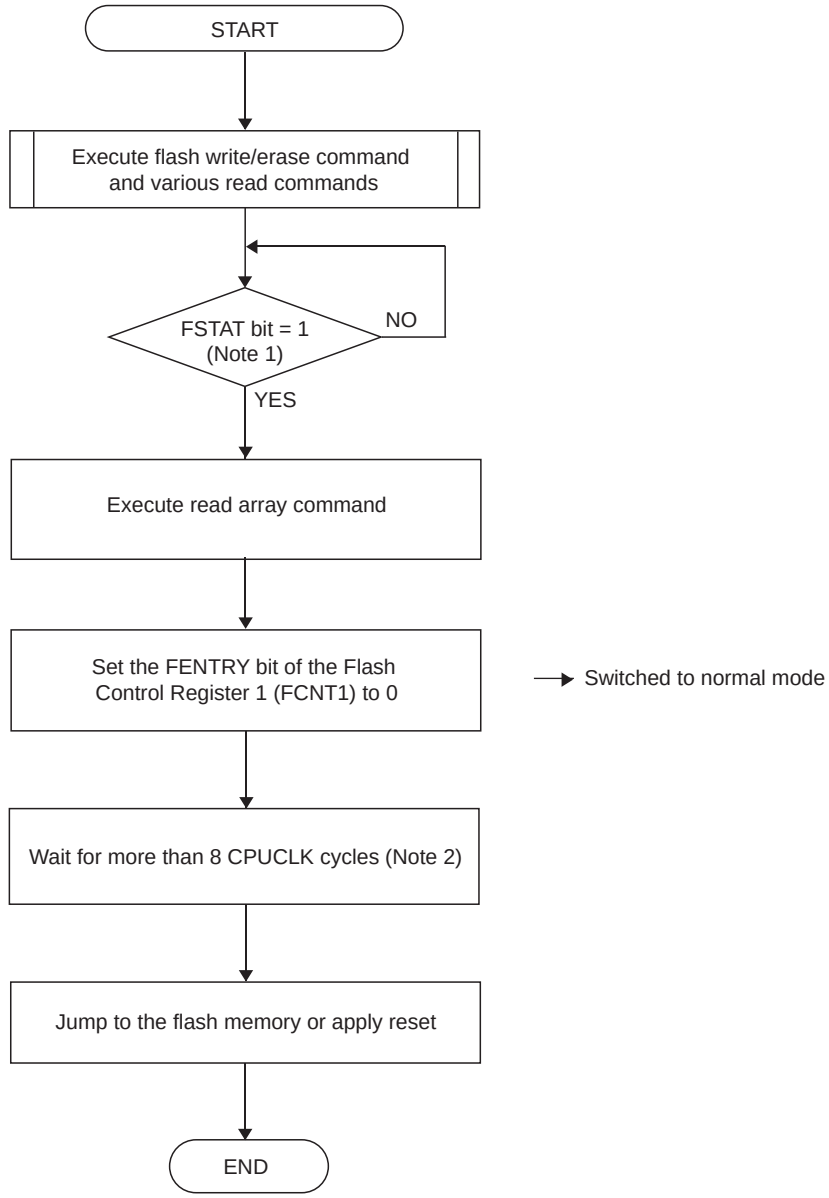
When using the 32176 Group



Note1: If it is checked that the value of FBUSY bit in Flash Status Register (FSTAT) is "1" after executing the command in flash E/W enable mode, it is not necessary to check that the value of FBUSY bit is "1".
Note2: If flash memory reset by FRESET bit in Flash Control Register 4 (FCNT4) is not executed, it is not necessary to check that the value of FAENS bit in Flash Mode Register (FMOD) is "1".
Note3: Insert any instructions for more than 4 CPUCLK waits other than NOP that do not require clock cycles (one that is automatically inserted by the assembler for alignment adjustment: instruction code H'F000). As the EI vector entry address is exchanged in the instructions for 4 CPUCLK waits, disenable the External Interrupt (EI).
Note: When switching to normal mode by entering a low-level signal to the RESET# pin in flash E/W enable mode, enter the signal to the RESET# pin after checking that the value of FBUSY bit is "1"(ready).

Figure 2 Procedure for switching from flash E/W enable mode to normal mode

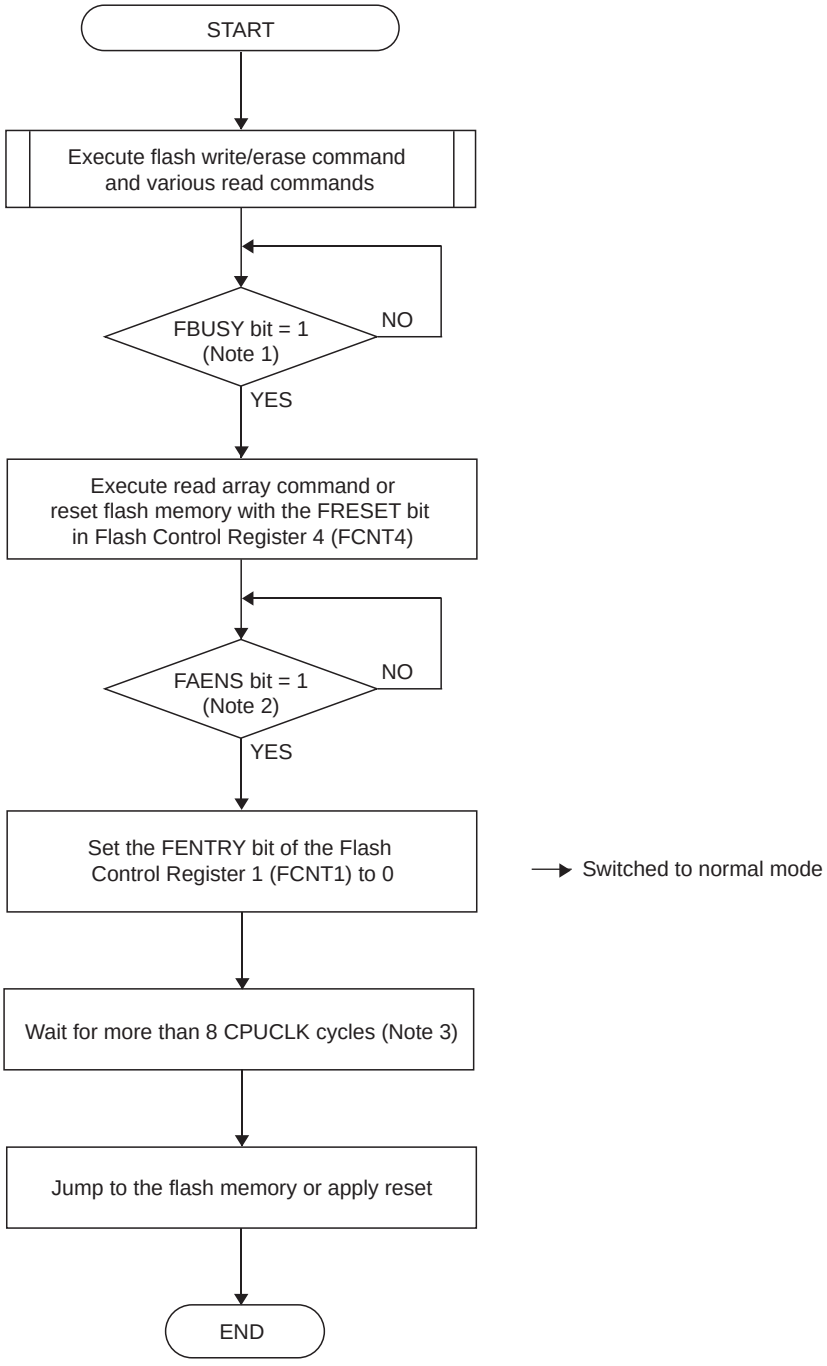
When using the 32180 Group or 32182 Group



Note1: If it is checked that the value of FSTAT bit in Flash Status Register 1 (FSTAT1) is "1" after executing the command in flash E/W enable mode, it is not necessary to check that the value of FSTAT bit is "1".
Note2: Insert any instructions for more than 8 CPUCLK waits other than NOP that do not require clock cycles (one that is automatically inserted by the assembler for alignment adjustment: instruction code H'F000). As the EI vector entry address is exchanged in the instructions for 8 CPUCLK waits, disenable the External Interrupt (EI).
Note: When switching to normal mode by entering a low-level signal to the RESET# pin in flash E/W enable mode, enter the signal to the RESET# pin after checking that the value of FSTAT bit is "1"(ready).

Figure 3 Procedure for switching from flash E/W enable mode to normal mode

When using the 32185/32186 Group, or 32192/32195/32196 Group



Note1: If it is checked that the value of FBUSY bit in Flash Status Register (FSTAT) is "1" after executing the command in flash E/W enable mode, it is not necessary to check that the value of FBUSY bit is "1".
Note2: If flash memory reset by FRESET bit in Flash Control Register 4 (FCNT4) is not executed, it is not necessary to check that the value of FAENS bit in Flash Mode Register (FMOD) is "1".
Note3: Insert any instructions for more than 8 CPUCLK waits other than NOP that do not require clock cycles (one that is automatically inserted by the assembler for alignment adjustment: instruction code H'F000). As the EI vector entry address is exchanged in the instructions for 8 CPUCLK waits, disenable the External Interrupt (EI).
Note: When switching to normal mode by entering a low-level signal to the RESET# pin in flash E/W enable mode, enter the signal to the RESET# pin after checking that the value of FBUSY bit is "1"(ready).

Figure 4 Procedure for switching from flash E/W enable mode to normal mode