NEC

Customer Notification

IE-703079-MC-EM1

In-Circuit Emulator Option Board

Operating Precautions

Target Device

V850/SF1
V850/SF1A

Document No. TPS-HE-B-2768
Date Published June 2004

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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M8E 02.10

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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(A) Table of Operating Precautions

No.	Outline		IE-703239-G1-EM1								
		Rev.	1.00	1.01	1.02	1.03	1.04	1.24	1.34	1.44	1.55
		Control Code[Note]	A	B	C	D	E	F	G	H	J
1	P00/NMI port function		✘	✔	✔	✔	✔	✔	✔	✔	✔
2	FCAN: Time stamp counter prescaler setting		✘	✘	✘	✘	✔	✔	✔	✔	✔
3	Double interrupt execution		✘	✘	✘	✘	✘	✘	✘	✘	✘
4	Initial port values		✘	✘	✘	✘	✘	✘	✘	✘	✘
5	POC function		✘	✘	✘	✘	✘	✘	✘	✘	✘
6	PM11 restriction		✘	✔	✔	✔	✔	✔	✔	✔	✔
7	FCAN: Resynchronisation		✘	✘	✘	✘	✘	✘	✘	✘	✘
8	FCAN: CACT Register access		✘	✘	✘	✘	✘	✘	✘	✘	✘
9	FCAN: Diagnostic Mode		✘	✘	✘	✘	✘	✘	✘	✘	✘
10	P00 High level output voltage		✘	✘	✘	✘	✘	✘	✘	✘	✘
11	FCAN: Restriction when WAIT pin is used		✘	✘	✘	✔	✔	✔	✔	✔	✔
12	FCAN: Caution using FCAN memory		✘	✘	✘	✘	✔	✔	✔	✔	✔
13	Wakeup from power down mode		✘	✘	✘	✘	✘	✘	✘	✘	✘
14	Timer 0, 1, 7 one-shot pulse mode		✘	✘	✘	✘	✘	✘	✘	✘	✘
15	Restrictions on external clock		✘	✘	✘	✘	✘	✘	✘	✘	✘
16	Emulation of ROM correction		✘	✘	✘	✘	✘	✘	✘	✘	✘
17	Oscillation stabilisation time		✘	✘	✘	✘	✘	✘	✘	✘	✘
18	Interrupt request and STOP/IDLE mode		✘	✘	✘	✘	✘	✘	✔	✔	✔
19	Change of the target CPU for emulation		✘	✘	✘	✘	✘	✔	✔	✔	✔
20	HI-Z on CLKOUT pin		✘	✘	✘	✘	✘	✘	✘	✘	✘
21	FCAN: Initialisations of emulator before using FCAN		✘	✘	✘	✘	✘	✘	✘	✘	✘
22	FCAN: Message search		✘	✔	✔	✔	✔	✔	✔	✔	✔
23	FCAN Main clock select		✘	✘	✘	✘	✘	✘	✘	✘	✘
24	External Bus Interface		✘	✘	✘	✘	✘	✘	✘	✔	✔
25	FCAN area access		✔	✔	✔	✔	✔	✔	✔	✘	✔

✔ : Not applicable
✘ : Applicable

Note: The Control Code is indicated by the letter appearing at the 2nd position from the left in the serial number of the product. If the product has been upgraded, a label indicating the new version is attached to the product and the x in V-UP LEVEL x on this label indicates the new control code.

(B) Description of Operating Precautions

No. 1	P00/NMI port function

Details

The internal connection to the port control gate is missing. Therefore this port cannot be used, including the NMI functionality. Based on this, higher current than specified may flow in stand-by modes (HALT, IDLE and STOP mode).

No. 2	FCAN: Time stamp counter prescaler setting

Details

It is not possible to change the global time stamp frequency$_{GTS}$ by changing the interval cycles (CGTS7 to CGTS0), if the prescaler clock selection (GTCS0/1) is set to 00B. Other settings of prescaler clock selection are not affected.

No. 3	Double interrupt execution

Details

An interrupt that should occur only once occurs twice if the following three conditions occur simultaneously while interrupts are enabled:

1) A bit manipulation instruction (set1, clr1, not1 or tst1) is executed on an interrupt request flag (xxIFn) of an interrupt control register (xxICn)
2) Interrupt processing involving the hardware of the same register occurs
3) There is a DMA startup while executing the above bit operation

Remark: xx: Identification name of a peripheral unit (WDT, P, WTNI, TM, CSI, SER, ST, AD, DMA, WTN, KR, IIC)
n: peripheral unit number

If the above mentioned condition appears the interrupt request flag which is normally reset to 0 at the acknowledge of interrupt processing will not be reset. Consequently after returning from interrupt processing (reti instruction) the interrupt processing is executed again. This does not happen, if DMA is not used.

Workaround

During a bit manipulation operation using the clr1 instruction on the interrupt request flag of the CSIC0 register (CSIF0), the non-masked INTCSI0 interrupt occurs at the same time as a DMA start up. As a result the INTCSI0 interrupt processing is executed twice.

To avoid this behaviour do one of the following:

1) Insert a DI instruction before and an EI instruction after executing a bit manipulation instruction on an interrupt request flag (xxIFn) of an interrupt control register (xxICn) to avoid carrying out interrupt processing immediately after executing the bit manipulation instruction.
2) When interrupt processing begins, the hardware enters a state where interrupts are disabled. Clear the interrupt request flag in all interrupt processing routines before executing the EI instruction.

No. 4	Initial port values

Details

When the In-Circuit-Emulator System is started up without connection to a target board, initial values of all Ports are indefinite.

No. 5	POC function

Details

POC function cannot be used on the IE-703079-MC-EM1.

No. 6	PM11 restriction

Details

When FCAN is used and P114 and P116 are set to output mode P11 and PM11 cannot be modified anymore. Therefore do not set PM114 and PM116 to output when CAN is used. Only set PAC register to select CAN function of output pins.

No. 8	FCAN: CACT Register access

Details

The register CxBA offers information on the current bus activity for each CAN channel in the field CACT. For the bus off status of the channel normally the code "17" is displayed. Erroneously, the value for bus off status is never provided. Instead, in bus off status the CPU will read always the activity status that preceded the bus off condition.
The CACT register is implemented to serve CAN experts while debugging new FCAN macros. The application should not use the CACT especially not for detecting a bus off condition. Instead, the bus off status can be derived from CxCTRL register (bit: BOFF).

No. 9	FCAN: Diagnostic Mode

Details

The diagnostic mode is not entered when setting MOM bit in CxDEF register to 1. This mode was considered for baud rate detection and diagnostic purposes. As a consequence the "receive only" operation of the FCAN is not available.
Applications that need to implement automatic baud rate detection may use one of the following procedure instead of "receive only" mode:

- Set TPE bit in CxCTRL register to 1. The transmit pin of the respective CAN module is disabled then.
- In case the device facilitates a shared port function for the CAN transmit pin, the output latch of this port bit has to be set to 1 and corresponding bit in the port mode register can be set to output mode. This provides recessive level for the CAN transmit line.

Any message on the CAN bus will update the VALID bit in the CxDEF register. The correct baud rate is achieved if the VALID bit reads 1.

Further Precaution: **Immediate Recovery from Bus Off Status**
Although the "receive only" operation is not usable, the receive and transmit error counters can be reset. The respective CAN module could be transferred into initialization status by the normal initialization request (INIT =1 in CxCTRL).
Applications that used the "receive only" operation in order to recover immediately from bus off conditions need to implement a software workaround. The application needs to monitor the transmit-error counter (TEC). This can be supported by the CAN bus error interrupt (CxINT5) indicating that REC or TEC incremented. Before the counter reaches the bus off value (TEC > 255) the application puts the CAN module into initialization status and restarts it. Since the TEC can increment by 8 for every bit sent on the CAN bus, the initialization has to be performed well ahead of a TEC reading of 255. The CAN error interrupt needs only to be enabled as long as the CAN node is in error passive state (TEC > 127).

No. 10	P00 High level output voltage

Details

For versions 1.00, 1.01 and 1.02 (Control code A, B and C) of IE-703079-MC-EM1 the following applies: On port P00 the highl level output voltage = PORTVDD - 1 V.
For version 1.03 (control code D) of IE-703079-MC-EM1 and later the high level output voltage = 5 V regardless of PORTVDD.

No. 11	FCAN: Restriction when WAIT pin is used

Details

The FCAN function cannot be used if the WAC flag of the PAC register is set to activate the WAIT pin.

No. 12	FCAN: Caution using FCAN memory

Details

The in-circuit emulator deadlocks if addresses between 0xnffe00 and 0xnfffff (n = 3, 7, b) of the FCAN address area are accessed (this area is unusable).

No. 13	Wakeup from power down mode

Details

When the uC wakes up from a power saving mode (IDLE or STOP) a discrepancy may occur between the address indicated by the program counter (PC) and the address at which an instruction is actually read if the conditions mentioned below apply.
This may result in the CPU ignoring 4 or 8 bytes of instruction code from between 4 bytes and 16 bytes after an instruction that writes to the PSC register. This could in turn result in execution of an erroneous instruction. Please note that this behaviour only occurs if all of the following conditions <1> to <3> below apply:
Conditions:

<1> A power save mode (IDLE or STOP) is set while an instruction is executed in external memory
<2> The power save mode is released by an interrupt
<3> Interrupts are in the pending state when the power save mode is released and the next instruction is executed

Note that interrupts are held pending under any of the following conditions:

<1> The NP flag of the PSW register is 1 (NMI is beeing serviced or flag has been set by software)
<2> The ID flag of the PSW register is 1 (Interrupt is beeing serviced or DI instruction was executed or flag has been set by software)
<3> The EI (interrupt enable) state has been set during interrupt servicing in order to enable nested interrupts and an interrupt of the same or lower priority occurs.

The behaviour is shown below using the power save mode setting example from the user's manual.

(rD: PSC setting value, rX: Value written to PSC, rY Value written to PSC after power save mode)

```
ldsr  rX,5              ;set PSW to the value of rX
st.b  r0,PRCMD[r0]      ;Writes to PRCMD
st.b  rD,PSC[r0]        ;Sets the PSC register
ldsr  rY,5              ;set PSW to the value of rY
nop                     ;
nop                     ;
nop                     ;
nop                     ;
nop                     ;
(next instruction)      ;
nop                     ;
nop                     ;
nop                     ;
nop                     ;
nop                     ;
br    $+2               ; <2> eliminate PC discrepancy
 (next instruction)     ;
```

No. 13	continuing

Workaround

Please implement one of the following countermeasures

<1> Do not use power saving modes IDLE or STOP while an instruction is executed in external memory.

<2> Take the software countermeasures shown below:

1 Insert 6 NOP instructions 4 bytes after an instruction that writes to the PSC register.

2 Insert the br $+2 instruction after the NOP instructions to eliminate the PC discrepancy

Example

(rD: PSC setting value, rX: Value written to PSC, rY Value written to PSC after power save mode)

```
ldsr  rX,5              ;set PSW to the value of rX
st.b  r0,PRCMD[r0]  ;write to PRCMD
st.b  rD,PSC[r0]        ;Sets the PSC register
ldsr  rY,5              ;set PSW to value of rY (4 bytes)
nop                     ; <1> 6 or more nop instructions
nop                     ;
nop                     ;
nop                     ;
nop                     ;
nop                     ;
br    $+2               ; <2> eliminate PC discrepancy
 (next instruction)     ;
```

No. 14	Timer 0, 1, 7 one-shot pulse mode

Details

When using the software trigger for one-shot pulse mode function of timers 0, 1 or 7 the level of the timer input pin or its alternate function must not be changed. Because the external trigger is also enabled in this case the timer will inadvertently clear and start if the level of the TI pin or its alternate function is changed. This will cause a pulse to be output at an unintended timing.

No. 15	Restrictions on external clock

Details

The emulation board does not operate with the main or subclock signal supplied externally. Therefore use the clock signal supplied by the emulator.

No. 16	Emulation of ROM correction

Details

The ROM correction function of the device cannot be emulated.

No. 17	Oscillation stabilization time

Details

Emulation of the oscillation stabilization time is not possible.

No. 18	Interrupt request and STOP/IDLE mode

Details

The emulator may become deadlocked if the STOP or IDLE mode is set while the interrupt request flag for an interrupt that is not masked is set.

Workaround

Therefore do one of the following:

1.) Clear the interrupt request flag of the unmasked interrupt before setting the device to STOP or IDLE mode. If the device is inadvertently set to STOP or IDLE mode before the flag is cleared, forcibly break the program execution in the debugger and reset the emulator.

2.) If applicable do not allow to set the device to STOP or IDLE mode while the interrupt request flag for an unmasked interrupt is set.

No. 19	Change of the target CPU for emulation

Details

The emulation target CPUs have been changed from uPD70F3079Y, (for emulation of non-A products uPD70(F)307xY) to the uPD70F3079AY (for emulation of A-products uPD70(F)307xAY). Care must be taken because the initial value (after RESET) of the oscillation stabilization time selection register (OSTS) differs between the non-A-products (uPD70(F)307xY) and the A-products (uPD70(F)307xAY).

Inital value of OSTS:

1.) non-A-product: 0x04
2.) A-product: 0x01

This change has been introduced with control code version 'F'.

No. 20	HI-Z on CLKOUT pin

Details

The CLKOUT signal of the emulator cannot be set to high impedance state. In the A-version of the chip the CLKOUT pin can be set to Hi-Z output by setting the power save control register (PSC) accordingly. This is not possible in the emulation board: Even if the PSC register is configured to set CLKOUT to Hi-Z output (DCLK1 = 0 and DCLK0 = 1), the same operation as 'output enable' (DCLK1 = 0 and DCLK0 = 0) is performed.

No. 21	FCAN: Initialisations of Emulator before using FCAN

Details

a) Before startup of the debugger, supply power to pin VDD0 (GC-package: pin 8, GF-package: pin 11) on the target board.

b) Set memory mapping of the debugger as follows:
Attribute: Target memory
Mapping address: 0xnff800 to 0xnfffff (n = 3, 7, b)

c) Do not mask WAIT and HLDRQ when accessing the FCAN memory.

No. 22	FCAN: Message search

Details

This behaviour applies to devices containing 2 FCAN (uPD70F3079Y, uPD703079Y)
When both FCAN channels are used simultaneously, the receive data may be stored in an incorrect message buffer or destroyed (case a) or erroneous data may be inadvertently transmitted (case b).

a) When both FCAN channels are being used simultaneously, the following behaviour will occur if one FCAN module (e. g. FCAN 2) starts transmitting while the other FCAN module is in the process of receiving i. e. performing the acceptance filtering immediately after the EOF of the acknowledged frame.
This behaviour occurs in two different ways, depending on the setting of the last message buffer (buffer 31):

1 If the last message buffer (buffer 31) is set as a receive buffer:
The data received by FCAN 1 is stored in message buffer 31 instead of the message buffer it was intended to be received in. Because data is not stored in the correct buffer or the contents of message buffer 31 have been destroyed, a program malfunction may occur.

2 If the last message buffer (buffer 31) is set as a transmit buffer:
The data received by FCAN 1 is not stored in any message buffer and is therefor lost. A total network system malfunction may occur because the expected data is not received.

The behaviour described above occurs when both of the following conditions are met:

- Both FCAN channels are used simultaneously
- Mask 2 (M_CONFn.MT = 4) or mask 3 (M_CONFn.MT = 5) is set for the FCAN 1 message buffer, or when FCAN 1 receives a message with an incorrect identifier, even if mask 2 or
mask 3 has not been set for the FCAN 1 message buffer.

b) When both FCAN channels are being used simultaneously, if one FCAN module (FCAN 1) starts transmitting / receiving just before the other FCAN module (FCAN 2) starts transmitting, the data in the final message buffer (buffer 31) may be transmitted instead of the data that should be transmitted from FCAN 2. If the incorrect data is inadvertently transmitted in this way, a total network system error may occur.

The behaviour described above occurs when both of the following conditions are met:

- Both FCAN channels are used simultaneously
- More than two transmit requests exist for FCAN 2

No. 23	FCAN Main clock select

Details

The FCAN macro features a CAN Main Clock Select register (CGCS). The usage of the bit field "Memory Clock Prescaler" (MCP[3:0]) requires attention concerning a certain transition from one value to another value.
When the bit field MCP[3:0] in CGCS register has been set to "0", any further write operation to this bit field that changes the value again will result in a unexpected behavior of the FCAN macro. The FCAN macro will not operate anymore until an external reset is applied. This caution is already given in the user's manual. This description informs about further details.

Most, if not all applications, change the value of MCP only once after the start of the program. As after reset of the CPU the bit field MCP [3:0] is initialized to 5 these applications do not encounter any problems and existing program codes do not have to be changed.
Applications changing the MCP-value more than once during runtime of the program need to avoid to change the MCP-value again after the MCP-value has been set to"0" or in general apply only MCP-values not equal to "0". Otherwise a H/W reset needs to be issued in order to resume communication on the FCAN macro.

Please consider two cases:

- MCP written once after RESET
  The application needs to avoid the critical transition from MCP = 0 to MCP = <any other value>. The application has to write the target value once after reset and afterwards this value is not changed again.
- MCP written more than once after RESET
  Applications that need to change the MCP-value dynamically need to perform a H/W reset when the MCP-value reads 0 and again another value (not equal 0) shall become effective. In this case follow the first case MCP written once after RESET.

No. 24	External Bus Interface

Details

When the external bus interface is used, the values of the data lines may not be read correctly. Data from external memory may be overdriven by internal data.

No. 25	FCAN area access

Details

When an instruction to access the FCAN address area (xxnFF800H to xxnFFFFFH (n = 3, 7, or B)) is allocated to the emulation memory or target memory mapped to the external area and the instruction is executed, the FCAN register may not be able to be read (but it can be written).

Workaround

Allocate the instructions to access the FCAN address area to the internal ROM area.

This restriction only applies to control code H products.

This restriction has been corrected in control code J.

(C) Valid Specification

Item	Date pulished	Document No.	Document Title
1	September 2001	U15447EJ1V0UM00	IE-703079-MC-EM1 (User's Manual)
2	September 2003	U14665EJ4V0UD00	V850/SF1 User's Manual

(D) Direction of Use

No. 1	Reading FCAN registers

Details

This is additional information for chapter 18.16 Cautions on Use, paragraph <4> of User's Manual U14665EJ4V0UD.

Each register content of FCAN is copied to a buffer register during read access in order not to disturb the FCAN macro activity. So, the value being read from FCAN is the content of this buffer register.The actualization of this buffer register is done in two cases:

1. The read address is changed. A different FCAN register is read. So, different FCAN registers can be read without notice of this caution.
2. By reading the same FCAN register again, the actualization is done every second read access. So, the first, third, fifth and every continuous odd read access of the same register (without reading a different register in between) will deliver the actual FCAN register content.

Even a long time between two equal read accesses will not update the buffer register content.

A program using interrupt functions or a complex program structures could read the same FCAN register again without reading a different register in between.
If you are unsure if the register you want to read is directly read before, you should read a different register before (dummy read). After the read access to a different register, the desired register could be read and will deliver the atual FCAN register content. Please ensure, that no interrupt function with FCAN read access could disrupt this procedure.
The dummy read to a FCAN register should be a different register without changing anything inside the FCAN macro. E.g. the CANn bus active register (CnBA) could be read before reading a different register.

(E) Revision History

Item	Date pulished	Document No.	Comment
1	May 15, 2000	TPS-HE-B-2760	First release
2	July 13, 2000	TPS-HE-B-2761	added V1.02
3	Jan 4, 2001	TPS-HE-B-2762	added V1.03 added operating precautions 8 to 13 added section c: 'additional cautions'
4	Mar 21, 2001	TPS-HE-B-2763	added V1.04 added operating precautions 14,15 modified operating precautions 11,13
5	Nov 29, 2001	TPS-HE-B-2764	added V1.24 added operating precautions 16 to 21
6	May 14, 2002	TPS-HE-B-2765	added V1.34 changed to new format, included section c 'additional cautions' to section b 'description of operating precautions' corrected several typos
7	Sep 26, 2002	TPS-HE-B-2766	added operating precaution 23 added new disclaimer
8	June 18, 2003	TPS-HE-B-2767	added V1.44 added new disclaimer added operating precaution 24 removed and added precautions
9	June 22, 2004	TPS-HE-B-2768	added V1.55 modified disclaimer added operating precaution 25