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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A0064A/E	Rev.	1.00
Title	Note on IO0FV[1:0] bits of the SPI Multi I/O Bus Controller of RZ/A2M Group Products		Information Category	Technical Notification		
Applicable Product	RZ/A2M Group	Lot No. All	Reference Document	RZ/A2M Group User's Manual: Hardware Rev.3.00 (R01UH0746EJ0300)		

This document is a cautionary note regarding IO0FV[1:0] bits in the Common Control Register (CMNCR) of the SPI Multi I/O Bus Controller in products of the RZ/A2M Groups.

[Description of the IO0FV[1:0] bits]

Bit	Bit Name	Initial Value	R/W	Description
9, 8	IO0FV[1:0]	11	R/W	QSPIn_IO0 Fixed Value for 1-bit Size Fixes the output value of QSPIn_IO0 pin for 1-bit size. 00 : The output value is 0. 01 : The output value is 1. 10 : The output value is that of the last bit in the previous transfer (the pin is placed in the Hi-Z state if that was the case in the previous transfer). 11 : The pin is placed in the Hi-Z state. Note. Set these bits to 11 (the pin is placed in the Hi-Z state) when data read transfer size is not 1-bit.