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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RZ*-A021A/E	Rev.	1.00
Title	Ethernet MAC reception issue in case TCPIP accelerator enabled		Information Category	Technical Notification		
Applicable Product	RZ/T1 GROUP	Lot No. All lots	Reference Document	RZ/T1 Group User's Manual: Hardware Rev1.2 R01UH0483EJ0120		

This document describes information about issues of Ethernet MAC in case TCPIP accelerator is used. Please use the Ethernet MAC considering those issues.

1 Issues

1.1 Reception issue in case Rx FIFO overflow is occurred

1.1.1 Contents

- It is possible that error information which is related to the previous error frame is included in frame information of normal reception frame.
- It is possible that abnormal frame which caused Rx FIFO overflow is regarded as normal frame because of illegal value is included in frame information

1.1.2 Condition

In case Rx FIFO overflow is occurred when Rx TCPIP accelerator is enabled.

1.2 Reception issue of frame more than 64 bytes with padding

1.2.1 Contents

It is possible that reception word size (RX_WORD[12:0]) in the frame information increases by 1 word (4 bytes) or decreases by 1 word compared with correct size. In case of decrease by 1 word, it is possible that RX_WORD indicates the size which causes lack of IP packet. IP packet itself is NOT lacked.

1.2.2 Conditions

In case all the following conditions are met,

(A) RX TCPIP accelerator enabled

(B) Reception frame meets all the following conditions;

(1) Frame size including FCS is more than 64 bytes.

(2) TCP/IP or UDP/IP packet is included.

(3) Padding (Trailer) is included between IP packet and FCS.

2 Workaround

2.1 Workaround for reception issue in case Rx FIFO overflow is occurred

Any of the following methods should be applied.

(A) Disable Rx TCPIP accelerator.

In detail, clear bit0 of GMAC_ACC register.

(B) When Rx FIFO is overflowed, discard all frames left in Rx FIFO and Buffer RAM. Specifically, apply the following procedure;

(1) Disable Rx MAC.

(2) Discard all frames left in Rx FIFO.

(3) Discard all frames left in Buffer RAM.

(4) Enable Rx MAC.

(5) Discard at least one frame with BUFID VALID bit = 1. This is because FIFO empty state can be read even if the frame which caused FIFO overflow remains in the FIFO. Receive normal frame once and discard remained abnormal frame with it.

Fig1~4 are the flowcharts of workaround described above.

- In case of products of R-IN engine incorporated and using HW-RTOS

  Fig1: Flowchart of RX FIFO overflow processing task

  Fig2: Flowchart of Reception processing task

✓ Create overflow processing task with higher priority than one of reception processing task ✓ Start overflow task by HWISR combined with FIFO overflow interrupt ✓ Discard the abnormal frame remained in the FIFO by HWISR combined with reception interrupt

- In case of products of R-IN engine not-incorporated or products of R-IN engine incorporated and not using HW-RTOS

  Fig3: Flowchart of RX FIFO overflow processing

  Fig4: Flowchart of Reception processing

✓ The abnormal frame remained in the FIFO is discarded in reception processing. Discard valid data once when overflow return flag is set. ✓ Overflow interrupt is disabled from reading BUFID till checking overflow return flag

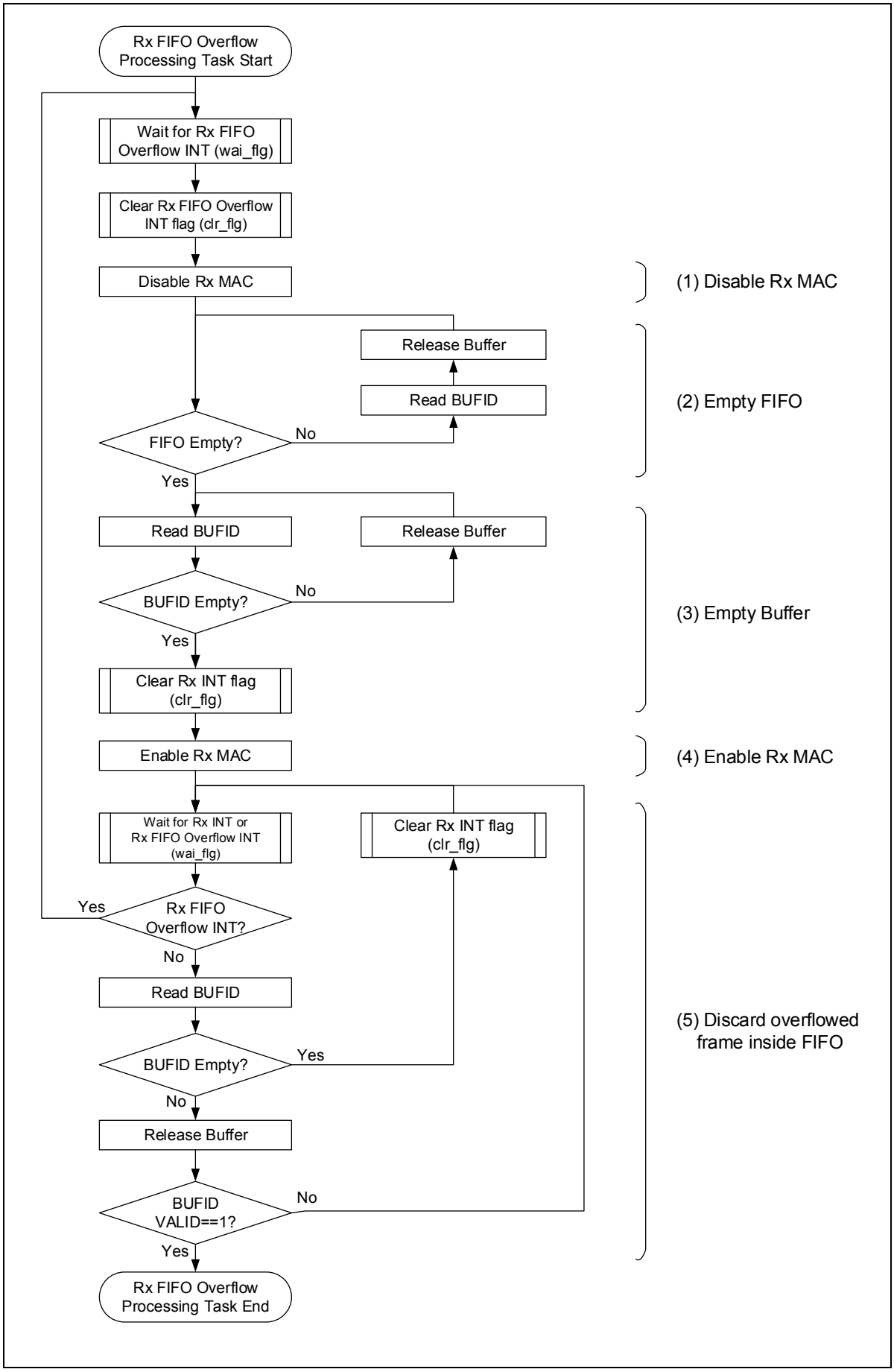

Fig1: Flowchart of RX FIFO overflow processing task (In case of using HW-RTOS)

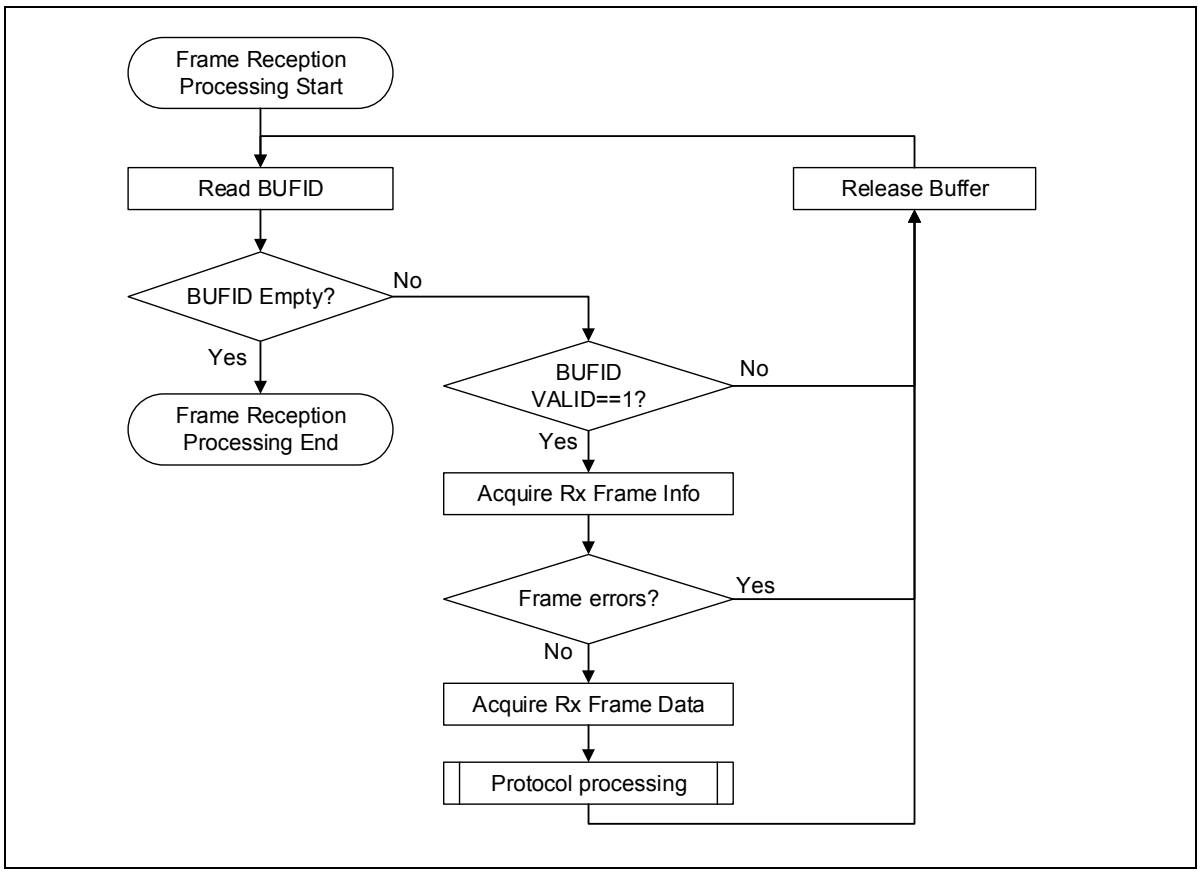

Fig2: Flowchart of Reception processing task (In case of using HW-RTOS)

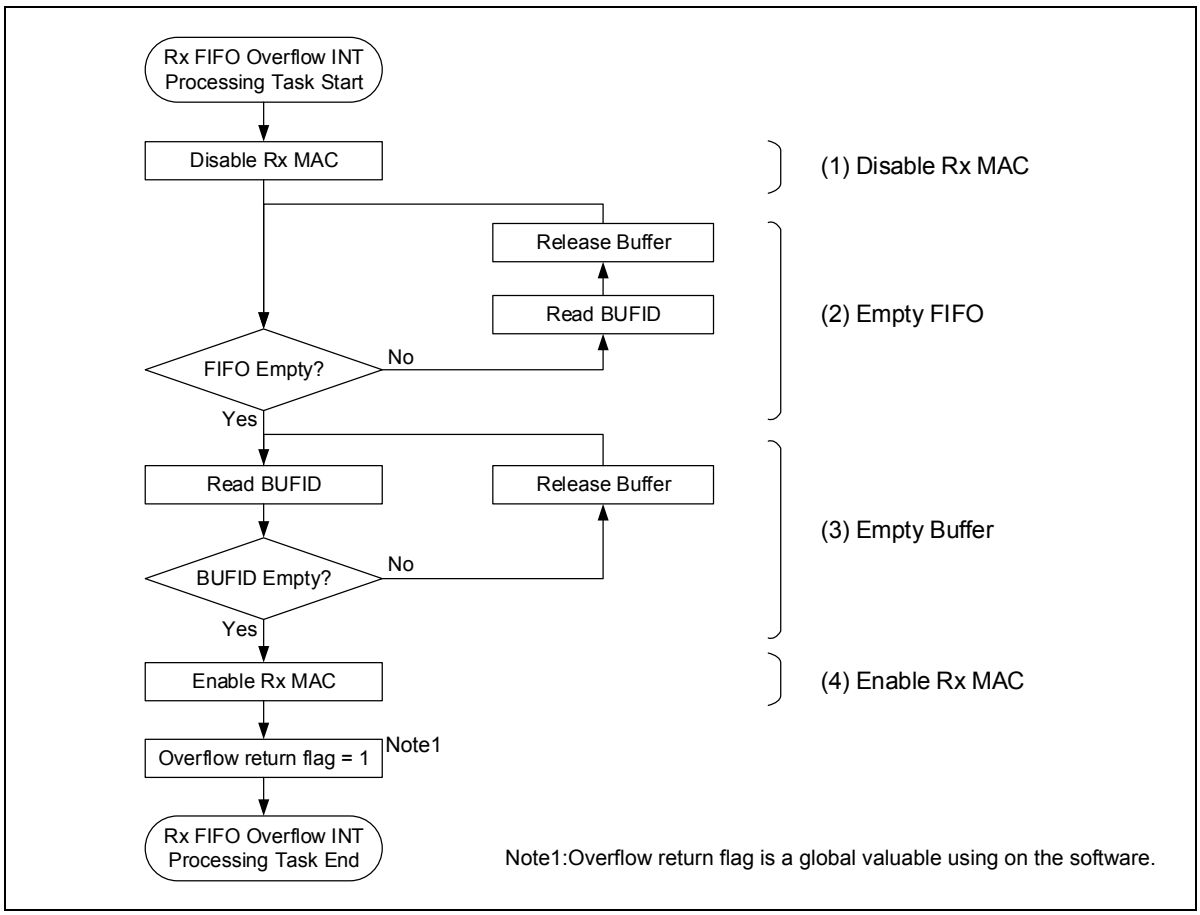

Fig3: Flowchart of RX FIFO overflow processing (In case of not using HW-RTOS)

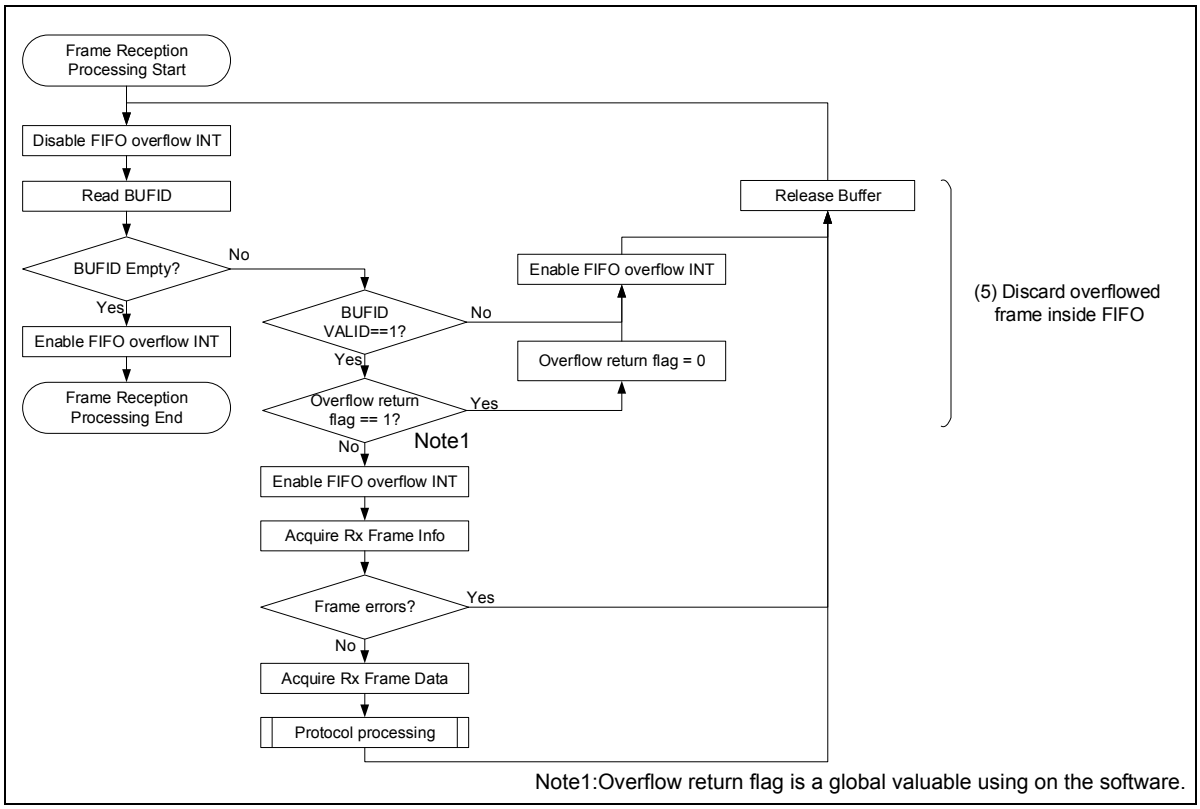

Fig4: Flowchart of Reception processing (In case of not using HW-RTOS)

2.2 Workaround for reception issue of frame more than 64 bytes with padding

Any of the following methods should be applied.

(A) Disable Rx TCPIP accelerator or checksum support for the RXTCPIP accelerator.

In detail, clear bit0 or set bit2 of GMAC_ACC register.

(B) In order to avoid lack of the IP packet, increase reception word size by 1 and transfer the size to protocol stack. In the protocol stack, payload data should be extracted based on size of Total Length field in IP header and the rest data should be discarded. Fig 5 is the flowchart of this workaround.

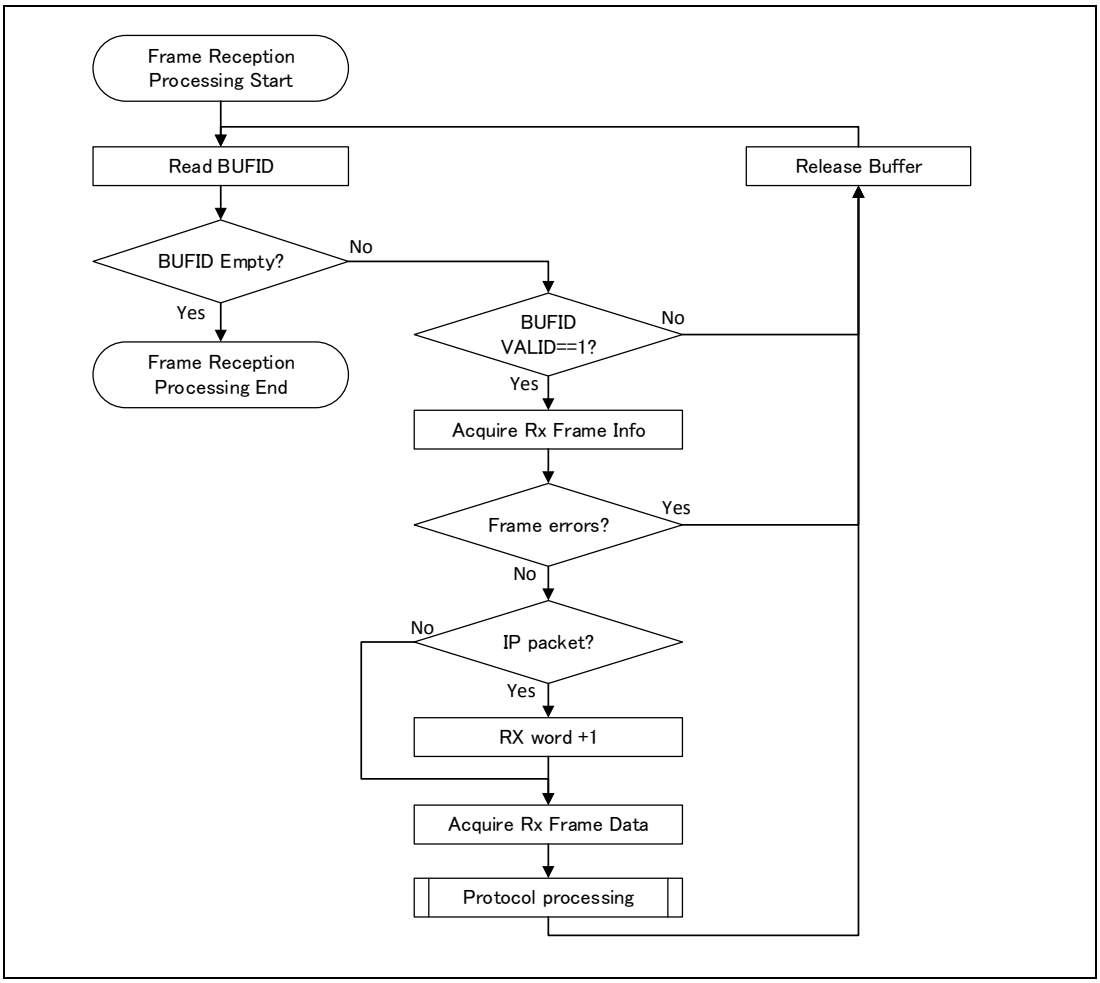

Fig 5: Flowchart of Reception processing

3 Update Plan

Renesas will update User's Manual Hardware and Ethernet MAC driver which are improved based the workaround on Renesas Web site.

[RZ/T1 sample software download site]

https://www.renesas.com/ja-jp/products/microcontrollers-microprocessors/rz/rzt/rzt1.html#

[Sample software related to this issues]

Target	Issue Date
TCP/IP, UDP/IP	February, 2017
Modbus TCP/RTU/ASCII	February, 2017
RZ/T1 Group User's Manual Hardware Rev1.3	March, 2017