Date: Jan. 20, 2023

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RL*-A0119A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/I1C Descriptions in the User's Manual: Hardware Rev. 2.11 Changed		Information Category	Technical Notification		
Applicable Product	RL78/I1C Group	Lot No. All lots	Reference Document	RL78/I1C User's Manual: Hardware Rev. 2.11 R01UH0587EJ0211 (Nov. 2022)		

This document describes misstatements found in the RL78/I1C User's Manual: Hardware Rev. 2.11 (R01UH0587EJ0211).

Corrections

Applicable Item	Applicable Page	Contents
41.3.2 Supply current characteristics	Page 1134 to Page 1139	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0587EJ0211	
1	41.3.2 Supply current characteristics		Page 1134 to Page 1139	Page 3 to Page 7

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/I1C Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0119A/E	Jan. 20, 2023	First edition issued Corrections No.1 revised (this document)

1. 41.3.2 Supply current characteristics (Page 1134 to Page 1139)

Incorrect:

41.3.2 Supply current characteristics

(T_A = −40 to +85° C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note8] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0V) (1/6)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (high-speed main) mode[Note 5]	f_{CLK} = 32 MHz[Note 3] PLL operation	Normal operation	V_{DD} = 5.0 V		5.2	8.5	mA
						V_{DD} = 3.0 V		5.2	8.5	mA
				f_{IH} = 24 MHz[Note 3]	Basic operation	V_{DD} = 5.0 V		1.7		mA
				f_{IL} = 15 kHz, T_A =+ 25°C [Note 7]	Normal operation			4.1	11.0	µA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, ΔΣA/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors.** When the VBAT pin (pin for battery backup) is selected, current flowing into VBAT.

2. When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

3. When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

4. When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1). **However, not including the current flowing into independent power supply RTC, 12-bit interval timer, and watchdog timer.**

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high-speed main) mode: 2.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
2.5 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 12 MHz
2.1 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 6 MHz
LS (low-speed main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LP (low-power main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz
LV (low-voltage main) mode: 1.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz

Correct:

41.3.2 Supply current characteristics

(T_A = −40 to +85° C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note8] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0V) (1/6)

Parameter	Symbol	Conditions					MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD1}	Operating mode	HS (high-speed main) mode[Note 5]	f_{CLK} = 32 MHz[Note 3] PLL operation	Normal operation	V_{DD} = 5.0 V		5.2	8.5	mA
						V_{DD} = 3.0 V		5.2	8.5	mA
				f_{IH} = 24 MHz[Note 3]	Basic operation	V_{DD} = 5.0 V		1.7		mA
				f_{IL} = 15 kHz, T_A =+ 25°C [Note 7]	Normal operation			4.1	11.0	µA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS} . When the VBAT pin (pin for battery backup) is selected, current flowing into VBAT. The following points apply in the HS (high-speed main), LS (low-speed main), LV (low-voltage main), and LP (low-power main) modes.
- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into the LCD controller/driver, A/D converter, ΔΣA/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the independent power supply RTC.

2. When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

3. When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

4. When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped. When setting ultra-low current consumption (AMPHS1 = 1).

6. When high-speed on-chip oscillator, low-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.
7. When high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.
8. Either V_{DD} or VBAT is selected by the battery backup function.

Remarks
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{IM}: Middle-speed on-chip oscillator clock frequency
4. f_{IL}: Low-speed on-chip oscillator clock frequency
5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

5. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
   HS (high-speed main) mode: 2.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
   2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
   2.5 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
   2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 12 MHz
   2.1 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 6 MHz
   LS (low-speed main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
   LP (low-power main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz
   LV (low-voltage main) mode: 1.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz
6. When high-speed on-chip oscillator, low-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.
7. When high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.
8. Either V_{DD} or VBAT is selected by the battery backup function.

Remarks
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{IM}: Middle-speed on-chip oscillator clock frequency
4. f_{IL}: Low-speed on-chip oscillator clock frequency
5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = −40 to +85° C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note10] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0V) (3/6)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	HS (high-speed main) mode[Note 7]	f_{CLK} = 32 MHz[Note 4], PLL operation	V_{DD} = 5.0 V		0.80	2.0	mA
					V_{DD} = 3.0 V		0.80	2.0	mA
				f_{IH} = 24 MHz[Note 4]	V_{DD} = 5.0 V		0.48	1.45	mA
					V_{DD} = 3.0 V		0.48	1.45	mA
				f_{IH} = 12 MHz[Note 4]	V_{DD} = 5.0 V		0.37	0.91	mA
					V_{DD} = 3.0 V		0.37	0.91	mA
				f_{IH} = 6 MHz[Note 4]	V_{DD} = 5.0 V		0.32	0.63	mA
					V_{DD} = 3.0 V		0.32	0.63	mA
				f_{IH} = 3 MHz[Note 4]	V_{DD} = 5.0 V		0.29	0.49	mA
					V_{DD} = 3.0 V		0.29	0.49	mA
			LS (low-speed main) mode[Note 7]	f_{IH} = 8 MHz[Note 4]	V_{DD} = 3.0 V		280	740	μA
					V_{DD} = 2.0 V		280	740	μA
				f_{IH} = 6 MHz[Note 4]	V_{DD} = 3.0 V		230	620	μA
					V_{DD} = 2.0 V		230	620	μA
				f_{IH} = 4 MHz[Note 4]	V_{DD} = 3.0 V		220	440	μA
					V_{DD} = 2.0 V		220	440	μA
				f_{IM} = 4 MHz[Note 9]	V_{DD} = 3.0 V		55	300	μA
					V_{DD} = 2.0 V		55	300	μA
				f_{IH} = 3 MHz[Note 4]	V_{DD} = 3.0 V		200	534	μA
					V_{DD} = 2.0 V		200	534	μA
			LV (low-voltage main) mode[Note 7]	f_{IH} = 4 MHz[Note 4]	V_{DD} = 3.0 V		450	825	μA
					V_{DD} = 2.0 V		450	825	μA
			LP (low-power main) mode[Note 7]	f_{IH} = 1 MHz[Note 4]	V_{DD} = 3.0 V		195	400	μA
					V_{DD} = 2.0 V		195	400	μA
				f_{IM} = 1 MHz[Note 9]	V_{DD} = 3.0 V		33	100	μA
					V_{DD} = 2.0 V		33	100	μA
			HS (high-speed main) mode[Note 7]	f_{MX} = 20 MHz[Note 3], V_{DD} = 5.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA

(T_A = −40 to +85° C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD}[Note10] ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0V) (3/6)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current[Note 1]	I_{DD2}[Note 2]	HALT mode	HS (high-speed main) mode[Note 7]	f_{CLK} = 32 MHz[Note 4], PLL operation	V_{DD} = 5.0 V		0.80	2.0	mA
					V_{DD} = 3.0 V		0.80	2.0	mA
				f_{IH} = 24 MHz[Note 4]	V_{DD} = 5.0 V		0.48	1.45	mA
					V_{DD} = 3.0 V		0.48	1.45	mA
				f_{IH} = 12 MHz[Note 4]	V_{DD} = 5.0 V		0.37	0.91	mA
					V_{DD} = 3.0 V		0.37	0.91	mA
				f_{IH} = 6 MHz[Note 4]	V_{DD} = 5.0 V		0.32	0.63	mA
					V_{DD} = 3.0 V		0.32	0.63	mA
				f_{IH} = 3 MHz[Note 4]	V_{DD} = 5.0 V		0.29	0.49	mA
					V_{DD} = 3.0 V		0.29	0.49	mA
			LS (low-speed main) mode[Note 7]	f_{IH} = 8 MHz[Note 4]	V_{DD} = 3.0 V		280	740	μA
					V_{DD} = 2.0 V		280	740	μA
				f_{IH} = 6 MHz[Note 4]	V_{DD} = 3.0 V		230	620	μA
					V_{DD} = 2.0 V		230	620	μA
				f_{IH} = 4 MHz[Note 4]	V_{DD} = 3.0 V		220	440	μA
					V_{DD} = 2.0 V		220	440	μA
				f_{IM} = 4 MHz[Note 5]	V_{DD} = 3.0 V		55	300	μA
					V_{DD} = 2.0 V		55	300	μA
				f_{IH} = 3 MHz[Note 4]	V_{DD} = 3.0 V		200	534	μA
					V_{DD} = 2.0 V		200	534	μA
			LV (low-voltage main) mode[Note 7]	f_{IH} = 4 MHz[Note 4]	V_{DD} = 3.0 V		450	825	μA
					V_{DD} = 2.0 V		450	825	μA
			LP (low-power main) mode[Note 7]	f_{IH} = 1 MHz[Note 4]	V_{DD} = 3.0 V		195	400	μA
					V_{DD} = 2.0 V		195	400	μA
				f_{IM} = 1 MHz[Note 5]	V_{DD} = 3.0 V		33	100	μA
					V_{DD} = 2.0 V		33	100	μA
			HS (high-speed main) mode[Note 7]	f_{MX} = 20 MHz[Note 3], V_{DD} = 5.0 V	Square wave input		0.31	1.08	mA
					Resonator connection		0.48	1.28	mA

(T_A = −40 to +85° C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 10 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0V) (4/6)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 5, T_A = −40°C	Square wave input		0.80	1.60	μA
					Resonator connection		1.00	1.80	μA
				f_{SUB} = 32.768 kHz Note 5, T_A = +25°C	Square wave input		0.93	1.70	μA
					Resonator connection		1.13	1.90	μA
				f_{SUB} = 32.768 kHz Note 5, T_A = +50°C	Square wave input		1.10	3.00	μA
					Resonator connection		1.30	3.20	μA
				f_{SUB} = 32.768 kHz Note 5, T_A = +70°C	Square wave input		1.50	5.00	μA
					Resonator connection		1.70	5.20	μA
				f_{SUB} = 32.768 kHz Note 5, T_A = +85°C	Square wave input		2.80	9.00	μA
					Resonator connection		3.00	9.20	μA
				f_{IL} = 15 kHz Note 9, T_A = −40°C			0.78	1.60	μA
									μA
				f_{IL} = 15 kHz Note 9, T_A = +25°C			1.01	1.76	μA
									μA
				f_{IL} = 15 kHz Note 9, T_A = +85°C			2.25	8.45	μA
									μA
	I_{DD3} Note 6	STOP mode Note 8	T_A = −40°C				0.47	0.90	μA
			T_A = +25°C				0.65	1.20	μA
			T_A = +50°C				0.84	2.80	μA
			T_A = +70°C				1.21	4.70	μA
			T_A = +85°C				1.82	9.00	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. **The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the LCD controller/driver, A/D converter, ΔΣA/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors.** When the VBAT pin (pin for battery backup) is selected, current flowing into VBAT.

2. During HALT instruction execution by flash memory.

3. When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

4. When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and Subsystem clock are stopped.

(T_A = −40 to +85° C, 1.7 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} Note 10 ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0V) (4/6)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	LS (low-speed main) mode Note 7	f_{MX} = 8 MHz Note 3, V_{DD} = 3.0 V	Square wave input		110	360	μA
					Resonator connection		160	420	μA
			Subsystem clock operation	f_{SUB} = 32.768 kHz Note 6, T_A = −40°C	Square wave input		0.80	1.60	μA
					Resonator connection		1.00	1.80	μA
				f_{SUB} = 32.768 kHz Note 6, T_A = +25°C	Square wave input		0.93	1.70	μA
					Resonator connection		1.13	1.90	μA
				f_{SUB} = 32.768 kHz Note 6, T_A = +50°C	Square wave input		1.10	3.00	μA
					Resonator connection		1.30	3.20	μA
				f_{SUB} = 32.768 kHz Note 6, T_A = +70°C	Square wave input		1.50	5.00	μA
					Resonator connection		1.70	5.20	μA
				f_{SUB} = 32.768 kHz Note 6, T_A = +85°C	Square wave input		2.80	9.00	μA
					Resonator connection		3.00	9.20	μA
				f_{IL} = 15 kHz Note 9, T_A = −40°C			0.78	1.60	μA
									μA
				f_{IL} = 15 kHz Note 9, T_A = +25°C			1.01	1.76	μA
									μA
				f_{IL} = 15 kHz Note 9, T_A = +85°C			2.25	8.45	μA
									μA
	I_{DD3}	STOP mode Note 8	T_A = −40°C				0.47	0.90	μA
			T_A = +25°C				0.65	1.20	μA
			T_A = +50°C				0.84	2.80	μA
			T_A = +70°C				1.21	4.70	μA
			T_A = +85°C				1.82	9.00	μA

Notes 1. Total current flowing into V_{DD}, EV_{DD}, and V_{RTC} including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD} or V_{SS}, EV_{SS}. When the VBAT pin (pin for battery backup) is selected, current flowing into VBAT. The following points apply in the HS (high-speed main), LS (low-speed main), LV (low-voltage main), and LP (low-power main) modes.

- The currents in the “TYP.” column do not include the operating currents of the peripheral modules.
- The currents in the “MAX.” column include the operating currents of the peripheral modules, except for those flowing into LCD controller/driver, the A/D converter, ΔΣA/D converter, LVD circuit, battery backup circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules. However, in HALT mode, including the current flowing into the independent power supply RTC.

In the STOP mode, the currents in both the “TYP.” and “MAX.” columns do not include the operating currents of the peripheral modules.

5. When operating independent power supply RTC and setting ultra-low current consumption (AMPHS1 = 1). When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped. **However, not including the current flowing into the 12-bit interval timer and watchdog timer. When high-speed on-chip oscillator and high-speed system clock are stopped**.
6. **When high-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. However, not including the current flowing into independent power supply RTC, 12-bit interval timer, and watchdog timer.**
7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

   HS (high-speed main) mode: 2.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
   2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
   2.5 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
   2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 12 MHz
   2.1 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 6 MHz
   LS (low-speed main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
   LP (low-power main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz
   LV (low-voltage main) mode: 1.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz
8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.
9. When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.
10. Either V_{DD} or VBAT is selected by the battery backup function.

Remarks
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{IM}: Middle-speed on-chip oscillator clock frequency
4. f_{IL}: Low-speed on-chip oscillator clock frequency
5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

2. During HALT instruction execution by flash memory.
3. When high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and clock are stopped.
4. When high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
5. When high-speed on-chip oscillator, low-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.
6. When operating independent power supply RTC and setting ultra-low current consumption (AMPHS1 = 1). When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.
7. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

   HS (high-speed main) mode: 2.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
   2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 24 MHz
   2.5 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
   2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 12 MHz
   2.1 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 6 MHz
   LS (low-speed main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
   LP (low-power main) mode: 1.9 V ≤ V_{DD} ≤ 5.5 V@1 MHz
   LV (low-voltage main) mode: 1.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz
8. If operation of the subsystem clock when STOP mode, same as when HALT mode of subsystem clock operation.
9. When high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.
10. Either V_{DD} or VBAT is selected by the battery backup function.

Remarks
1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
2. f_{IH}: High-speed on-chip oscillator clock frequency
3. f_{IM}: Middle-speed on-chip oscillator clock frequency
4. f_{IL}: Low-speed on-chip oscillator clock frequency
5. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C