

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	MPU/MCU		Document No.	TN-RL*-A0113A/E	Rev.	1.00
Title	Correction for Incorrect Description Notice RL78/G11 Descriptions in the User's Manual: Hardware Rev. 2.40 Changed		Information Category	Technical Notification		
Applicable Product	RL78/G11 Group	Lot No.	Reference Document	RL78/G11 User's Manual: Hardware Rev. 2.40 R01UH0637EJ0240 (Oct.2020)		
		All lots				

This document describes misstatements found in the RL78/G11 User's Manual: Hardware Rev. 2.40 (R01UH0637EJ0240).

Corrections

Applicable Item	Applicable Page	Contents
35.3.2 Supply current characteristics	Page 1006 to Page.1010	Incorrect descriptions revised
36.3.2 Supply current characteristics	Page 1072 to Page.1074	Incorrect descriptions revised

Document Improvement

The above corrections will be made for the next revision of the User's Manual: Hardware.

Corrections in the User's Manual: Hardware

No.	Corrections and Applicable Items			Pages in this document for corrections
	Document No.	English	R01UH0637EJ0240	
1	35.3.2 Supply current characteristics		Page 1006 to Page.1010	Page 3 to Page 6
2	36.3.2 Supply current characteristics		Page 1072 to Page.1074	Page 7 to Page 9

Incorrect: Bold with underline; Correct: Gray hatched

Revision History

RL78/G11 Correction for incorrect description notice

Document Number	Issue Date	Description
TN-RL*-A0113A/E	Jan. 20, 2023	First edition issued Corrections No.1 to No.2 revised (this document)

1. 35.3.2 Supply current characteristics (Page 1006 to Page.1010)

Incorrect:

35.3.2 Supply current characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = 0\text{ V}$)

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Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	I _{DD1}	Operating mode	Basic operation	HS (high-speed main) mode	f _{HOCO} = 48 MHz ^{Note 3} f _{HI} = 24 MHz ^{Note 3}	V _{DD} = 5.0 V		1.7		mA	
					V _{DD} = 3.0 V		1.7				
				f _{HOCO} = 24 MHz ^{Note 3} f _{HI} = 24 MHz ^{Note 3}	V _{DD} = 5.0 V		1.4				
				V _{DD} = 3.0 V		1.4					
				Normal operation	HS (high-speed main) mode	f _{HOCO} = 48 MHz ^{Note 3} f _{HI} = 24 MHz ^{Note 3}	V _{DD} = 5.0 V		3.5	6.9	mA
						V _{DD} = 3.0 V		3.5	6.9		
			f _{HOCO} = 24 MHz ^{Note 3} f _{HI} = 24 MHz ^{Note 3}			V _{DD} = 5.0 V		3.2	6.3		
			V _{DD} = 3.0 V				3.2	6.3			
			Normal operation	LS (low-speed main) mode (MCSEL = 0)	f _{HI} = 8 MHz ^{Note 3}	V _{DD} = 5.0 V		2.4	4.6	mA	
						V _{DD} = 3.0 V		2.4	4.6		
			Normal operation	LS (low-speed main) mode (MCSEL = 1)	f _{HI} = 4 MHz ^{Note 3}	V _{DD} = 3.0 V		0.72	1.3	mA	
						V _{DD} = 2.0 V		0.72	1.3		
					f _{IM} = 4 MHz ^{Note 6}	V _{DD} = 3.0 V		0.58	1.1		
						V _{DD} = 2.0 V		0.58	1.1		
			Normal operation	LV (low-voltage main) mode	f _{HI} = 4 MHz ^{Note 3}	V _{DD} = 3.0 V		1.2	1.8	mA	
						V _{DD} = 2.0 V		1.2	1.8		
			Normal operation	LP (low-power main) mode (MCSEL = 1)	f _{HI} = 1 MHz ^{Note 3}	V _{DD} = 3.0 V		290	480	μA	
						V _{DD} = 2.0 V		290	480		
					f _{IM} = 1 MHz ^{Note 6}	V _{DD} = 3.0 V		124	230		
						V _{DD} = 2.0 V		124	230		
			Normal operation	HS (high-speed main) mode	f _{MAX} = 20 MHz ^{Note 2}	V _{DD} = 5.0 V	Square wave input		2.7	5.3	mA
							Resonator connection		2.8	5.5	
						V _{DD} = 3.0 V	Square wave input		2.7	5.3	
							Resonator connection		2.8	5.5	
f _{MAX} = 10 MHz ^{Note 2}	V _{DD} = 5.0 V	Square wave input					1.8	3.1			
		Resonator connection					1.9	3.2			
	V _{DD} = 3.0 V	Square wave input				1.8	3.1				
		Resonator connection				1.9	3.2				
Normal operation	LS (low-speed main) mode (MCSEL = 0)	f _{MAX} = 8 MHz ^{Note 2}			V _{DD} = 3.0 V	Square wave input		0.9	1.9	mA	
						Resonator connection		1.0	2.0		
Normal operation	LS (low-speed main) mode (MCSEL = 1)	f _{MAX} = 8 MHz ^{Note 2}			V _{DD} = 2.0 V	Square wave input		0.9	1.9	mA	
						Resonator connection		1.0	2.0		
Normal operation	LS (low-speed main) mode (MCSEL = 1)	f _{MAX} = 4 MHz ^{Note 2}	V _{DD} = 3.0 V	Square wave input		0.6	1.1	mA			
				Resonator connection		0.6	1.2				
Normal operation	LS (low-speed main) mode (MCSEL = 1)	f _{MAX} = 4 MHz ^{Note 2}	V _{DD} = 2.0 V	Square wave input		0.6	1.1	mA			
				Resonator connection		0.6	1.2				
Normal operation	LP (low-power main) mode (MCSEL = 1)	f _{MAX} = 1 MHz ^{Note 2}	V _{DD} = 3.0 V	Square wave input		100	190	μA			
				Resonator connection		145	250				
Normal operation	LP (low-power main) mode (MCSEL = 1)	f _{MAX} = 1 MHz ^{Note 2}	V _{DD} = 2.0 V	Square wave input		100	190	μA			
				Resonator connection		145	250				

Correct:

35.3.2 Supply current characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $1.6\text{ V} \leq \text{EVDD0} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = 0\text{ V}$)

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Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	I _{DD1}	Operating mode	Basic operation	HS (high-speed main) mode	f _{HOCO} = 48 MHz ^{Note 3} f _{HI} = 24 MHz ^{Note 3}	V _{DD} = 5.0 V		1.7		mA	
					V _{DD} = 3.0 V		1.7				
				f _{HOCO} = 24 MHz ^{Note 3} f _{HI} = 24 MHz ^{Note 3}	V _{DD} = 5.0 V		1.4				
				V _{DD} = 3.0 V		1.4					
				Normal operation	HS (high-speed main) mode	f _{HOCO} = 48 MHz ^{Note 3} f _{HI} = 24 MHz ^{Note 3}	V _{DD} = 5.0 V		3.5	6.9	mA
						V _{DD} = 3.0 V		3.5	6.9		
			f _{HOCO} = 24 MHz ^{Note 3} f _{HI} = 24 MHz ^{Note 3}			V _{DD} = 5.0 V		3.2	6.3		
			V _{DD} = 3.0 V				3.2	6.3			
			Normal operation	LS (low-speed main) mode (MCSEL = 0)	f _{HI} = 8 MHz ^{Note 3}	V _{DD} = 5.0 V		2.4	4.6	mA	
						V _{DD} = 3.0 V		2.4	4.6		
			Normal operation	LS (low-speed main) mode (MCSEL = 1)	f _{HI} = 4 MHz ^{Note 3}	V _{DD} = 3.0 V		0.72	1.3	mA	
						V _{DD} = 2.0 V		0.72	1.3		
					f _{IM} = 4 MHz ^{Note 6}	V _{DD} = 3.0 V		0.58	1.1		
						V _{DD} = 2.0 V		0.58	1.1		
			Normal operation	LV (low-voltage main) mode	f _{HI} = 4 MHz ^{Note 3}	V _{DD} = 3.0 V		1.2	1.8	mA	
						V _{DD} = 2.0 V		1.2	1.8		
			Normal operation	LP (low-power main) mode (MCSEL = 1)	f _{HI} = 1 MHz ^{Note 3}	V _{DD} = 3.0 V		290	480	μA	
						V _{DD} = 2.0 V		290	480		
					f _{IM} = 1 MHz ^{Note 6}	V _{DD} = 3.0 V		124	230		
						V _{DD} = 2.0 V		124	230		
			Normal operation	HS (high-speed main) mode	f _{MAX} = 20 MHz ^{Note 2}	V _{DD} = 5.0 V	Square wave input		2.7	5.3	mA
							Resonator connection		2.8	5.5	
						V _{DD} = 3.0 V	Square wave input		2.7	5.3	
							Resonator connection		2.8	5.5	
f _{MAX} = 10 MHz ^{Note 2}	V _{DD} = 5.0 V	Square wave input					1.8	3.1			
		Resonator connection					1.9	3.2			
	V _{DD} = 3.0 V	Square wave input				1.8	3.1				
		Resonator connection				1.9	3.2				
Normal operation	LS (low-speed main) mode (MCSEL = 0)	f _{MAX} = 8 MHz ^{Note 2}			V _{DD} = 3.0 V	Square wave input		0.9	1.9	mA	
						Resonator connection		1.0	2.0		
Normal operation	LS (low-speed main) mode (MCSEL = 1)	f _{MAX} = 8 MHz ^{Note 2}			V _{DD} = 2.0 V	Square wave input		0.9	1.9	mA	
						Resonator connection		1.0	2.0		
Normal operation	LS (low-speed main) mode (MCSEL = 1)	f _{MAX} = 4 MHz ^{Note 2}	V _{DD} = 3.0 V	Square wave input		0.6	1.1	mA			
				Resonator connection		0.6	1.2				
Normal operation	LS (low-speed main) mode (MCSEL = 1)	f _{MAX} = 4 MHz ^{Note 2}	V _{DD} = 2.0 V	Square wave input		0.6	1.1	mA			
				Resonator connection		0.6	1.2				
Normal operation	LP (low-power main) mode (MCSEL = 1)	f _{MAX} = 1 MHz ^{Note 2}	V _{DD} = 3.0 V	Square wave input		100	190	μA			
				Resonator connection		145	250				
Normal operation	LP (low-power main) mode (MCSEL = 1)	f _{MAX} = 1 MHz ^{Note 2}	V _{DD} = 2.0 V	Square wave input		100	190	μA			
				Resonator connection		145	250				

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

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(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

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Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
		Operating mode	Normal operation	Subsystem clock operation	f _{IL} = 15 kHz, T _A = -40°C Note 5	Normal operation					
Supply current Note 1	I _{DD1}				f _{IL} = 15 kHz, T _A = -40°C Note 5	Normal operation		1.8	5.9	μA	
					f _{IL} = 15 kHz, T _A = +25°C Note 5	Normal operation		1.9	5.9		
					f _{IL} = 15 kHz, T _A = +85°C Note 5	Normal operation		2.3	8.7		

Parameter	Symbol	Conditions						MIN.	TYP.	MAX.	Unit
		Operating mode	Normal operation	Subsystem clock operation	f _{IL} = 15 kHz, T _A = -40°C Note 5	Normal operation					
Supply current Note 1	I _{DD1}				f _{IL} = 15 kHz, T _A = -40°C Note 5	Normal operation		1.8	5.9	μA	
					f _{IL} = 15 kHz, T _A = +25°C Note 5	Normal operation		1.9	5.9		
					f _{IL} = 15 kHz, T _A = +85°C Note 5	Normal operation		2.3	8.7		

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. ~~The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, D/A converter, comparator, programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.~~

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main), LS (low-speed main), LV (low-voltage main), and LP (low-power main) modes.

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

Note 4. When the high-speed system clock is stopped.

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 5. When the high-speed system clock, high-speed on-chip oscillator clock and middle-speed on-chip oscillator clock are stopped.

Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 6. When the high-speed system clock, high-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock is stopped.

Note 5. When the high-speed system clock, high-speed on-chip oscillator clock and middle-speed on-chip oscillator clock are stopped.

Note 6. When the high-speed system clock, high-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HI}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 2. f_{HI}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_M: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 3. f_M: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 4. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = 0 V)

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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode	fHOCO = 48 MHz ^{Note 4}	VDD = 5.0 V	0.59	2.43	mA
				fHOCO = 48 MHz ^{Note 4}	VDD = 3.0 V	0.59	2.43	
				fHOCO = 24 MHz ^{Note 4}	VDD = 5.0 V	0.41	1.83	
				fHOCO = 24 MHz ^{Note 4}	VDD = 3.0 V	0.41	1.83	
Subsystem clock operation			fIL = 15 kHz, TA = -40°C ^{Note 5}	0.48	1.22	μA		
			fIL = 15 kHz, TA = +25°C ^{Note 5}	0.55	1.22			
			fIL = 15 kHz, TA = +85°C ^{Note 5}	0.80	3.30			

Note 1. Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. **The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, D/A converter, comparator, programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.**

Note 2. When the HALT instruction is executed in the flash memory.

Note 3. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 5. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and high-speed system clock are stopped.

Note 6. When the high-speed system clock, high-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_H: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_M: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_L: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = 0 V)

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Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode	fHOCO = 48 MHz ^{Note 4}	VDD = 5.0 V	0.59	2.43	mA
				fHOCO = 48 MHz ^{Note 4}	VDD = 3.0 V	0.59	2.43	
				fHOCO = 24 MHz ^{Note 4}	VDD = 5.0 V	0.41	1.83	
				fHOCO = 24 MHz ^{Note 4}	VDD = 3.0 V	0.41	1.83	
Subsystem clock operation			fIL = 15 kHz, TA = -40°C ^{Note 5}	0.48	1.22	μA		
			fIL = 15 kHz, TA = +25°C ^{Note 5}	0.55	1.22			
			fIL = 15 kHz, TA = +85°C ^{Note 5}	0.80	3.30			

Note 1. Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The following points apply in the HS (high-speed main), LS (low-speed main), LV (low-voltage main), and LP (low-power main) modes.

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock is stopped.

Note 5. When the high-speed system clock, high-speed on-chip oscillator clock and middle-speed on-chip oscillator clock are stopped.

Note 6. When the high-speed system clock, high-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_H: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_M: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_L: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD3 Note 2	STOP mode Note 3	T _A = -40°C		0.19	0.51	μA
			T _A = +25°C		0.25	0.51	
			T _A = +50°C		0.28	1.10	
			T _A = +70°C		0.38	1.90	
			T _A = +85°C		0.60	3.30	

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. ~~The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pullup/pull-down resistors, and the current flowing during data flash rewrite.~~

~~**Note 2.** The values do not include the current flowing into the 12-bit interval timer and watchdog timer.~~

Note 3. For the setting of the current values when operating the subsystem clock in STOP mode, see the current values when operating the subsystem clock in HALT mode.

(T_A = -40 to +85°C, 1.6 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD3	STOP mode Note 2	T _A = -40°C		0.19	0.51	μA
			T _A = +25°C		0.25	0.51	
			T _A = +50°C		0.28	1.10	
			T _A = +70°C		0.38	1.90	
			T _A = +85°C		0.60	3.30	

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

Note 2. For the setting of the current values when operating the subsystem clock in STOP mode, see the current values when operating the subsystem clock in HALT mode.

2. 36.3.2 Supply current characteristics (Page 1072 to Page.1074)

Incorrect:

36.3.2 Supply current characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = 0\text{ V}$)

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Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	Basic operation	HS (high-speed main) mode	$f_{\text{HOCO}} = 48\text{ MHz}$ Note 3	$\text{VDD} = 5.0\text{ V}$		1.7	mA
					$f_{\text{IH}} = 24\text{ MHz}$ Note 3	$\text{VDD} = 3.0\text{ V}$		1.7	
					$f_{\text{HOCO}} = 24\text{ MHz}$ Note 3	$\text{VDD} = 5.0\text{ V}$		1.4	
					$f_{\text{IH}} = 24\text{ MHz}$ Note 3	$\text{VDD} = 3.0\text{ V}$		1.4	
			Normal operation	Subsystem clock operation	$f_{\text{IL}} = 15\text{ kHz}$, $T_A = -40^\circ\text{C}$ Note 4		1.8	5.9	μA
			$f_{\text{IL}} = 15\text{ kHz}$, $T_A = +25^\circ\text{C}$ Note 4		1.9	5.9			
			$f_{\text{IL}} = 15\text{ kHz}$, $T_A = +85^\circ\text{C}$ Note 4		2.3	8.7			
			$f_{\text{IL}} = 15\text{ kHz}$, $T_A = +105^\circ\text{C}$ Note 4		3.0	20.9			

Note 1. Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. **The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.**

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock, high-speed on-chip oscillator clock and middle-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH} : High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{IM} : Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL} : Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB} : Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

Correct:

36.3.2 Supply current characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = 0\text{ V}$)

(1/3)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD1	Operating mode	Basic operation	HS (high-speed main) mode	$f_{\text{HOCO}} = 48\text{ MHz}$ Note 3	$\text{VDD} = 5.0\text{ V}$		1.7	mA
					$f_{\text{IH}} = 24\text{ MHz}$ Note 3	$\text{VDD} = 3.0\text{ V}$		1.7	
					$f_{\text{HOCO}} = 24\text{ MHz}$ Note 3	$\text{VDD} = 5.0\text{ V}$		1.4	
					$f_{\text{IH}} = 24\text{ MHz}$ Note 3	$\text{VDD} = 3.0\text{ V}$		1.4	
			Normal operation	Subsystem clock operation	$f_{\text{IL}} = 15\text{ kHz}$, $T_A = -40^\circ\text{C}$ Note 4		1.8	5.9	μA
			$f_{\text{IL}} = 15\text{ kHz}$, $T_A = +25^\circ\text{C}$ Note 4		1.9	5.9			
			$f_{\text{IL}} = 15\text{ kHz}$, $T_A = +85^\circ\text{C}$ Note 4		2.3	8.7			
			$f_{\text{IL}} = 15\text{ kHz}$, $T_A = +105^\circ\text{C}$ Note 4		3.0	20.9			

Note 1. Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The following points apply in the HS (high-speed main) modes.

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

Note 2. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 3. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock, high-speed on-chip oscillator clock and middle-speed on-chip oscillator clock are stopped.

Remark 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{IH} : High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{IM} : Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_{IL} : Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB} : Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode	f _{HOCO} = 48 MHz Note 3	V _{DD} = 5.0 V	0.59	3.45	mA		
				f _{HI} = 24 MHz Note 4	V _{DD} = 3.0 V	0.59	3.45			
				f _{HOCO} = 24 MHz Note 3	V _{DD} = 5.0 V	0.41	2.85			
				f _{HI} = 16 MHz Note 4	V _{DD} = 3.0 V	0.41	2.85			
				f _{HOCO} = 16 MHz Note 3	V _{DD} = 5.0 V	0.39	2.08			
				f _{HI} = 16 MHz Note 4	V _{DD} = 3.0 V	0.39	2.08			
			HS (high-speed main) mode	f _{MX} = 20 MHz Note 3	V _{DD} = 5.0 V	Square wave input	0.20		2.45	mA
						Resonator connection	0.40		2.57	
						V _{DD} = 3.0 V	Square wave input		0.20	
					Resonator connection	0.40	2.57			
V _{DD} = 5.0 V	Square wave input	0.15			1.28					
	Resonator connection	0.30			1.36					
Subsystem clock operation	f _L = 15 kHz, T _A = -40°C Note 5	V _{DD} = 5.0 V	Square wave input	0.15	1.28	μA				
			Resonator connection	0.30	1.36					
			V _{DD} = 3.0 V	Square wave input	0.15		1.28			
				Resonator connection	0.30		1.36			
Subsystem clock operation	f _L = 15 kHz, T _A = +25°C Note 5	V _{DD} = 5.0 V	Square wave input	0.48	1.22	μA				
			Resonator connection	0.80	3.30					
			V _{DD} = 3.0 V	Square wave input	0.15		1.28			
				Resonator connection	0.30		1.36			
Subsystem clock operation	f _L = 15 kHz, T _A = +85°C Note 5	V _{DD} = 5.0 V	Square wave input	0.48	1.22	μA				
			Resonator connection	0.80	3.30					
			V _{DD} = 3.0 V	Square wave input	0.15		1.28			
				Resonator connection	0.30		1.36			
Subsystem clock operation	f _L = 15 kHz, T _A = +105°C Note 5	V _{DD} = 5.0 V	Square wave input	0.48	1.22	μA				
			Resonator connection	0.80	3.30					
			V _{DD} = 3.0 V	Square wave input	0.15		1.28			
				Resonator connection	0.30		1.36			

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. **The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, programmable gain amplifier, LVD circuit, I/O ports, and on-chip pull-up/pull-down resistors, and the current flowing during data flash rewrite.**

Note 2. When the HALT instruction is executed in the flash memory.

Note 3. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 5. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and high-speed system clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HI}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{IM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_L: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(T_A = -40 to +105°C, 2.4 V ≤ EV_{DD0} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode	f _{HOCO} = 48 MHz Note 3	V _{DD} = 5.0 V	0.59	3.45	mA		
				f _{HI} = 24 MHz Note 4	V _{DD} = 3.0 V	0.59	3.45			
				f _{HOCO} = 24 MHz Note 3	V _{DD} = 5.0 V	0.41	2.85			
				f _{HI} = 16 MHz Note 4	V _{DD} = 3.0 V	0.41	2.85			
				f _{HOCO} = 16 MHz Note 3	V _{DD} = 5.0 V	0.39	2.08			
				f _{HI} = 16 MHz Note 4	V _{DD} = 3.0 V	0.39	2.08			
			HS (high-speed main) mode	f _{MX} = 20 MHz Note 3	V _{DD} = 5.0 V	Square wave input	0.20		2.45	mA
						Resonator connection	0.40		2.57	
						V _{DD} = 3.0 V	Square wave input		0.20	
					Resonator connection	0.40	2.57			
V _{DD} = 5.0 V	Square wave input	0.15			1.28					
	Resonator connection	0.30			1.36					
Subsystem clock operation	f _L = 15 kHz, T _A = -40°C Note 5	V _{DD} = 5.0 V	Square wave input	0.15	1.28	μA				
			Resonator connection	0.30	1.36					
			V _{DD} = 3.0 V	Square wave input	0.15		1.28			
				Resonator connection	0.30		1.36			
Subsystem clock operation	f _L = 15 kHz, T _A = +25°C Note 5	V _{DD} = 5.0 V	Square wave input	0.48	1.22	μA				
			Resonator connection	0.80	3.30					
			V _{DD} = 3.0 V	Square wave input	0.15		1.28			
				Resonator connection	0.30		1.36			
Subsystem clock operation	f _L = 15 kHz, T _A = +85°C Note 5	V _{DD} = 5.0 V	Square wave input	0.48	1.22	μA				
			Resonator connection	0.80	3.30					
			V _{DD} = 3.0 V	Square wave input	0.15		1.28			
				Resonator connection	0.30		1.36			
Subsystem clock operation	f _L = 15 kHz, T _A = +105°C Note 5	V _{DD} = 5.0 V	Square wave input	0.48	1.22	μA				
			Resonator connection	0.80	3.30					
			V _{DD} = 3.0 V	Square wave input	0.15		1.28			
				Resonator connection	0.30		1.36			

Note 1. Total current flowing into V_{DD} and EV_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The following points apply in the HS (high-speed main) modes.

- The currents in the "TYP." column do not include the operating currents of the peripheral modules.
- The currents in the "MAX." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, D/A converter, comparator, programmable gain amplifier, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

In the subsystem clock operation, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.

Note 2. When the HALT instruction is executed in the flash memory.

Note 3. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 4. When the high-speed system clock, middle-speed on-chip oscillator clock and low-speed on-chip oscillator clock are stopped.

Note 5. When the high-speed on-chip oscillator clock, middle-speed on-chip oscillator clock and high-speed system clock are stopped.

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HI}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 3. f_{IM}: Middle-speed on-chip oscillator clock frequency (4 MHz max.)

Remark 4. f_L: Low-speed on-chip oscillator clock frequency

Remark 5. f_{SUB}: Subsystem clock frequency (Low-speed on-chip oscillator clock frequency)

Remark 6. Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD3 Note 2	STOP mode Note 3	TA = -40°C		0.19	0.51	μA
			TA = +25°C		0.25	0.51	
			TA = +50°C		0.28	1.10	
			TA = +70°C		0.38	1.90	
			TA = +85°C		0.60	3.30	
			TA = +105°C		1.5	17.0	

Note 1. Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. ~~The MAX values include the peripheral operating current. However, these values do not include the current flowing into the A/D converter, comparator, Programmable gain amplifier, LVD circuit, I/O ports, and on-chip pullup/pull-down resistors, and the current flowing during data flash rewrite.~~

~~**Note 2.** The values do not include the current flowing into the 12-bit interval timer and watchdog timer.~~

Note 3. For the setting of the current values when operating the subsystem clock in STOP mode, see the current values when operating the subsystem clock in HALT mode.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = 0 V)

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Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current Note 1	IDD3	STOP mode Note 3	TA = -40°C		0.19	0.51	μA
			TA = +25°C		0.25	0.51	
			TA = +50°C		0.28	1.10	
			TA = +70°C		0.38	1.90	
			TA = +85°C		0.60	3.30	
			TA = +105°C		1.5	17.0	

Note 1. Total current flowing into VDD and EVDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. **In the STOP mode, the currents in both the "TYP." and "MAX." columns do not include the operating currents of the peripheral modules.**

Note 2. For the setting of the current values when operating the subsystem clock in STOP mode, see the current values when operating the subsystem clock in HALT mode.