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RENESAS TECHNICAL UPDATE

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Renesas Electronics Corporation

Product Category	System LSI		Document No.	TN-RIN-A004A/E	Rev.	1.00
Title	Bus arbitration issue between Cortex-M3 and bus masters		Information Category	Technical Notification		
Applicable Product	See following	Lot No. All lots	Reference Document	R-IN32M3 Series User's Manual R-IN32M3-CL (R18UZ0007EJ0202) R-IN32M3 Series User's Manual R-IN32M3-EC (R18UZ0003EJ0301) R-IN32M3 Series User's Manual Peripheral Functions R-IN32M3-CL R-IN32M3-EC (R18UZ0005EJ0601)		

We would like to inform about potential issues regarding bus arbitration between Cortex-M3 and other bus masters as described below.

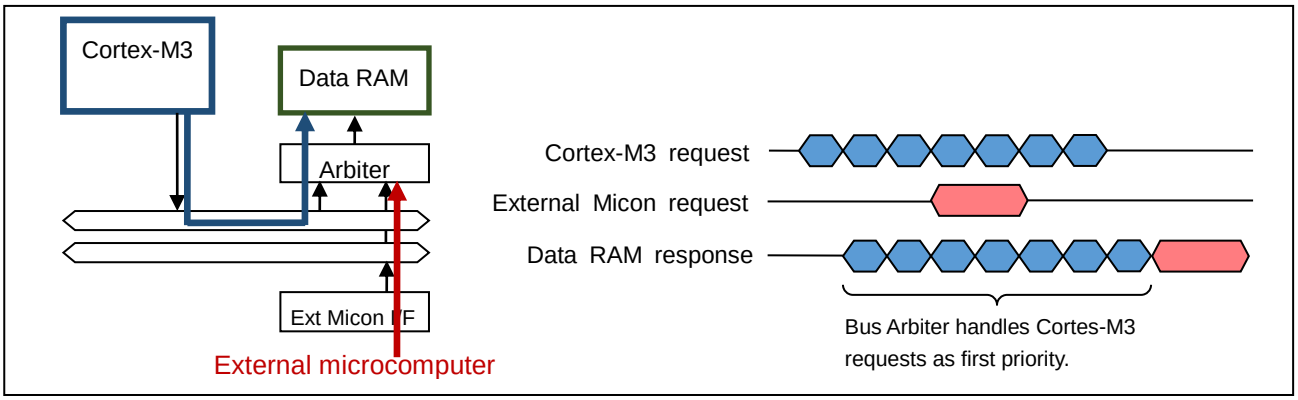
1. Applicable Product

Product Type	Model Marking	Product Code
R-IN32M3-EC	MC-10287F1	MC-10287F1-HN4-A
		MC-10287F1-HN4-M1-A
R-IN32M3-CL	D60510F1	UPD60510F1-HN4-A
		UPD60510F1-HN4-M1-A

2. Issue

During Cortex-M3 processor performs continuously read/write access to identical memory[*1], other bus masters[*2] cannot access the memory due to bus arbitration between Cortex-M3 and other master. Other master waits the memory access until Cortex-M3 releases the bus for the memory. Waiting time depends on time of continuous Cortex-M3 access.

e.g.) External microcomputer accesses data RAM during Cortex-M3 copies data in data RAM



Note: *1 e.g. Copy data in the below identical memory.

Data RAM: read data from data RAM and write the data to data RAM)

Instruction RAM: read data from instruction RAM and write the data to instruction RAM

External RAM: read data from external RAM and write the data to external RAM

*2 Other masters are below.

General purpose DMA controller

DMA controller for Real Time Port

External microcomputer interface

3. Condition

The bus arbitration issue during Cortex-M3 access occurs on the following conditions.

Case	Master	Slave	Detailed condition
1	External microcomputer	Data RAM	External microcomputer accesses data RAM during Cortex-M3 copies data in data RAM
2	DMAC	Data RAM	DMAC transfers data from/to data RAM during Cortex-M3 copies data in data RAM
3	External microcomputer	Instruction RAM	External microcomputer accesses instruction RAM during Cortex-M3 copies data in instruction RAM
4	DMAC	Instruction RAM	DMAC transfers data from/to instruction RAM during Cortex-M3 copies data in instruction RAM
5	DMAC	External memory	DMAC transfers data from/to external memory during Cortex-M3 copies data in external memory

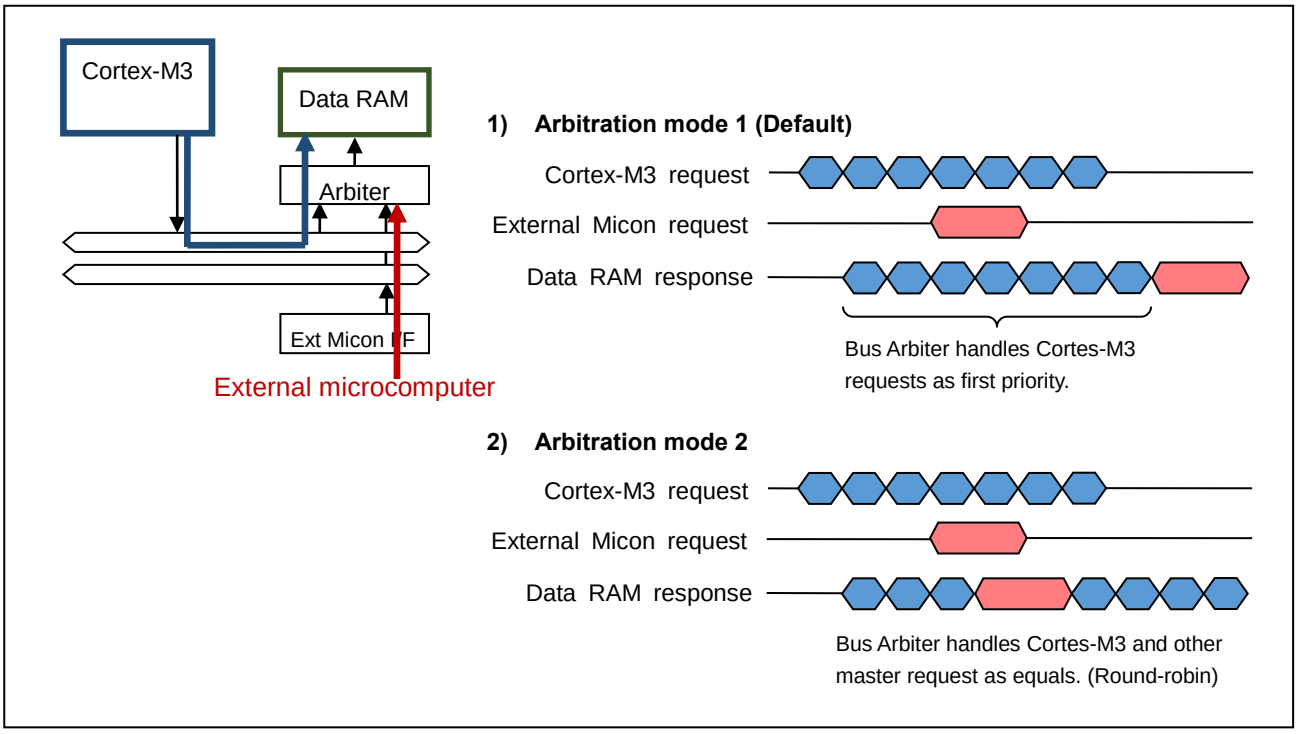
4. Usage note

Bus arbiter for data RAM, instruction RAM and external memory prioritizes Cortex-M3 access request over other master access request. Thus, waiting time for other master access might be longer than expectation depending on a programing performed on Cortex-M3.

If waiting time for other master access is a problem on your system, please contact to Renesas sales or distributers.

5. Revision Plan

Renesas revises the applicable products. In order to have compatibility, revised version adds a new mode register to select arbitration mode. The default mode is the same as current version.



Revised sample will be delivered as the following schedule.

ES: Nov 30, 2015

CS: Dec 25, 2015

MP: Jun 1, 2016