Date: Dec. 28, 2015

RENESAS TECHNICAL UPDATE

TOYOSU FORESIA, 3-2-24, Toyosu, Koto-ku, Tokyo 135-0061, Japan
Renesas Electronics Corporation

Product Category	System LSI		Document No.	TN-RIN-A006B/E	Rev.	2.00
Title	AC characteristics update for external microcomputer interface		Information Category	Technical Notification		
Applicable Product	See following	Lot No. All lots	Reference Document	R-IN32M3 Series Datasheet (R18DS0008EJ0204) R-IN32M3 Series User's Manual Peripheral Functions R-IN32M3-CL R-IN32M3-EC (R18UZ0005EJ0601)		

We would like to inform updated contents for symbol and value because the TU Rev1.00 released on Aug 7, 2015 didn't show the final AC characteristics for external microcomputer interface.

AC characteristics in R-IN32 Series Datasheet is updated and a note is added in User's Manual as below.

1. Applicable Product

Product Type	Model Marking	Product Code
R-IN32M3-EC	MC-10287F1	MC-10287F1-HN4-A
		MC-10287F1-HN4-M1-A
R-IN32M3-CL	D60510F1	UPD60510F1-HN4-A
		UPD60510F1-HN4-M1-A

2. Documentation update

A) R-IN32M3 Series Datasheet

AC timing definitions for external microcomputer interface are missing in the datasheet. The following specification and timing chart are revised.

And AC specification for synchronous mode and asynchronous mode is changed.

– 4.7.4 External microcomputer interface signal

(1) Synchronous mode

Symbols and values are updated from TU Rev.1. And there are the additional changes as follows:

- Data, HWAITZ out delay time, t_{HKOHD}, is changed.
  - MIN: 20ns to '-'
  - MAX: 10ns to 13.6ns
- HRDZ setup time and HRDZ hold time are added.

	#	Parameter	Symbol	MIN	MAX	Unit
	1	HBUSCLK high level width	t_{HBHIGH}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
	2	HBUSCLK low level width	t_{HBLOW}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
	3	HBUSCLK input cycle	$t_{HBUSCLK}$	20.0	-	ns
	4	Address, HCSZ/HPGCSZ input setup time	t_{SKHA}	4.0	-	ns
	5	HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTZ input setup time	t_{SKHWR}	4.0	-	ns
	6	Address, HCSZ/HPGCSZ input hold time	t_{HKHA}	1.0	-	ns
	7	HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTBZ input hold time	t_{HKHWR}	1.0	-	ns
Added	8	HWRZ0-HWRZ3, HWRSTBZ recovery time (high width)	t_{WHWR}	35.0	-	ns
	9	Data setup time	t_{SKIHD}	4.0	-	ns
	10	Data hold time	t_{HKIHD}	1.0	-	ns
Added	11	Data, HWAITZ output delay time	t_{DKHD}	2.0	-	ns
Added	12	HWAITZ output delay time	t_{DKHWT}	2.0	-	ns
Added	13	HWAITZ valid data output delay time	t_{DKHWTV}	2.0	10.0	ns
Added	14	HWAITZ valid data hold time	t_{HKHWTV}	3.0	-	ns
Added	15	HWIATZ output hold time	t_{HKWTWR}	-	13.6	ns
Added	16	Data, HWAITZ output hold time	t_{HKWTCS}	-	13.6	ns
Added	17	Address, HCSZ, HPGCSZ input setup time (HRDZ fall edge)	t_{SKHAHR}	4.3	-	ns
Added	18	Address, HCSZ/HPGCSZ input hold time (HRDZ rise edge)	t_{HKHAHR}	4.3	-	ns
Added	19	HRDZ recovery time (high width)	t_{WHRD}	35.0	-	ns
Added	20	Data, HWAITZ output delay time (HRDZ fall edge)	t_{DKHDHR}	2.0	-	ns
Added	21	HWAITZ valid data output delay time (HRDZ fall edge)	$t_{DKWTVHR}$	-	16.4	ns
Added	22	Data setup time	$t_{SKHDHWT}$	$t_{HBUSCLK}$-10	-	ns
Added	23	Data, HWAITZ valid data output hold time	$t_{HKHWTHR}$	3.0	-	ns
Revised Rev2	24	Data, HWAITZ output delay time (HRDZ rise edge)	t_{HKOHD}	-	13.6	ns
Added	25	Data, HWAITZ output delay time when on-page access	t_{DKPON}	3.0	16.4	ns
Added	26	Data, HWAITZ output delay time when off-page access	t_{DKPOFF}	3.0	16.4	ns
Added	27	HWAITZ valid data output delay time	$t_{DKWTVCS}$	-	16.4	ns
Added Rev2	28	HRDZ setup time (HBUSCLK rise edge)	t_{SKHRD}	4.0	-	ns
Added Rev2	29	HRDZ hold time (HBUSCLK rise edge)	t_{HKHRD}	1.0	-	ns

(a) SRAM and Page ROM write timing

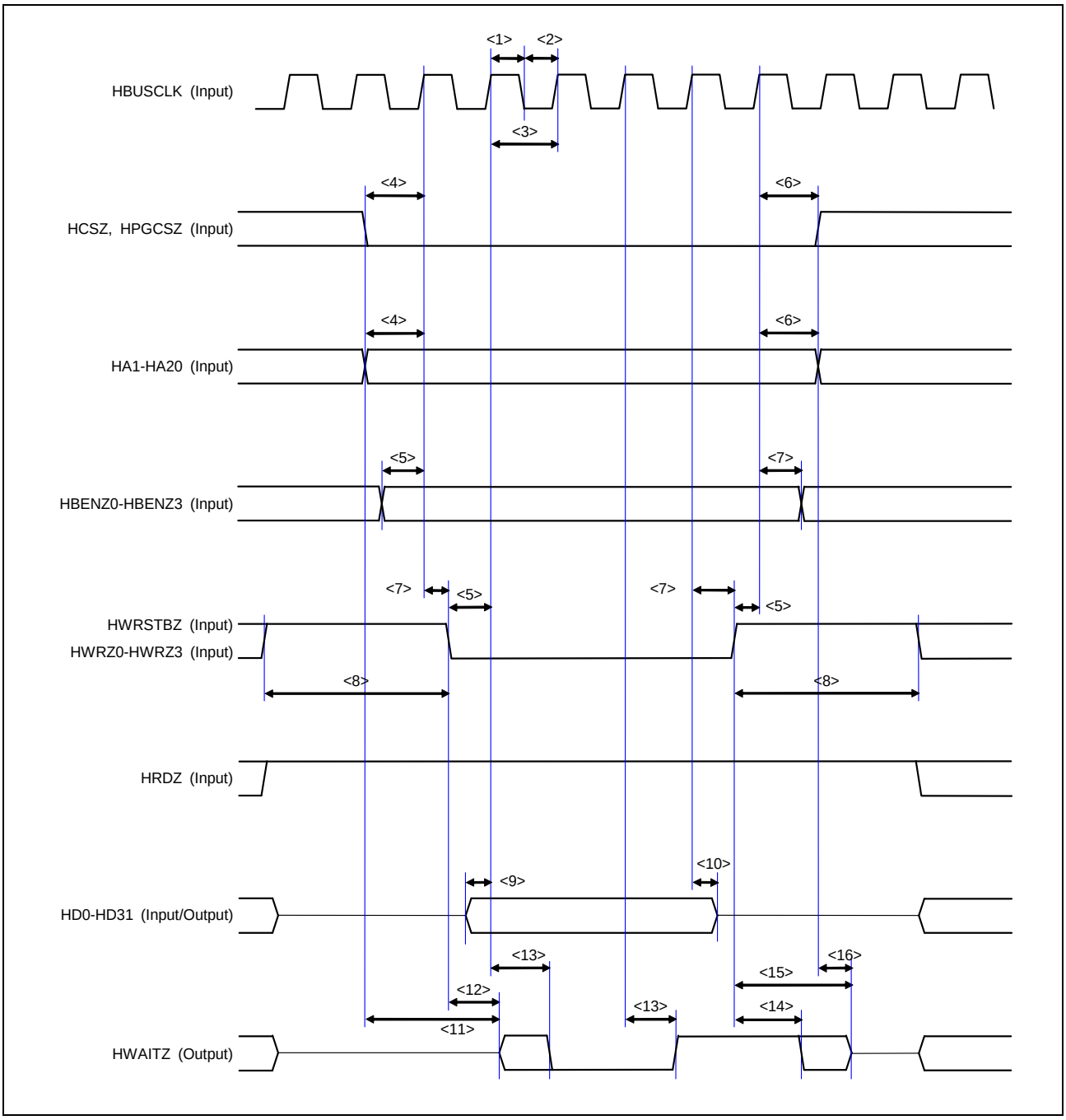

Figure External microcomputer interface write timing (SRAM and Page ROM)

(b) SRAM read timing

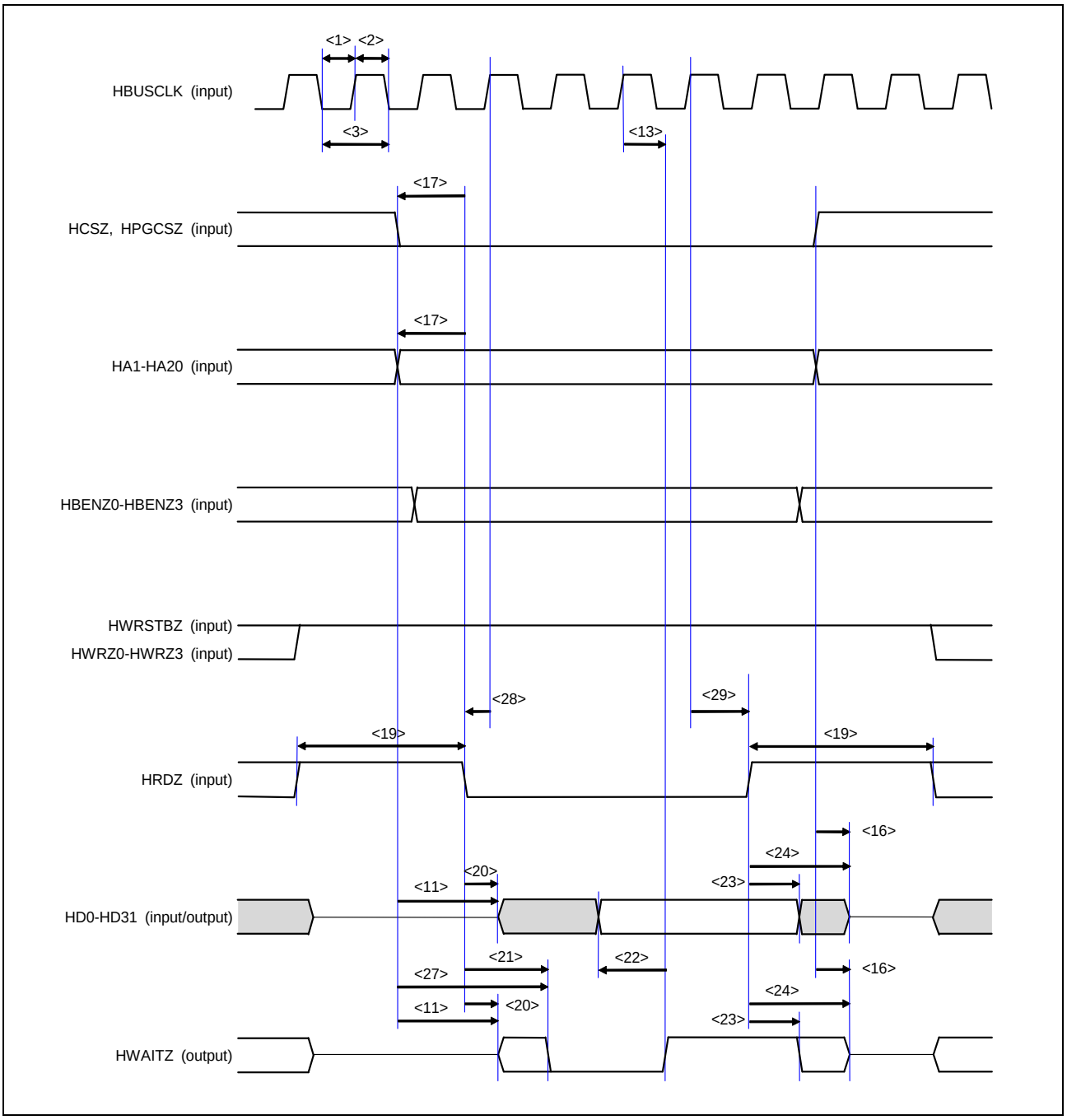

Figure External microcomputer interface read timing (SRAM)

(c) Page ROM read timing

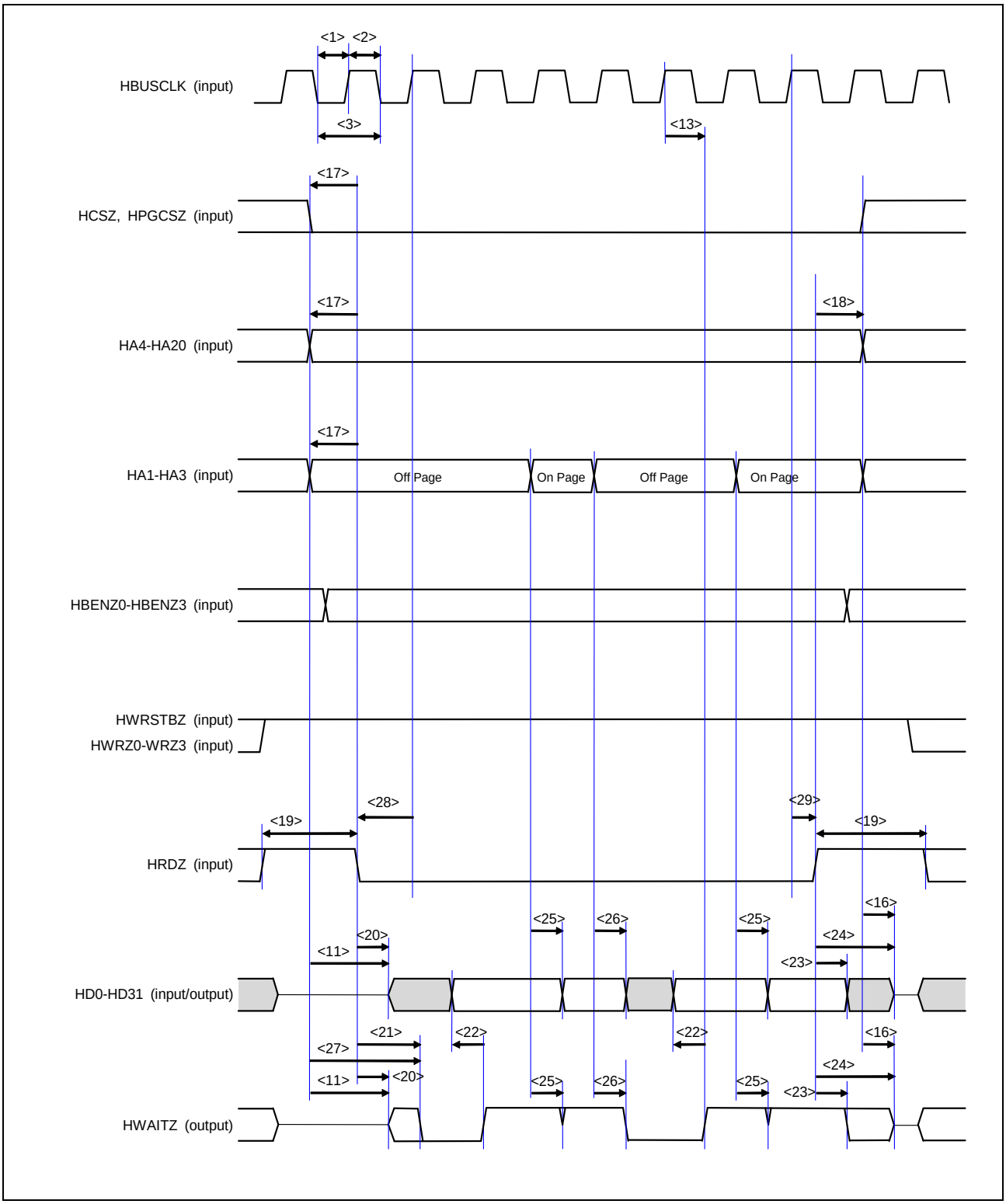

Figure External microcomputer interface read timing (Page ROM)

(2) Synchronous Mode (CC-Link IE Field)

This specification is newly added from TU Rev.1.

	#	Parameter	Symbol	MIN	MAX	Unit
Added	1	HBUSCLK high level width	t_{HBHIGH}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
Added	2	HBUSCLK low level width	t_{HBLOW}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$+2.1	ns
Added	3	HBUSCLK input cycle	$t_{HBUSCLK}$	20.0	-	ns
Added	4	Address, HCSZ/HPGCSZ input setup time (HBUSCLK fall edge)	t_{SKHA}	5.0	-	ns
Added	5	HBENZ0-HBENZ3 (HWRZ0-HWRZ3), HWRSTZ input setup time (HBUSCLK fall edge)	t_{SKHWR}	5.0	-	ns
Added	6	Address, HCSZ/HPGCSZ, HBENZ0-HBENZ3, Data input hold time (HRDZ, HWRSTBZ, HWRZ0-HWRZ3 rise edge)	t_{HKHA}	0	-	ns
Added	7	HWRZ0-HWRZ3, HWRSTBZ recovery time (high width)	t_{WHWR}	$t_{HBUSCLK}$ * 1	-	ns
Added	8	Data input setup time (HCSZ, HPGCSZ fall edge)	t_{SKIHD}	0	-	ns
Added	9	HWAITZ output delay time (HCSZ, HPGCSZ fall edge)	t_{DKHD}	2.0	-	ns
Added	10	HWAITZ output delay time (HWRSTBZ, HWRZ0-HWRZ3 fall edge)	t_{DKHWT}	2.0	-	ns
Added	11	HWAITZ enable data output delay time (HBUSCLK rise edge) “HWAITZ output in synchronization with HBUSCLK rise edge”	t_{DKHWTV}	3.0	11.0	ns
		HWAITZ enable data output delay time (HBUSCLK fall edge) “HWAITZ output in synchronization with HBUSCLK fall edge”	t_{DKHWTV}	3.0	11.0	ns
Added	12	HWAITZ enable data output hold time (HWRSTBZ, HWRZ0-HWRZ3 rise edge)	t_{HKHWTV}	3.0	-	ns
Added	13	HWAITZ output hold time (HWRSTBZ, HWRZ0-HWRZ3 rise edge)	t_{HKWTWR}	-	13.6	ns
Added	14	Data, HWAITZ output hold time (HCSZ, HPGCSZ rise edge)	t_{HKWTCS}	-	13.6	ns
Added	15	HRDZ recovery time (high width)	t_{SKHAHR}	$t_{HBUSCLK}$ * 1	-	ns
Added	16	Data, HWAITZ output delay time (HRDZ fall edge)	t_{HKHAHR}	2.0	-	ns
Added	17	HWAITZ enable data output delay time (to Latch timing of HRDZ, HWWRSTBZ, HWRZ0 - HWRZ3) “HWAITZ output in synchronization with HBUSCLK rise edge”	t_{WHRD}	-	$t_{HBUSCLK}$ / 2 + 11.0	ns
		HWAITZ enable data output delay time (to Latch timing of HRDZ, HWWRSTBZ, HWRZ0 - HWRZ3) “HWAITZ output in synchronization with HBUSCLK fall edge”	t_{DKHDHR}	-	$t_{HBUSCLK}$ / 2 + 11.0	ns
Added	18	Data settle time (from HWAITZ rise edge) “HWAITZ output in synchronization with HBUSCLK ride edge”	$t_{DKWTVHR}$	-	10 *1 - $t_{HBUSCLK}$ * n	ns
		Data settle time (from HWAITZ rise edge) “HWAITZ output in synchronization with HBUSCLK fall edge”	$t_{SKHDHWT}$	-	0 *1 - $t_{HBUSCLK}$ * n	ns
Added	19	Data, HWAITZ enable data output hold time (HRDZ rise edge)	$t_{HKHWTHR}$	3.0	-	ns
Added	20	Data, HWAITZ output delay time (HRDZ rise edge)	t_{HKOHD}	-	13.6	ns
Added	21	HRDZ input setup time HBUSCLK fall edge)	t_{DKPON}	5.0	-	ns

Note *1: The value is shown when WAITDLY2-0 in CIEWAITDLY register is set to $100_{B.}$

(a) Write timing

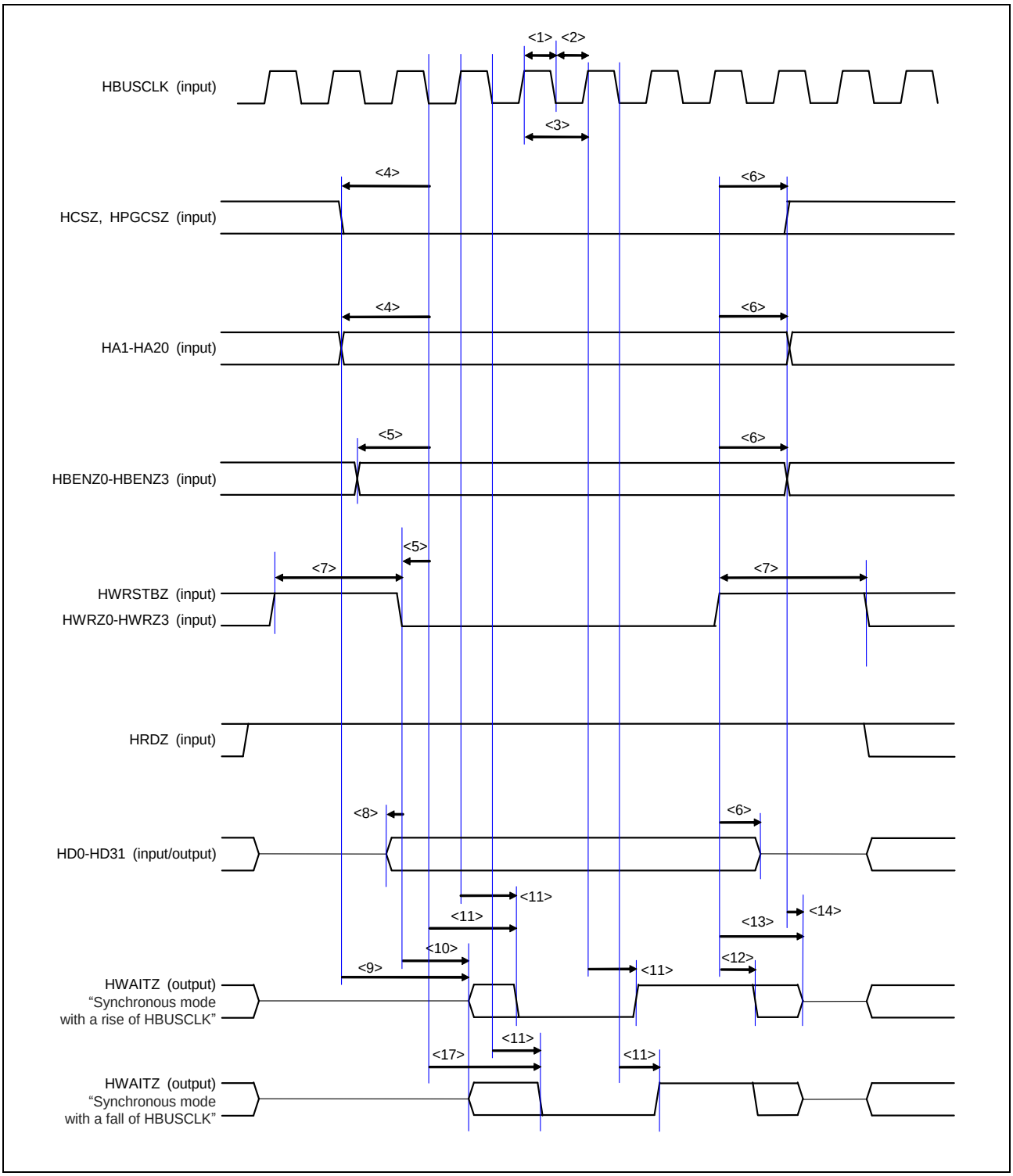

Figure External microcomputer interface write timing

(b) Read timing

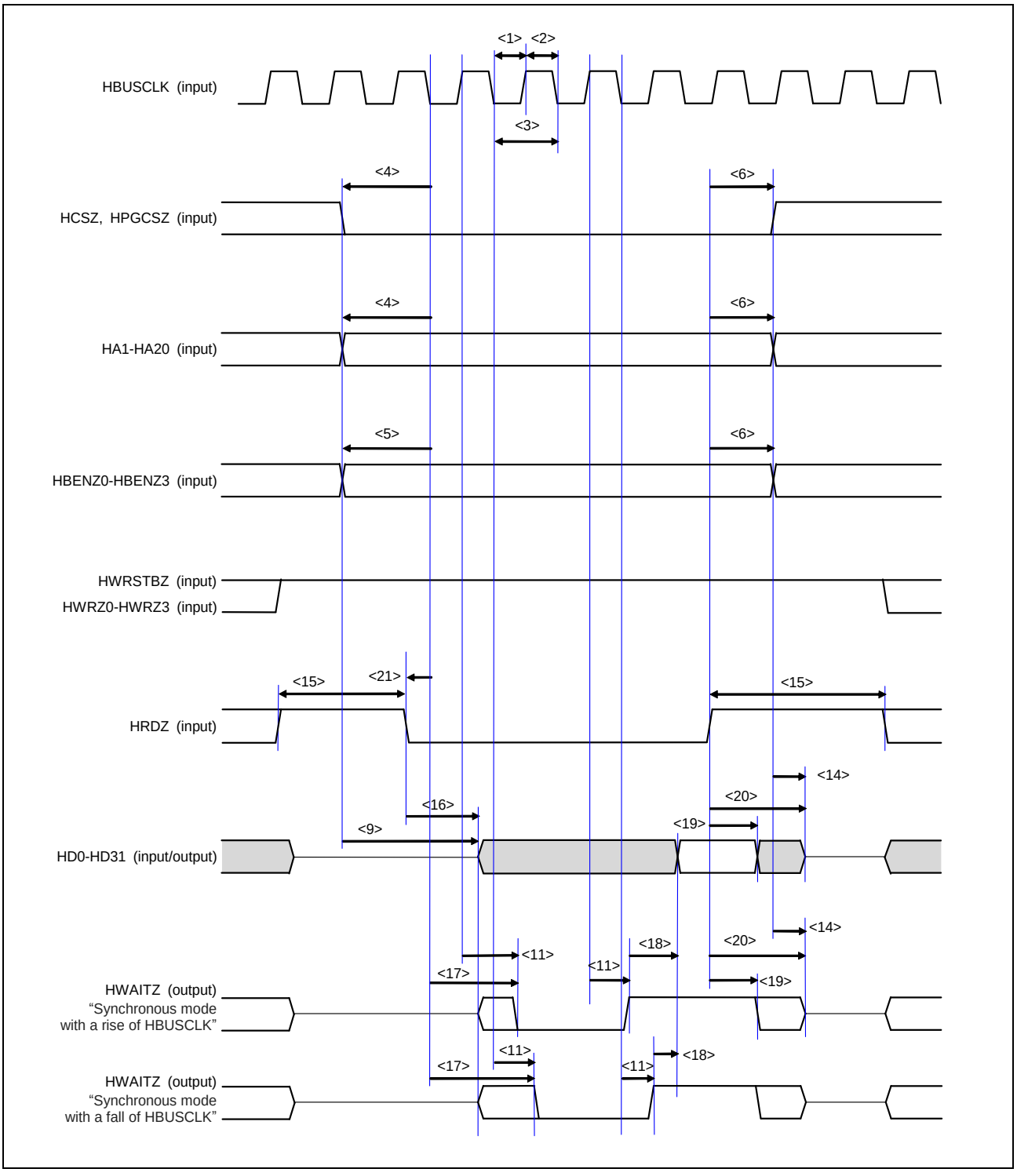

Figure External microcomputer interface read timing

(3) Asynchronous mode

Symbols and values are updated from TU Rev.1. And there are the additional changes as follows:

- HWRZ0-3, HWRSTBZ to data setup time, t_{WRS}, is changed from 1.0ns to 4.8-10*n ns.
- Wait active time, $t_{WRWAITF}$ and $t_{RDWAITF}$, is changed from 10.0ns to 16.4ns (TU Rev1 showed 40.0ns).
- Data, HWAITZ output delay time, t_{RDLZ}, is changed from MAX 10ns to MIN 2.0ns.
- Data valid to wait inactive time, t_{WAITR}, is changed from MIN 10ns to MAX -7.5+10*n ns.
- Data, HWAITZ output hold time, t_{RDHZ}, is changed from MIN 3.0ns to MAX 13.6ns.
- Address, HCSZ/HPGCSZ, HBENZ0-HBENZ3 input hold time, Data hold time when on-page access and Data hold time when off-page access are deleted.

	#	Parameter	Symbol	MIN	MAX	Unit
Added	1	Address, HCSZ/HPGCSZ, HBENZ0-HBENZ3 input setup time	t_{ADDWRS}	4.8-10*n *1	-	ns
Deleted Rev.2		~~Address, HCSZ/HPGCSZ, HBENZ0-HBENZ3 input hold time~~				~~ns~~
Added	2	HWRZ0-HWRZ3, HWRSTBZ recovery time (high width)	t_{WRW}	35.0	-	ns
Revised Rev.2	3	HWRZ0-3, HWRSTBZ to data setup	t_{WRS}	4.8-10*n *1	-	ns
Added	4	HWRZ0-3, HWRSTBZ to data hold	t_{WRH}	4.8	-	ns
Added	5	HWAITZ output delay time (Address, HCSZ/HPGCSZ)	t_{CLZ}	2.0	-	ns
Added	6	HWAITZ output delay time (HWRSTBZ, HWRZ0-HWRZ3)	t_{WAITD}	2.0	-	ns
Revised Rev.2	7	HWRZ0-3, HWRSTBZ to wait active	$t_{WRWAITF}$	-	**16.4**	ns
Added	8	HWRZ0-3, HWRSTBZ to wait hold	t_{WAITVH}	3.0	-	ns
Added	9	Data, HWAITZ output hold time (HWRZ0-HWRZ3, HERSTBZ)	t_{WAITH}	-	13.6	ns
Added	10	Data, HWAITZ output hold time (Address, HCSZ/HPGCSZ)	t_{CHZ}	-	13.6	ns
Added	11	HRDZ to Address, HCSZ/HPGCSZ setup time	t_{ADDRDS}	4.3-10*n *2	-	ns
Added	12	HRDZ to Address, HCSZ/HPGCSZ hold time	t_{ADDRDH}	4.3	-	ns
Added	13	HRDZ recovery time (high width)	t_{RDW}	35.0	-	ns
Revised Rev.2	14	Data, HWAITZ output delay time	t_{RDLZ}	2.0	-	ns
Revised Rev.2	15	HRDZ to wait active	$t_{RDWAITF}$	-	**16.4**	ns
Revised Rev.2	16	Data valid to wait inactive	t_{WAITR}	-	-7.5+10*n *3	ns
Added	17	Data, HWAITZ valid data output hold time	t_{DATAOH}	3.0	-	ns
Revised Rev.2	18	Data, HWAITZ output hold time	t_{RDHZ}	-	13.6	ns
Added	19	Data, HWAITZ output delay time when on-page access	$t_{PAGEOND}$	3.0	16.4	ns
Added	20	Data, HWAITZ output delay time when off-page access	$t_{PAGEOFD}$	3.0	16.4	ns
Deleted Rev.2		~~Data hold time when on-page access~~				~~ns~~
Deleted Rev.2		~~Data hold time when off-page access~~				~~ns~~
Added	21	HWAITZ valid data output delay time	t_{WAITVD}	-	16.4	ns

Note: *1 n is the setting value of WRSTD2-0 bits on HIFBTC register.

*2 n is the setting value of RDSTD1-0 bits on HIFBTC register.

*3 n is the setting value of RDDTS1-0 bits on HIFBTC register.

(a) SRAM and Page ROM write timing

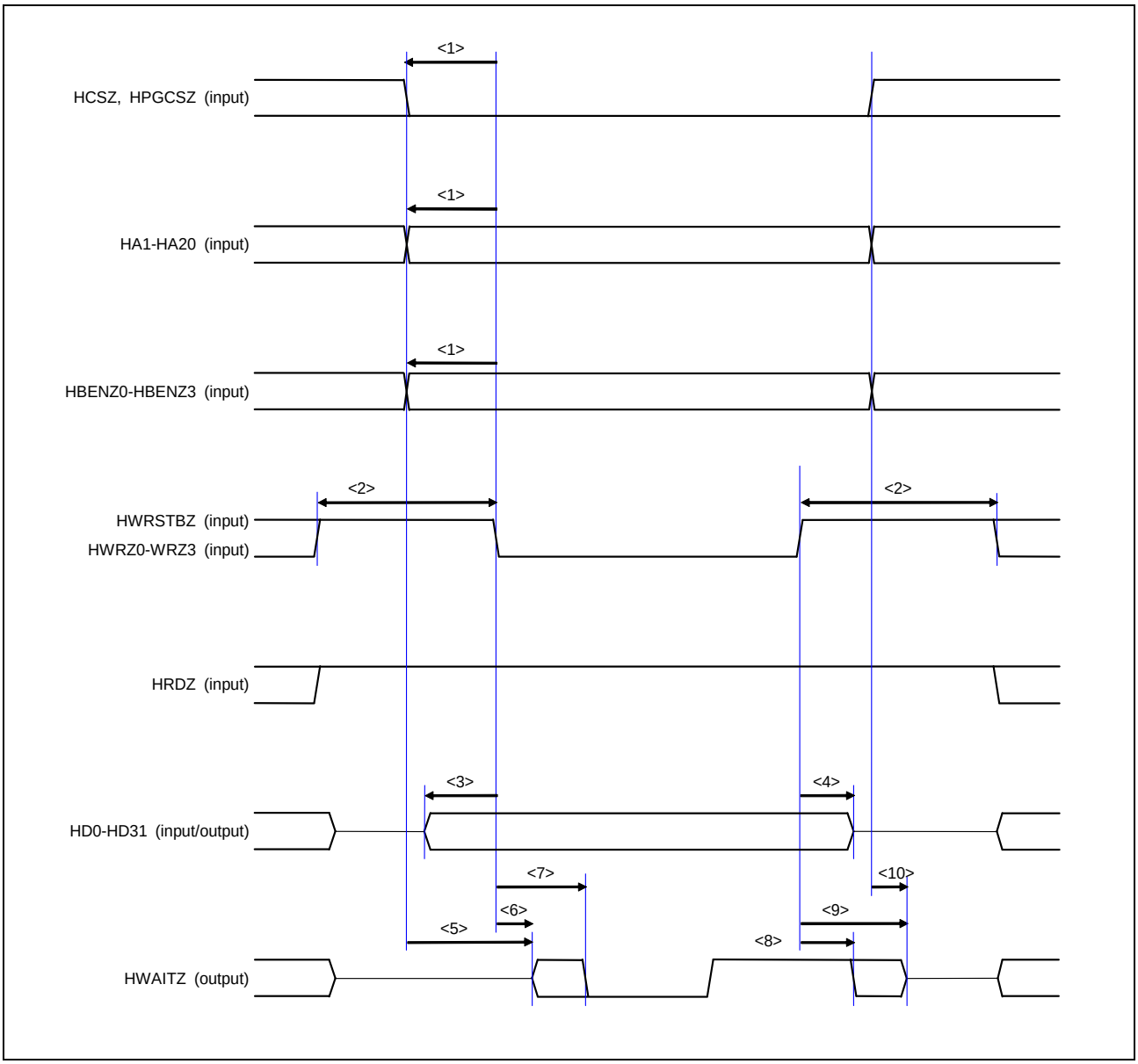

Figure External microcomputer interface write timing (SRAM and Page ROM)

(b) SRAM read timing

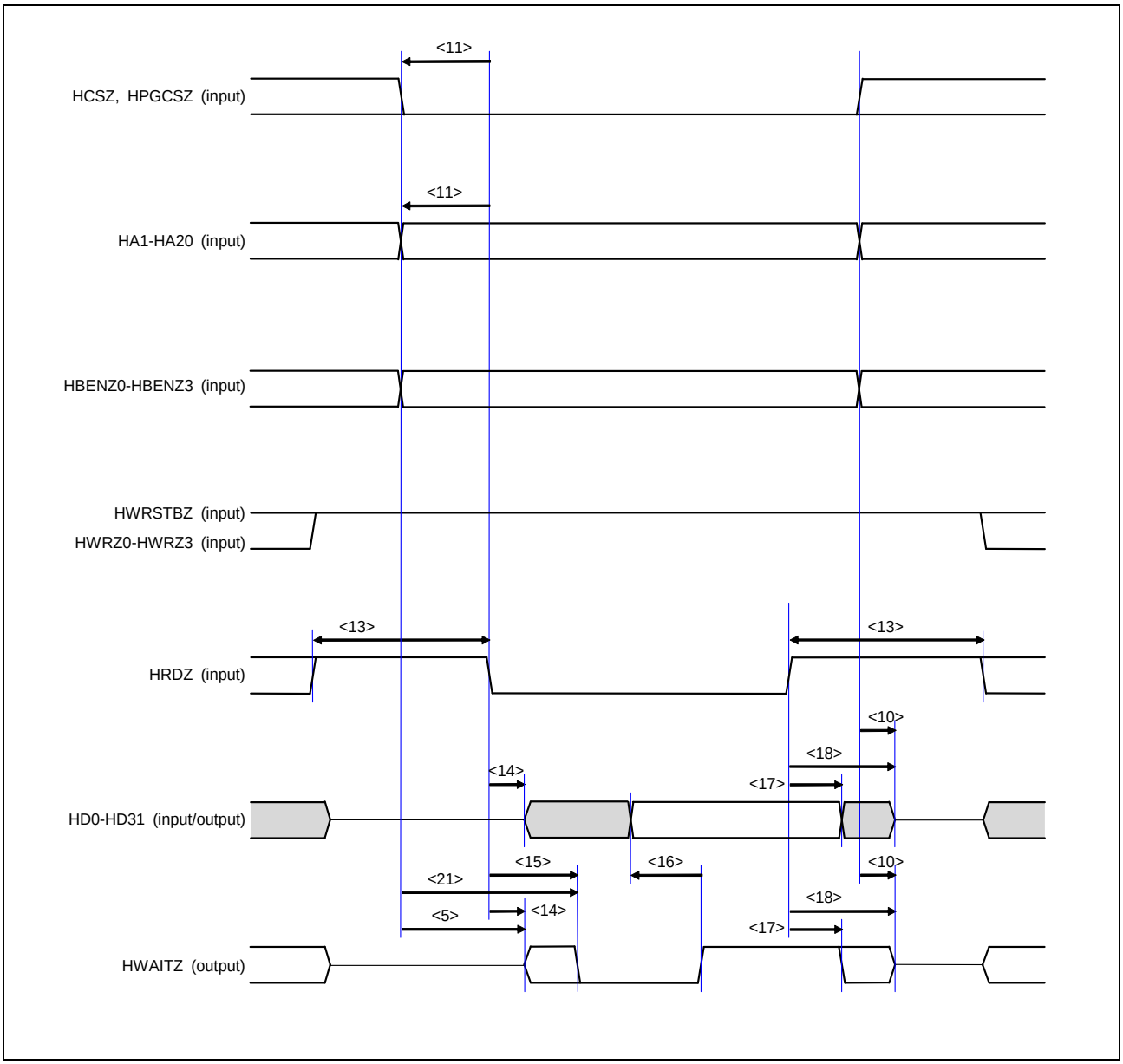

Figure External microcomputer interface read timing (SRAM)

(c) Page ROM read timing

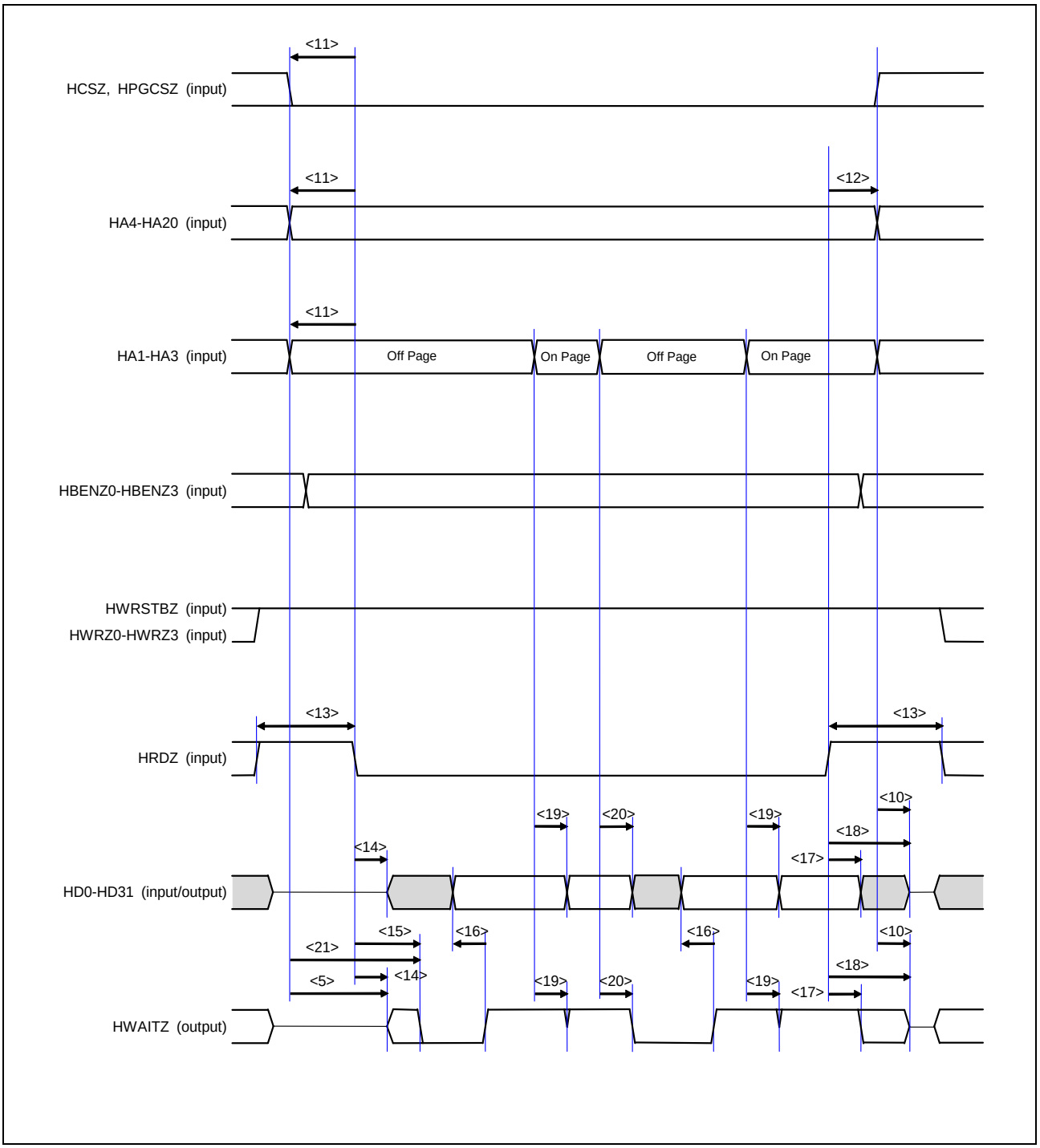

Figure External microcomputer interface read timing (Page ROM)

(4) Synchronous SRAM type transmission mode

All timing definitions are newly added. Symbols and values are updated from TU Rev.1.

#	Parameter	Symbol	MIN	MAX	Unit
1	HBUSCLK input cycle	t_{HBHIGH}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$-2.1	ns
2	HBUSCLK high level width	t_{HBLOW}	$0.5t_{HBUSCLK}$-2.1	$0.5t_{HBUSCLK}$-2.1	ns
3	HBUSCLK low level width	$t_{HBUSCLK}$	20.0	—	ns
4	Address, HCSZ/HPGCSZ input setup time (HBUSCLK rise edge)	t_{SKPHA}	4.0	—	ns
5	Address, HCSZ/HPGCSZ input hold time (HBUSCLK rise edge)	t_{HKPCS}	1.0	—	ns
6	Address, HCSZ/HPGCSZ input setup time (HBUSCLK fall edge)	t_{SKNHA}	4.0	—	ns
7	Address, HCSZ/HPGCSZ input hold time (HBUSCLK fall edge)	t_{HKNHA}	1.0	—	ns
8	HWRZ0-HWRZ3 input setup time (HBUSCLK rise edge)	t_{SKPHWR}	4.0	—	ns
9	HWRZ0-HWRZ3 input hold time (HBUSCLK rise edge)	t_{HKPHWR}	1.0	—	ns
10	HWRZ0-HWRZ3 input setup time (HBUSCLK fall edge)	t_{SKNHWR}	4.0	—	ns
11	HWRZ0-HWRZ3 input hold time (HBUSCLK fall edge)	t_{HKNHWR}	1.0	—	ns
12	HBCYSTZ, HWRSTBZ input setup time (HBUSCLK rise edge)	$t_{SKPHBCY}$	4.0	—	ns
13	HBCYSTZ, HWRSTBZ input hold time (HBUSCLK rise edge)	$t_{HKPHBCY}$	1.0	—	ns
14	HBCYSTZ, HWRSTBZ input setup time (HBUSCLK fall edge)	$t_{SKNHBCY}$	4.0	—	ns
15	HBCYSTZ, HWRSTBZ input hold time (HBUSCLK fall edge)	$t_{HKNHBCY}$	1.0	—	ns
16	HRDZ input setup time (HBUSCLK rise edge)	t_{SKPHRD}	4.0	—	ns
17	HRDZ input hold time (HBUSCLK rise edge)	t_{HKPHRD}	1.0	—	ns
18	HRDZ input setup time (HBUSCLK fall edge)	t_{SKNHRD}	4.0	—	ns
19	HRDZ input hold time (HBUSCLK fall edge)	t_{HKNHRD}	1.0	—	ns
20	Data input setup time (HBUSCLK rise edge)	t_{SKPHD}	4.0	—	ns
21	Data input hold time (HBUSCLK rise edge)	t_{HKPHD}	1.0	—	ns
22	Data input setup time (HBUSCLK fall edge)	t_{SKNHD}	4.0	—	ns
23	Data input hold time (HBUSCLK fall edge)	t_{HKNHD}	1.0	—	ns
24	Data output delay time (HBUSCLK rise edge)	t_{DKNHRD}	2.0	—	ns
25	Data output float time (HBUSCLK rise edge)	t_{HKPHRD}	—	13.6	ns
26	Data output delay time (HBUSCLK fall edge)	t_{DKPHD}	2.0	10.0	ns
27	Data output float time (HBUSCLK fall edge)	t_{DKNHD}	2.0	10.0	ns
28	HWAITZ output delay time (HBUS rise edge)	t_{DKPHWT}	2.0	10.0	ns
29	HWAITZ output delay time (HBUS fall edge)	t_{DKNHWT}	2.0	10.0	ns
30	Data output hold time (HCSZ/HPGCSZ rise edge)	t_{HKPHCS}	—	13.6	ns

(a) Write timing

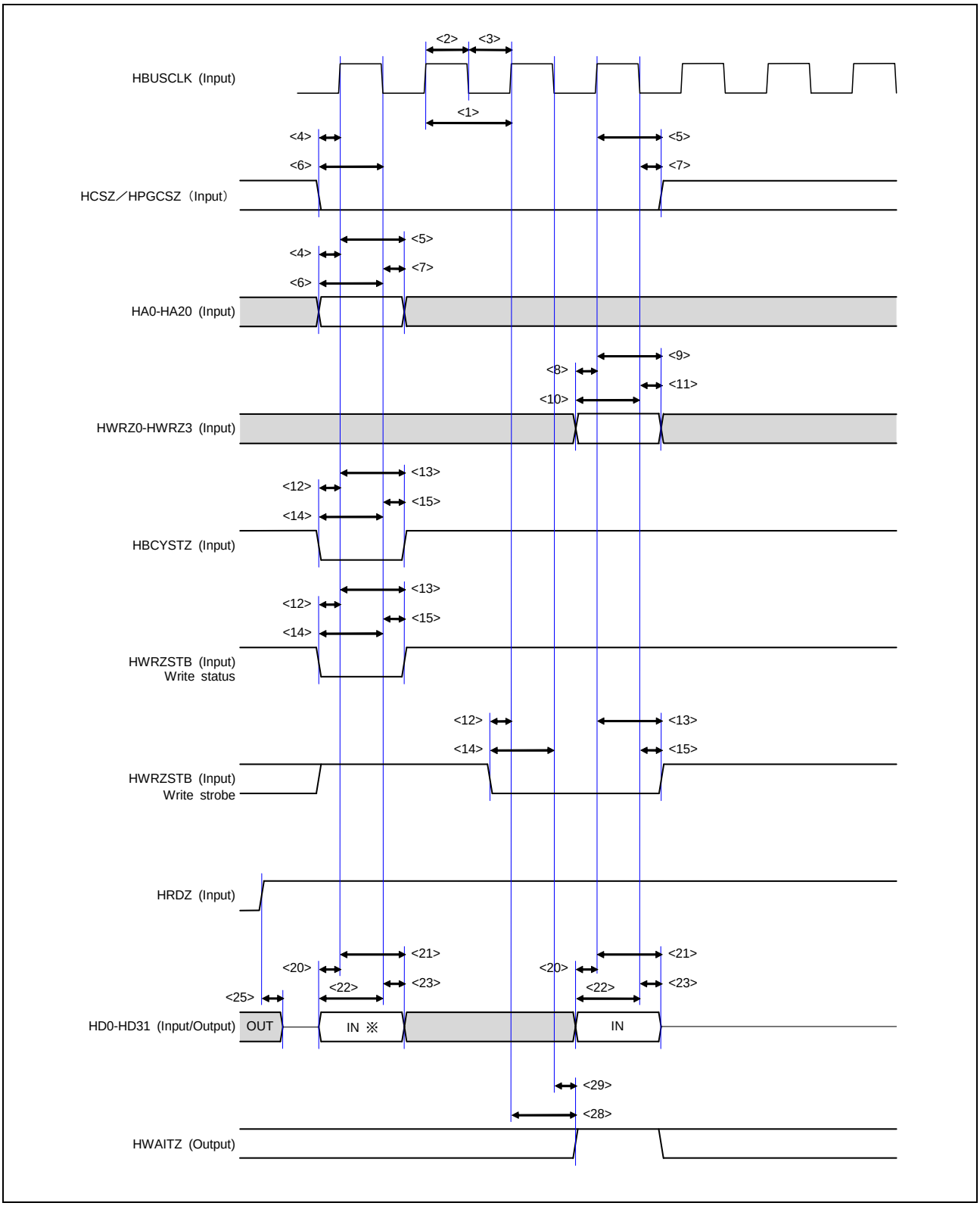

Figure External microcomputer interface write timing (Address/Data Multiplex)

(b) Read timing

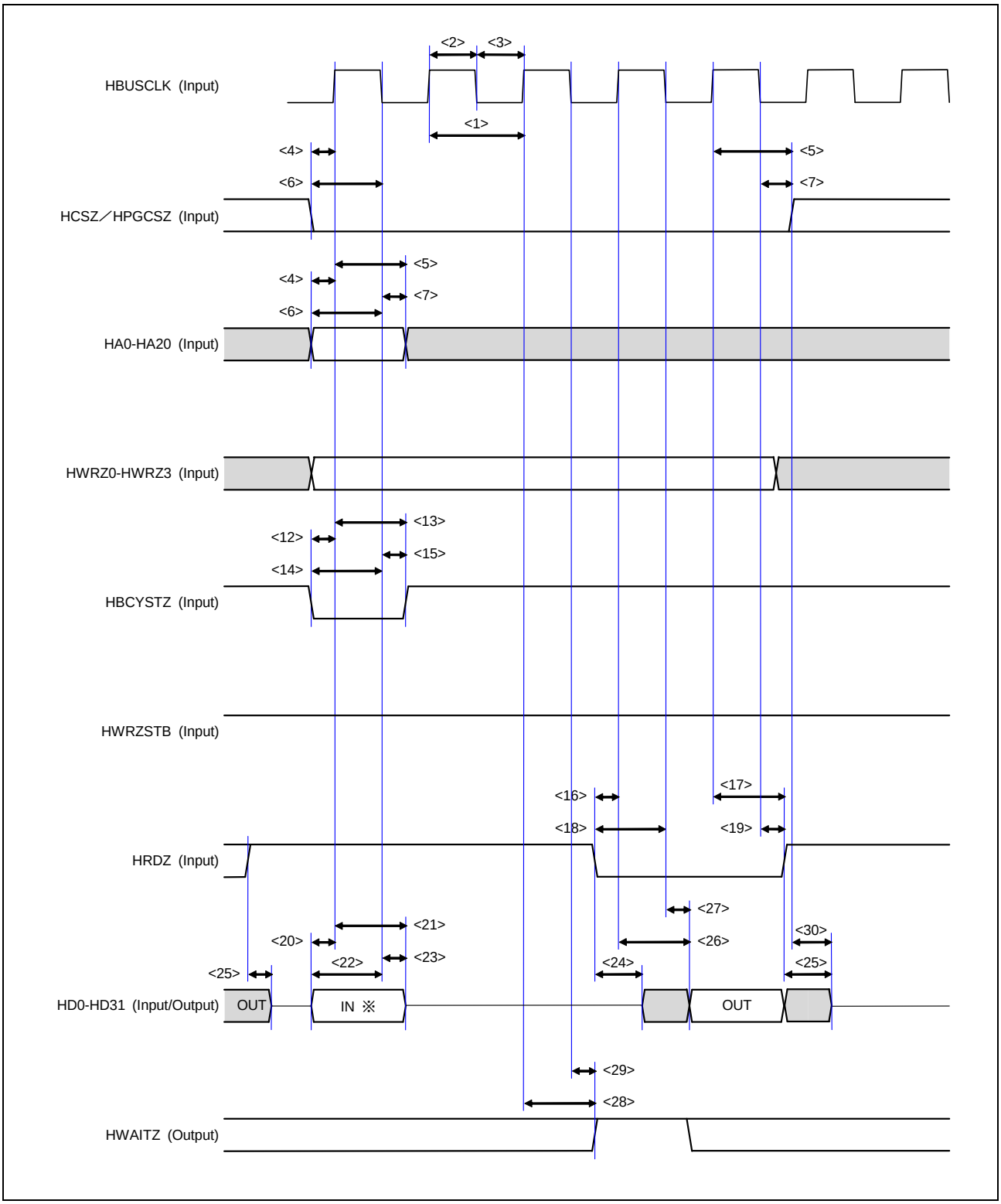

Figure External microcomputer interface read timing (Address/Data Multiplex)

B) R-IN32M3 Series User's Manual Peripheral Functions R-IN32M3-CL R-IN32M3-EC

The following note is added in 11. External Microcomputer Interface.

"Note: During a bus request for external microcomputer interface, address value must not vary. If address is changed during read access, it causes that incorrect data is returned and HWAITZ signal is NOT de-asserted."

3. Release documents

Document Title	Issue Date
R-IN32M3 Series Datasheet	Nov 30, 2015
R-IN32M3 Series User's Manual Peripheral Functions R-IN32M3-CL R-IN32M3-EC	Dec 11, 2015