

ISL70444SEH

Investigation of HTOL Effects on ISL70444SEH when Biased as a Railed Buffer

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Abstract

Renesas has performed an 800 hour High Temperature Operating Life (HTOL) test on the ISL70444SEH with all four amplifiers configured as buffers with their outputs railed high (worst case power dissipation condition – excluding comparator applications). Pre and post ATE data show zero failures for the 48 units (across three wafer lots) tested, which had a junction temperatures in excess of +150°C during the life test.

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Related Literature

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- [ISL70444SEH](#) product page

1. Pre HTOL Sample Selection and Characterization

To characterize the ISL70444SEH for the increase in channel current and for High Temperature Operating Life (HTOL) when it is used as a unity gain buffer with an input biased to one of the supply rails, a collection of 73 units was made. Of the total units, 53 were from lot X0A0PACAA, 10 units were from lot X7J8AKC, and 10 units were from lot X8W7AEH. The first lot of 53 units had failures at -58°C production testing (parametrically failing the input offset current), but it was adopted for this high temperature testing because it passed ATE at +25°C and +128°C, and the parameter in question did not relate to the output stage that sees the extra current over life. The other two lots (10 and 10 units) were from inventory so they passed all production testing. Only 48 units went on to the special HTOL; 28, 10, and 10 units respectively as the HTOL board accommodates only 48 units.

Prior to the HTOL and as a characterization of the excess current behavior, a specialized test routine was written. The basic parameters of the testing are given in [Table 1](#).

Table 1. Specialized Test Routine Parameters

Parameter	Values
Supplies (±VS)	±5V, ±10V, ±15V, ±18V, ±19.8V
Buffer Input (IN+)	+VS - 0.2V, -VS + 0.2V, +VS, -VS
Supply Current Measured (±IS)	+IS, -IS
Channels in Buffer Configuration	None, A, B, C, D

Note: Outline of the specialized excess current testing was done before and after HTOL. Outputs were unloaded.

The 180 current measurements were made for each part (all 73) at +25°C and at +128°C. As anticipated, the maximum excess channel currents were found for +IS and +128°C with the buffer input at +VS. For these conditions the positive supply current was on average slightly larger (246nA) than the negative supply current; therefore, the positive supply current was taken as the standard measure. The excess channel current statistics are presented in [Figure 1](#). The excess channel current is the difference between the supply current with a single channel biased as a buffer with the input at +VS and the supply current with no channels biased as a railed buffer. Thus, all excess channel currents are calculations and not direct measurements. Although there is some variation in the excess channel current with supply voltage, the case of ±19.8V represents the highest thermal load on the part and the subsequent focus is on that condition.

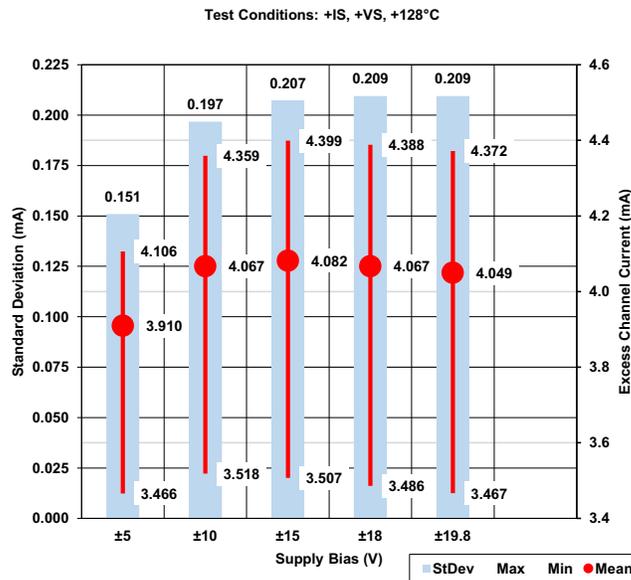


Figure 1. Statistics for Excess Channel Current on +IS for All Channels (292) at +128°C and with the Buffer Input at +VS

The next step was to look for systematic differences in the channels. The statistics that are presented in [Figure 2](#) indicate that the channels do not exhibit any systematic difference in their +IS excess channel current at +128°C and ±19.8V when configured as a buffer and biased with input at +VS.

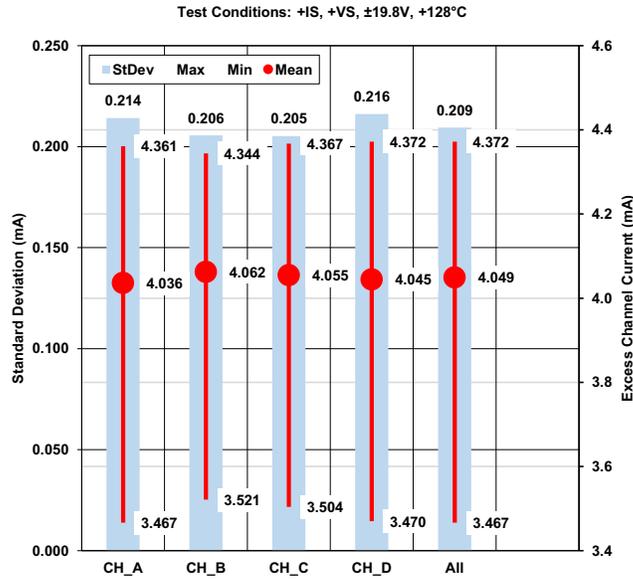


Figure 2. Statistics for Excess Channel Current on +IS by Channel at ±19.8V and +128°C with the Buffer Input at +VS

Because there appears to be no systematic channel variation, the focus is on unit behavior rather than individual channel behavior. Each device averages the channel currents to give an average unit channel current. The next variation of concern is the lot-to-lot variation. The statistics for unit average excess channel current by lot is shown in [Figure 3](#). There is a clear lot-to-lot variation.

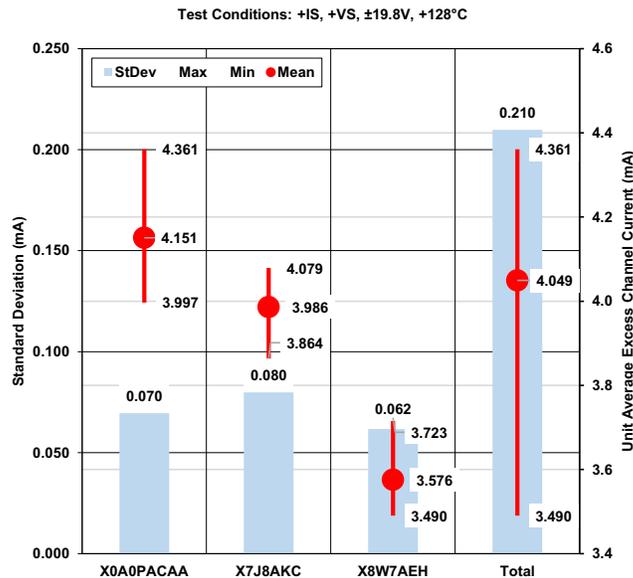


Figure 3. Statistics for Unit Average Excess Channel Current on +IS by lot at ±19.8V and +128°C with the Buffer Input at +VS

2. HTOL Set-Up

The focus now shifts to the HTOL situation which has total current (I_{total}) of a unit with all channels biased as buffers with a +VS input and at the test conditions $\pm 19.8V$, +IS, and $+128^{\circ}C$. The value of I_{total} is a calculation from the raw measurement data because the HTOL configuration has all four channels biased as railed buffers simultaneously, but the measurements were made one channel at a time. The calculation was to sum the supply currents for all four channels as railed buffers and subtract three times the base current (no channels as railed buffers). The data for this I_{total} parameter and the total current with no channels railed (I_{base}) are shown in [Table 2](#). The 48 units that were selected to go on to HTOL (in red in [Table 2](#)) were the 28 highest current parts in lot X0A0PACAA and all ten units in both lots X7J8AKC and X8W7AEH. The extreme current devices (X0A0PACAA-246 as high and X8W7AEH-930 as low) are highlighted in [Table 2](#).

Table 2. I_{total} and I_{base} Currents

Unit	I_{total} (mA)	I_{base} (mA)	Unit	I_{total} (mA)	I_{base} (mA)
X0A0PACAA-196	25.45	8.30	X0A0PACAA-299	25.10	8.58
X0A0PACAA-202	24.53	8.39	X0A0PACAA-305	25.28	8.56
X0A0PACAA-204	24.86	8.43	X0A0PACAA-306	25.42	8.64
X0A0PACAA-205	25.24	8.68	X0A0PACAA-307	25.51	8.56
X0A0PACAA-206	24.62	8.44	X0A0PACAA-308	25.06	8.54
X0A0PACAA-207	24.94	8.51	X0A0PACAA-309	24.89	8.48
X0A0PACAA-215	25.08	8.43	X0A0PACAA-310	25.37	8.66
X0A0PACAA-216	24.81	8.49	X0A0PACAA-314	25.43	8.95
X0A0PACAA-218	25.74	8.93	X0A0PACAA-317	25.77	8.91
X0A0PACAA-219	25.26	8.61	X0A0PACAA-320	25.43	8.63
X0A0PACAA-223	25.84	8.83	X0A0PACAA-321	25.32	8.66
X0A0PACAA-226	24.74	8.44	X0A0PACAA-324	24.87	8.53
X0A0PACAA-228	25.75	8.77	X0A0PACAA-327	25.45	8.64
X0A0PACAA-233	25.34	8.69	X0A0PACAA-328	25.07	8.59
X0A0PACAA-236	25.29	8.66	X0A0PACAA-329	24.65	8.45
X0A0PACAA-239	25.56	8.72	X0A0PACAA-335	25.34	8.74
X0A0PACAA-244	24.66	8.43	X7J8AKC-399	24.35	8.03
X0A0PACAA-246	26.17	9.02	X7J8AKC-400	23.94	8.16
X0A0PACAA-247	25.08	8.62	X7J8AKC-402	23.43	7.98
X0A0PACAA-248	25.40	8.77	X7J8AKC-403	24.63	8.57
X0A0PACAA-250	24.95	8.50	X7J8AKC-405	24.77	8.77
X0A0PACAA-252	24.89	8.48	X7J8AKC-407	24.34	8.22
X0A0PACAA-253	24.98	8.56	X7J8AKC-408	24.68	8.43
X0A0PACAA-255	24.91	8.44	X7J8AKC-410	24.72	8.47
X0A0PACAA-256	25.43	8.86	X7J8AKC-411	24.10	8.37
X0A0PACAA-260	25.22	8.55	X7J8AKC-413	23.72	8.25
X0A0PACAA-267	25.61	8.76	X8W7AEH-928	22.62	7.73
X0A0PACAA-271	24.40	8.41	X8W7AEH-929	22.11	7.83
X0A0PACAA-274	25.47	8.60	X8W7AEH-930	21.67	7.71
X0A0PACAA-277	25.46	8.81	X8W7AEH-932	22.06	7.80
X0A0PACAA-278	26.03	8.59	X8W7AEH-933	21.91	7.79
X0A0PACAA-283	25.16	8.53	X8W7AEH-935	22.05	7.85

Table 2. I_{total} and I_{base} Currents (Continued)

Unit	I _{total} (mA)	I _{base} (mA)	Unit	I _{total} (mA)	I _{base} (mA)
X0A0PACAA-284	25.25	8.58	X8W7AEH-936	21.98	7.78
X0A0PACAA-286	24.88	8.53	X8W7AEH-945	22.27	7.88
X0A0PACAA-287	25.07	8.56	X8W7AEH-946	22.33	7.89
X0A0PACAA-293	24.62	8.41	X8W7AEH-947	22.11	7.81
X0A0PACAA-298	25.50	8.79			

Note: The I_{total} (all four channels as +VS buffer inputs) and I_{base} (no buffers railed) currents were at +128°C, ±19.8V, and +IS for the 73 parts tested prior to HTOL. The red entries are the parts that were selected for HTOL. The yellow highlighted entries are the extremes of I_{total}.

The goal in HTOL was to have the coolest device in a condition that gave a “hot spot” silicon temperature of at least +150°C. The “hot spot” is created by a significant portion (43%) of the total channel current going through a small device with essentially the full applied supply voltage across it. The “hot spot” temperature had to be derived from the total current of the monitored devices and simulation results on the “hot spot” performance electrically and thermally. Calculating the “hot spot” temperature using a bulk junction to case thermal resistance of 4.2°C/W (this is a somewhat lower θ_{JC} than the datasheet 9°C/W based on later simulations), a simulated “hot spot” thermal resistance to case of 374°C/W, and a 43% portion of I_{total} flowing through the “hot spot” results in an estimated 38°C rise over case temperature for the low current (X8W7AEH-930) device and an estimated 46°C rise in temperature for the high current device (X0A0PACAA-246). To ensure that the coolest part has a “hot spot” temperature of +150°C means that the cool device (X8W7AEH-930) must have a case temperature of +112°C.

The HTOL board (six columns by eight rows) was loaded with the highest current device (X0A0PACAA-246) at one of the four center locations to give the highest local temperature on the hottest device. The lowest current unit (X8W7AEH-930) was loaded at one corner of the board to give the lowest local temperature on the coolest device. Both of these monitor devices had thermocouples epoxied to the bottom of the case to allow monitoring of the case temperature during HTOL. The map of how the HTOL board was loaded is presented in [Table 3 on page 5](#).

The HTOL board was powered up (±19.8V) first with the oven set at 60°C and allowed to stabilize. The monitor devices registered case temperatures of 100°C and 132°C. Based on the thermal calculations the oven was adjusted to 72°C to push the corner device to approximately 112°C for a projected maximum “hot spot” junction temperature of 150°C. After another stabilization period the monitor devices registered case temperatures of 114°C and 142°C. The total current for the 48 units was 1.202A, which was slightly higher than the 1.178A found by summing the I_{total} currents for the selected 48 units at +128°C. At this point the timing for the HTOL was begun (8:30 AM, May 8, 2018).

Table 3. HTOL Board Loading Diagram

X0A0PACAA 196	X0A0PACAA 205	X0A0PACAA 218	X0A0PACAA 219	X0A0PACAA 223	X0A0PACAA 228
X0A0PACA A233	X0A0PACAA 236	X0A0PACAA 239	X0A0PACAA 248	X0A0PACAA 256	X0A0PACAA 267
X0A0PACAA 274	X0A0PACAA 277	X0A0PACAA 278	X0A0PACAA 284	X0A0PACAA 298	X0A0PACAA 305
X0A0PACAA 306	X0A0PACAA 307	X0A0PACAA 310	X0A0PACAA 314	X0A0PACAA 317	X0A0PACAA 320
X0A0PACAA 321	X0A0PACAA 327	X0A0PACAA 335	X0A0PACAA 246	X7J8AKC 399	X7J8AKC 400
X7J8AKC 402	X7J8AKC 403	X7J8AKC 405	X7J8AKC 407	X7J8AKC 408	X7J8AKC 410
X7J8AKC 411	X7J8AKC 413	X8W7AEH 928	X8W7AEH 929	X8W7AEH 932	X8W7AEH 933
X8W7AEH 935	X8W7AEH 936	X8W7AEH 945	X8W7AEH 946	X8W7AEH 947	X8W7AEH 930

Note: The door to the oven is located at the bottom of the diagram. The entries in red indicate attached thermocouples for monitoring case temperature.

3. 168 Hour Downpoint at +128°C

The channel current measurements at +25°C and +128°C before HTOL identified each measurement by part number and channel. At the 168 hour downpoint the channel current measurements were repeated, keeping track of part number and channel. This allowed paired data to be used to find the delta in channel current by individual channels. This data was broken into the control units (25 parts) and the HTOL units (48 parts) and the results plotted in [Figure 4](#) for the case of ±19.8V, +IS, +VS, and +128°C. The 168 hour HTOL data appears to have a slight “tail” to the distribution with a few parts showing tens of μA increase in channel currents. The bulk of the control and HTOL distributions correlated quite well. The extremes of the current deltas are -14μA and +51μA with both being HTOL units. These correspond to -0.1115% and +0.3917% channel current changes. The extremes for the control group of parts were -9μA and +12μA, corresponding to -0.0727% and +0.0914%. These changes are within ±0.5% and represent reasonable measurement repeatability noise.

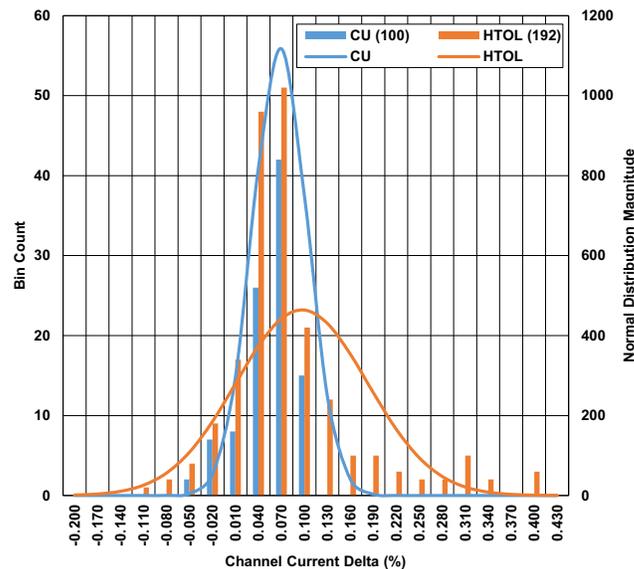


Figure 4. Channel Current Deltas for Conditions of ±19.8V, +IS, +VS, +128°C at the 168 hour Downpoint

After measuring the channel currents at the 168 hour downpoint, the HTOL parts were returned to the HTOL oven with the same device placement as before, according to the map of [Table 3 on page 5](#). The oven was still set to +72°C as before. After stabilization, the two parts with thermocouples registered +135°C and +142°C. The corner location (SN930) was markedly different from the temperature recorded at the 168 hour downpoint (+114°C). No good explanation exists for why the temperature of this device increased by 21°C due to the downpoint unloading and reloading. This particular part registered channel current deltas at +128°C ranging from -0.0731% to -0.0215%, so there was no indication of a change in the part at the downpoint measurements. The higher temperature is an indication that the part is operating at a higher temperature than originally calculated at the start of HTOL. Because this represents a more severe stressing than otherwise, the HTOL was allowed to continue. This places the calculated silicon temperatures between +173°C and +188°C. That puts both estimates well beyond a +150°C silicon temperature target.

4. 800 Hour HTOL Completion Results

At the 800 hour downpoint the production testing at both +25°C and at +125°C was performed on all parts, the control units and the HTOL units, passed. In addition, at the 800 hours downpoint the channel current measurements were repeated keeping track of part number and channel. This allowed paired data to be used to find the delta in channel current by individual channels from start to 800 hours. This data was broken into the control units (25 parts) and the HTOL units (48 parts) and the results are plotted in [Figure 5 on page 7](#) for the case of ±19.8V, +IS, +VS, and +128°C. The HTOL data appears to have a slight “tail” to the distribution with a few parts showing small fractional percentage increase in channel currents. The bulk of the distributions correlated quite well. The extremes of the current deltas were -0.196% and +0.282% with the former being a control unit (SN202) and the latter being an HTOL unit (SN307).

The controls ranged from -0.196% to +0.020% while the HTOL units ranged from -0.129% to +0.282%. The standard deviation for the HTOL units (192 channels) was slightly larger at 0.080% as compared to the controls at 0.034% (100 channels). The mean deviation for the control group was -0.046%, while the HTOL units came in at +0.008%. All of these results are within expected measurement repeatability variations so the conclusion was that the HTOL did not result in any systematic changes to the excess current behavior.

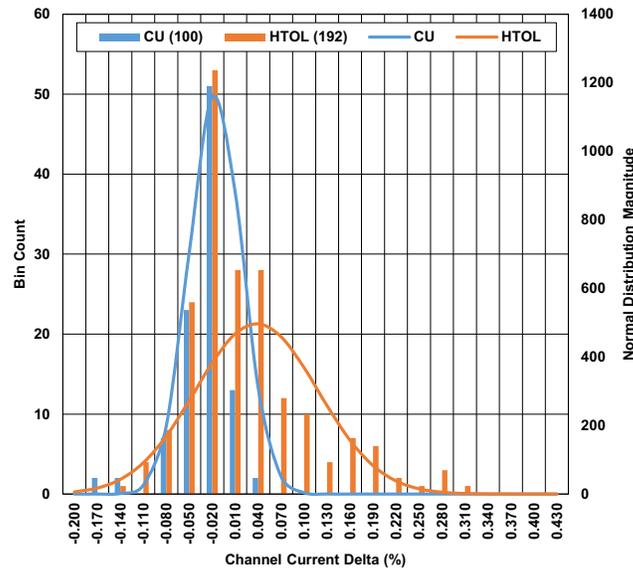


Figure 5. Channel Current Deltas for Conditions of $\pm 19.8V$, +IS, +VS, +128°C at the 800 hour Downpoint

5. Conclusions on Specialized HTOL of ISL70444SEH

The 48 ISL70444SEH units from three lots (28 from X0A0PACAA, 10 from X7J8AKC, and 10 from X8W7AEH) were subjected to specialized HTOL stressing to 800 hours. The 25 control units accompanied the test units at each testing point. The HTOL stress condition was to have all four channels biased as railed input buffers (+19.8V) with supply voltages of $\pm 19.8V$. This saturated the output against the positive rail. The parts were loaded into a 48 socket board which was placed in a +72°C oven. Two parts had thermocouples attached to the bottom of the packages; the highest current part (SN246 with 26.17mA at a central board location) and the lowest current part (SN930 with 21.67mA at a corner location) which registered +142°C and +135°C, respectively for the bulk of the HTOL duration. Calculations of the “hot spot” silicon temperatures indicate values between +173°C and +188°C.

All 73 units (48 HTOL and 25 controls) passed production ATE testing at +25°C and +128°C both before stressing and after the HTOL stressing. All units were also tested with a specialized program that measured the “excess current” under buffer operation conditions. The full set of test conditions is presented in [Table 1 on page 2](#). Only the case of the input at +19.8V with supplies at $\pm 19.8V$ are discussed here because these results encompassed all the other conditions.

The channel currents were treated as paired data and the delta over 800 hours of HTOL are presented in [Figure 5](#). The full range of channel current changes was confined to the range -0.196% and +0.282% with the control and HTOL data being very close. It is concluded that extended operation (800 hours) with all four channels as railed buffers does not represent a reliability threat if the case temperatures are maintained at +135°C or less.

6. Revision History

Rev.	Date	Description
0.00	Aug 10, 2018	Initial release

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