Smart Configurator for RX V2.1.0

Release Note

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Rev.1.01
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Introduction

Thank you for using the Smart Configurator for RX.

This document describes the restrictions and points for caution. Read this document before using the product.

Contents

1. Introduction

Smart Configurator is a utility for combining software to meet your needs. It supports the following three functions related to the embedding of Renesas drivers in your systems: importing middleware, generating driver code, and setting pins.

1.1 System requirements

The operating environment is as follows.

1.1.1 PC

- IBM PC/AT compatibles (Windows® 10, Windows® 8.1, Windows® 7)
- Processor: 1 GHz or higher (must support hyper-threading, multi-core CPUs)
- Memory capacity: 2 GB or more recommended. Minimum requirement is 1 GB or more (64-bit Windows requires 2 GB or more)
- Hard disk capacity: 200 MB or more spare capacity
- Display: 1024 x 768 or higher resolution, 65,536 or more colors
- All other necessary software environments in addition to Windows OS: .NET Framework version4.5

1.1.2 Development Environments

- Renesas electronics Compiler for RX [CC-RX] V3.01.00 or later
- GNURX 4.8.4.201803 or later
- IAR Embedded Workbench 4.10.2 or later

2. Support List

2.1 Support Devices List

Below is a list of devices supported by the Smart Configurator for RX V2.1.0.

Table 1-1 Support Devices

Group (HW Manual number)	PIN	Device name
RX110 Group (R01UH0421EJ0120)	36pin	R5F5110HAxLM, R5F5110JAxLM, R5F51101AxLM, R5F51103AxLM
	40pin	R5F51101AxNF, R5F51103AxNF, R5F5110HAxNF, R5F5110JAxNF
	48pin	R5F51101AxNE, R5F51103AxNE, R5F51104AxNE, R5F51105AxNE, R5F5110JAxNE, R5F51101AxFL, R5F51103AxFL, R5F51104AxFL, R5F51105AxFL, R5F5110JAxFL
	64pin	R5F51101AxLF, R5F51103AxLF, R5F51104AxLF, R5F51105AxLF, R5F5110JAxLF, R5F51101AxFK, R5F51103AxFK, R5F51104AxFK, R5F51105AxFK, R5F5110JAxFK, R5F51101AxFM, R5F51103AxFM, R5F51104AxFM, R5F51105AxFM, R5F5110JAxFM
RX111 Group (R01UH0365EJ0130)	36pin	R5F51111AxLM, R5F51113AxLM, R5F5111JAxLM
	40pin	R5F51111AxNF, R5F51113AxNF, R5F5111JAxNF
	48pin	R5F51111AxFL, R5F51113AxFL, R5F51114AxFL, R5F51115AxFL, R5F51116AxFL, R5F51117AxFL, R5F51118AxFL, R5F5111JAxFL, R5F51111AxNE, R5F51113AxNE, R5F51114AxNE, R5F51115AxNE, R5F51116AxNE, R5F51117AxNE, R5F51118AxNE, R5F5111JAxNE
	64pin	R5F51111AxFM, R5F51113AxFM, R5F51114AxFM, R5F51115AxFM, R5F51116AxFM, R5F51117AxFM, R5F51118AxFM, R5F5111JAxFM, R5F51111AxFK, R5F51113AxFK, R5F51114AxFK, R5F51115AxFK, R5F51116AxFK, R5F51117AxFK, R5F51118AxFK, R5F5111JAxFK, R5F51111AxLF, R5F51113AxLF, R5F51114AxLF, R5F51115AxLF, R5F51116AxLF, R5F51117AxLF, R5F51118AxLF, R5F5111JAxLF
RX113 Group (R01UH0448EJ0110)	64pin	R5F51135AxFM, R5F51136AxFM, R5F51137AxFM, R5F51138AxFM
	100pin	R5F51135AxLJ, R5F51136AxLJ, R5F51137AxLJ, R5F51138AxLJ, R5F51135AxFP, R5F51136AxFP, R5F51137AxFP, R5F51138AxFP
RX130 Group (R01UH0560EJ0200)	48pin	R5F51303AxFL, R5F51305AxFL, R5F51303AxNE, R5F51305AxNE, R5F51306AxNE, R5F51306AxFL, R5F51307AxNE, R5F51307AxFL, R5F51308AxNE, R5F51308AxFL, R5F51306BxFL
	64pin	R5F51303AxFM, R5F51305AxFM, R5F51303AxFK, R5F51305AxFK, R5F51306AxFK, R5F51306AxFM, R5F51307AxFK, R5F51307AxFM, R5F51308AxFK, R5F51308AxFM R5F51308AxFK, R5F51308AxFM, R5F51306BxFK, R5F51306BxFM
	80pin	R5F51303AxFN, R5F51305AxFN, R5F51306AxFN, R5F51306BxFN
	100pin	R5F51305AxFP, R5F51306AxFP, R5F51307AxFP, R5F51308AxFP, R5F51305BxFP, R5F51306BxFP
RX230 Group (R01UH0496EJ0110)	48pin	R5F52305AxNE, R5F52306AxNE, R5F52305AxFL, R5F52306AxFL
	64pin	R5F52305AxND, R5F52306AxND, R5F52305AxFM, R5F52306AxFM, R5F52305AxLF, R5F52306AxLF
	100pin	R5F52305AxLA, R5F52306AxLA, R5F52305AxFP, R5F52306AxFP

Table 1-2 Support Devices

Group (HW Manual number)	PIN	Device name
RX231 Group (R01UH0496EJ0110)	48pin	R5F52315AxNE, R5F52316AxNE, R5F52317AxNE, R5F52318AxNE, R5F52315CxNE, R5F52316CxNE, R5F52317BxNE, R5F52318BxNE, R5F52315AxFL, R5F52316AxFL, R5F52317AxFL, R5F52318AxFL, R5F52315CxFL, R5F52316CxFL, R5F52317BxFL, R5F52318BxFL
	64pin	R5F52315AxND, R5F52316AxND, R5F52317AxND, R5F52318AxND, R5F52315CxND, R5F52316CxND, R5F52317BxND, R5F52318BxND, R5F52315AxFM, R5F52316AxFM, R5F52317AxFM, R5F52318AxFM, R5F52315CxFM, R5F52316CxFM, R5F52317BxFM, R5F52318BxFM, R5F52315CxLF, R5F52316CxLF
	100pin	R5F52315AxLA, R5F52316AxLA, R5F52317AxLA, R5F52318AxLA, R5F52315CxLA, R5F52316CxLA, R5F52317BxLA, R5F52318BxLA, R5F52315AxFP, R5F52316AxFP, R5F52317AxFP, R5F52318AxFP, R5F52315CxFP, R5F52316CxFP, R5F52317BxFP, R5F52318BxFP
RX23T Group (R01UH0520EJ0110)	48pin	R5F523T3AxFL, R5F523T5AxFL
	52pin	R5F523T5AxFD, R5F523T3AxFD
	64pin	R5F523T5AxFM, R5F523T3AxFM
RX24T Group (R01UH0576EJ0200)	64pin	R5F524TAAxFM, R5F524T8AxFM
	80pin	R5F524TAAxFF, R5F524T8AxFF, R5F524TAAxFN, R5F524T8AxFN
	100pin	R5F524TCAxFP, R5F524T8AxFP, R5F524TBAxFP, R5F524TEAxFP, R5F524TAAxFP
RX24U Group (R01UH0658EJ0100)	100pin	R5F524UEAxFP, R5F524UCAxFP, R5F524UBAxFP
	144pin	R5F524UEAxFB, R5F524UBAxFB, R5F524UCAxFB
RX64M Group (R01UH0377EJ0110)	100pin	R5F564MFCxFP, R5F564MFCxLJ, R5F564MFDxFP, R5F564MFDxLJ, R5F564MGCxFP, R5F564MGCxLJ, R5F564MGDxFP, R5F564MGDxLJ, R5F564MJCxFP, R5F564MJCxLJ, R5F564MJDxFP, R5F564MJDxLJ, R5F564MLCxFP, R5F564MLCxLJ, R5F564MLDxFP, R5F564MLDxLJ
	144/145pin	R5F564MFCxFB, R5F564MFCxLK, R5F564MFDxFB, R5F564MFDxLK, R5F564MGCxFB, R5F564MGCxLK, R5F564MGDxFB, R5F564MGDxLK, R5F564MJCxFB, R5F564MJCxLK, R5F564MJDxFB, R5F564MJDxLK, R5F564MLCxFB, R5F564MLCxLK, R5F564MLDxFB, R5F564MLDxLK
	176/177pin	R5F564MFDxFC, R5F564MFDxBG, R5F564MFDxLC, R5F564MFCxFC, R5F564MFCxBG, R5F564MFCxLC, R5F564MGDxFC, R5F564MGDxBG, R5F564MGDxLC, R5F564MGCxFC, R5F564MGCxBG, R5F564MGCxLC, R5F564MJDxFC, R5F564MJDxBG, R5F564MJDxLC, R5F564MJCxFC, R5F564MJCxBG, R5F564MJCxLC, R5F564MLDxFC, R5F564MLDxBG, R5F564MLDxLC, R5F564MLCxFC, R5F564MLCxBG, R5F564MLCxLC

Table 1-3 Support Devices

Group (HW Manual number)	PIN	Device name
RX65N Group (R01UH0590EJ0210)	100pin	R5F565N9AxLJ, R5F565N9BxLJ, R5F565N9ExLJ, R5F565N9FxLJ, R5F565N7AxLJ, R5F565N7BxLJ, R5F565N7ExLJ, R5F565N7FxLJ, R5F565N4AxLJ, R5F565N4BxLJ, R5F565N4ExLJ, R5F565N4FxLJ, R5F565N9AxFP, R5F565N9BxFP, R5F565N9ExFP, R5F565N9FxFP, R5F565N7AxFP, R5F565N7BxFP, R5F565N7ExFP, R5F565N7FxFP, R5F565N4AxFP, R5F565N4BxFP, R5F565N4ExFP, R5F565N4FxFP, R5F565NCHxLJ, R5F565NCDxLJ, R5F565NEHxLJ, R5F565NEDxLJ, R5F565NCHxFP, R5F565NCDxFP, R5F565NEHxFP, R5F565NEDxFP
	144/145pin	R5F565N9AxFB, R5F565N9BxFB, R5F565N9ExFB, R5F565N9FxFB, R5F565N7AxFB, R5F565N7BxFB, R5F565N7ExFB, R5F565N7FxFB, R5F565N4AxFB, R5F565N4BxFB, R5F565N4ExFB, R5F565N4FxFB, R5F565NCHxFB, R5F565NCDxFB, R5F565NEHxFB, R5F565NEDxFB, R5F565N9AxLK, R5F565N9BxLK, R5F565N9ExLK, R5F565N9FxLK, R5F565N7AxLK, R5F565N7BxLK, R5F565N7ExLK, R5F565N7FxLK, R5F565N4AxLK, R5F565N4BxLK, R5F565N4ExLK, R5F565N4FxLK, R5F565NCHxLK, R5F565NCDxLK, R5F565NEHxLK, R5F565NEDxLK
	176/177pin	R5F565NCHxBG, R5F565NCDxBG, R5F565NEHxBG, R5F565NEDxBG, R5F565NCHxFC, R5F565NCDxFC, R5F565NEHxFC, R5F565NEDxFC, R5F565NCHxLC, R5F565NCDxLC, R5F565NEHxLC, R5F565NEDxLC
RX651 Group (R01UH0590EJ0210)	64pin	R5F5651CHxFM,R5F56514FxFM, R5F5651EHxFM, R5F5651CDxFM, R5F56514FxBP, R5F56514BxFM, R5F56519FxBP, R5F5651CDxBP, R5F5651EDxBP, R5F5651EDxFM, R5F56517BxBP, R5F5651EHxBP, R5F56519BxBP, R5F56517FxBP, R5F5651CHxBP, R5F56519FxFM, R5F56517BxFM, R5F56514BxBP, R5F56519BxFM, R5F56517FxFM
	100pin	R5F56519AxLJ, R5F56519BxLJ, R5F56519ExLJ, R5F56519FxLJ, R5F56517AxLJ, R5F56517BxLJ, R5F56517ExLJ, R5F56517FxLJ, R5F56514AxLJ, R5F56514BxLJ, R5F56514ExLJ, R5F56514FxLJ, R5F56519AxFP, R5F56519BxFP, R5F56519ExFP, R5F56519FxFP, R5F56517AxFP, R5F56517BxFP, R5F56517ExFP, R5F56517FxFP, R5F56514AxFP, R5F56514BxFP, R5F56514ExFP, R5F56514FxFP
	144/145pin	R5F56519AxFB, R5F56519BxFB, R5F56519ExFB, R5F56519FxFB, R5F56517AxFB, R5F56517BxFB, R5F56517ExFB, R5F56517FxFB, R5F56514AxFB, R5F56514BxFB, R5F56514ExFB, R5F56514FxFB, R5F5651CDxFB, R5F5651CHxFB, R5F5651EDxFB, R5F5651EHxFB, R5F56519AxLK, R5F56519BxLK, R5F56519ExLK, R5F56519FxLK, R5F56517AxLK, R5F56517BxLK, R5F56517ExLK, R5F56517FxLK, R5F56514AxLK, R5F56514BxLK, R5F56514ExLK, R5F56514FxLK, R5F5651CDxLK, R5F5651CHxLK, R5F5651EDxLK, R5F5651EHxLK
	176/177pin	R5F5651CDxBG, R5F5651CDxFC, R5F5651CHxBG, R5F5651CHxFC, R5F5651EDxBG, R5F5651EDxFC, R5F5651EHxBG, R5F5651EHxFC, R5F5651CDxLC, R5F5651CHxLC, R5F5651EDxLC, R5F5651EHxLC

Table 1-4 Support Devices

Group (HW Manual number)	PIN	Device name
RX66T Group (R01UH0749EJ0100)	64pin	R5F566TAAxFM, R5F566TAExDFM, R5F566TEAxFM, R5F566TEExFM
	80pin	R5F566TAAxFF, R5F566TAExFF, R5F566TEAxFF, R5F566TEExFF, R5F566TAAxFN, R5F566TAExFN, R5F566TEAxFN, R5F566TEExFN
	100pin	R5F566TKCxFP, R5F566TAExFP, R5F566TFFxFP, R5F566TFCxFP, R5F566TFExFP, R5F566TFBxFP, R5F566TFAxFP, R5F566TABxFP, R5F566TAFxFP, R5F566TEFxFP, R5F566TKFxFP, R5F566TKGxFP, R5F566TKAxFP, R5F566TKExFP, R5F566TKBxFP, R5F566TEBxFP, R5F566TEExFP, R5F566TEAxFP, R5F566TAAxFP, R5F566TFGxFP
	112pin	R5F566TAAxFH, R5F566TAExFH, R5F566TEExFH, R5F566TEAxFH
	144pin	R5F566TKCxFB, R5F566TFGxFB, R5F566TFCxFB, R5F566TKGxFB
RX71M Group (R01UH0493EJ0110)	100pin	R5F571MLCxFP, R5F571MLDxFP, R5F571MLGxFP, R5F571MLHxFP, R5F571MJCxFP, R5F571MJDxFP, R5F571MJGxFP, R5F571MJHxFP, R5F571MGCxFP, R5F571MGDxFP, R5F571MGGxFP, R5F571MGHxFP, R5F571MFCxFP, R5F571MFDxFP, R5F571MFGxFP, R5F571MFHxFP, R5F571MLCxLJ, R5F571MLDxLJ, R5F571MLGxLJ, R5F571MLHxLJ, R5F571MJCxLJ, R5F571MJDxLJ, R5F571MJGxLJ, R5F571MJHxLJ, R5F571MGCxLJ, R5F571MGDxLJ, R5F571MGGxLJ, R5F571MGHxLJ, R5F571MFCxLJ, R5F571MFDxLJ, R5F571MFGxLJ, R5F571MFHxLJ
	144/145pin	R5F571MLCxLK, R5F571MLDxLK, R5F571MLGxLK, R5F571MLHxLK, R5F571MJCxLK, R5F571MJDxLK, R5F571MJGxLK, R5F571MJHxLK, R5F571MGCxLK, R5F571MGDxLK, R5F571MGGxLK, R5F571MGHxLK, R5F571MFCxLK, R5F571MFDxLK, R5F571MFGxLK, R5F571MFHxLK, R5F571MLCxFB, R5F571MLDxFB, R5F571MLGxFB, R5F571MLHxFB, R5F571MJCxFB, R5F571MJDxFB, R5F571MJGxFB, R5F571MJHxFB, R5F571MGCxFB, R5F571MGDxFB, R5F571MGGxFB, R5F571MGHxFB, R5F571MFCxFB, R5F571MFDxFB, R5F571MFGxFB, R5F571MFHxFB
	176/177pin	R5F571MLCxFC, R5F571MLDxFC, R5F571MLGxFC, R5F571MLHxFC, R5F571MJCxFC, R5F571MJDxFC, R5F571MJGxFC, R5F571MJHxFC, R5F571MGCxFC, R5F571MGDxFC, R5F571MGGxFC, R5F571MGHxFC, R5F571MFCxFC, R5F571MFDxFC, R5F571MFGxFC, R5F571MFHxFC, R5F571MLCxLC, R5F571MLDxLC, R5F571MLGxLC, R5F571MLHxLC, R5F571MJCxLC, R5F571MJDxLC, R5F571MJGxLC, R5F571MJHxLC, R5F571MGCxLC, R5F571MGDxLC, R5F571MGGxLC, R5F571MGHxLC, R5F571MFCxLC, R5F571MFDxLC, R5F571MFGxLC, R5F571MFHxLC, R5F571MLCxBG, R5F571MLDxBG, R5F571MLGxBG, R5F571MLHxBG, R5F571MJCxBG, R5F571MJDxBG, R5F571MJGxBG, R5F571MJHxBG, R5F571MGCxBG, R5F571MGDxBG, R5F571MGGxBG, R5F571MGHxBG, R5F571MFCxBG, R5F571MFDxBG, R5F571MFGxBG, R5F571MFHxBG
RX72T Group (R01UH0803EJ0050)	100pin	R5F572TKExFP, R5F572TFFxFP, R5F572TKFxFP, R5F572TFGxFP, R5F572TKCxFP, R5F572TFBxFP, R5F572TFExFP, R5F572TFCxFP, R5F572TFAxFP, R5F572TKAxFP, R5F572TKBxFP, R5F572TKGxFP
	144pin	R5F572TKGxFB, R5F572TKCxFB, R5F572TFGxFB, R5F572TFCxFB

2.2 Support Components List

Below is a list of Components supported by the Smart Configurator for RX V2.1.0.

Table 2-1 Support Components **○: Support, /: Non-support**

No	Components	Mode	RX110	RX111	RX113	RX130	RX230, RX231	RX23T	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	RX2T	Remarks
1	8-Bit Timer	-	/	/	○	○	○	○	○	○	○	○	○	○	
2	CRC Calculator	-	○	○	○	○	○	○	○	○	○	○	○	○	
3	D/A Converter	-	/	○	○	○	○	○	○	○	○	○	○	○	
4	DMA Controller	-	/	/	/	/	○	/	/	○	○	○	○	○	
5	I2C Slave Mode	I2C mode	○	○	○	○	○	○	○	○	○	○	○	○	
		SMBus mode	○	○	○	○	○	○	○	○	○	○	○	○	
6	I2C Master Mode	I2C mode	○	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 3
		SMBus mode	○	○	○	○	○	○	○	○	○	○	○	○	
7	LCD Controller		/	/	○	/	/	/	/	/	/	/	/	/	
8	PWM Mode Timer	PWM mode 1	○	○	○	○	○	○	○	○	○	○	○	○	
		PWM mode 2	○	○	○	○	○	○	○	○	○	○	○	○	
9	SCI/SCIF Clock Synchronous Mode	Transmission	○	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Reception	○	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2, 3, 4 in Table 4
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
10	SCI/SCIF Asynchronous Mode	Transmission	○	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Reception	○	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Multi-processor Transmission	○	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Multi-processor Reception	○	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
		Multi-processor Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	○	Refer to No 2 in Table 4
11	SPI Clock Synchronous Mode	Slave transmit/receive	○	○	○	○	○	○	○	○	○	○	○	○	
		Slave transmit only	○	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit/receive	○	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit only	○	○	○	○	○	○	○	○	○	○	○	○	
12	SPI Operation Mode	Slave transmit/receive	○	○	○	○	○	○	○	○	○	○	○	○	
		Slave transmit only	○	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit/receive	○	○	○	○	○	○	○	○	○	○	○	○	
		Master transmit only	○	○	○	○	○	○	○	○	○	○	○	○	
		Multi-master transmit/receive	○	○	○	○	○	○	○	○	○	○	○	○	
		Multi-master transmit only	○	○	○	○	○	○	○	○	○	○	○	○	
13	Event Link Controller	-		○	○	○	○	/	/	○	○	○	○	○	
14	Watchdog Timer	-	○	○	○	○	○	○	○	○	○	○	○	○	
15	Clock Frequency Accuracy Measurement Circuit	-	○	○	○	○	○	○	○	○	○	○	○	○	

Table 2-2 Support Components

○: Support, /: Non-support

No	Components	Mode	RX110	RX111	RX113	RX130	RX230, RX231	RX23T	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	RX72T	Remarks
16	Group Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	○	○	
17	Comparator	-	/	/	○	○	○	/	/	/	/	○	/	○	
18	Compare Match Timer	-	○	○	○	○	○	○	○	○	○	○	○	○	Refer to No 3 in Table 3
19	Single Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	○	○	
20	Smart Card Interface Mode	Transmission	○	○	○	○	○	○	○	○	○	○	○	○	
		Reception	○	○	○	○	○	○	○	○	○	○	○	○	
		Transmission/Reception	○	○	○	○	○	○	○	○	○	○	○	○	
21	Dead-time Compensation Counter	-	○	○	○	○	○	○	○	○	○	○	○	○	
22	Data Transfer Controller	-	○	○	○	○	○	○	○	○	○	○	○	○	
23	Data Operation Circuit	-	○	○	○	○	○	○	○	○	○	○	○	○	
24	Normal Mode Timer		○	○	○	○	○	○	○	○	○	○	○	○	
25	Buses	-	○	○	○	○	○	○	○	○	○	○	○	○	
26	Programmable Pulse Generator	-	/	/	/	/	/	/	/	○	○	/	○	/	
27	Ports	-	○	○	○	○	○	○	○	○	○	○	○	○	
28	Port Output Enable	-	/	○	○	○	○	○	○	○	○	○	○	○	
29	Real Time Clock	Binary	○	○	○	○	○	/	/	○	○	/	○	/	
		Calendar	○	○	○	○	○	/	/	○	○	/	○	/	
30	Remote Control Signal Receiver	-	/	/	/	○	/	/	/	/	/	/	/	/	
31	Low-Power Timer	-	/	/	○	○	○	/	/	/	/	/	/	/	
32	Phase Counting Mode Timer	-	○	○	○	○	○	○	○	○	○	○	○	○	
33	Interrupt Controller	-	○	○	○	○	○	○	○	○	○	○	○	○	
34	General PWM Timer	Saw-wave PWM mode	/	/	/	/	/	○	○	○	/	○	○	○	Refer to No 1 in Table 4
		Saw-wave one-shot pulse mode	/	/	/	/	/	○	○	○	/	○	○	○	Refer to No 1 in Table 4
		Triangle-wave PWM mode 1	/	/	/	/	/	○	○	○	/	○	○	○	Refer to No 1 in Table 4
		Triangle-wave PWM mode 2	/	/	/	/	/	○	○	○	/	○	○	○	Refer to No 1 in Table 4
		Triangle-wave PWM mode 3	/	/	/	/	/	○	○	○	/	○	○	○	Refer to No 1 in Table 4
35	Low Power Consumption	-	○	○	○	○	○	○	○	○	○	○	○	○	
36	Complementary PWM Mode Timer	Complementary PWM mode 1	/	○	○	○	○	○	○	○	○	○	○	○	
		Complementary PWM mode 2	/	○	○	○	○	○	○	○	○	○	○	○	
		Complementary PWM mode 3	/	○	○	○	○	○	○	○	○	○	○	○	Refer to No 1 in Table 3
37	Continuous Scan Mode S12AD	-	○	○	○	○	○	○	○	○	○	○	○	○	
38	Voltage Detection Circuit	-	○	○	○	○	○	○	○	○	○	○	○	○	

3. Changes

This chapter describes changes to the Smart Configurator for RX V2.1.0.

3.1 New support

3.1.1 Supports RX72T and RX66T (RAM 128 Kbytes) group devices

Supported RX72T and RX66T (RAM 128Kbytes) group devices. For the supported components, refer to "2.2 Support Components List".

3.1.2 Supports GCC project creation for RX651, RX65N group devices with "_DUAL" device name

Smart Configurator for RX V.2.1.0 supports GCC project creation for RX651, RX65N group devices with "_DUAL" device name when using e² studio version V7.4.0 and above.

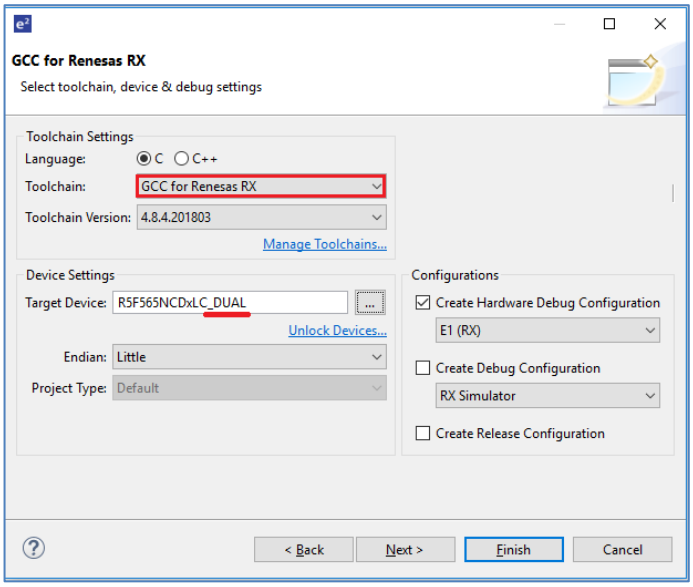

Figure 3-1 RX651, RX65N group devices with "_DUAL" for GCC projects

3.2 Correction of issues/limitations

3.2.1 Fixed issue of caution when using the GTIOCnm pin of the general PWM timer (GPTW) as a hardware source

Issue of caution when using the GTIOCnm pin (n = 0 to 9, m = A, B) of the general PWM timer (GPTW) as a hardware source has been fixed.

3.3 Specification changes

3.3.1 Updated specification to support start mode setting in Voltage Detection Circuit

Smart Configurator for RX V2.1.0 has been updated to support selection of register start mode or auto-start mode when using Voltage Detection Circuit component in RX110, RX111 and RX113.

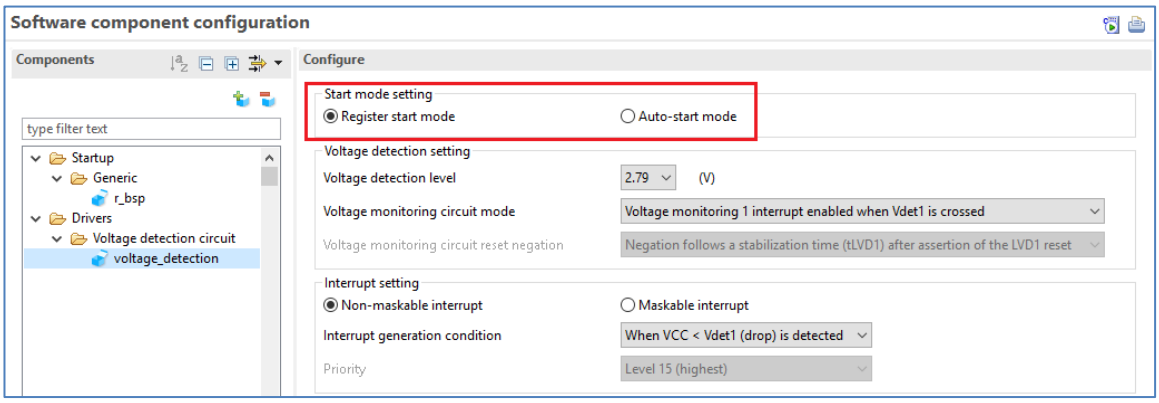

Figure 3-2 Start mode setting in Voltage Detection Circuit

4. List of RENESAS TOOL NEWS

Below is a list of notifications delivered by RENESAS TOOL NEWS.

Issue date	Document No.	Description	Applicable MCUs	Fixed version
Sep. 1, 2017	R20TS0198 EJ0100	When using the I2C bus interface in slave mode https://www.renesas.com/search/keyword-search.html#genre=document&q=R20TS0198	RX130, RX64M, RX651, RX65N	V1.3.0
Apr. 1, 2018	R20TS0294 EJ0100	When using the bus for peripheral functions https://www.renesas.com/search/keyword-search.html#genre=document&q=R20TS0294	RX230, RX231	V1.4.0
Oct. 01, 2018	R20TS0351 EJ0100	Setting TPU0 channel of PWM Mode Timer https://www.renesas.com/search/keyword-search.html#genre=document&q=R20TS0351	RX65N, RX651, RX64M	V1.5.0
Feb.01, 2019	R20TS0401 EJ0100	Point for caution when using the GTIOCnm pin (n = 0 to 9, m = A, B) of the general PWM timer (GPTW) as a hardware source https://www.renesas.com/search/keyword-search.html#genre=document&q=R20TS0401	RX66T	V2.1.0

5. Points for Limitation

This section describes points for limitation regarding the Smart Configurator for RX V2.1.0. Please refer to a document of each module about a caution of a FIT module.

5.1 List of Limitation

Table 3 List of Limitation

○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX230, RX231	RX23T	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	RX72T	Remarks
1	Note on using double buffer function in Complementary PWM Mode Timer	/	/	/	/	/	○	○	○	○	○	○	○	
2	Note on using 10-bit address mode in I2C Master Mode component	○	○	○	○	○	○	○	○	○	○	○	○	
3	Note on using Compare Match Timer CMTW1 channel	/	/	/	/	/	/	/	/	○ *	/	/	/	* Only affects RX651 LPC
4	Note on using output compare interrupt of CMTW channel in Compare Match Timer component	/	/	/	/	/	/	/	○	○	/	○	/	
5	Note on PWM Mode Timer after change device	○	○	○	○	○	○	○	○	○	○	○	○	
6	Note on using Single Scan Mode S12AD after change device	/	/	/	/	/	/	/	/	○	○	/	/	
7	Note on using Event Link Controller	/	/	/	/	○	/	/	/	○	/	/	/	* Only affects RX231 and RX651 LPC
8	Note on using Real Time Clock	/	/	/	/	/	/	/	○	○	/	○	/	
9	Note on using output buffer amplifier of D/A Converter	/	/	/	/	/	/	/	○	○	/	/	/	
10	Note on using Programmable Pulse Generator	/	/	/	/	/	/	/	○	○	/	○	/	
11	Note on using Bus	/	/	/	/	/	/	/	/	/	○	/	○	

5.2 Details of Limitation

5.2.1 Note on using double buffer function in Complementary PWM Mode Timer

When using double buffer function in Complementary PWM Mode Timer, the initial PWM duty ratio value of TGRE and TRGF registers are incorrect.
As workaround, manually change the value of TGRE and TGRF registers in API (R_<Configuration Name>_Create) to the desired value + 1.

Example: Complementary PWM Mode 3 (MTU3 and MTU4)

```
void R_Config_MTU3_MTU4_Create(void)
{
  /* Release MTU channel 3 from stop state */
  MSTP(MTU3) = 0U;

  /* Enable read/write to MTU3, MTU4 registers */
  MTU.TRWERA.BIT.RWE = 1U;

  /* Stop MTU channel 3 counter */
  MTU.TSTRA.BIT.CST3 = 0U;

  /* Set A/D conversion signal output for ADSM0, ADSM1 pins */
  MTU.TADSTRGR0.BYTE = _00_MTU_TADSTRS_NOSOURCE;
  MTU.TADSTRGR1.BYTE = _00_MTU_TADSTRS_NOSOURCE;

  /* MTU channel 3 is used as complementary PWM mode 3 */
  MTU3.TIER.BYTE = 0x00U;
  MTU4.TIER.BYTE = 0x00U;
  MTU.TITCR1A.BIT.T3AEN = 0U;
  MTU.TITCR1A.BIT.T4VEN = 0U;
  MTU3.TCR.BYTE = _00_MTU_PCLK_1 | _00_MTU_CKCL_DIS;
  MTU4.TCR.BYTE = _00_MTU_PCLK_1;
  MTU3.TCR2.BYTE = _00_MTU_PCLK_1;
  MTU4.TCR2.BYTE = _00_MTU_PCLK_1;
  MTU.TGCRA.BYTE = _80_MTU_BDC_OUT;
  MTU3.TCNT = _0280_3TCNT_VALUE;
  MTU4.TCNT = 0x0000U;
  MTU.TSYRA.BIT.SYNC3 = 0U;
  MTU.TSYRA.BIT.SYNC4 = 0U;
  MTU3.TGRB = _0064_3TGRB_VALUE;
  MTU3.TGRD = _0064_3TGRB_VALUE;
  MTU4.TGRA = _0064_4TGRA_VALUE;
  MTU4.TGRC = _0064_4TGRA_VALUE;
  MTU4.TGRB = _0064_4TGRB_VALUE;
  MTU4.TGRD = _0064_4TGRB_VALUE;
  MTU3.TGRE = _0063_3TGRE_VALUE;
  MTU4.TGRE = _0063_4TGRE_VALUE;
  MTU4.TGRF = _0063_4TGRF_VALUE;
  :  (codes are omitted)
}
```

Manually change the value of TGRE and TGRF to the desired value + 1 after code is generated.

Figure 5-1 Workaround for setting TGRE and TRGF registers value

5.2.2 Note on using 10-bit address mode in I2C Master Mode component

When configuring I2C-bus Interface (RIICa) by I2C Master Mode component in Smart Configurator, the slave address smaller than 0x80 cannot be sent with 10-bit address mode in master transmission operation triggered by calling R_<Configuration Name>_Master_Send function. The address mode is set to 7-bit address mode if the address value specified by the parameter of R_<Configuration Name>_Master_Send function is smaller than 0x80.

5.2.3 Note on using Compare Match Timer CMTW1 channel

Smart Configurator for RX V2.1.0 does not support configuration of Compare value 1 when using Compare Match Timer CMTW1 channel. Do not select "CMWCNT is cleared by CMWOCR1" option from Counter clear.

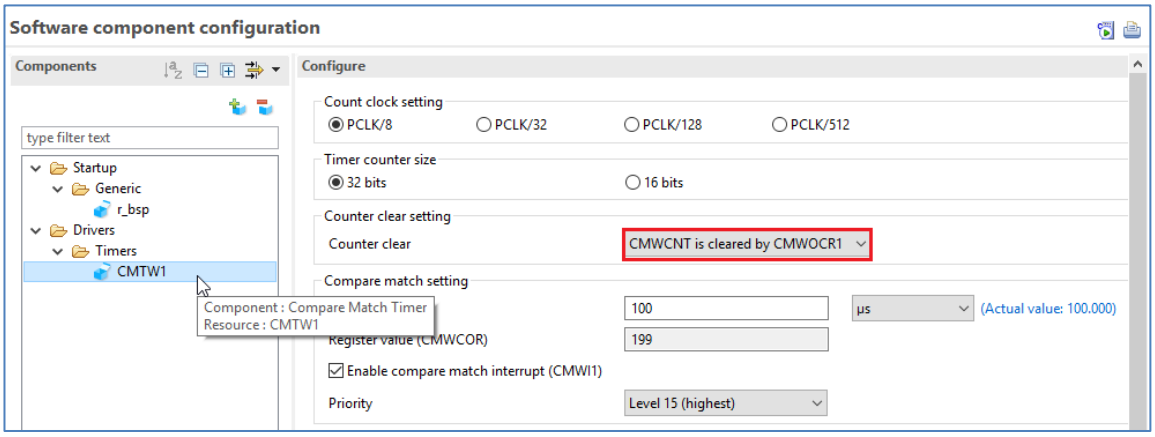

Figure 5-2 CMTW1 Counter clear setting

5.2.4 Note on using output compare interrupt of CMTW channel in Compare Match Timer component

TOCn pin (n = 0-3) has to be selected when using output compare interrupt of CMTW channel in Compare Match Timer component even though TOCn pin is not intended to be used.

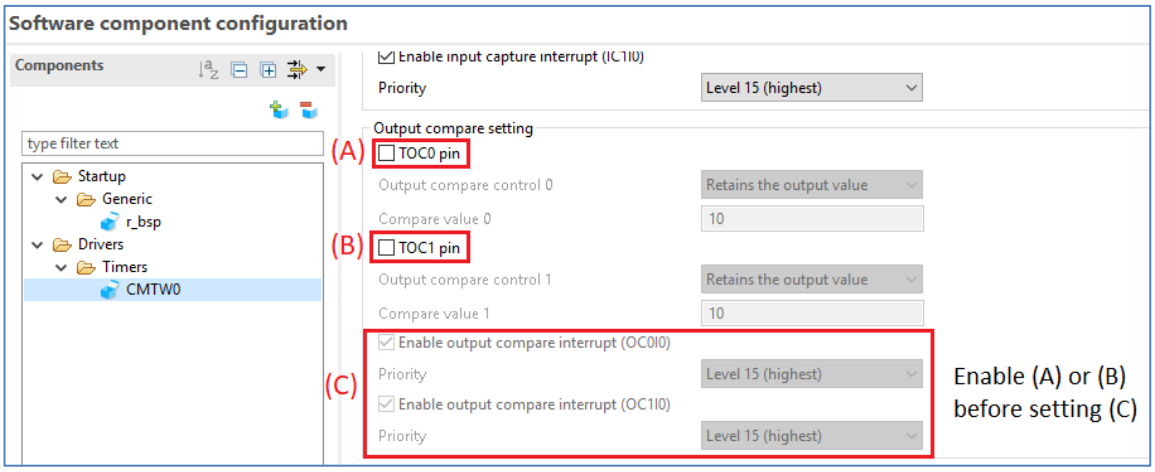

Figure 5-3 Select TOCn pin to enable output compare interrupt

5.2.5 Note on PWM Mode Timer after change device

When using PWM Mode Timer mode 2, setting of TIOCmn pin (m = A to D, n = 0 to 9) of TPU and MTU channels may change to Output disabled after change device. As workaround, reconfigure TIOCmn pin setting before generating new codes.

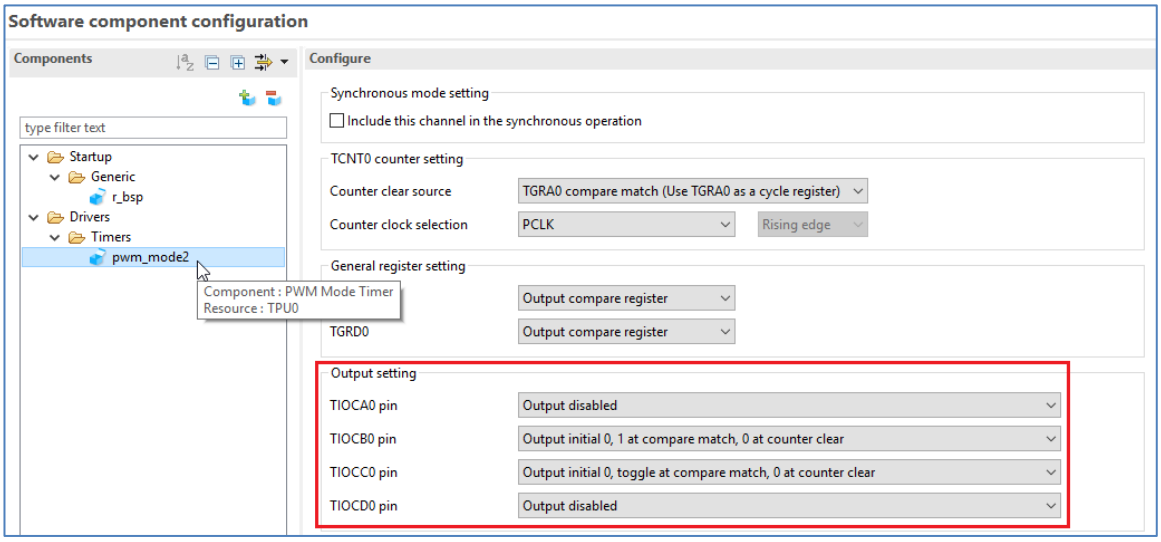

Figure 5-4 Reconfigure TIOCmn pin setting before generating new codes

5.2.6 Note on using Single Scan Mode S12AD after change device

When using Single Scan Mode S12AD, selection of analog input channels may not be ported over after change device. As workaround, reconfigure analog input channel setting.

5.2.7 Note on using Event Link Controller

When using Event Link Controller for RX231 and RX651 LPC group devices, macro definition value generated to mask Port Buffer Register n (PDBFn) (n = 1, 2) are incorrect for certain pin package.

```
 : (codes are omitted)
/***********************************************************************************************
Macro definitions
***********************************************************************************************/
/* Mask for PDBF1 */
#define _FF_ELC_PORTGRP1_PDBF_MASK          (0xFFU)
/* Mask for PDBF2 */
#define _FF_ELC_PORTGRP2_PDBF_MASK          (0xFFU)
 : (codes are omitted)
```

Figure 5-5 Generated code for RX651 64-pin package

As workaround, manually add the modification codes to user code editing area in <Event Link Controller configuration name.h>.

```
 : (codes are omitted)
/***********************************************************************************************
Global functions
***********************************************************************************************/
 : (codes are omitted)
/* Start user code for function. Do not edit comment generated here */
#undef _FF_ELC_PORTGRP1_PDBF_MASK
#define _FF_ELC_PORTGRP1_PDBF_MASK          (0xE0U)
#undef _FF_ELC_PORTGRP2_PDBF_MASK
#define _FF_ELC_PORTGRP2_PDBF_MASK          (0xC7U)
/* End user code. Do not edit comment generated here */
#endif
```

Figure 5-6 Example of adding modification codes for RX651 64-pin package

Device	Package	Port	Modification codes
RX231	64-pin	PORTE	#undef _2B_ELC_PORTGRP2_PDBF_MASK #define _2B_ELC_PORTGRP2_PDBF_MASK (0x3FU)
	48-pin	PORTB	#undef _3F_ELC_PORTGRP1_PDBF_MASK #define _3F_ELC_PORTGRP1_PDBF_MASK (0x2BU)
RX651	64-pin	PORTB	#undef _FF_ELC_PORTGRP1_PDBF_MASK #define _FF_ELC_PORTGRP1_PDBF_MASK (0xE0U)
		PORTE	#undef _FF_ELC_PORTGRP2_PDBF_MASK #define _FF_ELC_PORTGRP2_PDBF_MASK (0xC7U)

Figure 5-7 Modification codes

5.2.8 Note on using Real Time Clock

When using main clock oscillator as the clock source for Real Time Clock, the values generated for Frequency Register H/L (RFRH/RFRL) are incorrect.
As workaround, manually change the value written to RFRH and RFRL registers in API (R_<Configuration Name>_Create) to the following value.
Refer to the user's manual hardware about setting value.

Example: RFRH/RFRL register setting value

Main Clock Frequency	RFRH/RFRL register setting value
4MHz	0000 7A11h
8MHz	0000 F423h
10MHz	0001 312Ch
12MHz	0001 6E35h
16MHz	0001 E847h

Figure 5-8 Example RFRH/RFRL Register Settings by the Main Clock Frequency

Example : Real Time Clock (Clock source : Main Clock 10 MHz)

```
void R_Config_RTC_Create(void)
{
 : (codes are omitted)
  /* Set frequency register H/L */
  RTC.RFRH.WORD = 0x0000U;
  RTC.RFRL.WORD = 0x17C7U;
 : (codes are omitted)
}
```

Before change

```
void R_Config_RTC_Create(void)
{
 : (codes are omitted)
  /* Set frequency register H/L */
  RTC.RFRH.WORD = 0x0001U;
  RTC.RFRL.WORD = 0x312CU;
 : (codes are omitted)
}
```

After change

Figure 5-9 Change the value written to RFRH and RFRL registers

5.2.9 Note on using output buffer amplifier of D/A Converter

When using output buffer amplifier of D/A Converter, generated stabilization time for output buffer amplifier may not be updated after changing clock setting.
As workaround, open D/A Converter configuration at [Components] page after changing clock setting at [Clocks] page. Click Generate Code button to update stabilization time.

5.2.10 Note on using Programmable Pulse Generator

If only configure even number Group (Group 0,2,4,6) of pins on Programmable Pulse Generator GUI and output trigger signal other than MTU0/TPU0 is selected, pulse output pins cannot output signal as intended.

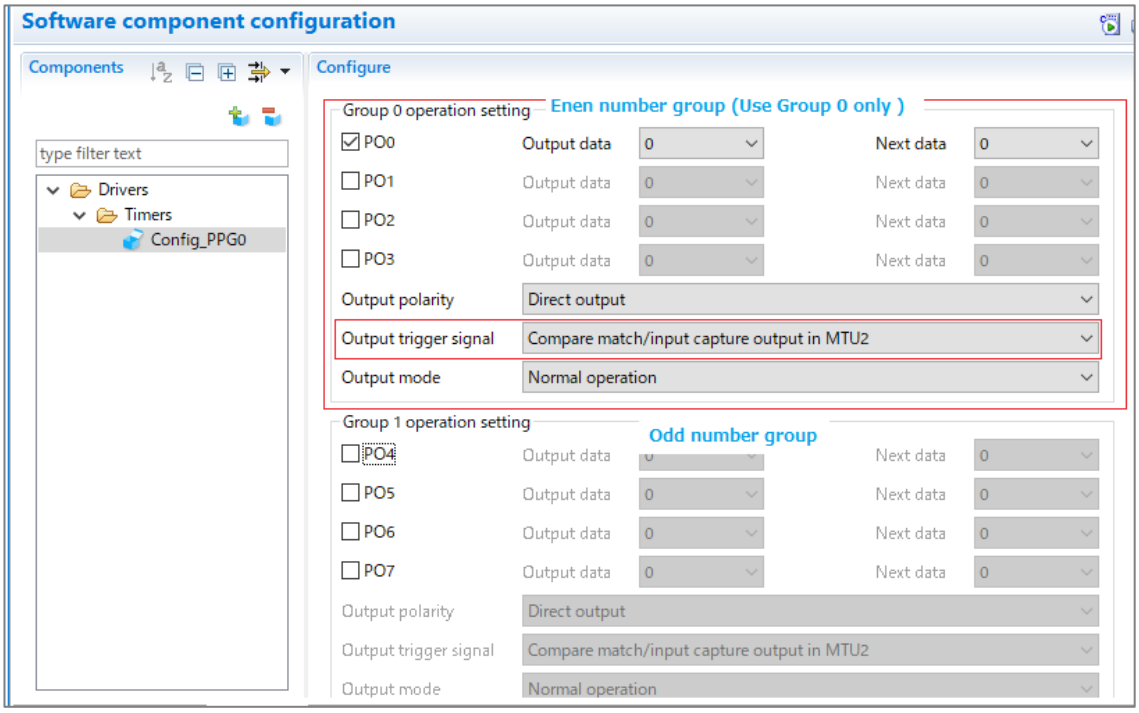

Figure 5-10 Configure only Group 0

As workaround, add code at PPGn.PCR register (n = 0, 1) to initialize the same output trigger signal for even group and odd group.
Refer to each device User's Manual: Hardware for the setting to initialize PCR register.

```
void R_Config_PPG0_Create_UserInit(void)
{
    /* Start user code for user init. Do not edit comment generated here */: (codes are omitted)
  PPG0.PCR.BYTE = _02_PPG_GROUP0_COMPARE_MTU2 | _08_PPG_GROUP1_COMPARE_MTU2;
  /* End user code. Do not edit comment generated here */
}
```

Figure 5-11 Example (Use PO0 pin only, MTU2 is trigger signal)

5.2.11 Note on using Buses

When using Buses for RX66T and RX72T group devices, PMR.Bn bit of WR1#, WR0#, A0, D8 to D15 pins are not initialized to 0 in API (R_<Configuration Name>_Create).
As workaround, add code in API (R_<Configuration Name>_Create) to initialize PMR.Bn bit of WR1#, WR0#, A0, D8 to D15 pins to 0 if these pins are used. For example, if WR0# is assigned to PE1, initialize bit 1 of PORTE.PMR register to 0 :

```
PORTE.PMR.BYTE &= 0xFDU;
```

Note: Code for WR1#, WR0#, A0, D8 to D15 pins are generated in API (R_Pins_Create) as reference. Refer to set register and value.

6. Points for Caution

This section describes points for caution regarding the Smart Configurator for RX V2.1.0. Please refer to a document of each module about a caution of a FIT module.

6.1 List of Caution

Table 4 List of Caution

○: Applicable, /: Not Applicable

No	Description	RX110	RX111	RX113	RX130	RX230, RX231	RX23T	RX24T, RX24U	RX64M	RX65N, RX651	RX66T	RX71M	RX72T	Remarks
1	Note on configuring GPT interrupt	/	/	/	/	/	/	○	○	/	○	○	○	
2	Note on SCR.TE bit setting sequence in SCI Clock Synchronous Mode and SCI Clock Asynchronous Mode	○	○	○	○	○	○	○	○	○	○	○	○	
3	Note on using only reception in SCI Clock Synchronous Mode	○	○	○	○	○	○	○	○	○	○	○	○	
4	Notes on using high transfer speed in SCIF Synchronous Mode	/	/	/	/	/	/	/	○	/	/	○	/	
5	Note on device change functionality	○	○	○	○	○	○	○	○	○	○	○	○	

6.2 Details of Caution

6.2.1 Note on configuring GPT interrupts

The GPT interrupts are not specified as the Software Configurable Interrupt in the initial state even after the GPT interrupts are configured by GPT component. To specify GPT interrupts as Software Configurable Interrupt source, release unused Software Configurable interrupt source on the Interrupt sheet and allocate GPT interrupts instead.

6.2.2 Note on SCR.TE bit setting sequence in SCI Clock Synchronous Mode and SCI Clock Asynchronous Mode

Sequence of setting SCR.TE bit does not follow the usage note in User's Manual: Hardware.
Instead, SCR.TE bit is set to 1 after changing the pin function to TXDn. Output of TXDn pin becomes high impedance.
Please connect a pull-up resistor to the TXDn line, prevent the TXDn line from becoming high impedance.

6.2.3 Note on using only reception in SCI Clock Synchronous Mode

In SCI Clock Synchronous Mode using internal clock, if only reception is enabled in high communication speed, extra clocks are generated even though reception has been completed.
This is due to the delay in disabling RE to stop the clock after the desired number of data is received.
To prevent this issue, select Transmission/Reception work mode when using Smart Configurator. Use “R_<Configuration Name>_Serial_Send_Receive” function instead of “R_<Configuration Name>_Serial_Receive”. The same number of data for tx_num and rx_num should be specified.
Disable TXDn pin in Smart Configurator Pins page and send dummy data if transmission is not required.
There will be warnings when TXDn pin is disabled. These warnings can be ignored as TXDn pin is not intended to be used originally.

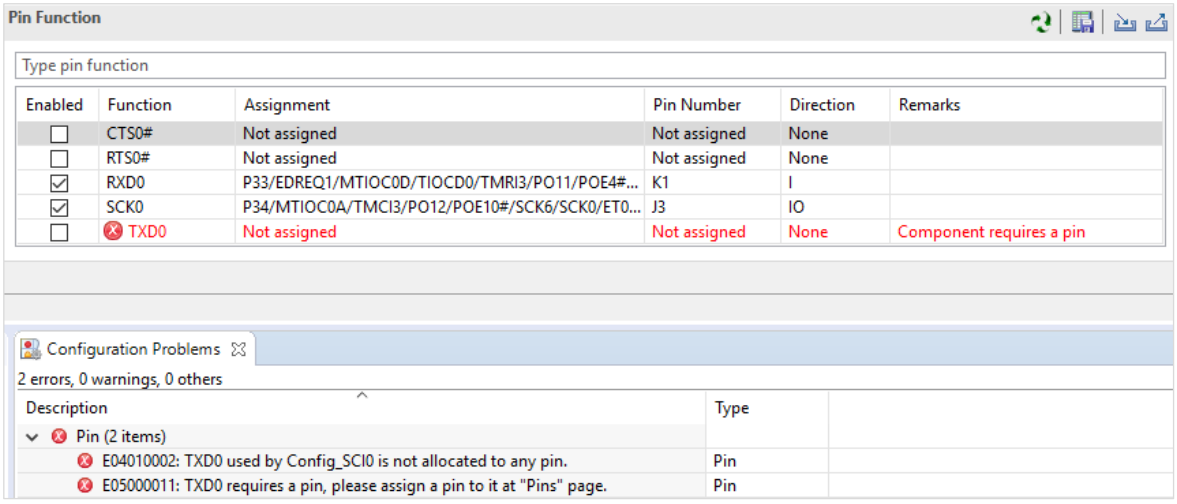

Figure 6-1 Ignore warnings when TXDn pin is disabled (Example with TXD0)

6.2.4 Note on using high transfer speed in SCIF Synchronous Mode

If the number of reception data specified for the API (R_<Configuration Name>_Serial_Receive or R_<Configuration Name>_Serial_Send_Receive) and reception FIFO threshold specified on GUI do not satisfy the formula below:

(Reception Data Size) = n * (Reception FIFO threshold) (n=1,2,3,,,,)

extra clock generation may occur after the desired number of data is received in high communication speed when using internal clock.
To prevent this issue, specify the reception data size and reception FIFO threshold that satisfy the formula.

6.2.5 Note on device change functionality

Save project settings before performing change device operation. After change device, perform these operations:
1. Visual check on Components window and Configuration Problems window. Resolve error and conflicts if there is any.
2. Check each component and converted settings.
3. Re-generate codes.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr.22 19	21	Create new
1.01	Jun.4 19	13, 16~19	Update Details of Limitation (5.2.6 ~ 5.2.11)

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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