# CubeSuite+ Simulator for 78K0R/Ix3 V3.00.03

Release Note

R20UT2512EJ0100
Rev.1.00
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## Contents

# Chapter 1. Target Devices

Below is a list of devices supported by the 78K0R/Ix3 simulator.

| Nick Name | Device name |
|---|---|
| 78K0R/IB3 | μPD78F1201(30pin), μPD78F1203(30pin) |
| 78K0R/IC3 | μPD78F1211(38pin), μPD78F1213(38pin), μPD78F1211(44pin), μPD78F1213(44pin), μPD78F1213(48pin), μPD78F1214(48pin), μPD78F1215(48pin) |
| 78K0R/ID3 | μPD78F1223(52pin), μPD78F1224(52pin), μPD78F1225(52pin) |
| 78K0R/IE3 | μPD78F1233(64pin), μPD78F1234(64pin), μPD78F1235(64pin) |
| 78K0R/KC3-L | μPD78F1000(40pin), μPD78F1001(40pin), μPD78F1002(40pin), μPD78F1003(40pin), μPD78F1000(44pin), μPD78F1001(44pin), μPD78F1002(44pin), μPD78F1003(44pin), μPD78F1001(48pin), μPD78F1002(48pin), μPD78F1003(48pin) |
| 78K0R/KD3-L | μPD78F1004(52pin), μPD78F1005(52pin), μPD78F1006(52pin) |
| 78K0R/KE3-L | μPD78F1007(64pin), μPD78F1008(64pin), μPD78F1009(64pin) |
| 78K0R/KF3-L | μPD78F1010(80pin), μPD78F1011(80pin), μPD78F1012(80pin), μPD78F1027(80pin), μPD78F1028(80pin) |
| 78K0R/KG3-L | μPD78F1013(100pin), μPD78F1014(100pin), μPD78F1029(100pin), μPD78F1030(100pin) |

# Chapter 2. User's Manuals

Please read the following user's manuals together with this document.

| Manual Name | Document Number |
|---|---|
| CubeSuite+ V1.01.00 78K0R Debug | R20UT0732EJ0100 |
| CubeSuite+ V2.00.00 Message | R20UT2448EJ0100 |

# Chapter 3. Key Word for Uninstallation

To uninstall this product, use the integrated uninstaller (uninstalls CubeSuite+).

# Chapter 4. Changes

This chapter describes changes from V3.00.02 to V3.00.03.

## 4.1 Specifications changed

### 4.1.1 Simulation on CubeSuite+ V2.00.00

Support simulation on CubeSuite+ V2.00.00. There is no functional change.

# Chapter 5. Cautions

This section describes cautions for using the 78K0R/Ix3 simulator. The following two types of caution are described:

•Differences between target devices and simulator : Differences from behavior of target devices due to simulator specifications

•Cautions for using simulator GUI : Cautions for using the simulator GUI window

## 5.1 Differences between target devices and simulator

### 5.1.1 Unsupported peripheral functions

The simulator does not support the following peripheral functions of the target device (the following functions cannot be debugged on the simulator).

* Regulator
* Serial Interface IICA
* Simplified IIC (Serial array unit)

### 5.1.2 Flash self programming function

The following differences exist between the target device and simulator regarding the flash self programming function.

1. Operation when a pull-down resistor is connected to the FLMD0 pin
   In the target device, whether the flash self programming mode can be set via software is determined based on its resistance when a pull-down resistor is externally connected to the FLMD0 pin.

| FLMD0 Pin Handling | Setting via Software |
|---|---|
| Pulled down with a resistance of 100k ohm or more | Available |
| Pulled down with a  resistance of less than 100k ohm | Not guaranteed |

On the other hand, in the simulator, connection of a pull-down resistor to the FLMD0 pin can be specified in the I/O Panel window but this panel does not have the function to set the resistance value. As a result, if connection of a pull-down resistor to the FLMD0 pin is specified, it is regarded as an operation equivalent to that being pulled down with a resistance of 100k ohm or more.

2. Errors that are not generated

The simulator does not generate the following errors.

| Function Name | Error Name | Return Value |
|---|---|---|
| FSL_Init | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_Init_cont | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_BlankCheck | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_Erase | Erase error | 0x1A |
| | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_IVerify | Verification (internal verification) error | 0x1B |
| | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_Write | Write error | 0x1C |
| | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_EEPROMWrite | Write error | 0x1C |
| | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_InvertBootFlag | Erase error | 0x1A |
| | Verification (internal verification) error | 0x1B |
| | Write error | 0x1C |
| | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_SwapActiveBootCluster | Erase error | 0x1A |
| | Verification (internal verification) error | 0x1B |
| | Write error | 0x1C |
| | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_SetChipEraseProtectFlag | Erase error | 0x1A |
| | Verification (internal verification) error | 0x1B |
| | Write error | 0x1C |
| | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_SetBlockEraseProtectFlag | Erase error | 0x1A |
| | Verification (internal verification) error | 0x1B |
| | Write error | 0x1C |
| | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_SetWriteProtectFlag | Erase error | 0x1A |
| | Verification (internal verification) error | 0x1B |
| | Write error | 0x1C |
| | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_SetBootClusterProtectFlag | Erase error | 0x1A |
| | Verification (internal verification) error | 0x1B |
| | Write error | 0x1C |
| | Processing abortion due to interrupt occurrence | 0x1F |
| FSL_SetFlashShieldWindow | Erase error | 0x1A |
| | Verification (internal verification) error | 0x1B |
| | Write error | 0x1C |
| | Processing abortion due to interrupt occurrence | 0x1F |

3. Voltage modes

Voltage modes (full-speed mode/wide voltage mode) are not simulated.

4. Operation of the FSL_SetInterruptMode function

The FSL_SetInterruptMode simulation is not complete.

Even if the FSL_SetInterruptMode function is called during interrupt processing, the function that had been suspended for the interrupt may continue executing, instead of returning to the user program.

### 5.1.3 Division processing by the multiplier/divider

There are the following differences between the target device and the simulator when the multiplier/divider performs division.

[Target device]

It takes 16 clock cycles from the start to the end of division.

[Simulator]

It takes 1 clock cycle from the start to the end of division.

### 5.1.4 Reset

If a reset is generated by the Power-on-Clear circuit (POC) or low-voltage detector (LVI) circuit, the simulator will display "STANDBY" in the status bar. (The status is actually reset, not standby.)

And the behavior differs as follows if a reset is generated by the RESET pin.

[Target device]

Goes into reset status when the RESET pin goes to low level. Reset status is released when it goes to high level.

[Simulator]

Does not go into reset status when the RESET pin goes to low level. When it goes to high level, the simulator momentarily goes into reset status, and then the reset status is released immediately.

### 5.1.5 1-Hz pin output of real-time counter

If the waveform of the RTC1HZ pin is checked in the timing chart window using 1 Hz pin output of the real-time counter, the output waveform has a frequency of 32.768 Hz.

In this case, determine that 1 Hz output is being performed without problems.

### 5.1.6 Noise elimination digital filter of Comparator

The simulator does not simulate the noise elimination digital filter of Comparator. So, simulator always operates without noise filter.

### 5.1.7 Oscillation stabilization time of Clock Generator

The simulator does not simulate the clock oscillator oscillation stabilization time.

The oscillation stabilization time is always 0 seconds when a reset or standby is released, regardless of the OSTS register settings. The OSTS register is set to the following values.

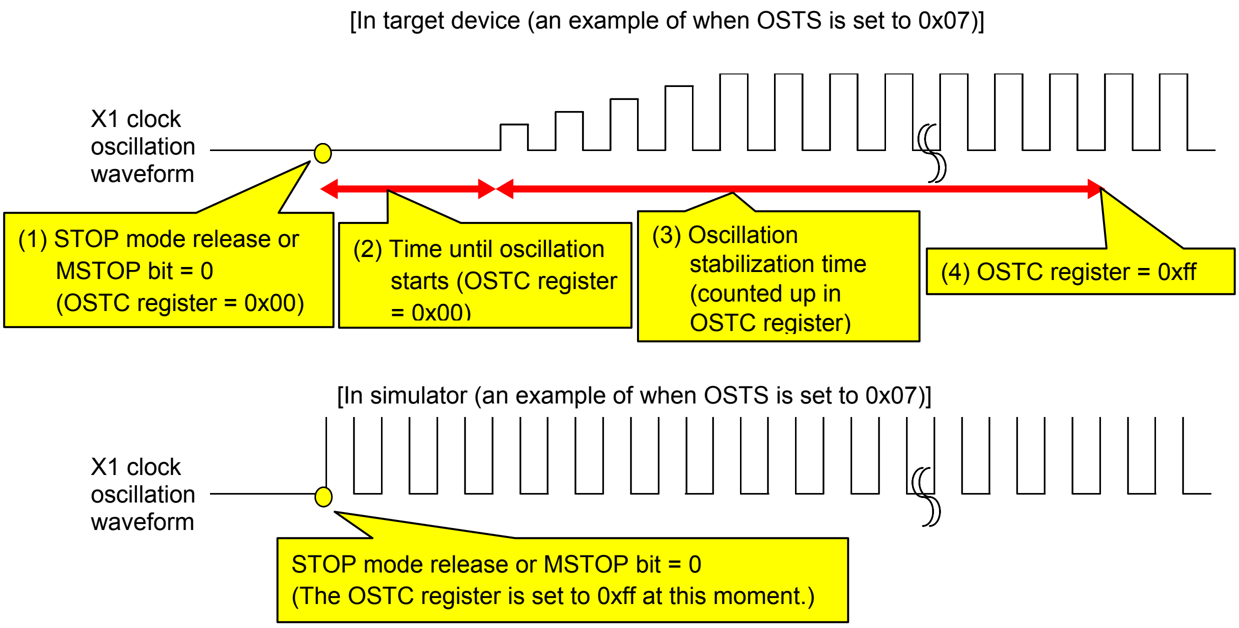
- Initial value after reset, during STOP mode, when MSTOP of CSC register = 1: 0x00
- MSTOP of CSC register = 0 after STOP mode release: Values shown in the following table

(Maximum value in the target device)

| OSTS Setting Value | OSTC Value |
|---|---|
| 0x0 ($2^8$/fx) | 0x80 |
| 0x1 ($2^9$/fx) | 0xc0 |
| 0x2 ($2^{10}$/fx) | 0xe0 |
| 0x3 ($2^{11}$/fx) | 0xf0 |
| 0x4 ($2^{13}$/fx) | 0xf8 |
| 0x5 ($2^{15}$/fx) | 0xfc |
| 0x6 ($2^{17}$/fx) | 0xfe |
| 0x7 ($2^{18}$/fx) | 0xff |

The following figure illustrates this operation.

In the target device, the X1 clock oscillation starts after the states (1) to (4) have passed. In the simulator, states (1) to (4) end instantly and the X1 clock oscillation starts.



Therefore, pay attention to the code that waits for oscillation stabilization.

There is no problem if a program is created with the condition that the execution exits the oscillation stabilization wait period when the OSTC register value becomes the maximum value, or when the OSTC register value exceeds the specified value, but if a program is created with the condition that the execution exits the oscillation stabilization wait period when the OSTC register value becomes a value other than the maximum value, the execution enters an infinite loop.

The following shows examples of code that causes/does not cause problems.

(This is an example of when OSTS is set to 0x07)

Correct program example (1)

```
while(OSTC != 0xff)
{
NOP();/* wait */
}
```

Correct program example (2)

```
while(OSTC <= 0xf0)
{
NOP();/* wait */
}
```

Example of program that may cause problems

```
while(OSTC != 0xf0)
{
NOP();/* wait */
}
```

### 5.1.8 SFR with clock generator (AMPH/AMPHS0/AMPHS1/FSEL)

The simulator does not simulate the following SFRs, which belong to the clock generator. Read/write for each register can be performed normally, but the operation does not change even if its value is changed.

- Bit 0 (AMPH) of clock operation mode control register (CMC)
- Bit 1 (AMPHS0) and Bit2 (AMPHS1) of clock operation mode control register (CMC)
- Bit 0 (FSEL) of operation speed mode control register (OSMC)

[Bit 0 (AMPH) of clock operation mode control register (CMC)]

This register is used to set the oscillator gain according to the frequency when oscillating the high-speed system clock. If a wrong setting is made, the high-speed system clock may not oscillate in the target device. In the simulator, however, wrong settings do not affect the oscillation of the high-speed system clock.

[Bit 1 (AMPHS0) and Bit2 (AMPHS1) of clock operation mode control register (CMC)]

This register is used to set the oscillation mode of subsystem clock ( Normal oscillation mode / Low power consumption oscillation mode / Ultra-low power consumption oscillation mode ). If a wrong setting is made, the subsystem clock may not oscillate in the target device. In the simulator, however, wrong settings do not affect the oscillation of the subsystem clock.

[Bit 0 (FSEL) of operation speed mode control register (OSMC)]

This register is used to control the step-up circuit for the high-speed flash memory operation.

If a wrong setting is made, read or instruction fetch from the flash memory may fail, or self programming may fail in the target device. In the simulator, however, wrong settings do not affect the operation.

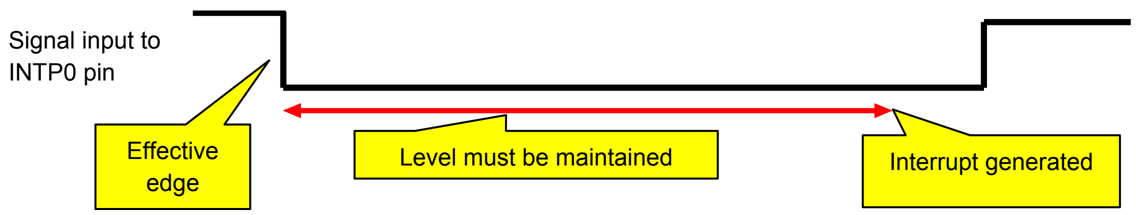
### 5.1.9 Noise reduction circuit for external-interrupt pin

The simulator does not simulate the noise reduction circuit. For example, if you input the active level to an external-interrupt pin with a noise reduction circuit, the interrupt will be received even if the active-level amplitude is too low.

The example below considers the case when there is input to the INTP0 pin.

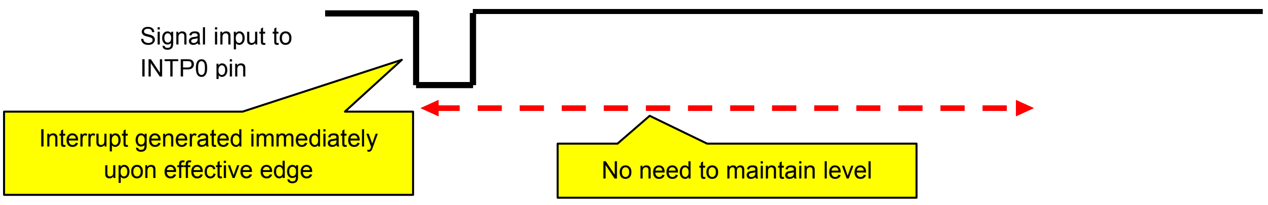
There is a noise reduction circuit on the INTP0 pin of the target device. For this reason, in order to generate an interrupt, it is necessary to input an effective edge to the target device, and subsequently maintain the signal level. (See the user's manual of the target device for the length of time it must be maintained.)

**Target device behavior (falling effective edge)**




In the case of the simulator, however, this noise reduction circuit is not simulated. For this reason, an interrupt will be generated any time a valid edge is generated. (No need to maintain signal level).

**Simulator behavior (falling effective edge)**




### 5.1.10 DMA controller

The transfer speeds of the target device and simulator differ as follows when simulating the DMA controller.

[Target device]

* It takes two clock cycles to complete one DMA transfer. The CPU waits during this period.
* If there is contention for transfer timing with another channel's DMA, then one of the DMA transfers will be placed on hold; after the other DMA transfer is completed, the one on hold will begin.

[Simulator]

* It takes zero clock cycles to complete one DMA transfer. For this reason, the CPU does not wait.
* If there is contention for transfer timing with another channel's DMA, then both of the DMA transfers are performed simultaneously.

### 5.1.11 Operation clock of timer array unit

Do not specify an operation clock that is 233 Hz or lower. If the operation clock (CKmk) of the timer array unit  is 233 Hz or lower, then the timer array unit will not operate correctly (it will behave as if operating via a clock that is faster than the one selected).

### 5.1.12 Input pulse interval measurement mode of timer array unit

When the input pulse interval measurement mode of the timer array unit is being used, the behavior when an effective edge is detected on the TImn pin differs.

[Target device]

The TCRmn timer counter register is initialized to 0x0000.

[Simulator]

The TCRmn timer counter register is to 0xFFFF.

For this reason, the pulse width count will be one less than on the target device.

### 5.1.13 Noise filter of timer array unit

Although the target device's timer array unit has a function to turn the noise filter on and off in order to reduce noise on the timer input pin, the simulator does not simulate this. (There is no difference in behavior whether filtering is on or off.) Since there is no noise in the simulator's signal, it would be meaningless to simulate this function.

### 5.1.14 Clock output / buzzer output controller

Do not specify an output clock that is 233 Hz or lower. If the output clock is 233 Hz or lower, then the output clock will not operate correctly (it will behave as if operating via a clock that is faster than the one selected). If the output clock is $f_{MAIN}$, it is impossible to see waveform on timing chart window. The output clock that can be used to see waveform on timing chart window is up to fMAIN/2.

### 5.1.15 Operation clock of serial array unit

Do not use INTTM02 as the operation clock for the serial array unit. (Doing so will prevent the serial array unit from operating at all.)

### 5.1.16 Noise filter of serial array unit

Although the target device's serial array unit has a function to turn the noise filter on and off in order to reduce noise on the input pin, the simulator does not simulate this. (There is no difference in behavior whether filtering is on or off.) Since there is no noise in the simulator's signal, it would be meaningless to simulate this function.

### 5.1.17 SDRmn register of serial array unit

The following differences occur between the target device and simulator when the serial data register (SDRmn) is read during serial operation.

[Target device]

The value read from the upper 7 bits is 0.

[Simulator]

The values read from the upper 7 bits are the values immediately before start of serial operation.

### 5.1.18 SFR 0/1 constant bit

The SFR has bits that are always 0 or 1.

For example, bits 3 to 7 are always 0 for the oscillation stabilization time selection register (OSTS).

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| OSTS | 0 | 0 | 0 | 0 | 0 | OSTS2 | OSTS1 | OSTS0 |

Bits are always 0

Although the values of these bits cannot be changed in the case of the target device, the values can be changed in the case of the simulator. Note that changing these values has no effect on behavior.

### 5.1.19 Comparator stabilization time of A/D converter

The comparator stabilization times of the A/D converter are different for the target device and simulator.

[Target device]

It takes 1 microsecond from the start of operation of the comparator until it stabilizes. Any A/D conversion results obtained before stabilization will be invalid. For this reason, it is necessary to ignore the first A/D conversion results.

[Simulator]

Comparator operation stabilizes immediately upon startup. For this reason, A/D conversion results obtained within 1 microsecond of the start of operation will be correct, and there is thus no need to ignore the first A/D conversion results.

### 5.1.20 Default voltage of $AV_{REF}$ pin

Default voltage of $AV_{REF}$ pin is 5.0V.

Note : The meaning of "Default voltage " is the voltage when the pin have no connection.

### 5.1.21 Interrupt response time

The interrupt response times of the target device and simulator differ.

[Target device]

It takes 9 to 14 clock cycles from the generation of an interrupt until actual vector interrupt processing begins.

[Simulator]

Vector interrupt processing begins immediately upon the interrupt.

### 5.1.22 Execution of illegal instructions

If an illegal instruction (instruction code: 0xFF) is executed, the target device will be reset, but the simulator will go into an infinite loop (the illegal instruction will be executed repeatedly).

## 5.2 Cautions for using simulator GUI

### 5.2.1 Cautions for controlling each windows

The following keyboard operations are not available in the simulator windows (signal-data editor window, I/O panel window, and serial window).

* Navigation via tab or arrow keys (←, ↑, →, ↓)
* Deletion via the Del or Backspace keys
* Copy & paste and other operations via the Ctrl + C, V, X, A, or Z keys.

Perform the above operations as follows.

* Navigation: Navigate using the mouse.
* Deletion: Right click and perform the action via the context menu.
* Copy & paste, etc.: Right click and perform the action via the context menu.

### 5.2.2 Cautions for closing simulator GUI window

The simulator GUI window can only be closed by disconnecting from the debugging tool, or by closing CubeSuite+ proper. (The X button cannot be clicked.)

Additionally, although it appears that the X button can be pressed if Aero is enabled in Windows Vista, pressing this button will not close the GUI window.

### 5.2.3 Cautions for showing help for the simulator GUI window

Pressing the F1 key in the simulator GUI window will not display the help if none of the internal windows are visible (e.g. the I/O panel window).

To display the help for the simulator GUI window, from the GUI window's menu, select [Help] > [Main Window].

### 5.2.4 Cautions for disconnecting the debug tool

CubeSuite+ may exit if the debugging tool is disconnected while any of the following dialog boxes is open from the simulator GUI window. Make sure that the following dialog boxes are closed before disconnecting the debugging tool.

| | |
|---|---|
| •Save As | •Parts Button Properties |
| •Open | •Analog Button Properties |
| •New | •Parts Key Properties |
| •Color | •Parts Level Gauge Properties |
| •Font | •Parts Led Properties |
| •Customize | •Parts Segment LED Properties |
| •Loop | •Parts Matrix Led Properties |
| •Select Pin | •Parts Buzzer Properties |
| •Search Data | •Pull up / Pull down |
| •Format (UART) | •Entry Bitmap |
| •Format (CSI) | •Object Properties |
| •Message (e.g. Error) | |

### 5.2.5 Cautions for setting the Host Machine's language and region

If a Japanese OS is installed on your Host Machine, then if the language or region is set to other than Japanese/Japan, the menus and dialog-box names of the simulator GUI window will be shown in English. Similarly, if a non-Japanese OS is installed on your Host Machine, then if the language or region is set to Japanese/Japan, the menus and dialog-box names of the simulator GUI window will be shown in Japanese.

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Colophon 2.2