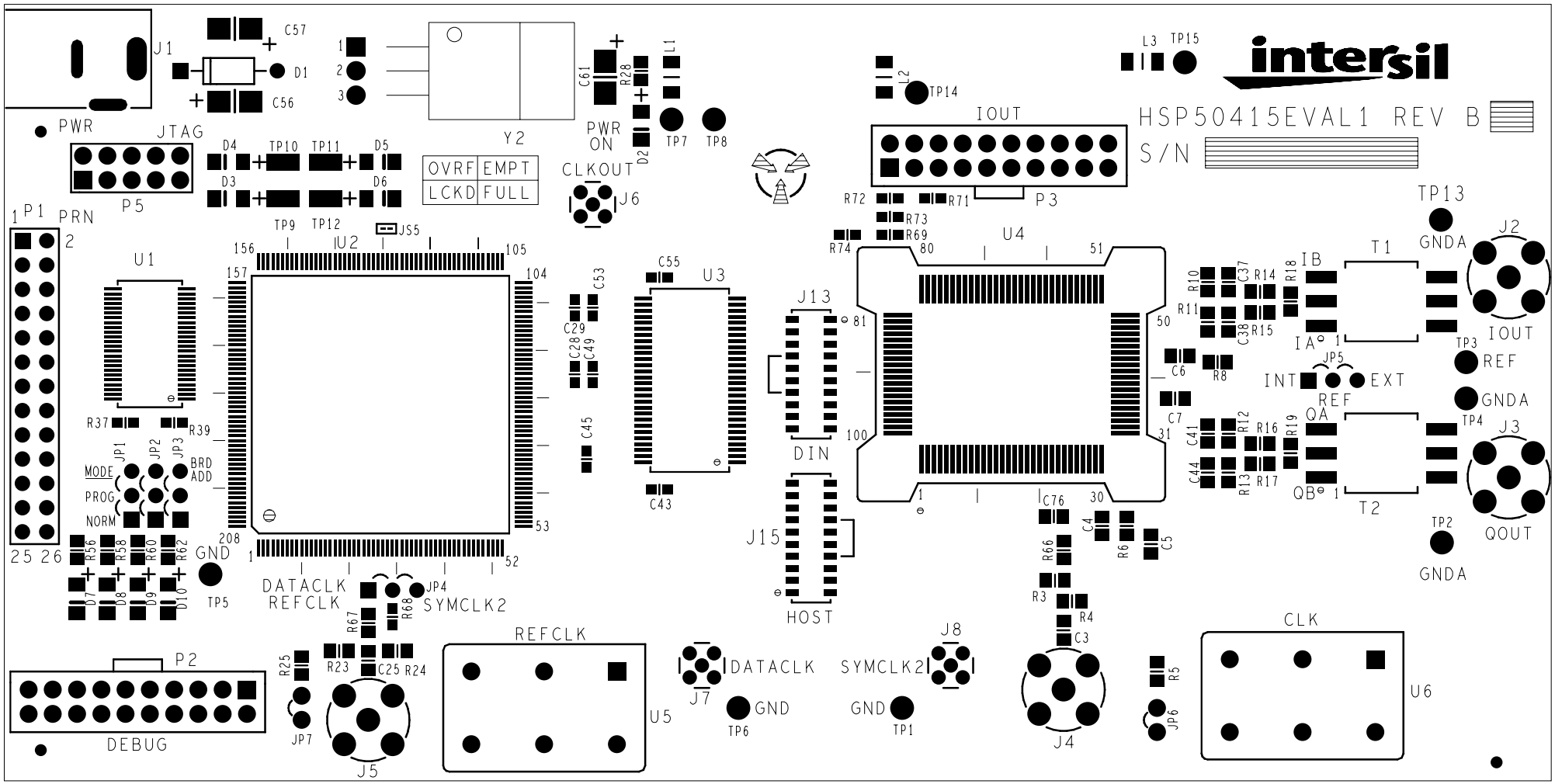
intersil
HSP50415EVAL1 REV B
S/N
PWR
JTAG
P5
P1
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U2
U3
U4
Y2
OVRF
EMPT
LCKD
FULL
CLKOUT
J6
PWR ON
IOUT
P3
TP13
GNDA
J2
IOUT
T1
IB
IA
TP3
REF
GNDA
JP5
INT
EXT
REF
QA
QB
T2
TP4
J3
QOUT
TP2
GNDA
J13
DIN
J15
HOST
MODE
PROG
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JP2
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BRD ADD
GND
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DATACLK
REFCLK
SYMCLK2
JP4
JS5
TP9
TP12
REFCLK
J5
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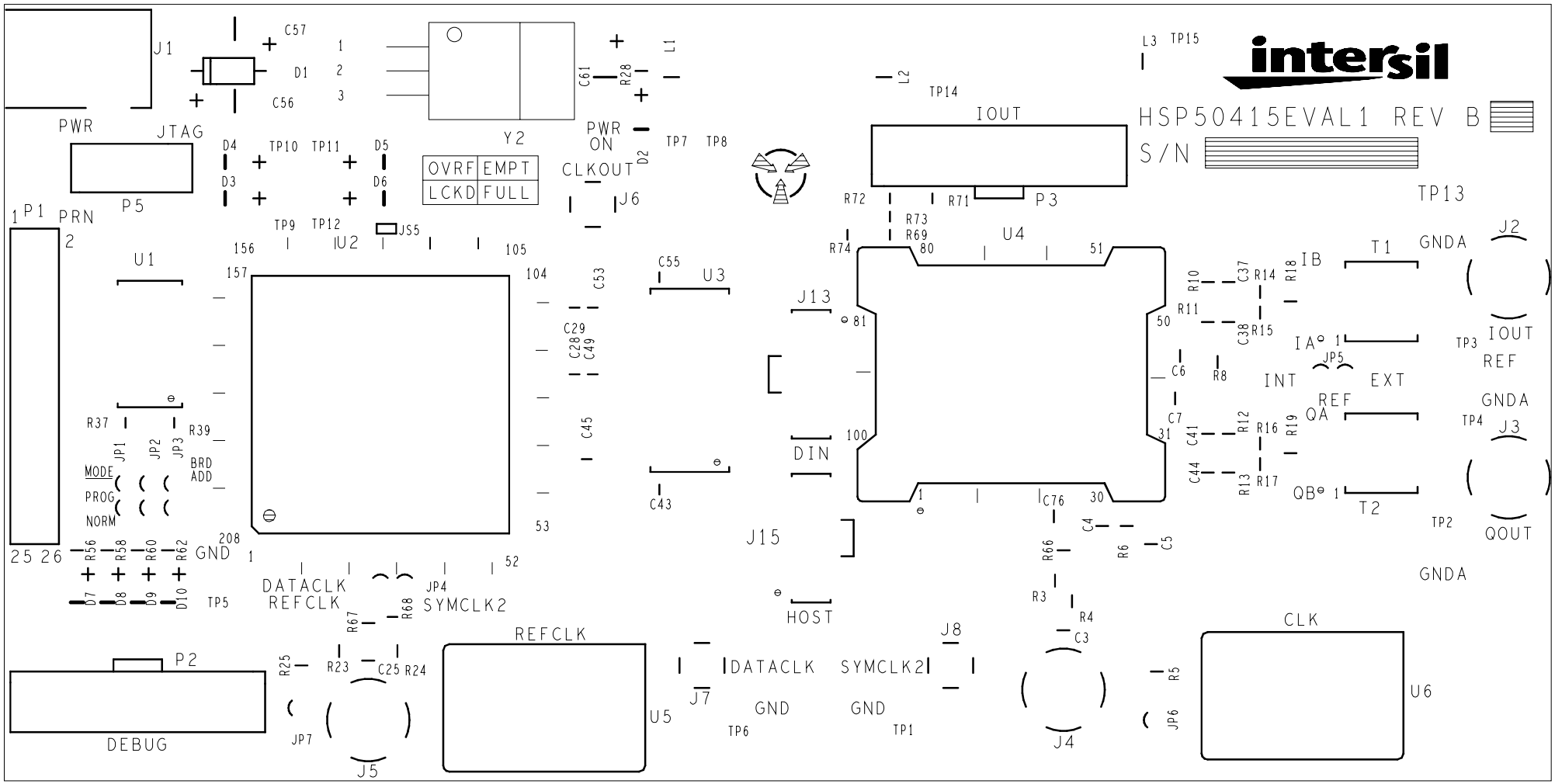
intersil
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CLKOUT
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OVRF
EMPT
LCKD
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PRN
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U2
JS5
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157
104
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DEBUG
REFCLK
U5
J7
DATACLK
SYMCLK2
GND
GND
TP6
TP1
J8
J4
R3
R4
C3
R5
JP6
CLK
U6
L2
TP14
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U4
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J13
81
100
DIN
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R66
R6
C5
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TP13
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GNDA
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IB
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R14
R18
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C38
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IA
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INT
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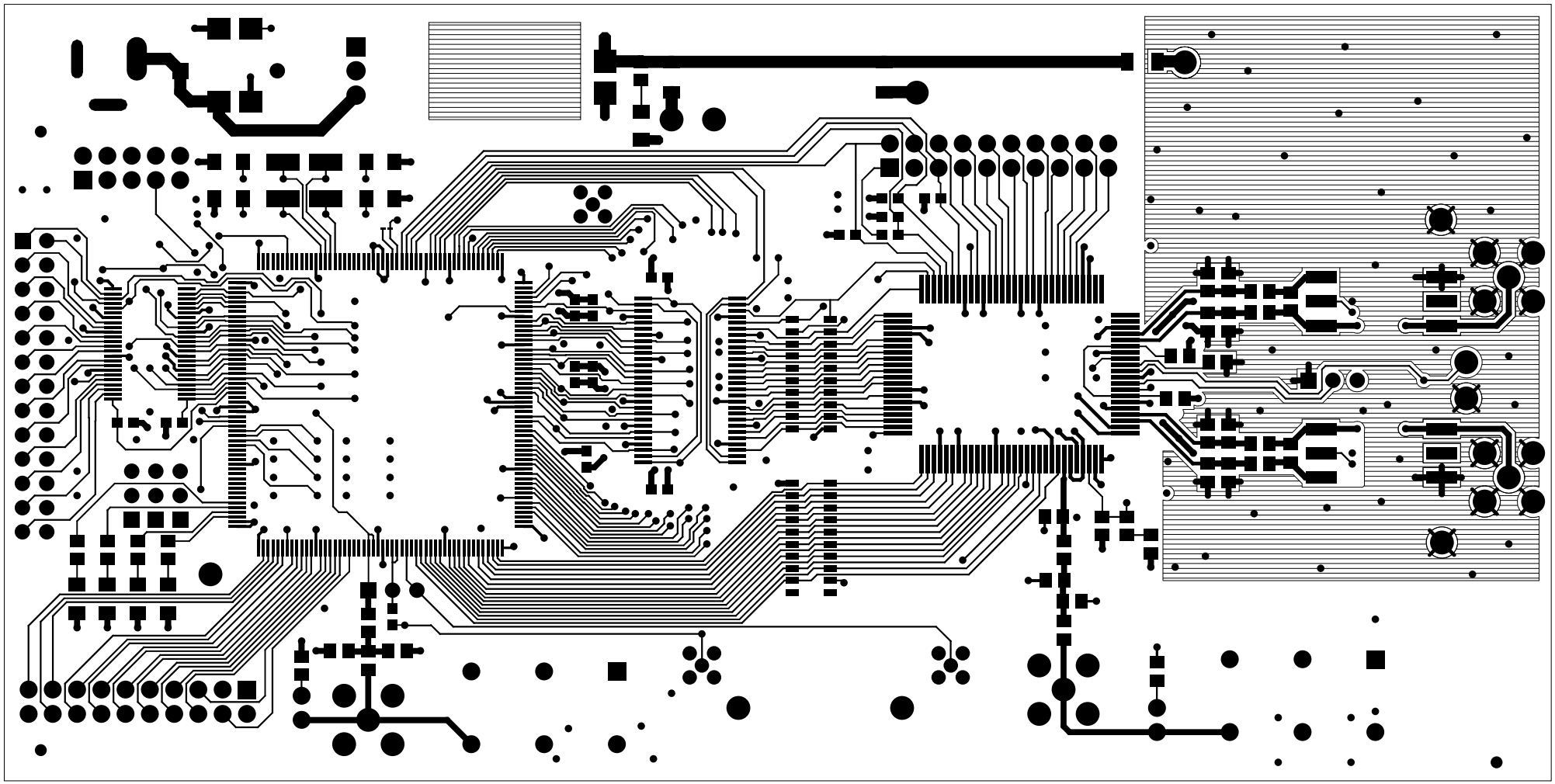
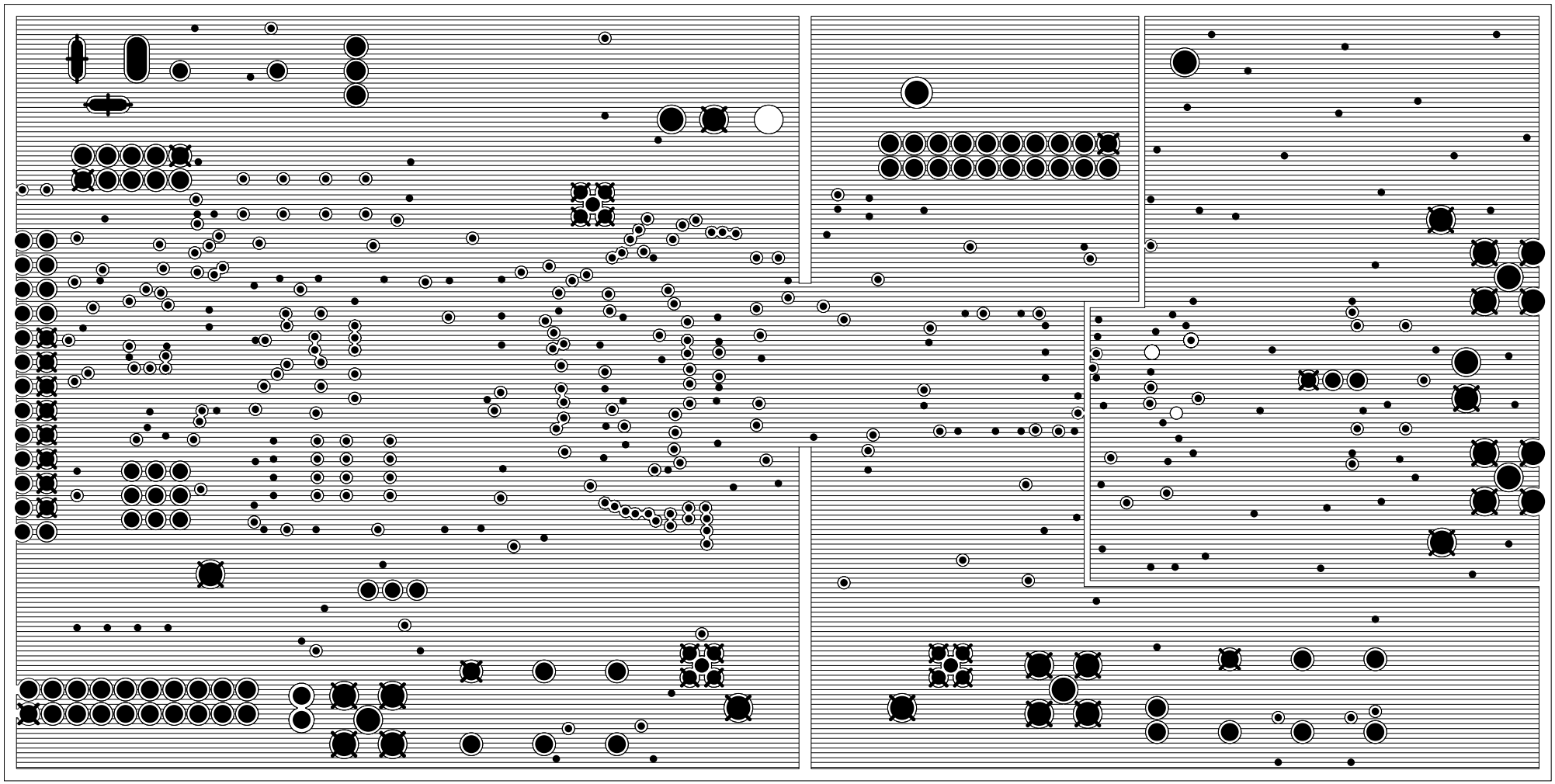
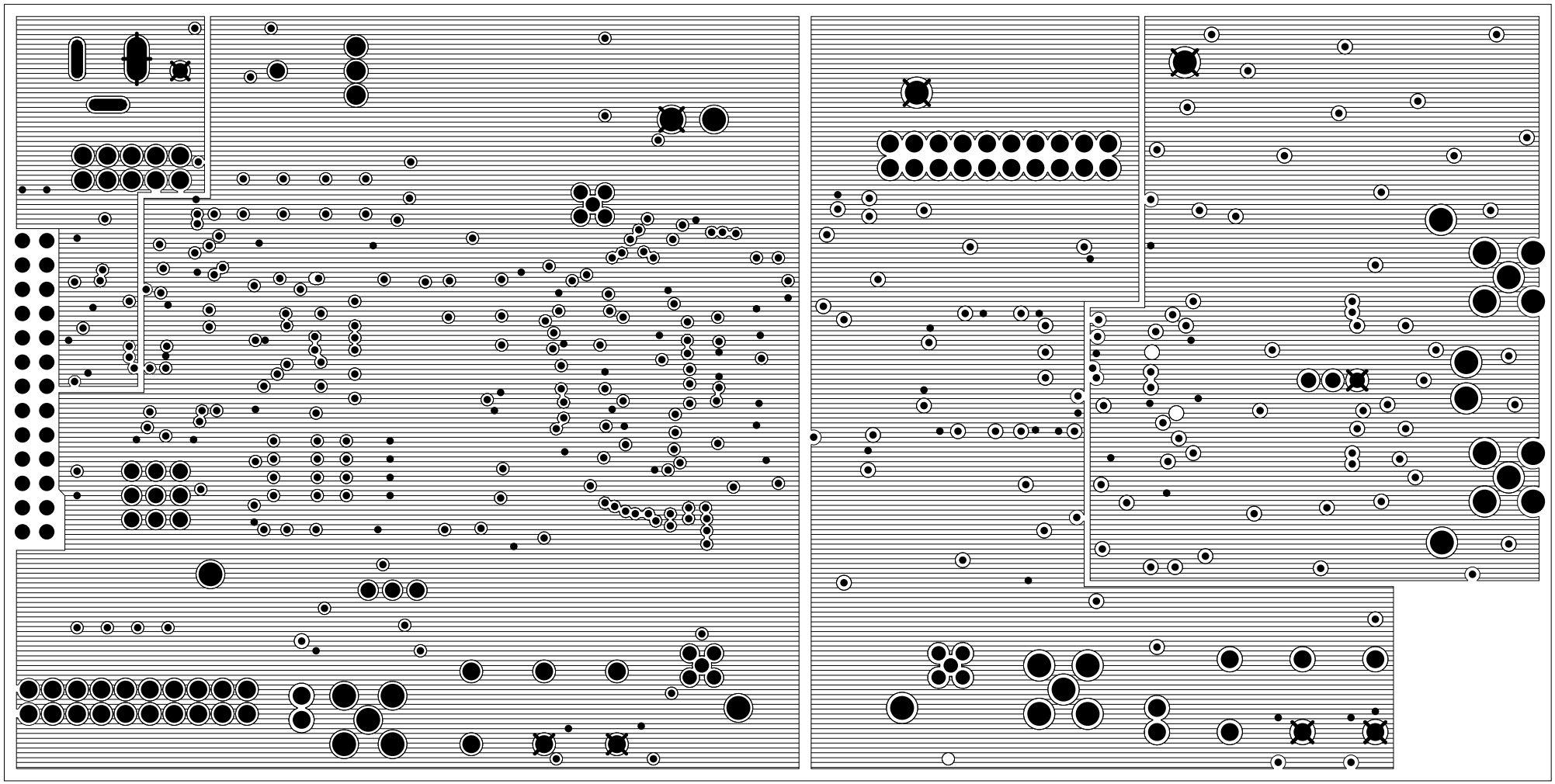
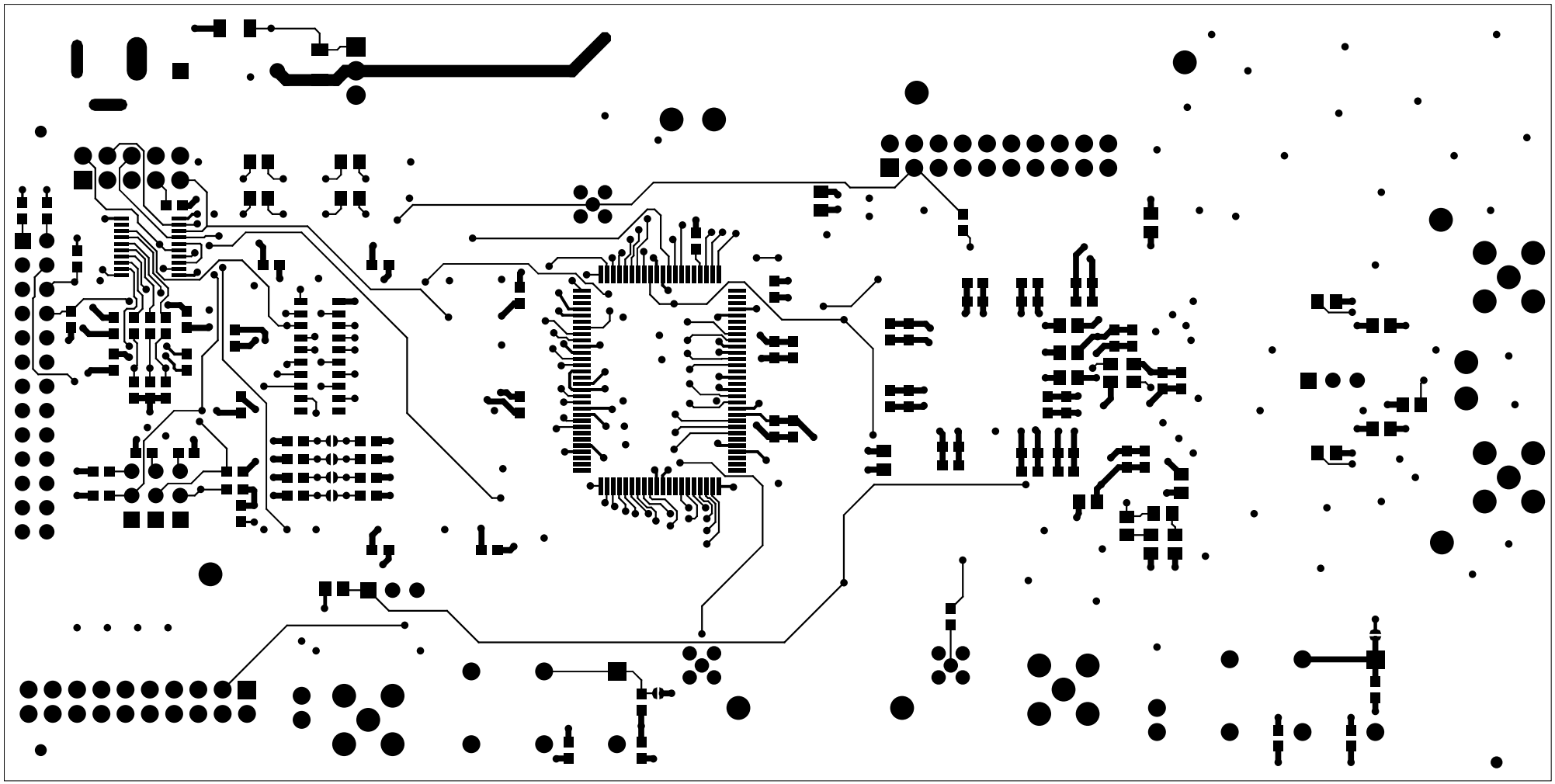
QOUT
GNDA









P2
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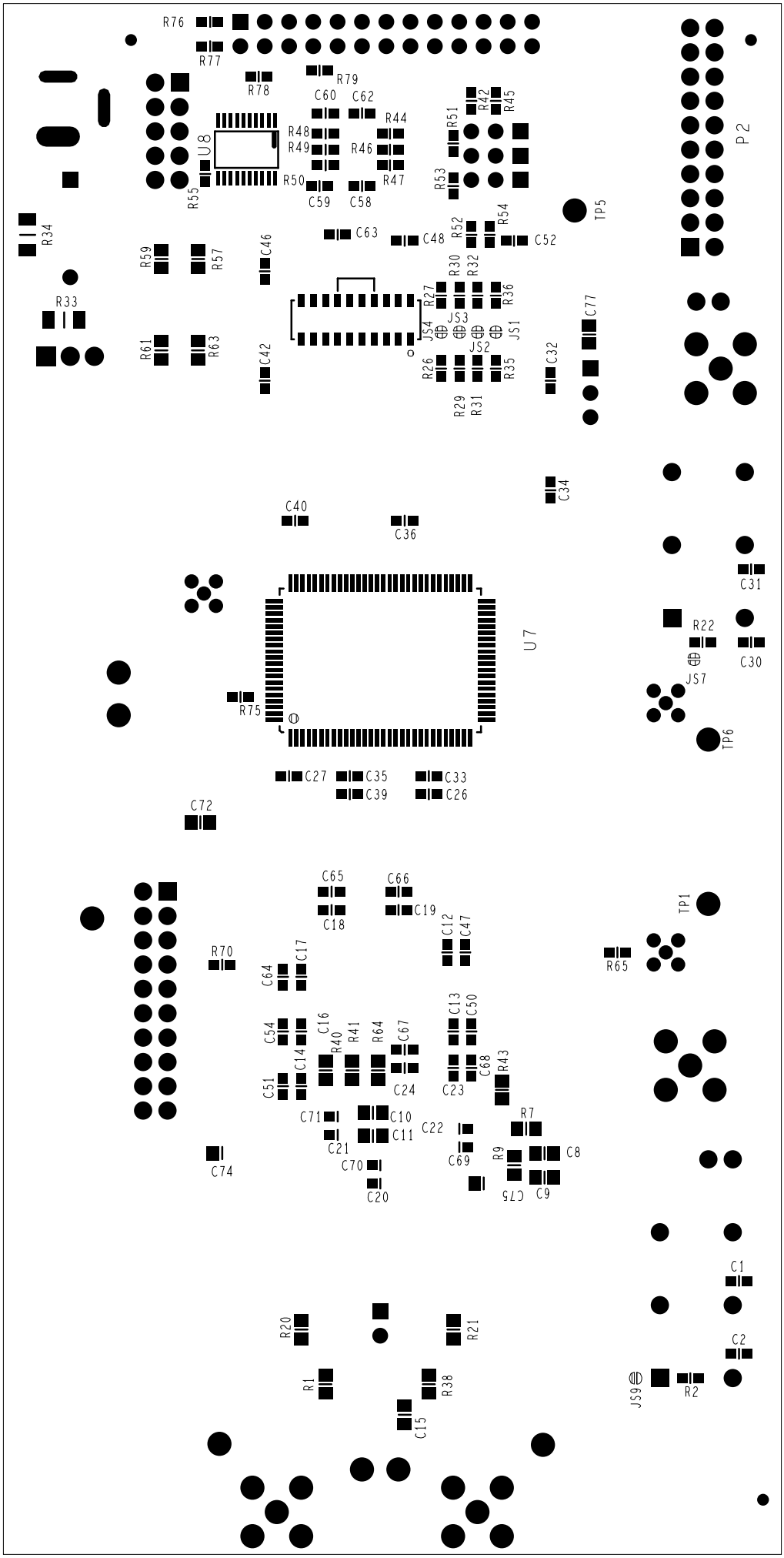
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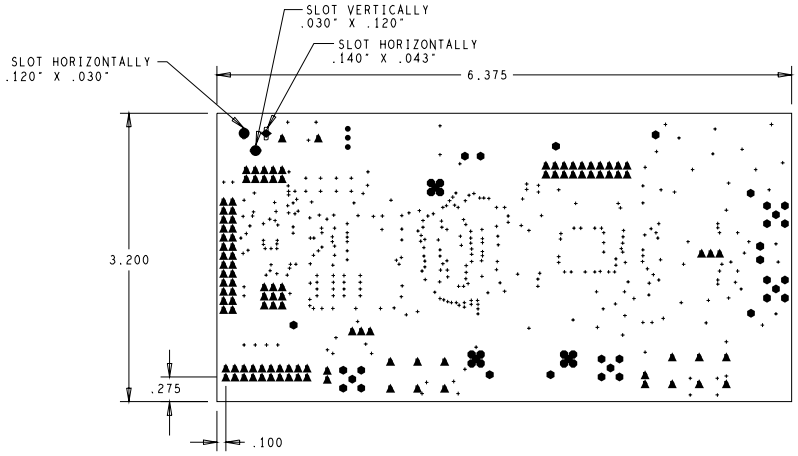
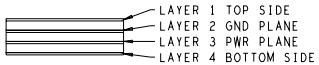
R2
C15

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPROVED
		DWG IN: CH IN: ECO NO: ———		





.062 THK
4 LAYERS

NOTES:

1. PRINTED WIRING BOARD DESIGN AND ACCEPTANCE CRITERIA SHALL BE IAW WITH THE REQUIREMENTS OF IPC-2221ß-2222 AND IPC-6011ß-6012.
2. MATERIAL: LAMINATED PLASTIC SHEET GFN (FR-4) .062 THICK IAW IPC-4101. MUST HAVE UL FLAMMIBILTY RATING OF 94V-0 OR BETTER.
3. FINISH: TIN/LEAD PLATE FUSED OR SOLDER COAT IAW IPC-2221ß-2222.
4. ALL PATTERNS ARE VIEWED FROM THE COMPONENT SIDE LOOKING THROUGH THE BOARD.
5. APPLY SOLDER MASK, BOTH SIDES OVER BARE COPPER IAW IPC-SM-840, CLASS 2 TYPE B1 (LPI) USE BLUE MASK
6. UNLESS OTHERWISE SPECIFIED ALL HOLE DIAMETERS ARE AFTER PLATING. TOLERANCE OF +/-.003.
7. DIMENSIONING AND TOLERANCING IAW ANSI Y14.5.
8. REMOVE ALL BURRS AND SHARP EDGES.
9. MINIMUM FINISHED LINE WIDTH SHALL BE .006.
10. APPLY SILKSCREEN TO BOTH SIDES IAW MARKING TEMPLATES, USING WHITE NON-CONDUCTIVE EPOXY INK.
11. PWB MUST BE 100% ELECTRICALLY TESTED FOR SHORTS AND CONTINUITY.
12. MARK DATE CODE AND MANUFACTURERS IDENTIFICATION ON SOLDER SIDE PER IPC-6011ß-6012.

DRILL CHART			
FIGURE	SIZE	PLATED	QTY
+	.012	PLATED	358
●	.030	PLATED	2
●	.037	PLATED	15
▲	.041	PLATED	109
◆	.043	PLATED	1
●	.048	PLATED	11
•	.055	PLATED	3
▪	.068	PLATED	20

REV	REVISION ASSY	MADE ON	
APPLICATION			

PART TO BE FREE OF BURRS AND SHARP EDGES. CONNECTOR TOLERANCES APPLY AT EDGE TO BE MEASURED WITH CONTACT PLT MARKS NORMALLY PLT UNDER. CONTACTS ARE PER ASTC-2221-6 CONNECTOR PER ASTC-2222-6 LEAD FINISH PER ASTC-2221-6 DIMENSIONING AND TOLERANCING PER ANSI Y14.5 ELEVATION AND ELECTRONIC DRAWING PER ANSI Y14.5 GRAPHIC SYMBOLS FOR ELECTRICAL AND ELECTRONIC DIAGRAMS PER ANSI Y32.2 REFERENCE AND ELECTRONIC REFERENCE DESIGNATIONS PER ANSI Y32.16 MODIFIED PER MIL-STD-806-9E-2 INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

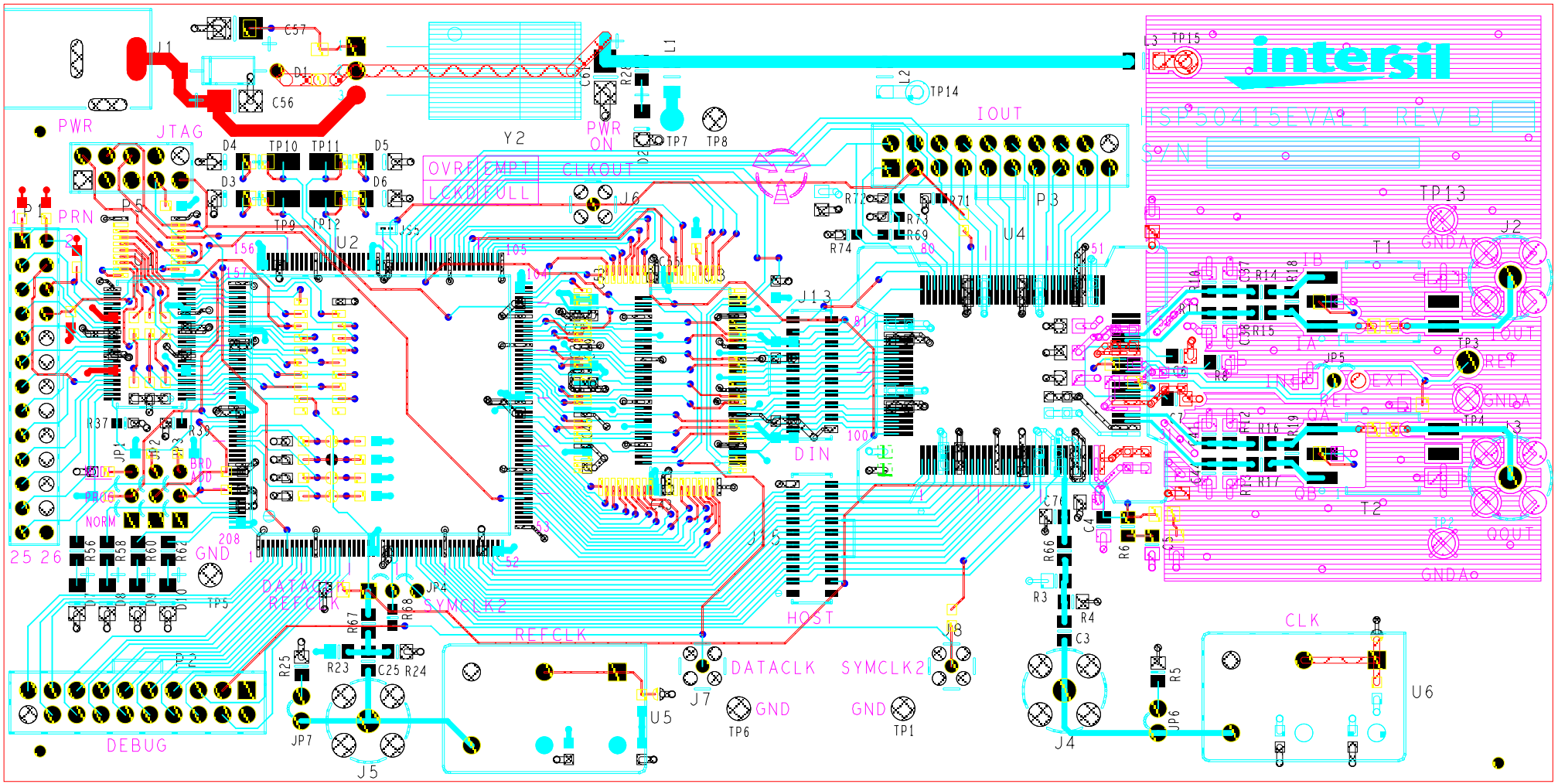
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND INCLUDE APPLIED FINISH THICKNESS
2 PLACE DIM. ± .xx — 3 PLACE DIM. ± .xxx — ANGLES ± —°
MATL: X
FINISH: X

CONTRACT NO. XXXXXX
DRN BY 10-28-99 CHK BY
APD Inc.
ENGR ELEC ENGR
PROJ ENGR MFG ENGR
RELIABILITY COMPONENTRY
APPROVAL - EPIS QA
APPROVAL SYS ENGR

intersil

PRINTED WIRING BOARD-
HSP50415EVAL1

SIZE	CAGE CODE	DWG NO.	REV
E	77245	X	B
SCALE 2/1		SHEET 1 OF 1	


intersil
HSP50415EVAL1 REV B
S/N
PWR
JTAG
PWR ON
IOUT
CLKOUT
OVRFL EMPTY
LCKD FULL
PRN
DIN
HOST
DATACLK
SYMCLK2
REFCLK
GND
CLK
DEBUG
J1
J2
J3
J4
J5
J6
J7
J8
J13
J15
U2
U4
U5
U6
P3
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Y2
T1
T2
TP13
TP14
TP15
GNDA
IOUT
QOUT
IA
IB
QA
QB
EXT
REF