Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

PCN #: **N1508-01** Date: September 21, 2015

Product Affected: 8T73S208-01NLGI (8)
8T74S208-01NLGI (8)
(Refer to Table 1 for the affected part#)

Date Effective: December 21, 2015

MEANS OF DISTINGUISHING CHANGED DEVICES:

- ■ Product Mark Change in ordering part#
- ☐ Back Mark
- ☐ Date Code
- ☐ Other

Contact: TSD Clock Team
E-mail: clocks@idt.com

Attachment: ■ Yes ☐ No
Samples: Samples are available now.

DESCRIPTION AND PURPOSE OF CHANGE:

- ☐ Die Technology
- ☐ Wafer Fabrication Process
- ☐ Assembly Process
- ☐ Equipment
- ☐ Material
- ☐ Testing
- ☐ Manufacturing Site
- ■ Data Sheet
- ■ Other - Die Revision Change

This notice is to advise our customers that the IDT Part 8T73S208A-01NLGI (8) / 8T74S208A-01NLGI (8) is an updated version of the 8T73S208-01NLGI (8) / 8T74S208-01NLGI (8) to improve the noise immunity for an overall better performance in I2C operations.

There is a minor change to the top metal. The is no change to the die/package technology or manufacturing. The change in datasheet parameters is shown in page 3 and page 4.

We are requesting a last time buy of the previous version by December 21, 2015.

RELIABILITY/QUALIFICATION SUMMARY:

There is no change in die technology/process.

CUSTOMER ACKNOWLEDGMENT OF RECEIPT:

IDT records indicate that you require written notification of this change. Please use the acknowledgement below or E-Mail to grant approval or request additional information. If IDT does not receive acknowledgement within 30 days of this notice it will be assumed that this change is acceptable.
IDT reserves the right to ship either version manufactured after the process change effective date until the inventory on the earlier version has been depleted.

Customer: _____ ☐ ***Approval for shipments prior to effective date.***

Name/Date: _____ E-Mail Address: _____

Title: _____ Phone # /Fax #: _____

CUSTOMER COMMENTS: _____

IDT ACKNOWLEDGMENT OF RECEIPT:

RECD. BY: _____ DATE: _____

Integrated Device Technology, Inc.
6024 Silver Creek Valley Road, San Jose, CA 95138

PRODUCT/PROCESS CHANGE NOTICE (PCN)

ATTACHMENT 1 - PCN #: N1508-01

PCN Type: Die Revision Change / Datasheet

Data Sheet Change: Yes

Detail of Change: This notice is to advise our customers that the IDT Part 8T73S208A-01NLGI (8) / 8T74S208A-01NLGI (8) is an updated version of the 8T73S208-01NLGI (8) / 8T74S208-01NLGI (8) to improve the noise immunity for an overall better performance in I2C operations.

There is a minor change to the top metal. The is no change to the die/package technology or manufacturing. The change in datasheet parameters is shown in page 3 and page 4.

We are requesting a last time buy of the previous version by December 21, 2015.

Table 1

Old Ordering Part Number	New Ordering Part Number
8T73S208-01NLGI	8T73S208A-01NLGI
8T73S208-01NLGI8	8T73S208A-01NLGI8
8T74S208-01NLGI	8T74S208A-01NLGI
8T74S208-01NLGI8	8T74S208A-01NLGI8

Qualification Test Plan and Result:

Qual Vehicle: 8T73S208A-01NLGI, 8T74S208A-01NLGI

Test Description	Test Method (Latest specs in effect)	Test Results (SS / Rej)	
		8T73S208A-01NLGI	8T74S208A-01NLGI
ESD: Human Body Model @ 2000V	JS-001	3/0	3/0
ESD: Charged Device Model @ 500V	JESD22-C101	3/0	3/0
Latch-up	JESD78	6/0	6/0

A)

FROM

8T73S208-01

Table 4B. LVCMOS/LVTTL Input DC Characteristics, $V_{CC} = V_{CCO} = 2.5V \pm 5\%$ or $3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage[1]		$V_{CC} = 3.3V$	2.2		$V_{CC} + 0.3$	V
			$V_{CC} = 2.5V$	1.7		$V_{CC} + 0.3$	V
V_{IL}	Input Low Voltage[1]		$V_{CC} = 3.3V$	-0.3		0.8	V
			$V_{CC} = 2.5V$	-0.3		0.7	V
I_{IH}	Input High Current	FSEL[1:0], ADR[1:0]	$V_{CC} = V_{IN} = 2.625$ or $3.465V$			150	µA
		SCL, SDA	$V_{CC} = V_{IN} = 2.625$ or $3.465V$			10	µA
I_{IL}	Input Low Current	FSEL[1:0], ADR[1:0]	$V_{CC} = 2.625$ or $3.465V$, $V_{IN} = 0V$	-10			µA
		SCL, SDA	$V_{CC} = 2.625$ or $3.465V$, $V_{IN} = 0V$	-150			µA

NOTE 1: V_{IL} should not be lower than -0.3V and V_{IH} should not be higher than $V_{CC} + 0.3V$.

TO

8T73S208A-01

Table 4B. LVCMOS/LVTTL Input DC Characteristics, $V_{CC} = V_{CCO} = 2.5V \pm 5\%$ or $3.3V \pm 5\%$, $V_{EE} = 0V$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage[1]	FSEL[1:0], ADR[1:0]	$V_{CC} = 3.3V \pm 5\%$	2.2		$V_{CC} + 0.3V$	V
		SCL, SDA	$V_{CC} = 3.3V \pm 5\%$	2.4		$V_{CC} + 0.3V$	V
		FSEL[1:0], ADR[1:0]	$V_{CC} = 2.5V \pm 5\%$	1.7		$V_{CC} + 0.3V$	V
		SCL, SDA	$V_{CC} = 2.5V \pm 5\%$	1.9		$V_{CC} + 0.3V$	V
V_{IL}	Input Low Voltage[1]	FSEL[1:0], ADR[1:0]	$V_{CC} = 3.3V \pm 5\%$	-0.3		0.8	V
		SCL, SDA	$V_{CC} = 3.3V \pm 5\%$	-0.3		0.8	V
		FSEL[1:0], ADR[1:0]	$V_{CC} = 2.5V \pm 5\%$	-0.3		0.7	V
		SCL, SDA	$V_{CC} = 2.5V \pm 5\%$	-0.3		0.5	V
I_{IH}	Input High Current	FSEL[1:0], ADR[1:0]	$V_{CC} = V_{IN} = 2.625$ or $3.465V$			150	µA
		SCL, SDA	$V_{CC} = V_{IN} = 2.625$ or $3.465V$			10	µA
I_{IL}	Input Low Current	FSEL[1:0], ADR[1:0]	$V_{CC} = 2.625$ or $3.465V$, $V_{IN} = 0V$	-10			µA
		SCL, SDA	$V_{CC} = 2.625$ or $3.465V$, $V_{IN} = 0V$	-150			µA

NOTE 1: V_{IL} should not be lower than -0.3V and V_{IH} should not be higher than $V_{CC} + 0.3V$.

B)

FROM

8T74S208-01

Table 4B. LVCMOS/LVTTL Input DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage[1]			1.7		$V_{DD} + 0.3$	V
V_{IL}	Input Low Voltage[1]			-0.3		0.7	V
I_{IH}	Input High Current	FSEL[1:0], ADR[1:0]	$V_{DD} = V_{IN} = 2.625$			150	µA
		SCL, SDA	$V_{DD} = V_{IN} = 2.625$			5	µA
I_{IL}	Input Low Current	FSEL[1:0], ADR[1:0]	$V_{DD} = 2.625$, $V_{IN} = 0V$	-10			µA
		SCL, SDA	$V_{DD} = 2.625$, $V_{IN} = 0V$	-150			µA

NOTE: 1. V_{IL} should not be lower than -0.3V and V_{IH} should not be higher than $V_{DD} + 0.3V$.

TO

8T74S208A-01

Table 4B. LVCMOS/LVTTL Input DC Characteristics, $V_{DD} = V_{DDO} = 2.5V \pm 5\%$, $T_A = -40°C$ to $85°C$

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage[1]	FSEL[1:0], ADR[1:0]	$V_{DD} = 2.5V \pm 5\%$	1.7		$V_{CC} + 0.3V$	V
		SCL, SDA	$V_{DD} = 2.5V \pm 5\%$	1.9		$V_{CC} + 0.3V$	V
V_{IL}	Input Low Voltage[1]	FSEL[1:0], ADR[1:0]	$V_{DD} = 2.5V \pm 5\%$	-0.3		0.7	V
		SCL, SDA	$V_{DD} = 2.5V \pm 5\%$	-0.3		0.5	V
I_{IH}	Input High Current	FSEL[1:0], ADR[1:0]	$V_{DD} = V_{IN} = 2.625$			150	µA
		SCL, SDA	$V_{DD} = V_{IN} = 2.625$			5	µA
I_{IL}	Input Low Current	FSEL[1:0], ADR[1:0]	$V_{DD} = 2.625$, $V_{IN} = 0V$	-10			µA
		SCL, SDA	$V_{DD} = 2.625$, $V_{IN} = 0V$	-150			µA

NOTE 1: V_{IL} should not be lower than -0.3V and V_{IH} should not be higher than $V_{DD} + 0.3V$.