RENESAS
BIG IDEAS FOR EVERY SPACE

RF TIMING FAMILY

As part of its broad, market-leading timing portfolio, Renesas offers highly differentiated RF timing devices for applications where synchronization, phase alignment, jitter attenuation, and low phase noise signal generation are critical for system performance, such as wireless infrastructure 4G / 5G radio, communication systems, mmWave, CATV, test and measurement equipment and industrial systems. Our broad portfolio of RF timing solutions delivers exceptional performance by combining our technology and technical innovations in compact packages.

Radio synchronizers and JESD204B/C clock jitter attenuator offer leading phase noise and jitter for best 4G /5G radio EVM / EMR, excellent close-in phase noise for eCPRI and CPRI applications, high fanout for high-density radios, and JESD204B/C support for converter synchronization. These devices remove virtually all noise from input reference clock and some also support Synchronous Ethernet and IEEE 1588 synchronization.

RF and mmWave synthesizers offer leading phase noise and spurious performance, low-power consumption and integrate wideband VCOs with frequencies supporting multi-carrier, multi-mode FDD and TDD base station radio card applications.

The industry's broadest buffer portfolio provides copies of RF clock signals with extremely low additive jitter and a wide range of optional features including phase delay adjustment, multi-chip phase alignment, frequency-division capabilities and JESD204B/C support. Renesas RF buffers are available in a variety of fanout options.

For 5G massive MIMO and beamforming applications, our RF timing solutions also support extremely low phase skew drift in temperature to reduce occurrences of recalibration events in the radio paths and optimize actual data transmission.

Product categories

- Radio synchronizers
- JESD204B/C clock jitter attenuator
- RF Synthesizers
- RF Buffers

Features

- Highly differentiated RF timing products
- Synchronous Ethernet and IEEE1588
- Lowest clock phase noise and jitter
- Best spurious suppression
- Flexible frequency generation

Applications

Wireless Infrastructure

- Base transceiver station
- Radio synchronization
- Distributed antenna system and repeater
- Reference clocks for high speed converter and transceiver (RF / IF)

Test and Measurement

- High-speed converter clocking
- Signal generator and spectrum analyzer
- Automated test equipment (ATE)

Military

- Tactical communication systems
- Radar

Wireless and Broadband Infrastructure

- Wireless and broadband
- Infrastructure
- Broadband CATV
- Headend (CMTS), edge QAM
- Distribution nodes
- Cable modem, set-top box,
- DVR / PVR
- DOCSIS 3.1
- Satellite receivers and modems

RF TIMING FAMILY

Radio Synchronizer

The single chip radio synchronization devices integrate digital PLLs with a high-performance RF-PLL for transceiver clock generation and jitter attenuation. With support for PTP (Precision Timing Protocol, IEEE1588), synchronous Ethernet and JESD204B/C, the devices simplify highly accurate synchronization designs. Devices implement multiple, independent frequency domains. 1PPS I/O signals can be used for synchronizing frequency, phase, and time of day. Devices are also suitable as PTP hardware clocks where phase is controlled by external software.

Part Number	Application	Main Frequencies	Outputs	Phase Noise (dBc/Hz) 1MHz offset
8V19N850D	eCPRI, IEEE1588, Sync-E, JESD204B/C	2 DPLLs: 1PPS (1 Hz) to 1 GHz input/output RF-PLL out: 2949.12 MHz and integer divisions	16	-150.8 dBc/Hz (156.25 MHz clock) -149.4 dBc/Hz (245.76 MHz clock

JESD204B/C Clock Jitter Attenuator

Renesas JESD204B/C clock jitter attenuators address radio designs including the latest 5G radio development, and continue to provide the industry's lowest phase noise clock signals. The low noise capability relies on an external VCXO and the RF frequency generation on an internal VCO. These devices generate up to eight clock frequencies on up to 18, tightly phase-aligned outputs. An integrated pulse generator provides JESD204B/C-compliant SYSREF synchronization signals aligned to the clock signals.

Part Number	Application	Main Frequencies (MHz)	Outputs	Phase Noise (12kHz-20MHz range)
8V19N880, 8V19N882	4G/5G/mmWave, CPRI, JESD204B/C	3932.16 and integer divisions ≤6000 with external VCO	18, 16	74 fs RMS
8V19N492-39	4G/5G, CPRI, JESD204B/C	3932.16 and integer divisions	15	46 fs RMS
8V19N491-36	4G/5G, CPRI, JESD204B/C	3686.4 and integer divisions	18	65 fs RMS
8V19N492, 8V19N490B	4G/5G, CPRI, JESD204B/C	2949.12 and integer divisions	15	57 fs RMS, 52 fs RMS
8V19N491-24, 8V19N490-24	4G/5G, CPRI, JESD204B/C	2457.6 and integer divisions	15, 18	66 fs RMS, 57 fs RMS
8V19N490-19	4G/5G, CPRI, JESD204B/C	1966.08 and integer divisions	18	57 fs RMS

RF Synthesizers

Renesas RF synthesizer PLLs integrate voltage-controlled oscillators (VCO) offering leading performance and an octave of frequency tuning range as a multi-band local oscillator (LO) up to 18 GHz. The wideband capability supports the reuse in different applications. Low phase noise variation in temperature and operation up to 105°C case temperature reduces the thermal constraints for the application.

Part Number	Application	Input Frequency Range (MHz)	VCO Frequency Range (MHz)	Output Frequency Range (MHz)	FOM (dBc/Hz)	Max. Output Power (dBm)
8V97003	5G/mmWave	10 to 1600	5500 to 11000	172 to 18000	-237 (Integer) -231 (Fractional	+14
8V97051L, 8V97053L	GSM900, 1800	10 to 310	2200 to 4400	34.375 to 4400	-231	-4 to 7
8V97052	SAT Com	5 to 310	2200 to 4400	34.375 to 4400	-228	-4 dBm to 11.5 dBm

RF Fanout Buffers

RF buffers extend the fanout of clock generators and RF synthesizer components. Typically driven by PLL components, RF buffers maintain the low phase noise and noise floor of the differential input signal. Each buffer provides exact copies of the input clock or data signal. Buffers have either a single or dual channels for driving clock and radio synchronization signals at the same propagation delay.

Part Number	Application / I/O	Output	Features	Frequency Max.
8V79S680 / 8V79S683	JESD204B/C	16 LVDS / LVPECL	Dual channel, Phase delay, Multi-chip alignment	3000 MHz
8T79S308 / 8T39210 / 8T39204	Universal	8 / 10 / 4 Differential, LVCMOS	Individual output enable, XTAL input	1500 to 3000 MHz
8SLVP family	LVPECL 3.3V/2.5V	1:2 – 1:12, single and dual	Low additive phase noise	2000 MHz
8SLVD family	LVDS 2.5V	1:2 – 1:12, single and dual	Low additive phase noise	2000 MHz
8P34S family	LVDS 1.8V	1:2 – 1:12, single and dual	Low additive phase noise, low power	1200 to 2000 MHz

To request samples, download documentation or learn more visit: **renesas.com/rftiming**

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