
Abstract

This document provides a checklist of important items and common pitfalls to go over during the layout of computing power regulators. The checklist should be used in conjunction with an internal design review as well as Intersil FAE and applications support to ensure an optimal layout before the tape out of a PCB in an attempt to minimize performance issues in the end application.

Sensitive/quiet/small signals include feedback, compensation, VCC sense, VSS sense, and anything else defined as such in the product datasheet.

Noisy and power signals include VIN, PHASE, PWM, upper gate, lower gate, boot, any communication lines such as SVID, and other signals called out as such in the datasheet.

Table of Contents

Abstract	1
General	2
Power Layout – See Appendix A and B	2
Signal Layout – See Appendix A and C	2
Appendix A – Example Power Path Layout	3
Appendix B – PVCC/AVCC Decoupling	4
Appendix C - Signal Routing Example	5

List of Figures

FIGURE 1. Appendix A – Example Power Path Layout	3
FIGURE 2. Incorrect Decoupling	4
FIGURE 3. Correct Decoupling	4
FIGURE 4. Incorrect Routing	5
FIGURE 5. Correct Routing	6

General

- All special requirements from the datasheet have been implemented
- Adequate physical clearance for components
- Adequate number of vias in power planes
- Separate AGND and PGND if required
- Multi-phase parts: Each PHASE node is laid out identically
- Integrated FET parts: VIN, PHASE, and GND should be on multiple layers for optimal thermal performance
- Multiple layers of copper also reduce parasitic resistance which, increases FETG $r_{DS(ON)}$ and reduces efficiency
- Integrated FET parts: Inductor(s) should be located close to the IC to aid with heatsinking

Power Layout – See Appendix A and B

- VIN is properly decoupled with the shortest possible power path
- PVCC/AVCC are decoupled according to the datasheet recommendation
- Adequate PHASE copper to handle max current and minimize parasitic resistance and inductance
- PHASE is not routed near sensitive analog signals and shielded through the use of ground pours and/or planes.
- Power path area (VIN, PHASE, VOUT, GND) is minimized to reduce parasitic resistance, inductance, and capacitance
- Upper and lower gate traces kept to a minimum length and sized appropriately (20mm to 25mm typically)
- Thermal pad on IC adequately connected to appropriate node if applicable
- Inductor current sense resistor node has sufficient copper to ensure proper thermal performance if using resistor sensing instead of DCR sensing
- Snubber components placed close to the inductor in the power path with a short path to GND

Signal Layout – See Appendix A and C

- Isolation of quiet signals from noisy ones
 - Quiet signals should be routed on a separate layer from noisy ones or shielded by GND copper
 - Avoid long parallel runs of sensitive and noisy signals
- All NTC are placed properly and close to their respective components
 - The DCR NTC should be in parallel with the appropriate inductor
 - The NTC on the NTC pin should be placed near the FETs
- Extra component hooks are in place in case they are needed during validation
- SVID lines are routed according to Intel's guidelines and shielded from any sensitive analog traces

Appendix A – Example Power Path Layout

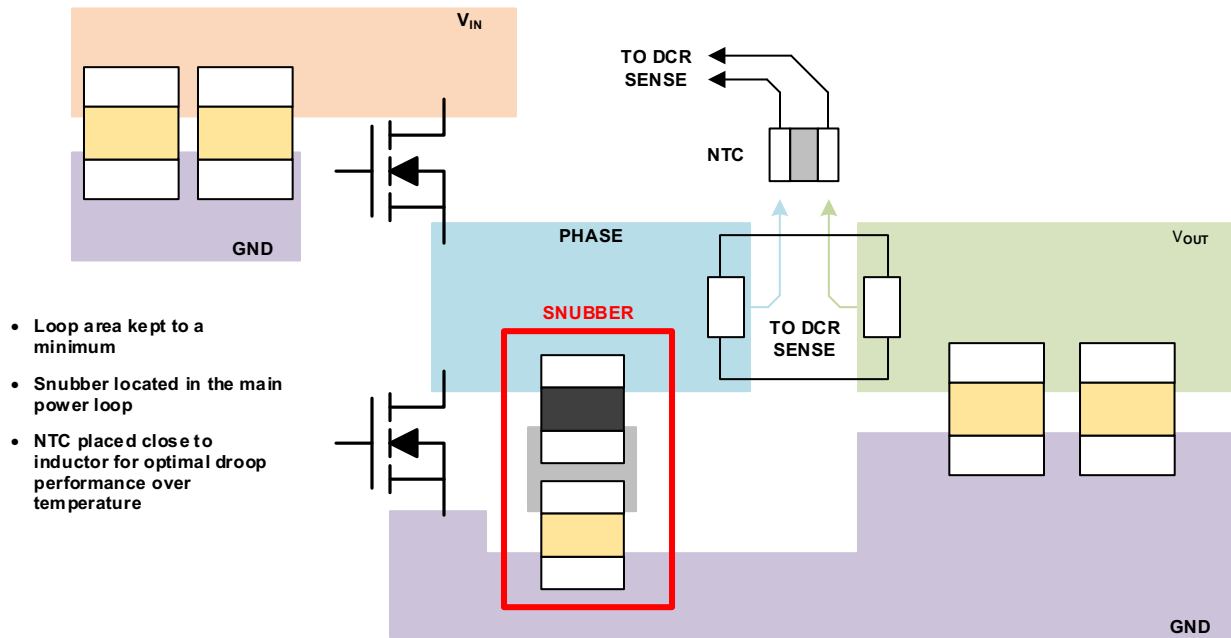


FIGURE 1. APPENDIX A – EXAMPLE POWER PATH LAYOUT

Appendix B – PVCC/AVCC Decoupling

- AVCC connected directly to PVCC
- One decoupling cap for both pins
- Possible noise injection from PVCC to AVCC

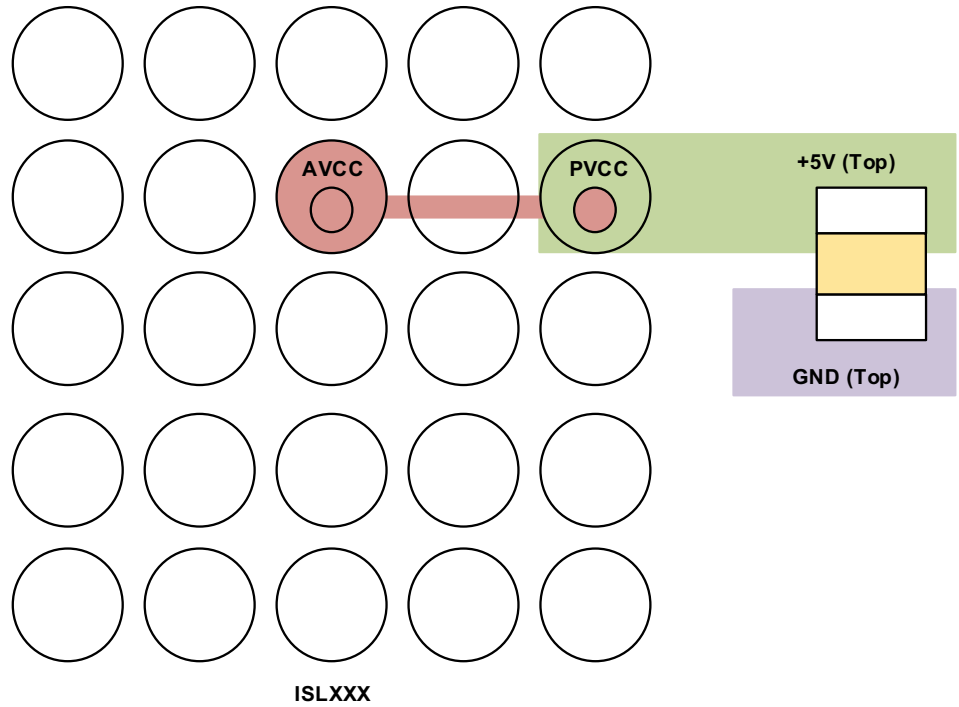


FIGURE 2. INCORRECT DECOUPLING

- Separate caps for each pin on the top and bottom of the PCB
- Avoids noise injection from PVCC to AVCC
- AVCC not directly connected to PVCC without a decoupling cap

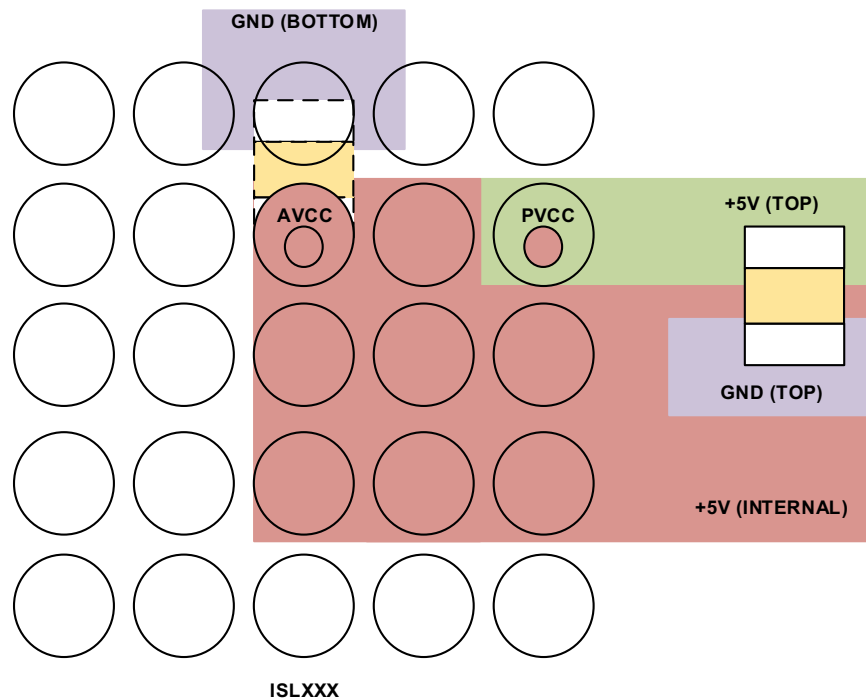


FIGURE 3. CORRECT DECOUPLING

Appendix C - Signal Routing Example

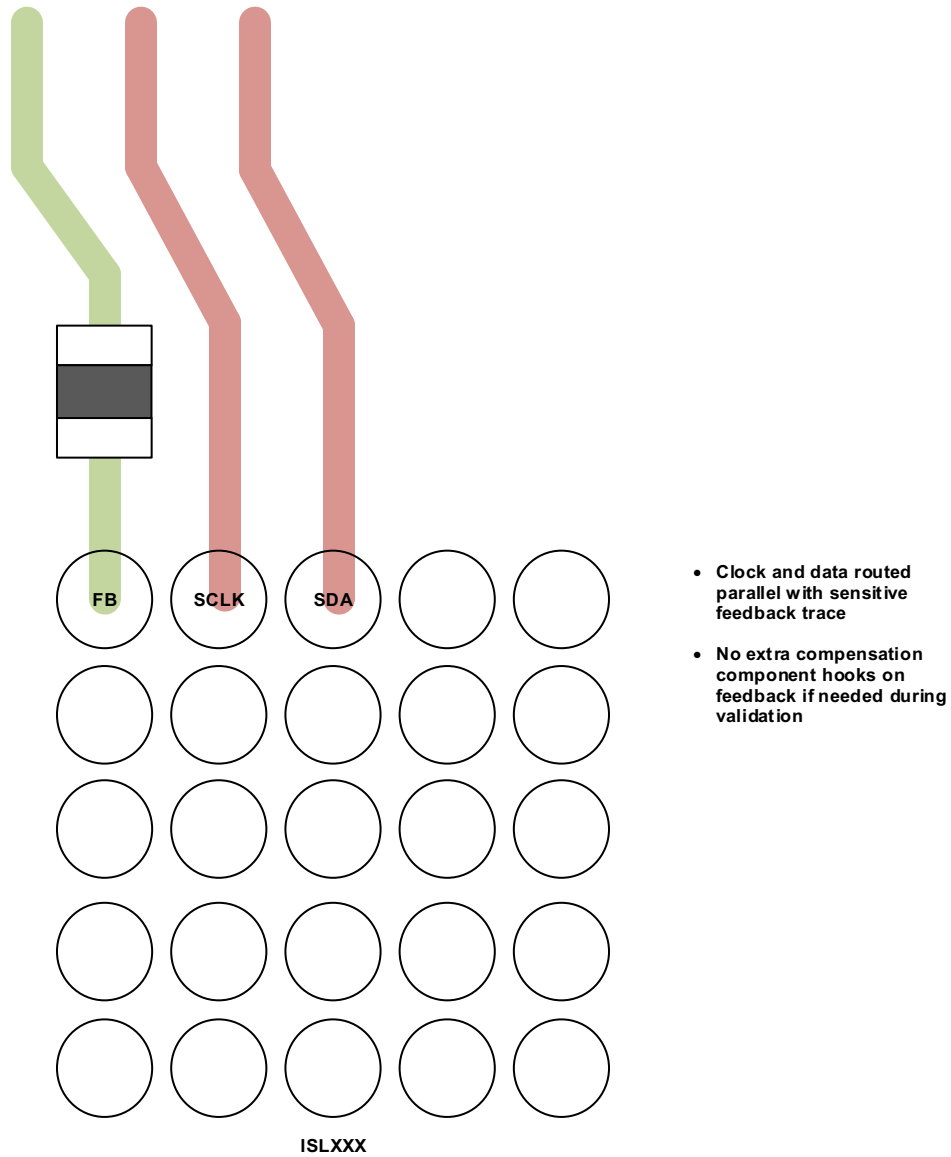
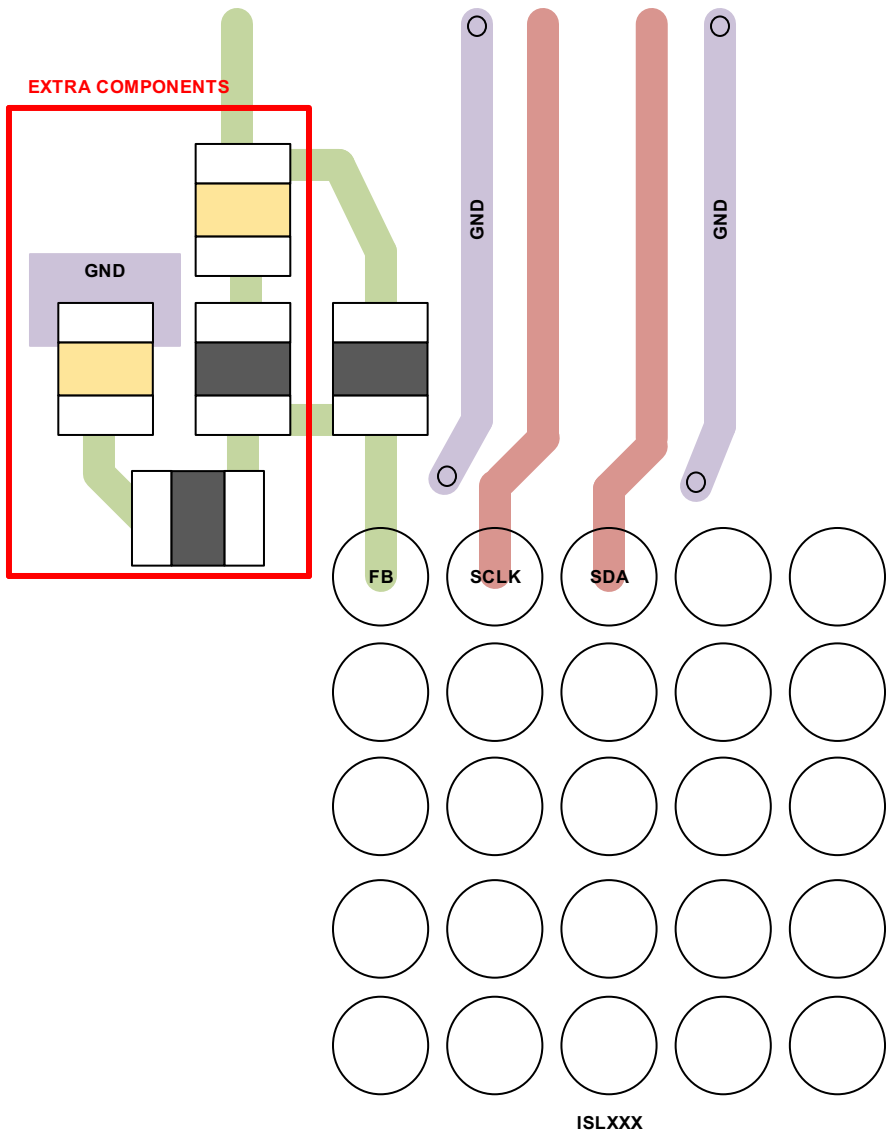


FIGURE 4. INCORRECT ROUTING

Appendix C - Signal Routing Example (Continued)



- Feedback shielded from clock and data as much as possible using GND traces
- Extra compensation components in place on feedback for tuning during validation

FIGURE 5. CORRECT ROUTING

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