User's Manual

32

RZ/T2L Group

Renesas Starter Kit+ for RZ/T2L
User's Manual

RZ/T Series for Real-Time Control

RZ Family

64-Bit & 32-Bit Arm®-Based High-End MPUs

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Disclaimer

By using this Renesas Starter Kit (RSK+), the user accepts the following terms:

The RSK+ is not guaranteed to be error free, and the entire risk as to the results and performance of the RSK+ is assumed by the User. The RSK+ is provided by Renesas on an “as is” basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title and non-infringement of intellectual property rights with regard to the RSK+. Renesas expressly disclaims all such warranties. Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this RSK+, even if Renesas or its affiliates have been advised of the possibility of such damages.

Precautions

The following precautions should be observed when operating any RSK+ product:

This Renesas Starter Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

- ensure attached cables do not lie across the equipment
- reorient the receiving antenna
- increase the distance between the equipment and the receiver
- connect the equipment into an outlet on a circuit different from that which the receiver is connected
- power down the equipment when not in use
- consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

- The user is advised that mobile phones should not be used within 10m of the product when in use.
- The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

The intention of this manual is to assist users in understanding the hardware functionality and electrical characteristics of this RSK+ product in overview. The target users of this manual are engineers designing sample code that runs on the RSK+ platform, with the use of various peripheral devices.

Though this manual includes an overview of the functionality of the RSK+ product, it is not intended to be a guide for embedded programming or hardware design.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Handling Precautions section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RSK+RZT2L. Be sure to refer to the latest versions of these documents. The newest versions of the listed documents are available on the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's manual	Explanation of the hardware specifications of the CPU board	Renesas Starter Kit+ for RZ/T2L User's Manual	R20UT5164EJ (this manual)
Quick start guide	Simple setup guide consisting of one piece of A4 paper	Renesas Starter Kit+ for RZ/T2L Quick Start Guide	R20UT5235EJ
User's manual for the hardware	Hardware specifications (pin assignments, memory maps, peripheral function specifications, electrical characteristics, timing charts) and descriptions of operation	RZ/T2L Group User's Manual: Hardware	R01UH0985EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
DIP	Dual In-line Package
DNF	Do Not Fit
EEPROM	Electronically Erasable Programmable Read Only Memory
ESC	EtherCAT Slave Controller
ESD	Electrostatic Discharge
EtherCAT	Ethernet for Control Automation Technology
GPT	General PWM Timer
I^2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
J-Link®	SEGGER debug probe
J-Link® OB	SEGGER On-board debug probe
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MAC	Media Access Control
MCU	Micro Controller Unit
MPU	Micro Processor Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
NMI	Non-Maskable Interrupt
PC	Personal Computer
PCB	Printed Circuit Board
POE	Port Output Enable
POEG	Port Output Enable for GPT
PWM	Pulse Width Modulation
RAM	Random Access Memory
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
ROM	Read Only Memory
RSK+	Renesas Starter Kit+
SCI	Serial Communications Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Table of Contents

1. Overview

1.1 Purpose

This RSK+ is an evaluation tool for a Renesas microprocessor. This manual describes the technical elements of the RSK+ hardware in detail. The method for installing software and the debugging environment are explained in the quick start guide.

1.2 Features

This RSK+ has the following features.

- Programming of a Renesas microprocessor
- Debugging of user code
- User circuits for switches, LEDs, and potentiometers
- Sample applications

This RSK+ is equipped with all of the circuits that are required for operating the microprocessor.

1.3 Board Specifications

Table 1-1 and Table 1-2 list the board specifications.

Table 1-1 Board Specifications (1)

Item	Specification
Microprocessor	Part No.: R9A07G074M04GBG*1
	Package: 196-pin FBGA
	On-chip memory: 1 Mbyte of RAM
On-board memory	OctaFlash: 512 Mbits
	HyperRAM: 64 Mbits
	QSPI serial flash memory: 128 Mbits
	I^2C EEPROM: 16 Kbits
Input clocks	RZ/T2L main: 25 MHz
	RL78/G1C main: 12 MHz
Power supplies	Power-supply connector: 5-V input
	USB type-C connector: 5-V input
	Power-supply IC: 5-V input, 3.3-V output
	Power-supply IC: 5-V input, 1.8-V output
	Power-supply IC: 5-V input, 1.1-V output
	Power-supply IC: 5-V input, 1.0-V output (for Ethernet PHY)
	Power-supply IC: 5-V input, 2.5-V output (for Ethernet PHY)
Debug interfaces	MIPI-10: 1.27-mm pitch, 10-pin box header
	MIPI-20: 1.27-mm pitch, 20-pin box header
	Mictor-38: 0.64-mm pitch, 38-pin box header
	J-Link® OB: USB micro-B
Slide switch	Power-supply switch: Single-pole double-throw type × 1
DIP switches	Mode setting: 8 switches × 1
	Signal selection: 10 switches × 4
	User switch: 4 switches × 1
Push switches	Reset switch × 1
	User switch × 3
Potentiometer (for A/D conversion)	Single-turn type (10 kΩ)
LEDs	For the power supply: green × 1
	For the user: (green) × 3, (yellow) × 1, (red) × 2 Among the above, (green) × 3 and (red) × 1 are also used for indicating the EtherCAT status.
	Ethernet status: (green) × 3 and (yellow) × 3 (built in to each RJ-45)
	J-Link® OB status: (yellow) × 1
2-port EtherCAT, 1-port Ethernet	Connector: RJ-45 × 3
	PHY: Single-channel PHY × 3

CAN	Connector*2: 2.54-mm pitch, 3 pins × 1
	CAN transceiver × 1
USB	USB function: USB mini-B
	USB host: USB type-A
RS485	Connector*2: 10 pins × 1
	RS485 transceiver × 1
USB-to-serial conversion interface	Connector: USB mini-B
	Driver: RL78/G1C microcontroller (part No.: R5F10JBCAFP)

Notes: 1. OTP cannot be evaluated with the device installed in this product.
2. The connector is not mounted on the product as shipped.

Table 1-2 Board Specifications (2)

Item	Specification
Pmod™	PMOD-2A, 6A: 12-pin connector
	PMOD-3A: 12-pin connector
mikroBUS™	2.54-mm pitch, 8 pins × 2 (J21, J22)
Grove®	2.00-mm pitch, 4 pins × 2 (J27, J28)
QWIIC®	1.00-mm pitch, 4 pins × 1 (J30)
Serial host interface	2.54-mm pitch, 14 pins × 1 (CN27)
Pin headers	2.54-mm pitch, 20 pins × 2 (CN1, CN3)*
	2.54-mm pitch, 14 pins × 1 (CN28)
Application header*	2.54-mm pitch, 26 pins × 2 (JA1, JA2), 50 pins × 1 (JA3), 24 pins × 2 (JA5, JA6)

Note: The connector is not mounted on the product as shipped.

2. Power Supply

2.1 Specifications of Power Supply

This board has a USB type-C connector (CN5) and a barrel power jack (CN6), and power can be supplied from either of these. Table 2-1 lists the specifications of power supply.

Table 2-1 Specifications of Power Supply

Connector	Specifications and Supply Voltage
CN5	USB type-C VBUS (5-V DC)
CN6	2.0-mm center-positive barrel connector, 5-V DC input*

Note: Though some RSK+ products require a 12-V power supply, the power supply of this board is 5 V. Be careful not to accidentally connect a 12-V power supply. When supplying power through CN6, use a stabilized power source that is capable of supplying at least 15 W.

2.2 Methods for Turning the Power On and Off

This board is equipped with a power switch (POWER_SW slide switch). When turning the power on, connect the power to CN5 or CN6 with the power switch turned off, and then turn the power switch on to start the power supply. To end the supply of power, turn the power switch off and then disconnect the power cable from CN5 or CN6. Figure 2-1 shows the arrangement and manipulation method of the power switch.

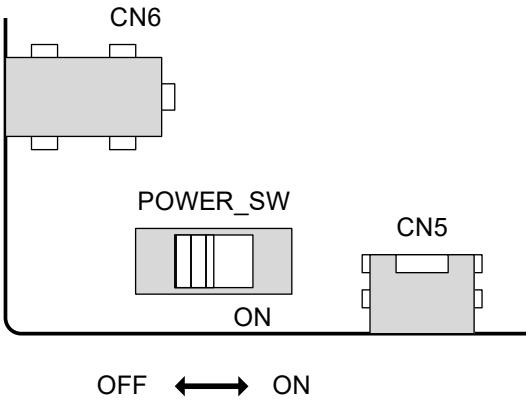


Figure 2-1 Arrangement and Method of Manipulating the Power Switch

2.3 Connectors for Current Measurement

This board has connectors for measuring currents, and each current value can be measured by inserting an ammeter between pins 1-2 of the given connector. Table 2-2 is a list of the connectors for measuring currents.

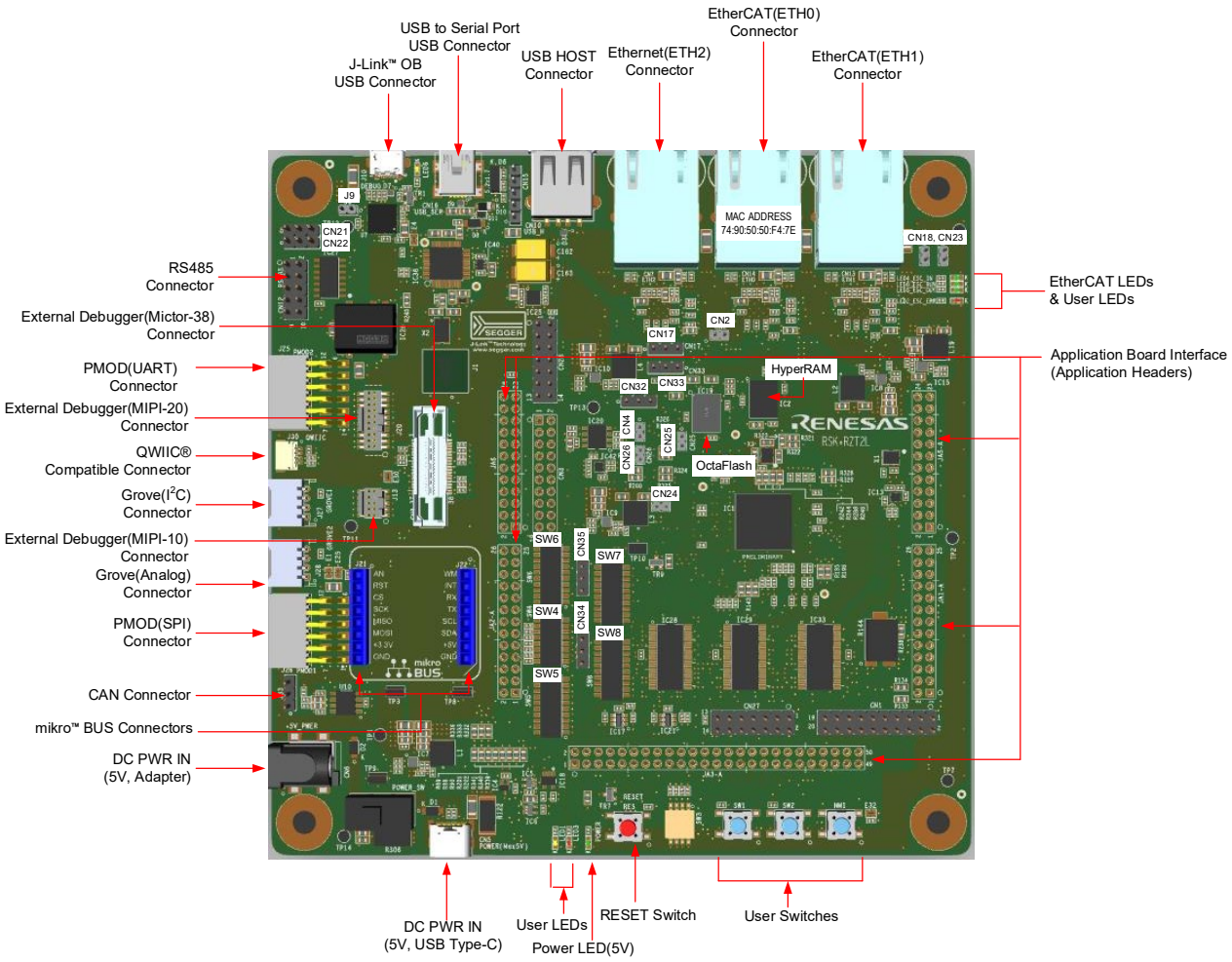
Table 2-2 List of Connectors for Current Measurement

Connector	Purpose
CN24	For measuring the current of the power supply (VCC11_RZCORE) line input to the 1.1-V power supply of the RZ/T2L
CN25	For measuring the current of the power supply (CPU1V8) line input to the 1.8-V power supply of the RZ/T2L
CN26	For measuring the current of the power supply (CPU3V3) line input to the 3.3-V power supply of the RZ/T2L
CN2	For measuring the current of the power supply (CPU_VCC1833_2) line input to the VCC1833_2 power supply of the RZ/T2L
CN4	For measuring the current of the power supply (CPU_VCC1833_3) line input to the VCC1833_3 power supply of the RZ/T2L

3. Board Layout

3.1 Component Layouts

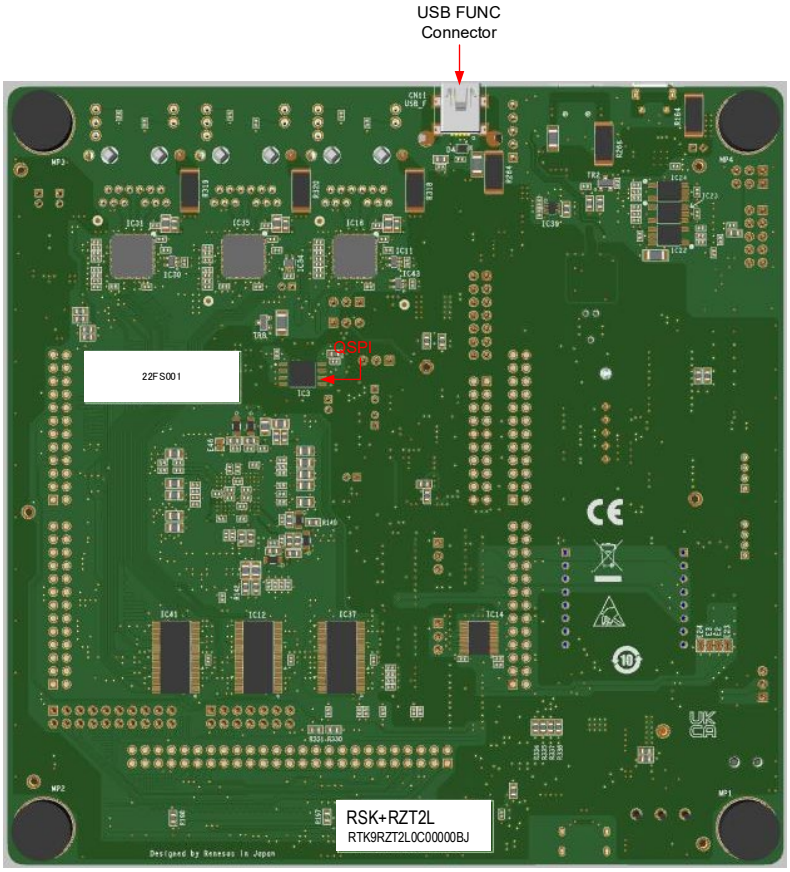
Figure 3-1 and Figure 3-2 show the component layouts on the top and on the soldered side of this board.



Notes: 1. For the details of each function, refer to chapter 7.

2. The MAC address shown in the figure is an example. Use a unique MAC address when running Ethernet software.

Figure 3-1 Board Layout (Top Side)



Note: The serial number (22FS001) is an example.

Figure 3-2 Board Layout (Soldered Side)

3.2 Board Dimensions

Figure 3-3 shows the board dimensions and positions of connectors on this board. The through-hole connectors of application headers are placed on a 2.54-mm pitch grid.

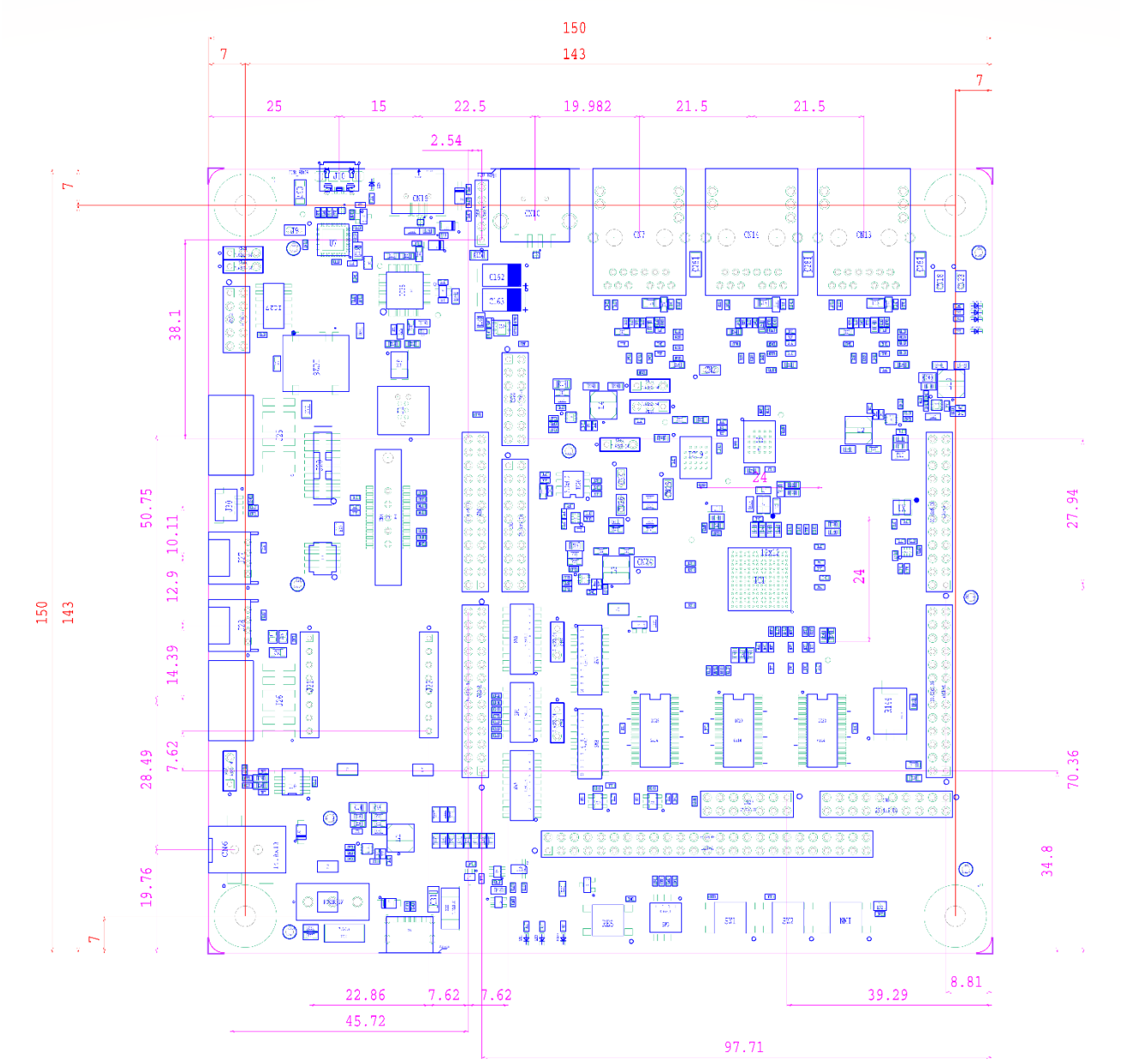


Figure 3-3 Board Dimensions (Unit: mm)

3.3 Arrangement of Components

For the arrangement of components on this board, refer to "11. Appendix".

4. Connections

4.1 Internal Connections of the Board

Figure 4-1 shows the connections between components of this board and the RZ/T2L.

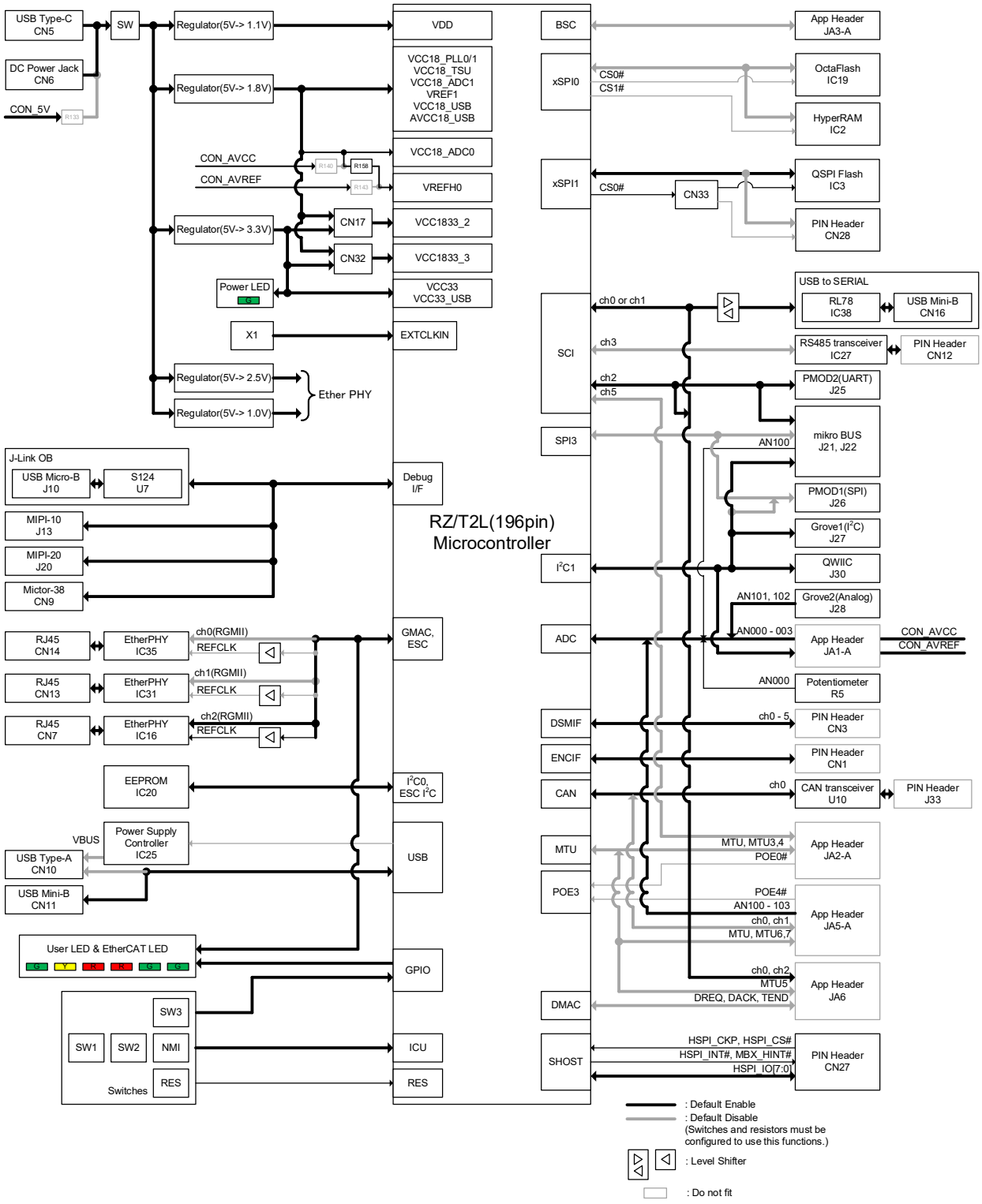


Figure 4-1 Internal Connections of the Board

4.2 Connections in the Debugging Environment

Figure 4-2 shows the connection between this board, the emulator, and the host PC. Figure 4-3 shows the connection between this board and the host PC when J-Link® OB on this board is used.

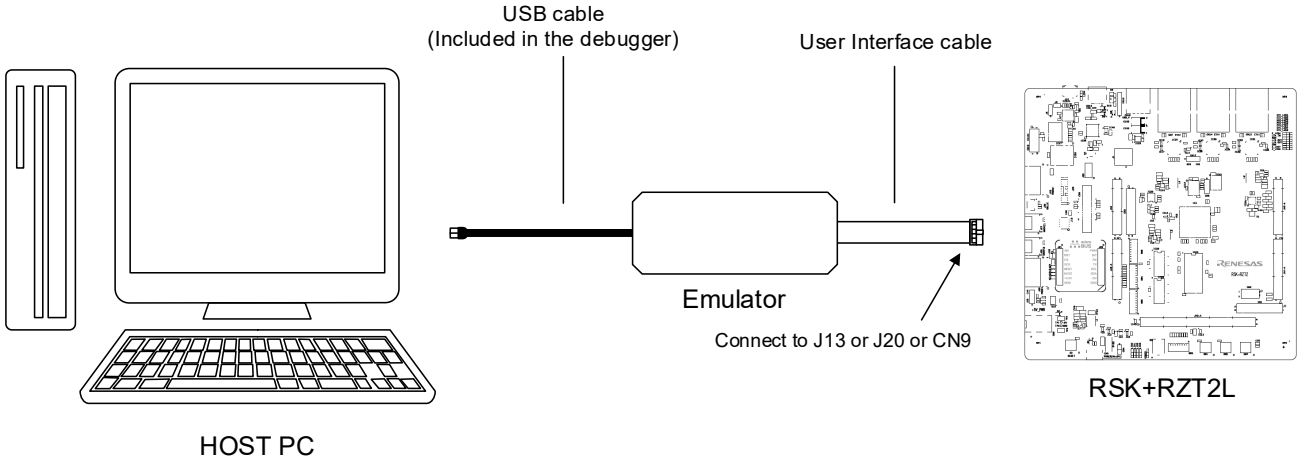


Figure 4-2 Connections in the Debugging Environment (with an Emulator)

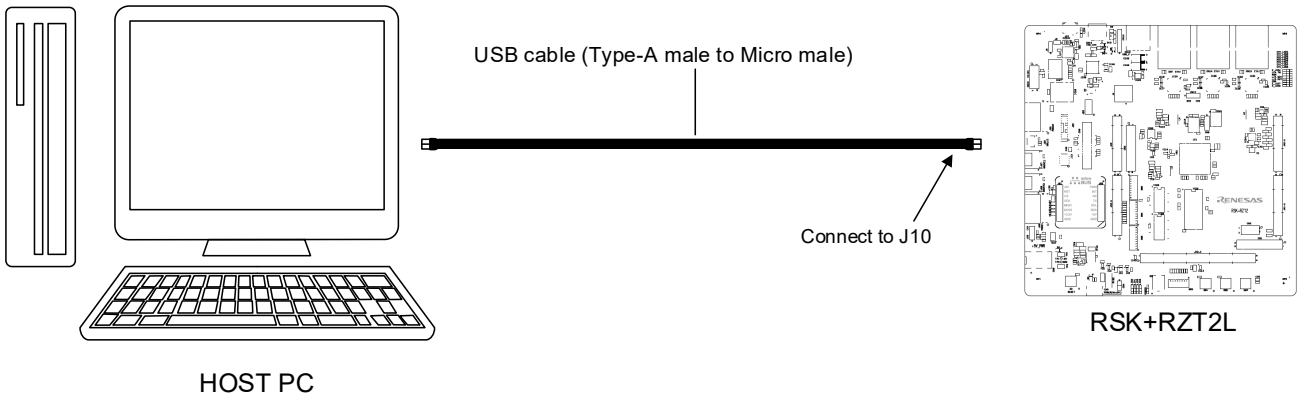


Figure 4-3 Connections in the Debugging Environment (with J-Link® OB)

5. List of RZ/T2L Pin Functions

Table 5-1 to Table 5-12 are lists of the functions of RZ/T2L pins used on this board. **Text in bold blue type** in the tables indicates the settings at the time of shipment of the board and the functions available with those settings.

Table 5-1 List of RZ/T2L Pin Function Selections (1)

Pin No.	Pin Name	Function	Description	Connector	Remarks
A1	VSS				
A2	P01_3/AH#/MTIOC4D/GTIOC3B/ETH2_TXD2/IRQ2/POUTZ	P01_3	GPIO for use with PMOD2	J25-9	CN17: 1-2, SW4-6: OFF
		AH#	ALE of JA3-A	JA3-A-46	CN17: 1-2, SW4-6: OFF, R330: DNF, R331: Fit
		ETH2_TXD2	**TXD2 of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**
A3	P00_3/RD/WR#/MTIC5W/SS2#/CTS2#/RTS2#/ETH2_REFCLK/RMII2_REFCLK/IRQ1/SI1#/HDSL1_CLK1	RTS2#	RTS for use with PMOD2	J25-4	CN17: 1-2, SW4-6: OFF
		RD/WR#	WR of JA3-A	JA3-A-26	CN17: 1-2, SW4-6: OFF
		ETH2_REFCLK	**XTAL1 of Ethernet port**	**—**	**CN17: 2-3, SW4-6: ON**
A4	P24_1/D13/CAS#/MTIOC0C/POE8#/GTETRGC/ETH2_RXCLK/MCLK5	MCLK5	MCLK5 of pin header CN3	CN3-3	CN17: 1-2, SW4-6: OFF
		ETH2_RXCLK	**RXCLK of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**
A5	P22_3/D10/MTIOC8D/GTETRGSB/RXD5/SCL5/MISO5/USB_VBUSEN/SPI_SSL00/ENCIFDI1	**GMAC_RESETOUT#**	**PHY reset of Ethernet port**	**—**	**SW8-1: ON, SW8-2: OFF, SW8-3: OFF**
		BSC_D10	D10 of JA3-A	JA3-A-31	SW8-2: ON, SW8-1: OFF **SW8-3: OFF**
		USB_VBUSEN	VBUS control for USB host interface	—	SW8-3: ON, SW8-1: OFF, **SW8-2: OFF**
A6	P22_2/TRACECLK/D9/MTIOC8C/GTETRGSA/SPI_SSL12/MCLK1/IRQ4/ENCIFDO1	TRACECLK	TRACE_CLK of debug interface	J20-12, CN9-6	SW8-10: ON
		D9	**D9 of JA3-A**	**JA3-A-30**	**SW8-10: OFF**
		MCLK1	**MCLK1 of pin header CN3**	**CN3-15**	**SW8-10: OFF**
A7	P21_6/TRACEDATA5/D5/TEND/MTIOC7B/GTIOC16B/CTS0#/ESC_LINKACT0/MDAT2/IRQ9/HSPI_IO4	**P21_6/ESC_LINKACT0**	**Control of LED4_ESC_IN**	**—**	**SW8-10: OFF, CN23: Short-circuit**
		TRACEDATA5	TRACEDATA5 of debug interface	CN9-20	SW8-10: ON
		D5	**D5 of JA3-A**	**JA3-A-22**	**SW8-10: OFF**
		HSPI_IO4	**IO4 of serial host interface**	**CN27-8**	**SW8-10: OFF**

A8	P21_1/TRACEDATA0/D0/MTIOC6A/GTIOC14A/CMTW0_TIC0/SCK5/IIC_SCL1/ESC_SYNC0/ESC_SYNC1/SPI_SSL20/MCLK0/HSPI_INT#	TRACEDATA0	TRACEDATA0 of debug interface	J20-14, CN9-38	SW8-10: ON
		D0	**D0 of JA3-A**	**JA3-A-17**	**SW8-10: OFF**
		MTIOC6A/GTIOC14A	**M2_Toggle of JA5-A**	**JA5-A-15**	**SW8-10: OFF**
		IIC_SCL1	**SCL of Grove1, QWIIC, or mikroBUS**	**J27-1, J30-4, J22-5**	**SW8-10: OFF**
			SCL for use with PMOD1	J26-3	**SW8-10: OFF,** E2: Short-circuit, E23: Open-circuit
		MCLK0	**MCLK0 of pin header CN3**	**CN3-17**	**SW8-10: OFF**
		HSPI_INT#	**INT# of serial host interface**	**CN27-2**	**SW8-10: OFF**
A9	P20_4/MDV3/GMAC_PTPOUT0/ESC_LINKACT1	**MDV3**	**Input of MDV3 setting**	**—**	
		P20_4/ESC_LINKACT1	**Control of LED5_ESC_OUT**	**—**	
A10	VSS				
A11	AN100	**AN100**	**AN for use with mikroBUS, ADC4 of JA5-A**	**J21-1, JA5-A-1**	
A12	AN002	**AN002**	**ADC2 of JA1-A**	**JA1-A-11**	

Table 5-2 List of RZ/T2L Pin Function Selections (2)

Pin No.	Pin Name	Function	Description	Connector	Remarks
A13	AN000	**AN000**	**Input of potentiometer**	**—**	**R238: Fit**
			ADC0 of JA1-A	JA1-A-9	R238: DNF
A14	VSS				
B1	P01_7/TRACEDATA1/A19/MTIOC1B/GTIOC9B/SCK1/ETH2_TXER/CANRX0/SPI_RSPCK3/ADTRG0#/ENCIFOE0	A19	A19 of JA3-A	JA3-A-40	SW5-4: ON, SW5-1: OFF, **SW5-2: OFF, SW5-3: OFF, SW5-5: OFF**
		SPI_RSPCK3	SCK for use with PMOD1	J26-4	SW5-2: ON, SW5-1: OFF, **SW5-3: OFF, SW5-4: OFF, SW5-5: OFF, E24: Short-circuit, E3: Open-circuit**
		CANRX0	**RX of CAN interface**	**—**	**SW5-1: ON, SW5-2: OFF, SW5-3: OFF, SW5-4: OFF, SW5-5: OFF**
			CAN1RX of JA5-A	JA5-A-6	SW5-5: ON, SW5-1: OFF, **SW5-2: OFF, SW5-3: OFF, SW5-4: OFF**
		SPI_RSPCK3	SCK for use with mikroBUS	J21-4	SW5-3: ON, SW5-1: OFF, **SW5-2: OFF, SW5-4: OFF, SW5-5: OFF**
B2	P01_5/WE0#/DQMLL/CS0#/MTIOC4A/GTIOC2A/ETH2_TXD0/SPI_RSPCK1/TST_OUT0/HDSL0_SMPL	WE0#/DQMLL	LWRn/DQML of JA3-A	JA3-A-48	CN17: 1-2, SW4-6: OFF
		ETH2_TXD0	**TXD0 of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**
B3	P01_2/CS2#/MTIOC4B/GTIOC2B/ETH2_TXD3/IRQ2/POUTB	P01_2	RESET for use with PMOD2	J25-8	CN17: 1-2, SW4-6: OFF
		ETH2_TXD3	**TXD3 of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**
B4	P00_1/A13/MTIC5U/RXD2/SCL2/MISO2/ETH2_RXDV/MCLK0/IRQ0	RXD2	SCIbRX of JA6	JA6-7	CN17: 1-2, SW4-6: OFF
		ETH2_RXDV	**RXDN of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**
B5	P23_7/D11/BS/MTIOC0A/GTETRGA/SCK1/ETH2_RXD0/MCLK4	P23_7	IO_6 of JA1-A	JA1-A-21	CN17: 1-2, SW4-6: OFF
		ETH2_RXD0	**RXD0 of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**

B6	P21_7/TRACEDATA6/D6/DREQ/MTIOC7C/GTIOC17A/DE0/MCLK3/IRQ10/HSPI_IO5	TRACEDATA6	TRACEDATA6 of debug interface	CN9-18	SW8-10: ON
		D6	**D6 of JA3-A**	**JA3-A-23**	**SW8-10: OFF**
		MCLK3	**MCLK3 of pin header CN3**	**CN3-7**	**SW8-10: OFF**
		HSPI_IO5	**HSPI_IO5 of serial host interface**	**CN27-7**	**SW8-10: OFF**
B7	P21_5/TRACEDATA4/D4/MTIOC7A/GTIOC16A/CMTW1_TOC1/CTS5#/SPI_MISO0/MCLK2/IRQ6/ADTRG1#/HSPI_IO3/ENCIFDI0	TRACEDATA4	TRACEDATA4 of debug interface	CN9-22	SW8-10: ON
		D4	**D4 of JA3-A**	**JA3-A-21**	**SW8-10: OFF**
		MCLK2	**MCLK2 of pin header CN3**	**CN3-13**	**SW8-10: OFF**
		HSPI_IO3	**HSPI_IO3 of serial host interface**	**CN27-9**	**SW8-10: OFF**

Table 5-3 List of RZ/T2L Pin Function Selections (3)

Pin No.	Pin Name	Function	Description	Connector	Remarks
B8	P21_2/TRACEDATA1/D1/MTIOC6B/GTIOC14B/GTIOC15A/CMTW0_TIC1/RXD5/SCL5/MISO5/IIC_SDA1/ESC_SYNC0/ESC_SYNC1/SPI_MISO2/MDAT0/HSPI_CS#	TRACEDATA1	TRACEDATA1 of debug interface	CN9-28	SW8-10: ON
				J20-16	SW8-10: ON, **R42: DNF, R43: Fit**
		D1	**D1 of JA3-A**	**JA3-A-18**	**SW8-10: OFF**
		IIC_SDA1	**SDA of Grove1, QWIIC, or mikroBUS**	**J27-2, J30-3, J22-6**	**SW8-10: OFF**
			SDA for use with PMOD1	J26-4	**SW8-10: OFF,** E3: Short-circuit, E24: Open-circuit
		MDAT0	**MDAT0 of pin header CN3**	**CN3-18**	**SW8-10: OFF**
		HSPI_CS#	**CS# of serial host interface**	**CN27-4**	**SW8-10: OFF**
B9	VSS				
B10	AN103	**AN103**	**ADC7 of JA5-A**	**JA5-A-4**	
B11	AN101	**AN101**	**AN101 of Grove2, ADC5 of JA5-A**	**J28-1, JA5-A-2**	
B12	AN001	**AN001**	**ADC1 of JA1-A**	**JA1-A-10**	
B13	VSS				
B14	P18_6/TRACECLK/A15/MTIC5W/SCK4/DE4/IIC_SCL2/GMAC_PTPOUT2/SPI_MISO2/XSPI1_IO7/IRQ11ADTRG0#/HSPI_CK/SI0#/HDSL0_CLK1	MTIC5W	M1_Win of JA6	JA6-16	SW8-9: OFF
		XSPI1_IO7	**IO7 of SPI expansion connector**	**CN28-5**	**SW8-9: ON**
		HSPI_CK	**CK of serial host interface**	**CN27-3**	
C1	P02_1/MDW/A17/DE1/GMAC_PTPOUT1/ESC_SYNC0/ESC_SYNC1/HDSL0_MISO1	**MDW**	**Input of MDW setting**	**—**	
		A17	**A17 of JA3-A**	**JA3-A-38**	
C2	P01_6/TRACEDATA0/A20/MTIOC1A/MTIOC3A/GTIOC0A/GTIOC9A/CTS1#/GMAC_PTPTRG1/ESC_LATCH1/ESC_LATCH0/ESC_PHYLINK0/CANTXDP1/SI0#/HDSL0_CLK1	**P01_6**	**Input of SW3-1**	**—**	
		MTIOC1A/ /GTIOC0A	**M1_EncZ of JA2-A**	**JA2-A-23**	**R195: Fit, R196: DNF**
		A20	A20 of JA3-A	JA3-A-41	R196: Fit, R195: DNF
C3	P01_1/CKE/MTIOC3D/GTIOC1B/GTETRGC/DE2/GMAC_MDC/ESC_MDC/ESC_PHYLINK2/MDAT1/POUTA	P01_1	IO_0 of JA1-A	JA1-A-15	CN17: 1-2, SW4-6: OFF
		GMAC_MDC	**MDC of Ethernet port**	**—**	**CN17: 2-3, SW4-6: ON**
C4	P00_2/RD#/MTIC5V/TXD2/SDA2/MOSI2/ETH2_TXEN/USB_OVRCUR/TST_OUT1/HDSL0_MOSI2	RD#	RDn of JA3-A	JA3-A-25	CN17: 1-2, SW4-6: OFF
		TXD2	SCIbTX of JA6	JA6-8	CN17: 1-2, SW4-6: OFF
		ETH2_TXEN	**TXEN of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**

C5	P24_2/D14/RAS#/MTIOC0D/GTETRGD/TXD1/SDA1/MOSI1/ETH2_RXD2/MDAT5	TXD1	TXD of USB-to-serial conversion	—	CN17: 1-2, SW4-6: OFF, CN34: 2-3
		MDAT5	MDAT5 of pin header CN3	CN3-4	CN17: 1-2, SW4-6: OFF
		ETH2_RXD2	**RXD2 of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**
C6	P22_0/TRACEDATA7/D7/MTIOC7D/GTIOC17B/DE5/MDAT3/IRQ15/HSPI_IO6	TRACEDATA7	TRACEDATA7 of debug interface	CN9-16	SW8-10: ON
		D7	**D7 of JA3-A**	**JA3-A-24**	**SW8-10: OFF**
		MDAT3	**MDAT3 of pin header CN3**	**CN3-8**	**SW8-10: OFF**
		HSPI_IO6	**IO6 of serial host interface**	**CN27-6**	**SW8-10: OFF**
C7	P21_3/TRACEDATA2/D2/MTIOC6C/GTIOC14B/GTIOC15A/TXD5/SDA5/MOSI5/ESC_LEDRUN/ESC_LEDSTER/SPI_SSL33/MCLK1 NMI/HSPI_IO2	TRACEDATA2	TRACEDATA2 of debug interface	J20-18, CN9-26	SW8-10: ON
		D2	**D2 of JA3-A**	**JA3-A-19**	**SW8-10: OFF**
		P21_3/ESC_LEDRUN	**Control of LED0_ESC_RUN**	**—**	**SW8-10: OFF, CN18: Short-circuit**
		HSPI_IO2	**IO2 of serial host interface**	**CN27-10**	**SW8-10: OFF**
C8	P20_3/MDV2/GMAC_PTPOUT1/ESC_LEDERR/CANTX1	**MDV2**	**Input of MDV2 setting**	**—**	
		P20_3/ESC_LEDERR	**Control of LED2_ESC_ERR**	**—**	

Table 5-4 List of RZ/T2L Pin Function Selections (4)

Pin No.	Pin Name	Function	Description	Connector	Remarks
C9	VSS				
C10	AN102	**AN102**	**AN102 of Grove2, ADC6 of JA5-A**	**J28-2, JA5-A-3**	
C11	AN003	**AN003**	**ADC3 of JA1-A**	**JA1-A-12**	
C12	AVCC18_TSU				
C13	P18_5/TRACECTL/RAS#/MTIC5V/RXD4/SCL4/MISO4/ETH2_COL/CANRX0/SPI_MOSI2/XSPI1_IO6/HSPI_IO0/TST_OUT0/HDSL0_SMPL	MTIC5V	M1_Vin of JA6	JA6-15	SW8-9: OFF
		XSPI1_IO6	**IO6 of SPI expansion connector**	**CN28-6**	**SW8-9: ON**
		HSPI_IO0	**IO0 of serial host interface**	**CN27-12**	
C14	P18_4/CAS#/MTIC5U/TXD4/SDA4/MOSI4/ETH2_RXER/CANTX0/SPI_RSPCK2/XSPI1_IO5/IRQ1/HSPI_IO1/DUEI0/HDSL0_LINK	MTIC5U	M1_Uin of JA6	JA6-14	SW8-9: OFF
		XSPI1_IO5	**IO5 of SPI expansion connector**	**CN28-7**	**SW8-9: ON**
		HSPI_IO1	**IO1 of serial host interface**	**CN27-11**	
D1	P02_3/A15/AH#/MTIOC2B/POE11#/GTIOC10B/SS1#/CTS1#/RTS1#/ETH2_COL/CANRX1/SPI_SSL30/IRQ15/ENCIFDO0	A15	A15 of JA3-A	JA3-A-16	SW6-7: ON, **SW6-5: OFF, SW6-6: OFF,** SW6-8: OFF
		CANRX1	**CAN2RX of JA5-A**	**JA5-A-8**	**SW6-8: ON, SW6-5: OFF, SW6-6: OFF, SW6-7: OFF**
		SPI_SSL30	SS for use with PMOD1, CS for use with mikroBUS	J26-1, J21-3	SW6-6: ON, **SW6-5: OFF, SW6-7: OFF,** SW6-8: OFF
		IRQ15	MDINT of EtherCAT port 1	—	SW6-5: ON, **SW6-6: OFF, SW6-7: OFF,** SW6-8: OFF

D2	P02_0/TRACEDATA2/A18/MTIOC3C/GTIOC0B/GTADSML0/RXD1/SCL1/MISO1/ETH2_CRS/USB_OTGID/CANTX1/SPI_MISO3/IRQ4/ENCIFCK0	A18	A18 of JA3-A	JA3-A-39	SW5-8: ON, **SW5-6: OFF, SW5-7: OFF,** SW5-9: OFF
		CANTX1	**CAN2TX of JA5-A**	**JA5-A-7**	**SW5-9: ON, SW5-6: OFF, SW5-7: OFF, SW5-8: OFF**
		SPI_MISO3	MISO for use with mikroBUS	J21-5	SW5-7: ON, **SW5-6: OFF, SW5-8: OFF,** SW5-9: OFF
			MISO for use with PMOD1	J26-3	SW5-7: ON, **SW5-6: OFF, SW5-8: OFF,** SW5-9: OFF, **E23: Short-circuit, E2: Open-circuit**
		IRQ4	MDINT of EtherCAT port 0	—	SW5-6: ON, **SW5-7: OFF, SW5-8: OFF,** SW5-9: OFF
D3	P01_0/CAS#/MTIOC3C/MTIOC4C/GTIOC0B/GTIOC3A/CTS2#/GMAC_MDIO/ESC_MDIO/MCLK1/IRQ13	CTS2#	CTS for use with PMOD2	J25-1	CN17: 1-2, SW4-6: OFF
		GMAC_MDIO	**MDIO of Ethernet port**	**—**	**CN17: 2-3, SW4-6: ON**
D4	P00_6/CS5#/MTIOC3A/MTIOC3B/GTIOC0A/GTIOC1A/ETH2_TXCLK/MDAT0	CS5#	CSa of JA3-A	JA3-A-27	CN17: 1-2, SW4-6: OFF
		ETH2_TXCLK	**TXCLK of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**
D5	P24_0/D12/CKE/DREQ/MTIOC0B/GTETRGB/RXD1/SCL1/MISO1/ETH2_RXD1/MDAT4	P24_0	IO_7 of JA1-A	JA1-A-22	CN17: 1-2, SW4-6: OFF
		RXD1	RXD of USB-to-serial conversion	—	CN17: 1-2, SW4-6: OFF, CN35: 2-3
		ETH2_RXD1	**RXD1 of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**

Table 5-5 List of RZ/T2L Pin Function Selections (5)

Pin No.	Pin Name	Function	Description	Connector	Remarks
D6	P22_1/TRACECTL/D8/POE4#/GTETRGB/SS4#/CTS4#/RTS4#/ESC_LINKACT2/SPI_MOSI0/IRQ13/HSPI_IO7	TRACECTL	TRACECTL of debug interface	CN9-36	SW8-10: ON
		D8	**D8 of JA3-A**	**JA3-A-29**	**SW8-10: OFF, SW8-4: ON, SW8-5: OFF**
		POE4#	**M2_POE of JA5-A**	**JA5-A-16**	**SW8-10: OFF, SW8-4: ON, SW8-5: OFF**
		HSPI_IO7	**IO7 of serial host interface**	**CN27-5**	**SW8-10: OFF, SW8-4: ON, SW8-5: OFF**
		IRQ13	MDINT of Ethernet port	—	**SW8-10: OFF**, SW8-5: ON, SW8-4: OFF
D7	P21_4/TRACEDATA3/D3/MTIOC6D/GTIOC15B/SS5#/CTS5#/RTS5#/GMAC_PTPOUT1/ESC_SYNC0/ESC_SYNC1/SPI_SSL02/MDAT1/MBX_HINT#/ENCIFDO0	TRACEDATA3	TRACEDATA3 of debug interface	J20-20, CN9-24	SW8-10: ON
		D3	**D3 of JA3-A**	**JA3-A-20**	**SW8-10: OFF**
		MDAT1	**MDAT1 of pin header CN3**	**CN3-16**	**SW8-10: OFF**
		MBX_HINT#	**HINT# of serial host interface**	**CN27-13**	**SW8-10: OFF**
D8	VCC33				
D9	VREFH1				
D10	VREFH0				
D11	VSS				
D12	P18_2/BS/MTIOC4B/MTIOC4D/GTIOC2B/GTIOC3B/SCK0/IIC_SDA2/GMAC_PTPOUT3/XSPI1_CS0#	MTIOC4B	M1_WP of JA2-A	JA2-A-17	SW8-9: OFF, R338: Fit, R337: DNF
		GTIOC2B	M1_VN of JA2-A	JA2-A-16	SW8-9: OFF, **R337: Fit, R338: DNF**
		XSPI1_CS0#	**CS# of QSPI**	**—**	**SW8-9: ON, CN33: 1-2**
			CS of SPI expansion connector	CN28-4	**SW8-9: ON,** CN33: 2-3

D13	P18_3/CKE/MTIOC4B/MTIOC4D/GTIOC2B/GTIOC3B/CMTW1_TIC1/DE3/ETH2_CRS/CANRXDP1/XSPI1_IO4/IRQ0	P18_3	RST for use with mikroBUS	J21-2	SW8-9: OFF, R89: Fit, R88: DNF, **R90: DNF**
		MTIOC4D/GTIOC3B	M1_WN of JA2-A	JA2-A-18	SW8-9: OFF
		DE3	DE of RS485	—	SW8-9: OFF, **R88: Fit,** **R89: DNF,** **R90: DNF**
			ENCIFOE1 of pin header CN1	CN1-3	SW8-9: OFF, R90: Fit, R88: DNF, **R89: DNF**
		XSPI1_IO4	**IO4 of SPI expansion connector**	**CN28-8**	**SW8-9: ON**
D14	P18_1/WE1#/DQMLU/MTIOC3D/GTIOC1B/SS3#/CTS3#/RTS3#/IRQ10/ADTRG1#	**P18_1**	**Control of LED3**	**—**	**SW7-10: ON,** **SW7-7: OFF,** **SW7-8: OFF,** **SW7-9: OFF**
		MTIOC3D/GTIOC1B	M1_UN of JA2-A	JA2-A-14	SW7-9: ON, **SW7-7: OFF,** **SW7-8: OFF,** SW7-10: OFF
		IRQ10	INT for use with PMOD1	J26-7	SW7-7: ON, **SW7-8: OFF,** **SW7-9: OFF,** SW7-10: OFF
		ADTRG1#	ADTRG of JA1-A	JA1-A-8	SW7-8: ON, **SW7-7: OFF,** **SW7-9: OFF,** SW7-10: OFF

Table 5-6 List of RZ/T2L Pin Function Selections (6)

Pin No.	Pin Name	Function	Description	Connector	Remarks
E1	P02_5/TDI/WE1#/DQMLU/SCK5/SPI_SSL31	**TDI**	**TDI of debug interface**	**J13-8, J20-8, CN9-19**	
E2	P02_2/A16/MTIOC2A/POE10#/GTIOC10A/RTCAT1HZ/TXD1/SDA1/MOSI1/CANTX0/SPI_MOSI3/IRQ14/ENCIFDI0	A16	A16 of JA3-A	JA3-A-37	SW6-3: ON, SW6-1: OFF, **SW6-2: OFF, SW6-4: OFF**
		CANTX0	**TX of CAN interface**	**—**	**SW6-1: ON, SW6-2: OFF, SW6-3: OFF, SW6-4: OFF**
			CAN1TX of JA5-A	JA5-A-5	SW6-4: ON, SW6-1: OFF, **SW6-2: OFF, SW6-3: OFF**
		SPI_MOSI3	MOSI for use with PMOD1, MOSI for use with mikroBUS	J26-2, J21-6	SW6-2: ON, SW6-1: OFF, **SW6-3: OFF, SW6-4: OFF**
E3	P02_4/TDO/WE0#/DQMLL/DE1/SPI_SSL33	**TDO**	**TDO of debug interface**	**J13-6, J20-6, CN9-11**	
E4	P01_4/WE1#/DQMLU/POE0#/ETH2_TXD1/IRQ3/DUEI0/HDSL0_LINK	P01_4	GPIO for use with PMOD2	J25-10	CN17: 1-2, SW4-6: OFF
		WE1#/DQMLU	HWRn/DQMH of JA3-A	JA3-A-47	CN17: 1-2, SW4-6: OFF
		ETH2_TXD1	**TXD1 of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**
E5	P00_0/D15/SCK2/DE2/ETH2_RXD3/DUEI1/HDSL0_SEL1	SCK2	SCIbCK of JA6	JA6-10	CN17: 1-2, SW4-6: OFF
		ETH2_RXD3	**RXD3 of Ethernet port in RGMII mode**	**—**	**CN17: 2-3, SW4-6: ON**
E6	VCC1833_2				
E7	VDD				
E8	VDD				
E9	VCC18_ADC1				
E10	VCC18_ADC0				
E11	VSS				
E12	P17_4/TRACECLK/DACK/MTIOC3C/GTIOC0A/GTETRGB/CTS3#/ETH2_TXER/ESC_PHYLINK2/SPI_SSL32/SPI_RSPCK0/XSPI1_IO3/HDSL1_CLK2	**XSPI1_IO3**	**IO3 of QSPI and SPI expansion connector**	**CN28-9**	**SW8-9: ON**
		HDSL1_CLK2	HDSL1_CLK2 of pin header CN1	CN1-16	SW8-9: OFF

E13	P17_7/RD#/DACK/MTIOC4A/MTIOC4C/GTIOC2A/GTIOC3A/RXD3/SCL3/MISO3/XSPI1_CKP	MTIOC4A/GTIOC2A	M1_VP of JA2-A	JA2-A-15	SW8-9: OFF, **R341: Fit,** **R339: Fit,** **R340: DNF**
		RXD3	RXD3 of pin header CN1	CN1-5	SW8-9: OFF, R340: Fit, R339: DNF, R341: DNF
			RXD of RS485	—	SW8-9: OFF, **R245: Fit**
		XSPI1_CKP	**CKP of QSPI and SPI expansion connector**	**CN28-3**	**SW8-9: ON**

Table 5-7 List of RZ/T2L Pin Function Selections (7)

Pin No.	Pin Name	Function	Description	Connector	Remarks
E14	P18_0/WE0#/DQMLL/MTIOC4A/MTIOC4C/GTIOC2A/GTIOC3A/TXD3/SDA3/MOSI3/XSPI1_IO0	MTIOC4C	M1_VN of JA2-A	JA2-A-16	SW8-9: OFF, R335: Fit, **R333: DNF,** R334: DNF, **R336: DNF**
		GTIOC3A	M1_WP of JA2-A	JA2-A-17	SW8-9: OFF, R336: Fit, **R333: DNF,** R334: DNF, **R335: DNF, R338: DNF**
		TXD3	TXD3 of pin header CN1	CN1-4	SW8-9: OFF, R333: Fit, R332: DNF, R334: DNF, **R335: DNF, R336: DNF**
			TXD of RS485	—	SW8-9: OFF, **R334: Fit, R333: DNF, R335: DNF, R336: DNF**
		XSPI1_IO0	**IO0 of QSPI and SPI expansion connector**	**CN28-12**	**SW8-9: ON**
F1	P04_1/CKIO/TXD3/SDA3/MOSI3/IIC_SDA2/SPI_MOSI0	**P04_1**	**Input of SW3-2**	**—**	**R197: Fit, R198: DNF**
		CKIO	SDCLK of JA3-A	JA3-A-44	R198: Fit, R197: DNF
F2	P02_7/TCK/TXD5/SDA5/MOSI	**TCK**	**TCK of debug interface**	**J13-4, J20-4, CN9-15**	
F3	P02_6/TMS/RXD5/SCL5/MISO5	**TMS**	**TMS of debug interface**	**J13-2, J20-2, CN9-17**	
F4	TRST#	**TRST#**	**TRST# of debug interface**	**—**	
F5	VCC33				
F6	VDD				
F7	VSS				
F8	VSS				
F9	VDD				
F10	VCC33				
F11	P17_0/MDD/SS0#/CTS0#/RTS0#/ESC_IRQ/SPI_SSL01/XSPI1_IO1/HDSL1_MISO2	**MDD**	**Input of MDD setting**	**—**	
		XSPI1_IO1	**IO1 of QSPI and SPI expansion connector**	**CN28-11**	**SW8-9: ON**

F12	P17_6/RD/WR#/MTIOC3B/GTIOC1A/SCK3/XSPI1_DS	**P17_6**	**Control of LED1**	**—**	**SW7-6: ON, SW7-4: OFF, SW7-5: OFF**
		MTIOC3B/GTIOC1A	PWM for use with mikroBUS	J22-1	SW7-4: ON, **SW7-5: OFF,** SW7-6: OFF
			M1_UP of JA2-A	JA2-A-13	SW7-5: ON, **SW7-4: OFF,** SW7-6: OFF
F13	P17_3/TRACECTL/DREQ/POE0#/GTETRGA/CANRX1/SPI_SSL31/XSPI1_IO2/ADTRG1#	POE0#/GTETRGA	M1_POE of JA2-A	JA2-A-24	SW8-9: OFF
		XSPI1_IO2	**IO2 of QSPI and SPI expansion connector**	**CN28-10**	**SW8-9: ON**
F14	P17_5/RSTOUT#/TEND/MTIOC3A/GTIOC0B/GTETRGC/USB_OVRCUR	**USB_OVRCUR**	**OVRCUR input for USB host interface**	**—**	
G1	P06_0/A12/GTIOC16A/CMTW1_TOC0/SS4#/CTS4#/RTS4#/ETH1_TXD3/CANRX1/SPI_SSL23/HDSL0_MOSI1	**P06_0**	**RESET for use with PMOD1**	**J26-8**	**SW8-8: OFF**
		A12	**A12 of JA3-A**	**JA3-A-13**	**SW8-8: OFF**
		ETH1_TXD3	TXD3 of EtherCAT port 1 in RMII mode	—	SW8-8: ON

Table 5-8 List of RZ/T2L Pin Function Selections (8)

Pin No.	Pin Name	Function	Description	Connector	Remarks
G2	P05_6/A13/GTIOC14A/CMTW1_TIC0/ETH1_RXER/SPI_SSL22/IRQ12/HDSL1_MOSI2	**P05_6**	**GPIO for use with PMOD1**	**J26-10**	**SW8-8: OFF**
		A13	**A13 of JA3-A**	**JA3-A-14**	**SW8-8: OFF**
		ETH1_RXER	RXER of EtherCAT port 1 in RMII mode	—	SW8-8: ON
G3	P05_5/A14/GTIOC14B/CMTW0_TOC1/ESC_PHYLINK1/SPI_RSPCK2/HDSL1_LINK	A14	A14 of JA3-A	JA3-A-15	SW7-2: ON, **SW7-1: OFF,** SW7-3: OFF
		ESC_PHYLINK1	LINK of EtherCAT port 1	—	SW7-1: ON, **SW7-2: OFF,** SW7-3: OFF
		HDSL1_LINK	**HDSL1_LINK of pin header CN1**	**CN1-10**	**SW7-3: ON, SW7-1: OFF, SW7-2: OFF**
G4	BSCANP	**BSCANP**	**GROUND connection**	**—**	
G5	VDD				
G6	VSS				
G7	VSS				
G8	VSS				
G9	VSS				
G10	VDD				
G11	P16_1/CS2#/CMTW0_TOC1/RXD0/SCL0/MISO0/SPI_MISO3/XSPI0_RESET0#/MDAT3/ADTRG0#/ENCIFOE0/HDSL1_SEL1	**P16_1**	**IO_5 of JA1-A**	**JA1-A-20**	**CN32: 1-2, SW4-7: OFF**
		RXD0	**RXD of USB-to-serial conversion**	**—**	**CN32: 1-2, SW4-7: OFF, CN35: 1-2**
		XSPI0_RESET0#	RESET# to OctaFlash	—	CN32: 2-3, SW4-7: ON
G12	P16_0/TXD0/SDA0/MOSI0/ETH2_REFCLK/SPI_MOSI3/XSPI0_CS1#/MCLK3/ENCIFCK0/HDSL0_MOSI2	**P16_0**	**IO_4 of JA1-A**	**JA1-A-19**	**CN32: 1-2, SW4-7: OFF**
		TXD0	**TXD of USB-to-serial conversion**	**—**	**CN32: 1-2, SW4-7: OFF, CN34: 1-2**
		XSPI0_CS1#	CS# to HyperRAM	—	CN32: 2-3, SW4-7: ON
G13	P16_2/CTS0#/USB_EXICEN/SPI_RSPCK3/SPI_SSL03/XSPI0_RESET1#/NMI/ENCIFCK1/HDSL1_MISO1	**NMI**	**NMI SW and NMI of JA2-A**	**JA2-A-3**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_RESET1#	RESET# to HyperRAM	—	CN32: 2-3, SW4-7: ON
G14	P16_3/CS3#/GTADSMP1/SCK0/ETH2_RXER/SPI_SSL30/XSPI0_RSTO0#/IRQ7/ENCIFOE1/HDSL1_MOSI1	**IRQ7**	**SW2 and IRQb of JA2-A**	**JA2-A-9**	

H1	P06_4/A7/GTIOC11A/ETH1_TXCLK/SPI_MOSI1/HDSL0_SEL2	**A7**	**A7 of JA3-A**	**JA3-A-8**	**SW8-8: OFF**
		ETH1_TXCLK	TXCLK of EtherCAT port 1 in RMII mode	—	SW8-8: ON
H2	P06_2/MD1/A9/ETH1_TXD1/CANRXDP1	**MD1**	**Input of MD1 setting**	**—**	
		A9	**A9 of JA3-A**	**JA3-A-10**	**SW8-8: OFF**
		ETH1_TXD1	TXD1 of EtherCAT port 1 in RMII mode	—	SW8-8: ON
H3	P06_1/A10/GTIOC16B/CTS4#/ETH1_REFCLK/RMII1_REFCLK/CANTX1/SPI_SSL22/HDSL0_CLK2	**A10**	**A10 of JA3-A**	**JA3-A-10**	**SW8-8: OFF**
		ETH1_REFCLK	REFCLK of EtherCAT port 1	—	SW8-8: ON
H4	P05_7/MD2/A11/CMTW1_TOC1/ETH1_TXD2/SPI_SSL23	**MD2**	**Input of MD2 setting**	**—**	
		P05_7	**GPIO for use with PMOD1**	**J26-9**	**SW8-8: OFF**
		A11	**A11 of JA3-A**	**JA3-A-12**	**SW8-8: OFF**
		ETH1_TXD2	TXD2 of EtherCAT port 1 in RMII mode	—	SW8-8: ON
H5	VDD				
H6	VSS				
H7	VSS				
H8	VSS				
H9	VSS				
H10	VDD				
H11	P15_6/D14/SPI_SSL12/XSPI0_IO7/MDAT2	**D14**	**D14 of JA3-A**	**JA3-A-35**	**CN32: 1-2, SW4-7: OFF**
		MDAT2	**MDAT2 of pin header CN3**	**CN3-14**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_IO7	IO7 of OctaFlash or HyperRAM	—	CN32: 2-3, SW4-7: ON

Table 5-9 List of RZ/T2L Pin Function Selections (9)

Pin No.	Pin Name	Function	Description	Connector	Remarks
H12	P15_5/D13/XSPI0_IO6/MCLK2 IRQ7	**D13**	**D13 of JA3-A**	**JA3-A-34**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_IO6	IO6 of OctaFlash or HyperRAM	—	CN32: 2-3, SW4-7: ON
H13	P15_4/D12/MTIOC8D/XSPI0_IO5/MDAT1/IRQ3	**D12**	**D12 of JA3-A**	**JA3-A-33**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_IO5	IO5 of OctaFlash or HyperRAM	—	CN32: 2-3, SW4-7: ON
H14	P15_7/TEND/CTS5#/SPI_SSL13/XSPI0_CS0#	**TEND**	**TEND of JA6**	**JA6-3**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_CS0#	CS# of OctaFlash	—	CN32: 2-3, SW4-7: ON
J1	P06_7/A4/GTIOC12B/ETH1_RXD1/SPI_SSL11/DUEI1/HDSL1_LINK	**A4**	**A4 of JA3-A**	**JA3-A-5**	**SW8-8: OFF**
		DUEI1	**DUEI1 of pin header CN1**	**CN1-6**	**SW8-8: OFF**
		ETH1_RXD1	RXD1 of EtherCAT port 1 in RMII mode	—	SW8-8: ON
J2	P06_5/A6/GTIOC11B/ETH1_TXEN/SPI_MISO1/HDSL0_MISO2	**A6**	**A6 of JA3-A**	**JA3-A-7**	**SW8-8: OFF**
		ETH1_TXEN	TXEN of EtherCAT port 1 in RMII mode	—	SW8-8: ON
J3	P06_6/A5/GTIOC12A/ETH1_RXD0/SPI_SSL10/HDSL1_SMPL	**A5**	**A5 of JA3-A**	**JA3-A-6**	**SW8-8: OFF**
		HDSL1_SMPL	**HDSL1_SMPL of pin header CN1**	**CN1-11**	**SW8-8: OFF**
		ETH1_RXD0	RXD0 of EtherCAT port 1 in RMII mode	—	SW8-8: ON
J4	P06_3/MD0/A8/DE4/ETH1_TXD0/CANTXDP1	**MD0**	**Input of MD0 setting**	**—**	
		A8	**A8 of JA3-A**	**JA3-A-9**	**SW8-8: OFF**
		ETH1_TXD0	TXD0 of EtherCAT port 1 in RMII mode	—	SW8-8: ON
J5	VCC33				
J6	VDD				
J7	VSS				
J8	VSS				
J9	VDD				
J10	VCC1833_3				
J11	P15_3/D11/MTIOC8C/XSPI0_IO4/MCLK1/NMI	**D11**	**D11 of JA3-A**	**JA3-A-32**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_IO4	IO4 of OctaFlash or HyperRAM	—	CN32: 2-3, SW4-7: ON

J12	P15_0/A23/CKE/RXD5/SCL5/MISO5/SPI_MOSI1/XSPI0_IO1	**CKE**	**ALE/SDCKE of JA3-A**	**JA3-A-46**	**CN32: 1-2, SW4-7: OFF, R330: Fit, R331: DNF**
		RXD5	**SCIaRX of JA2-A**	**JA2-A-8**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_IO1	IO1 of OctaFlash or HyperRAM	—	CN32: 2-3, SW4-7: ON
J13	P15_1/A24/CAS#/MTIOC0C/TXD5/SDA5/MOSI5/SPI_SSL10/XSPI0_IO2	**CAS#**	**CAS of JA3-A**	**JA3-A-49**	**CN32: 1-2, SW4-7: OFF**
		TXD5	**SCIaTX of JA2-A**	**JA2-A-6**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_IO2	IO2 of OctaFlash or HyperRAM	—	CN32: 2-3, SW4-7: ON
J14	P15_2/A25/RAS#/MTIOC0D/SS5#/CTS5#/RTS5#/SPI_SSL11/XSPI0_IO3	**RAS#**	**RAS of JA3-A**	**JA3-A-49**	**CN32: 1-2, SW4-7: OFF**
		CTS5#/RTS5#	**CTSa/RTSa of JA2-A**	**JA2-A-12**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_IO3	IO3 of OctaFlash or HyperRAM	—	CN32: 2-3, SW4-7: ON
K1	P07_0/A3/GTIOC13A/ETH1_RXD2/TST_OUT1/HDSL1_SMPL	**A3**	**A3 of JA3-A**	**JA3-A-4**	**SW8-8: OFF**
		TST_OUT1	**TST_OUT1 of pin header CN1**	**CN1-9**	**SW8-8: OFF**
		ETH1_RXD2	RXD2 of EtherCAT port 1 in RMII mode	—	SW8-8: ON
K2	P07_2/A1/GTIOC17A/ETH1_RXDV/HDSL1_SEL1	**A1**	**A3 of JA3-A**	**JA3-A-4**	**SW8-8: OFF**
		HDSL1_SEL1	**HDSL1_SEL1 of pin header CN1**	**CN1-12**	**SW8-8: OFF**
		ETH1_RXDV	RXDV of EtherCAT port 1 in RMII mode	—	SW8-8: ON
K3	P07_3/A0/GTIOC17B/ETH1_RXCLK/SPI_SSL00/HDSL1_MISO1	**A0**	**A0 of JA3-A**	**JA3-A-1**	**SW8-8: OFF**
		HDSL1_MISO1	**HDSL1_MISO1 of pin header CN1**	**CN1-13**	**SW8-8: OFF**
		ETH1_RXCLK	RXCLK of EtherCAT port 1 in RMII mode	—	SW8-8: ON

Table 5-10 List of RZ/T2L Pin Function Selections (10)

Pin No.	Pin Name	Function	Description	Connector	Remarks
K4	P07_1/A2/TIOC13B/ETH1_RXD3/SI1#/HDSL1_CLK1	**A2**	**A2 of JA3-A**	**JA3-A-3**	**SW8-8: OFF**
		SI1#/HDSL1_CLK1	**SI1#/HDSL1_CLK1 of pin header CN1**	**CN1-8**	**SW8-8: OFF**
		ETH1_RXD3	RXD3 of EtherCAT port 1 in RMII mode	—	SW8-8: ON
K5	P09_0/CS0#/MTIOC4A/MTIOC7A/GTIOC6A/RXD3/SCL3/MISO3/GMAC_MDIO/ESC_MDIO	**MTIOC7A/GTIOC6A**	**M2_VP of JA5-A**	**JA5-A-21**	**SW8-7: OFF**
		ESC_MDIO	MDIO of EtherCAT port 0 or port 1	—	SW8-7: ON
K6	VDD				
K7	VDD				
K8	VDD				
K9	VCC33				
K10	VCC1833_3				
K11	P14_2/MTIOC8B/GTIOC8B/ETH2_CRS/SPI_SSL10/XSPI0_ECS0#/IRQ6/POUTA/HDSL0_CLK2	**P14_2/IRQ6**	**SW1 input and IRQd/IRQAEC/M2_HSIN0 of JA1-A**	**JA1-A-23**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_ECS0#	ECS# of OctaFlash	—	CN32: 2-3, SW4-7: ON
K12	P14_7/A22/BS/SCK5/SPI_MISO1/XSPI0_IO0	**A22**	**A22 of JA3-A**	**JA3-A-43**	**CN32: 1-2, SW4-7: OFF**
		SCK5	**SCIaCK of JA2-A**	**JA2-A-10**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_IO0	IO0 of OctaFlash or HyperRAM	—	CN32: 2-3, SW4-7: ON
K13	P14_4/BS/MTIOC0B/ESC_IRQ/SPI_SSL13/XSPI0_DS/POUTZ/HDSL0_MISO2	**P14_4**	**IO_3 of JA1-A**	**JA1-A-18**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_DS	DS of OctaFlash or HyperRAM	—	CN32: 2-3, SW4-7: ON
K14	P14_6/A21/XSPI0_CKP	**A21**	**A21 of JA3-A**	**JA3-A-42**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_CKP	CKP of OctaFlash or HyperRAM	—	CN32: 2-3, SW4-7: ON
L1	VSS				
L2	P08_5/MTIOC3C/MTIOC6B/GTIOC5A/RXD2/SCL2/MISO2/ETH0_RXDV/MCLK2 IRQ5	**MTIOC6B/GTIOC5A**	**M2_UP of JA5-A**	**JA5-A-19**	**SW8-7: OFF**
		RXD2	**RXD for use with PMOD2 or mikroBUS**	**J25-3, J22-3**	**SW8-7: OFF**
		ETH0_RXDV	RXDV of EtherCAT port 0 in RMII mode	—	SW8-7: ON
L3	P08_4/CS5#/MTIOC3A/MTIOC6A/GTIOC4A/SCK2/ETH0_RXD3/CANTXDP1/SPI_SSL32/IRQ14/HDSL1_MOSI1	**MTIOC3A/GTIOC4A**	**M1_Toggle of JA6**	**JA6-13**	**SW8-7: OFF**
		HDSL1_MOSI1	**HDSL1_MOSI1 of pin header CN1**	**CN1-6**	**SW8-7: OFF**
		ETH0_RXD3	RXD3 of EtherCAT port 0 in RMII mode	—	SW8-7: ON

L4	P09_4/GTADSMP0/TXD4/SDA4/MOSI4/ETH0_TXD2/SPI_SSL21/HDSL1_MISO2	**HDSL1_MISO2**	**HDSL1_MISO2 of pin header CN1**	**CN1-18**	**SW8-7: OFF**
		ETH0_TXD2	TXD2 of EtherCAT port 0 in RMII mode	—	SW8-7: ON
L5	P10_1/POE10#/CTS3#/ETH0_RXD0/SPI_RSPCK1/IRQ10/ENCIFDI1	**ENCIFDI1**	**ENCIFDI1 of pin header CN1**	**CN1-5**	**SW8-7: OFF, R339: Fit, R340: DNF**
		ETH0_RXD0	RXD0 of EtherCAT port 0 in RMII mode	—	SW8-7: ON
L6	VCC33				
L7	P07_4/USB_VBUSIN/IRQ1/ADTRG0#/HDSL1_SEL2	**USB_VBUSIN**	**VBUSIN of USB function interface**	**CN11-1**	**R199: Fit, R200: DNF**
		IRQ1	IRQa/WKUP/M1_HSIN0 of JA2-A	JA2-A-7	R200: Fit, R199: DNF
L8	VDD				
L9	P13_2/TRACEDATA6/D9/MTIOC0A/GTIOC10A/POE8#/SS1#/CTS1#/RTS1#/IIC_SCL0/GMAC_PTPOUT2/ESC_I2CCLK/SPI_MISO0/MCLK4/IRQ5	**ESC_I2CCLK**	**SCL of EEPROM and JA1-A**	**JA1-A-26**	**R324: Fit, R325: DNF**
L10	P13_3/TRACEDATA7/D8/RD#/MTIOC0B/MTIOC0C/GTIOC10B/CMTW1_TOC0/CTS1#/IIC_SDA0/GMAC_PTPOUT3/ESC_I2CDATA/SPI_RSPCK0/MDAT4	**ESC_I2CDATA**	**SDA of EEPROM and JA1-A**	**JA1-A-25**	**R326: Fit, R327: DNF**
		MDAT4	MDAT4 of pin header CN3	CN3-6	R327: Fit, R326: DNF

Table 5-11 List of RZ/T2L Pin Function Selections (11)

Pin No.	Pin Name	Function	Description	Connector	Remarks
L11	P13_7/MTCLKC/GMAC_PTPTRG1/ESC_LATCH0/ESC_LATCH1/SPI_MOSI1/XSPI0_ECS1#/MBX_HINT#/HDSL0_SEL1	**MTCLKC**	**M2_TRCCLK of JA5-A**	**JA5-A-17**	
L12	P13_5/MTCLKA/IIC_SCL2/GMAC_PTPTRG0/ESC_LATCH0/ESC_LATCH1/SPI_RSPCK1/XSPI0_WP1#	**MTCLKA**	**M1_TRCCLK of JA2-A**	**JA2-A-25**	
L13	P14_3/MTIOC0A/ETH2_COL/SPI_SSL11/XSPI0_RSTO1#/POUTB/HDSL0_SEL2	**P14_3**	**SW3-4 input and IO_2 of JA1-A**	**JA1-A-17**	
L14	P14_5/CS3#/POE8#/XSPI0_CKN/IRQ15/HSPI_INT#	**CS3#**	**CSb of JA3-A**	**JA3-A-28**	**CN32: 1-2, SW4-7: OFF**
		XSPI0_CKN	CK# of HyperRAM	—	CN32: 2-3, SW4-7: ON
M1	P08_7/WAIT#/MTIOC3D/MTIOC6D/GTIOC5B/TXD2/SDA2/MOSI2/GMAC_MDC/ESC_MDC/SPI_SSL13/MDAT2/IRQ8	**MTIOC6D/GTIOC5B**	**M2_UN of JA5-A**	**JA5-A-20**	**SW8-7: OFF**
		TXD2	**TXD for use with PMOD2 or mikroBUS**	**J25-2, J22-4**	**SW8-7: OFF**
		ESC_MDC	MDC of EtherCAT port 0 or port 1	—	SW8-7: ON
M2	P08_6/MTIOC3B/MTIOC6C/GTIOC4B/CMTW1_TIC1/SCK3/ETH0_RXCLK/IRQ9	**IRQ9**	**INT for use with PMOD2, mikroBUS, and SPI expansion connector**	**J25-7, J22-2, CN28-13**	**SW8-7: OFF**
		ETH0_RXCLK	RXCLK of EtherCAT port 0 in RMII mode	—	SW8-7: ON
M3	P09_1/MTIOC4C/MTIOC7B/GTIOC7A/GTETRGSA/DE3/ETH0_REFCLK/RMII0_REFCLK/GMAC_PTPOUT0/ESC_SYNC0/ESC_SYNC1/SPI_SSL10	**MTIOC7B/GTIOC7A**	**M2_WP of JA5-A**	**JA5-A-23**	**SW8-7: OFF**
		ETH0_REFCLK	REFCLK of EtherCAT port 0	—	SW8-7: ON
M4	P09_7/DACK/GTIOC15B/RXD4/SCL4/MISO4/ETH0_TXCLK/USB_OVRCUR/CANTXDP0/SPI_SSL00/IRQ12/ENCIFOE1	**DACK**	**DACK of JA6**	**JA6-2**	**SW8-7: OFF**
		IRQ12	IRQ12 of SPI expansion connector	CN28-2	**SW8-7: OFF,** R202: Fit, R201: DNF
		ENCIFOE1	**ENCIFOE1 of pin header CN1**	**CN1-3**	**SW8-7: OFF, R201: Fit, R202: DNF, R90: DNF**
		ETH0_TXCLK	TXCLK of EtherCAT port 0 in RMII mode	—	SW8-7: ON
M5	P10_2/MTIC5U/TXD0/SDA0/MOSI0/ETH0_RXD1	**TXD0**	**SCIcTX of JA6**	**JA6-9**	**SW8-7: OFF**
		ETH0_RXD1	RXD1 of EtherCAT port 0 in RMII mode	—	SW8-7: ON

M6	VSS				
M7	MDX	**MDX**	**Input of MDX setting**	**—**	
M8	VCC18_PLL1				
M9	VSS				
M10	VCC33_USB				
M11	VSS_USB				
M12	P13_4/A0/WAIT#/MTIOC0D/GTIOC8B/ESC_RESETOUT#/SPI_SSL12	WAIT#	CSc/Wait of JA3-A	JA3-A-45	R329: Fit, R328: DNF
		ESC_RESETOUT#	**RESET# of EtherCAT port 0 or port 1**	**—**	**R328: Fit, R329: DNF**
M13	P13_6/MTCLKB/GMAC_PTPOUT0/ESC_SYNC0/ESC_SYNC1/XSPI0_WP0#	**MTCLKB**	**M1_TRDCLK of JA2-A**	**JA2-A-26**	
M14	P14_1/MTIOC8A/GTIOC8A/GMAC_PTPTRG1/ESC_LATCH0/ESC_LATCH1/SPI_MISO1/XSPI0_INT1#/HDSL0_MOSI1	**P14_1**	**IO_1 input of SW3-3 and JA1-A**	**JA1-A-16**	
N1	P09_2/RAS#/DACK/MTIOC4B/MTIOC7C/GTIOC6B/RTCAT1HZ/ETH0_RXER/IRQ0/HDSL1_CLK2	**MTIOC7C/GTIOC6B**	**M2_VN of JA5-A**	**JA5-A-22**	**SW8-7: OFF**
		ETH0_RXER	RXER of EtherCAT port 0 in RMII mode	—	SW8-7: ON
N2	P09_3/CS3#/MTIOC4D/MTIOC7D/GTIOC7B/GTETRGSB/CMTW0_TOC0/SS5#/CTS5#/RTS5#/ETH0_TXD3/USB_VBUSEN/CANTXDP0/MCLK3/IRQ12/HDSL1_SEL2	**MTIOC7D/GTIOC7B**	**M2_Wn of JA5-A**	**JA5-A-24**	**SW8-7: OFF**
		HDSL1_SEL2	**HDSL1_SEL2 of pin header CN1**	**CN1-17**	**SW8-7: OFF**
		ETH0_TXD3	TXD3 of EtherCAT port 0 in RMII mode	—	SW8-7: ON

Table 5-12 List of RZ/T2L Pin Function Selections (12)

Pin No.	Pin Name	Function	Description	Connector	Remarks
N3	P09_5/DREQ/GTADSML1/CMTW0_TOC0/DE5/IIC_SCL1/ETH0_TXD1/USB_VBUSEN/CANRX0/IRQ14/HDSL1_MOSI2	**DREQ**	**DREQ of JA6**	**JA6-1**	**SW8-7: OFF**
		HDSL1_MOSI2	**HDSL1_MOSI2 of pin header CN1**	**CN1-19**	**SW8-7: OFF**
		ETH0_TXD1	TXD1 of EtherCAT port 0 in RMII mode	—	SW8-7: ON
N4	P10_0/POE11#/CMTW0_TIC0/SCK4/IIC_SDA1/ETH0_TXEN/USB_EXICEN/CANTX0/IRQ15/ENCIFDO1	**ENCIFDO1**	**ENCIFDO1 of pin header CN1**	**CN1-4**	**SW8-7: OFF, R332: Fit, R333: DNF**
		ETH0_TXEN	TXEN of EtherCAT port 0 in RMII mode	—	SW8-7: ON
N5	RES#	**RES#**	**Input of reset**	**—**	
N6	EXTCLKIN	**EXTCLKIN**	**Connection of crystal oscillator**	**—**	**R252: Fit, E46: Open-circuit**
			Input of external clock	JA2-A-2	R252: DNF, E46: Short-circuit
N7	VSS				
N8	VCC18_PLL0				
N9	VSS_USB				
N10	VSS_USB				
N11	AVCC18_USB				
N12	VSS_USB				
N13	VSS_USB				
N14	P14_0/MTCLKD/GMAC_PTPOUT1/ESC_SYNC0/ESC_SYNC1/XSPI0_INT0#/HDSL0_MISO1	**MTCLKD**	**M2_TRDCLK of JA5-A**	**JA5-A-18**	
P1	VSS				
P2	P09_6/GTIOC15A/CMTW0_TIC1/CTS5#/ETH0_TXD0/USB_EXICEN/CANRXDP0/MDAT3/IRQ13/ENCIFCK1	**ENCIFCK1**	**ENCIFCK1 of pin header CN1**	**CN1-2**	**SW8-7: OFF**
		ETH0_TXD0	TXD0 of EtherCAT port 0 in RMII mode	—	SW8-7: ON
P3	P10_3/MTIC5V/RTCAT1HZ/RXD0/SCL0/MISO0/ETH0_RXD2/IRQ8	**IRQ8**	**IRQe/M2_EncZ/M2HSIN1 of JA5-A**	**JA5-A-9**	**SW8-7: OFF**
		RXD0	**SCIcRX of JA6**	**JA6-12**	**SW8-7: OFF**
		ETH0_RXD2	RXD2 of EtherCAT port 0 in RMII mode	—	SW8-7: ON
P4	P10_4/D15/MTIC5W/SCK0/ESC_PHYLINK0/SPI_SSL01/MBX_HINT#/IRQ11	D15	D15 of JA3-A	JA3-A-36	R322: Fit, R321: DNF, **R323: DNF**
		SCK0	SCIcCK of JA6	JA6-11	R323: Fit, R321: DNF, **R322: DNF**
		ESC_PHYLINK0	**PHYLINK of EtherCAT port 0**	**—**	**R321: Fit, R322: DNF, R323: DNF**

P5	VSS				
P6	EXTAL	EXTAL	Connection of crystal resonator	—	
P7	XTAL	XTAL			
P8	VSS				
P9	USB_DM	**USB_DM**	**Input/output of USB DM**	**CN10-2, CN11-2**	
P10	USB_DP	**USB_DP**	**Input/output of USB DP**	**CN10-3, CN11-3**	
P11	VCC18_USB				
P12	USB_RREF	**USB_RREF**	**Input of USB reference**	**—**	
P13	VSS_USB				
P14	VSS				

6. Circuitry for Configuration

6.1 Types of Configuration Circuits

Since multiple functions are assigned to single pins and each function has to be selected for use in the RZ/T2L, the functions to be used should be selected through the following methods on this board.

(1) Switches

DIP switches SW4 to SW8 are mounted for selecting functions.

(2) Jumper blocks

CN2, CN4, CN17, CN18, CN21 to CN26, CN32 to CN35, and J9 are mounted for selecting functions.

(3) Option links

The option links are as follows:

— Solder bridges and trace cuts

A solder bridge consists of two pads, which are insulated from each other at the time of shipment. Conduction can be set up for such pads by connecting them with solder or the like. A trace cut is a thin copper trace that connects two pads and sets up conduction between them. Such pads can be insulated from each other by cutting the trace between the pads.

Figure 6-1 Solder Bridge and Trace Cut

— 0-Ω resistor

A different function to be used can be selected by switching the factory state of a 0-Ω resistor between mounted and unmounted.

The subsequent sections describe which peripheral functions of the multi-functional RZ/T2L signals are enabled or disabled through the settings of switches, jumpers, and option links. The connection information for ICs and headers other than the RZ/T2L will also be shown. **Text in bold blue type** in the tables indicates the initial state of the configuration on the board as shipped. For the positions of switches, jumpers, and option links, refer to "3.3 Arrangement of Components".

When removing soldered components, do not apply a soldering iron to the board for more than 5 seconds. This time restriction is to avoid any damage to components mounted nearby on the board.

When modifying an option link, always check the related option links to ensure that no signal contention or short circuit has occurred. Most of the RZ/T2L pins have multiplexed functions and some of the peripheral functions must be used exclusively of each other. Refer to the RZ/T2L Group User's Manual: Hardware and CPU board schematics for further information.

6.2 Configuration by Switches

This board is equipped with DIP switches SW4 to SW8 for selecting functions. The functions set by individual switches are explained below.

6.2.1 Mode Setting Switch SW4

SW4 is used to set the mode pins of the RZ/T2L. Table 6-1 lists the settings of SW4.

Table 6-1 Functions of Mode Setting Switch SW4

<table>
<tr><th>No.</th><th colspan="2">Setting</th><th>Function</th></tr>
<tr><td rowspan="2">SW4-1
MD0</td><td>OFF</td><td>MD0 = H</td><td rowspan="9">The operating mode of the RZ/T2L is selected with the combination of MD2, MD1, and MD0.
<table><tr><th>MD[2:0]</th><th>Operating Mode</th></tr><tr><td>0 (L, L, L)</td><td>xSPI0 boot mode (x1 boot serial flash)</td></tr><tr><td>1 (L, L, H)</td><td>xSPI0 boot mode (x8 boot serial flash) *3</td></tr><tr><td>2 (L, H, L)</td><td>16-bit bus boot mode (NOR flash)*1</td></tr><tr><td>3 (L, H, H)</td><td>Serial host interface boot mode</td></tr><tr><td>4 (H, L, L)</td><td>xSPI1 boot mode (x1 boot serial flash)</td></tr><tr><td>5 (H, L, H)</td><td>SCI (UART) boot mode</td></tr><tr><td>6 (H, H, L)</td><td>USB boot mode</td></tr><tr><td>7 (H, H, H)</td><td>Reserved (setting prohibited)</td></tr></table></td></tr>
<tr><td>ON</td><td>MD0 = L</td></tr>
<tr><td rowspan="2">SW4-2
MD1</td><td>OFF</td><td>MD1 = H</td></tr>
<tr><td>ON</td><td>MD1 = L</td></tr>
<tr><td rowspan="2">SW4-3
MD2</td><td>OFF</td><td>MD2 = H</td></tr>
<tr><td>ON</td><td>MD2 = L</td></tr>
<tr><td rowspan="2">SW4-4
MDW</td><td>OFF</td><td>MDW = H</td><td>ATCM wait cycle = 1 wait cycle</td></tr>
<tr><td>ON</td><td>MDW = L</td><td>ATCM wait cycle = 0 wait cycles</td></tr>
<tr><td rowspan="2">SW4-5
MDD</td><td>OFF</td><td>MDD = H</td><td>JTAG mode = JTAG authentication in hash mode</td></tr>
<tr><td>ON</td><td>MDD = L</td><td>JTAG mode = Normal mode</td></tr>
<tr><td rowspan="2">SW4-6
MDV2*2</td><td>OFF</td><td>MDV2 = H</td><td>VCC1833_2 = 3.3 V (CN17 : 1-2 are short-circuit)</td></tr>
<tr><td>ON</td><td>MDV2 = L</td><td>VCC1833_2 = 1.8 V (CN17 : 2-3 are short-circuit)</td></tr>
<tr><td rowspan="2">SW4-7
MDV3*2</td><td>OFF</td><td>MDV3 = H</td><td>VCC1833_3 = 3.3 V (CN32 : 1-2 are short-circuit)</td></tr>
<tr><td>ON</td><td>MDV3 = L</td><td>VCC1833_3 = 1.8 V (CN32 : 2-3 are short-circuit)</td></tr>
<tr><td>SW4-8</td><td colspan="2">Unused</td><td>— (At the time of shipment = OFF)</td></tr>
</table>

Notes: 1. This setting is prohibited because NOR flash memory is not mounted.
2. MDV2, MDV3 setting by SW4-6, SW4-7 and supply voltage for VCC1833_2, VCC1833_3 selected by CN17, CN32 must be matched. Otherwise it may cause malfunctions or permanent damage to the device.
3. Setting is prohibited because it is equipped with OctaFlash.

6.2.2 Signal Function Selection Switches SW5 to SW8

SW5 is used to select the functions of P01_7 and P02_0. Table 6-2 to Table 6-5 list the settings of SW5 to SW8.

Table 6-2 Signal Function Selection Switch SW5

No.	Setting					Function
SW5-1 to SW5-5	-1	-2	-3	-4	-5	
	ON	**OFF**	**OFF**	**OFF**	**OFF**	**P01_7 is used as CAN_RX_OB of the CAN interface.**
	OFF	ON	OFF	OFF	OFF	P01_7 is used as SCK for use with PMOD1.
	OFF	OFF	ON	OFF	OFF	P01_7 is used as SPI_RSPCK3 for use with mikroBUS.
	OFF	OFF	OFF	ON	OFF	P01_7 is used as BSC_A19 of JA3-A.
	OFF	OFF	OFF	OFF	ON	P01_7 is used as CAN_RX0_JA5 of JA5-A.
SW5-6 to SW5-9	-6	-7	-8	-9		
	ON	OFF	OFF	OFF		P02_0 is used as ETH0_INT# of EtherCAT port 0.
	OFF	ON	OFF	OFF		P02_0 is used as SPI_MISO3 for use with PMOD1 and mikroBUS.
	OFF	OFF	ON	OFF		P02_0 is used as BSC_A18 of JA3-A.
	OFF	**OFF**	**OFF**	**ON**		**P02_0 is used as CAN_TX1_JA5 of JA5-A.**
SW5-10	Unused					**— (At the time of shipment = OFF)**

SW6 is used to select the functions of P02_2 and P02_3.

Table 6-3 Signal Function Selection Switch SW6

No.	Setting				Function
SW6-1 to SW6-4	-1	-2	-3	-4	
	ON	**OFF**	**OFF**	**OFF**	**P02_2 is used as CAN_TX_OB of the CAN interface.**
	OFF	ON	OFF	OFF	P02_2 is used as SPI_MOSI3 for use with PMOD1 and mikroBUS.
	OFF	OFF	ON	OFF	P02_2 is used as BSC_A16 of JA3-A.
	OFF	OFF	OFF	ON	P02_2 is used as CAN_TX0_JA5 of JA5-A.
SW6-5 to SW6-8	-5	-6	-7	-8	
	ON	OFF	OFF	OFF	P02_3 is used as ETH1_INT# of EtherCAT port 1.
	OFF	ON	OFF	OFF	P02_3 is used as SPI_SSL30 for use with PMOD1 and mikroBUS.
	OFF	OFF	ON	OFF	P02_3 is used as BSC_A15 of JA3-A.
	OFF	**OFF**	**OFF**	**ON**	**P02_3 is used as CAN_RX1_JA5 of JA5-A.**
SW6-9, SW6-10	Unused				**— (At the time of shipment = OFF)**

SW7 is used to select the functions of P05_5, P17_6, and P18_1.

Table 6-4 Signal Function Selection Switch SW7

No.	Setting				Function
SW7-1 to SW7-3	-1	-2	-3		
	ON	OFF	OFF		P05_5 is used as ETH1_LINK of EtherCAT port 1.
	OFF	ON	OFF		P05_5 is used as BSC_A14 of JA3-A.
	OFF	**OFF**	**ON**		**P05_5 is used as HDSL1_LINK of pin header CN1.**
SW7-4 to SW7-6	-4	-5	-6		
	ON	OFF	OFF		P17_6 is used as MIK_PWM for use with mikroBUS.
	OFF	ON	OFF		P17_6 is used as M1_UP of JA2-A.
	OFF	**OFF**	**ON**		**P17_6 is used as LED1 for user LED control.**
SW7-7 to SW7-10	-7	-8	-9	-10	
	ON	OFF	OFF	OFF	P18_1 is used as IRQ10 for use with PMOD1.
	OFF	ON	OFF	OFF	P18_1 is used as ADTRG1# of JA1-A.
	OFF	OFF	ON	OFF	P18_1 is used as M1_UN of JA2-A.
	OFF	**OFF**	**OFF**	**ON**	**P18_1 is used as LED3 for user LED control.**

SW8 is used to select the function of P22_3, the function of P22_1 when it is not to be used as a trace signal (when TRACE_OPTION_SEL = H), and options for signal functions using the bus switch IC.

Table 6-5 Signal Function Selection Switch SW8

No.	Setting			Function
SW8-1 to SW8-3	-1	-2	-3	
	ON	**OFF**	**OFF**	**P22_3 is used as GMAC_RESETOUT# of the Ethernet port.**
	OFF	ON	OFF	P22_3 is used as BSC_D10 of JA3-A.
	OFF	OFF	ON	P22_3 is used as USB_VBUSEN when the USB host interface is used.
SW8-4, SW8-5	-4	-5		
	ON	**OFF**		**P22_1 is used as HSPI_IO7_M2POE_BSC_D08 of the serial host interface, JA5-A, and JA3-A.** **(SW8-10 = OFF: When TRACE_OPTION_SEL = H)**
	OFF	ON		P22_1 is used as ETH2_INT# of the Ethernet port. (SW8-10 = OFF: When TRACE_OPTION_SEL = H)
SW8-6	Unused			**— (At the time of shipment = OFF)**
SW8-7	**OFF**			**ECAT0_OPTION_SEL = H** **A signal other than an ETH0-related signal is selected by bus switch IC33.**
	ON			ECAT0_OPTION_SEL = L An ETH0-related signal is selected by bus switch IC33.
SW8-8	**OFF**			**ECAT1_OPTION_SEL = H** **A signal other than an ETH1-related signal is selected by bus switch IC41.**
	ON			ECAT1_OPTION_SEL = L An ETH1-related signal is selected by bus switch IC41.
SW8-9	OFF			XSPI1_OPTION_SEL = H A signal other than an XSPI1-related signal is selected by bus switch IC37.
	ON			**XSPI1_OPTION_SEL = L** **An XSPI1-related signal is selected by bus switch IC37.**
SW8-10	**OFF**			**TRACE_OPTION_SEL = H** **A signal other than a TRACE-related signal is selected by bus switch IC12.**
	ON			TRACE_OPTION_SEL = L A TRACE-related signal is selected by bus switch IC12.

6.3 Configuration by Jumper Blocks

This board is equipped with jumper blocks CN2, CN4, CN17, CN18, CN21 to CN26, CN32 to CN35, and J9 for selecting functions. The functions set by individual jumper blocks are explained below.

6.3.1 I/O Power Selection Jumper Blocks **CN17 and CN32**

CN17 and CN32 are used to select the power supply to the I/O power domain of the RZ/T2L.

Supply voltage for VCC1833_2, VCC1833_3 selected by CN17, CN32 and MDV2, MDV3 setting by SW4-6, SW4-7 must be matched. Otherwise it may cause malfunctions or permanent damage to the device.

Table 6-6 I/O Power Selection Jumper Blocks CN17 and CN32

No.	Setting	Function
CN17	1-2 are short-circuit	3.3-V power is supplied to VCC1833_2.（SW4-6 : OFF, MDV2 = 'H')
	2-3 are short-circuit	**1.8-V power is supplied to VCC1833_2. (SW4-6 : ON, MDV2 = 'L')**
CN32	**1-2 are short-circuit**	**3.3-V power is supplied to VCC1833_3. (SW4-7 : OFF, MDV3 = 'H')**
	2-3 are short-circuit	1.8-V power is supplied to VCC1833_3. (SW4-7 : ON, MDV3 = 'L')

6.3.2 Debugging Function Selection Jumper Block J9

J9 is used to enable or disable the on-board debugging function J-Link® OB.

Table 6-7 Debugging Function Selection Jumper Block J9

No.	Setting	Function
J9	Open-circuit	The on-board debugging function J-Link® OB is enabled.
	Short-circuit	**The on-board debugging function J-Link® OB is disabled. Connect an external emulator to J13, J20, or CN9 at debugging.**

6.3.3 RS485 Interface Communication Mode Selection Jumper Blocks CN21 and CN22

CN21 and CN22 are used to select the communication mode of the RS485 interface.

Table 6-8 RS485 Interface Communication Mode Selection Jumper Blocks CN21 and CN22

No.	Setting	Function
CN21, CN22	1-2 are short-circuit	Full-duplex communication
	2-3 are short-circuit	**Half-duplex communication**

6.3.4 USB-to-Serial Conversion Signal Selection Jumper Blocks CN34 and CN35

CN34 and CN35 are used to select the signals to be used in the USB-to-serial conversion interface.

Table 6-9 USB-to-Serial Conversion Signal Selection Jumper Blocks CN34 and CN35

No.	Setting	Function
CN34, CN35	**1-2 are short-circuit**	**TXD0_P16_0_JA1 is used as the transmit data signal and RXD0_P16_1_JA1 is used as the receive data signal (SCI channel 0 is used).**
	2-3 are short-circuit	TXD1_MDAT5 is used as the transmit data signal and RXD1_P24_0_JA1 is used as the receive data signal (SCI channel 1 is used).

6.3.5 XSPI1 CS0 Signal Selection Jumper Block CN33

CN33 is used to select where to connect the CS0# signal of XSPI1.

Table 6-10 XSPI1_CS0# Selection Jumper Block CN33

No.	Setting	Function
CN33	**1-2 are short-circuit**	**XSPI1_CS0# is connected to CS# of Quad SPI flash memory (IC3).**
	2-3 are short-circuit	XSPI1_CS0# is connected to CS# of the SPI expansion connector (CN28).

6.3.6 LED Control Port Connection Jumper Blocks CN18 and CN23

CN18 and CN23 are used to connect or disconnect the ports for LED control.

Table 6-11 LED Control Port Connection Jumper Blocks CN18 and CN23

No.	Setting	Function
CN18	**Short-circuit**	**P21_3 is connected to LED0_ESC_RUN.**
	Open-circuit	P21_3 is not connected to LED0_ESC_RUN.
CN23	**Short-circuit**	**P21_6 is connected to LED4_ESC_IN.**
	Open-circuit	P21_6 is not connected to LED4_ESC_IN.

6.3.7 Current Measurement Jumper Blocks CN2, CN4, and CN24 to CN26

CN2, CN4, and CN24 to CN26 are jumper blocks for measuring the current drawn by the target device (RZ/T2L). When measuring the current, insert an ammeter between pins 1-2 of the corresponding jumper block.

Table 6-12 Current Measurement Jumper Blocks CN2, CN4, and CN24 to CN26

No.	Function	Description
CN2	Current of VCC1833_2 is measured.	**The jumper blocks are short-circuit at the time of shipment.** To measure current, remove the relevant jumper block and insert an ammeter between pins 1-2.
CN4	Current of VCC1833_3 is measured.	
CN24	Current of VCC11_RVCORE is measured.	
CN25	Current of CPU1V8 is measured.	
CN26	Current of CPU3V3 is measured.	

6.4 Configuration by Option Links

6.4.1 Settings by Solder Bridges and Trace Cuts

This board is equipped with solder bridges E1 to E3 and E46, and trace cuts E4, E23 to E25, E30, and E32 for selecting functions. Table 6-13 lists the settings of each solder bridge and trace cut.

Table 6-13 Settings of Solder Bridges and Trace Cuts

No.	Setting	Function
E1	**Open-circuit**	**PMOD1 (J26) is to be used with 3.3 V.**
	Short-circuit	PMOD1 (J26) is to be used with 5.0 V. (In this case, E25 should be left open-circuit.)
E2	**Open-circuit**	**PMOD1 (J26) is not to be used with the I²C interface.**
	Short-circuit	PMOD1 (J26) is to be used with the I²C interface. (In this case, E23 should be left open-circuit.)
E3	**Open-circuit**	**PMOD1 (J26) is not to be used with the I²C interface.**
	Short-circuit	PMOD1 (J26) is to be used with the I²C interface. (In this case, E24 should be left open-circuit.)
E4	Open-circuit	Setting prohibited
	Short-circuit	**3.3-V power is supplied to the J-Link® OB circuit.**
E23	Open-circuit	PMOD1 (J26) is not to be used with the SPI interface.
	Short-circuit	**PMOD1 (J26) is to be used with the SPI interface. (In this case, E2 should be left open-circuit.)**
E24	Open-circuit	PMOD1 (J26) is not to be used with the SPI interface.
	Short-circuit	**PMOD1 (J26) is to be used with the SPI interface. (In this case, E3 should be left open-circuit.)**
E25	Open-circuit	PMOD1 (J26) is to be used with 5.0 V.
	Short-circuit	**PMOD1 (J26) is to be used with 3.3 V. (In this case, E1 should be left open-circuit.)**
E30	Open-circuit	Setting prohibited
	Short-circuit	**Pin J13-9 should be connected to the ground. (In this case, an external emulator should be used.)**
E32	Open-circuit	Pin JA2-A-3 is to be used as the NMI input.*
	Short-circuit	**The SW_NMI switch is to be used as the NMI input.***
E46	**Open-circuit**	**The external clock input from JA2-A is not to be used.**
	Short-circuit	The external clock input from JA2-A is to be used. (In this case, R252 should not be mounted.)

Note: Pins 1-2 in CN32 must be short-circuit (3.3-V power supply to VCC1833_3).

6.4.2 Settings by 0-Ω Resistors

The following 0-Ω resistors are or can be placed on this board, and the function to be used can be selected by changing the Fit/DNF state from the state as shipped. Table 6-14, Table 6-15, and Table 6-16 list the settings of 0-Ω resistors.

Table 6-14 Settings of 0-Ω Resistors Related to the Power Supply, Clock, and Reset

No.	Setting		Function
R140	Fit		Analog power (CON_AVCC) is supplied to JA1-A.
	DNF		**Analog power (CON_AVCC) is not supplied to JA1-A.**
R142	Fit		Analog ground (CON_AVSS) is supplied to JA1-A.
	DNF		**Analog ground (CON_AVSS) is not supplied to JA1-A.**
R143	Fit		Analog reference voltage (CON_AVREF) is supplied to JA1-A.
	DNF		**Analog reference voltage (CON_AVREF) is not supplied to JA1-A.**
R133	**Fit**		**5-V power (CON_5V) is supplied to JA1-A.**
	DNF		5-V power (CON_5V) is not supplied to JA1-A.
R134	**Fit**		**3.3-V power (CON_3V3) is supplied to JA1-A.**
	DNF		3.3-V power (CON_3V3) is not supplied to JA1-A.
R52, R53	R52	R53	
	Fit	**DNF**	**The regulator for the 3.3-V power supply is controlled by the RL78/G1C.**
	DNF	Fit	Setting prohibited
R54, R55	R54	R55	
	Fit	**DNF**	**The regulator for the 1.8-V power supply is controlled by the RL78/G1C.**
	DNF	Fit	Setting prohibited
R56, R57	R56	R57	
	Fit	**DNF**	**The regulator for the 1.1-V power supply is controlled by the RL78/G1C.**
	DNF	Fit	Setting prohibited
R58, R59	R58	R59	
	Fit	**DNF**	**The regulator for the 1.0-V power supply is controlled by the RL78/G1C.**
	DNF	Fit	Setting prohibited
R280, R281	R280	R281	
	Fit	**DNF**	**The regulator for the 2.5-V power supply is controlled by the RL78/G1C.**
	DNF	Fit	Setting prohibited
R252*1	**Fit**		**Oscillator X1 is used as the clock of the RZ/T2L.**
	DNF		CON_EXTAL of JA2-A-2 is used as the clock of the RZ/T2L.*2
R37, R40	R37	R40	
	Fit	**DNF**	**RESET_SW# is not included in the sources of TRST#.**
	DNF	Fit	RESET_SW# is included in the sources of TRST#.

Notes: 1. The resistance is 18 Ω.
2. E46 must be short-circuit.

Table 6-15 Settings of 0-Ω Resistors Related to the Debug Interface

No.	Setting		Function
R42, R43	R42	R43	
	Fit	DNF	TRST_OUT# is connected to pin J20-16 of the connector.
	DNF	**Fit**	**TRACE_D1 is connected to pin J20-16 of the connector.**

Table 6-16 Settings of 0-Ω Resistors for Selecting Signal Functions

No.	Setting			Function
R195, R196	R195	R196		
	Fit	**DNF**		**P01_6 is used as M1_ENCZ of JA2-A.*9**
	DNF	Fit		P01_6 is used as BSC_A20 of JA3-A.*9
R197, R198	R197	R198		
	Fit	**DNF**		**P04_1 is used as an input from SW3-2.**
	DNF	Fit		P04_1 is used as BSC_CKIO of JA3-A.
R199, R200	R199	R200		
	Fit	**DNF**		**P07_4 is used as USB_VBUSIN of the USB function interface.**
	DNF	Fit		P07_4 is used as IRQ1 of JA2-A.
R321, R322, R323	R321	R322	R323	
	Fit	**DNF**	**DNF**	**P10_4 is used as ETH0_LINK of EtherCAT port 0.**
	DNF	Fit	DNF	P10_4 is used as BSC_D15 of JA3-A.
	DNF	DNF	Fit	P10_4 is used as SCK0 of JA6.
R324, R325	R324	R325		
	Fit	**DNF**		**P13_2 is used as ESC_I2CCLK for EEPROM control and JA1-A.**
	DNF	Fit		P13_2 is used as MCLK4 of pin header CN3.
R326, R327	R326	R327		
	Fit	**DNF**		**P13_3 is used as ESC_I2CDATA for EEPROM control and JA1-A.**
	DNF	Fit		P13_3 is used as MDAT4 of pin header CN3.
R328, R329	R328	R329		
	Fit	**DNF**		**P13_4 is used as ESC_RESETOUT# of EtherCAT port 0 and port 1.**
	DNF	Fit		P13_4 is used as BSC_WAIT# of JA3-A.
R88, R89, R90	R88	R89	R90	
	Fit	**DNF**	**DNF**	**P18_3 is used as RS485_DE3 of the RS485 interface.*1**
	DNF	Fit	DNF	P18_3 is used as MB_RST# for use with mikroBUS.*1
	DNF	DNF	Fit	P18_3 is used as CN1_3PIN of pin header CN1.*1, *3
R201, R202	R201	R202		
	Fit	**DNF**		**P09_7 is used as CN1_3PIN of pin header CN1.*2, *3**
	DNF	Fit		P09_7 is used as IRQ12 of SPI expansion connector CN28.*2
R330, R331	R330	R331		
	Fit	**DNF**		**P15_0 is used as JA3_46PIN of JA3-A.*4**
	DNF	Fit		P01_3 is used as JA3_46PIN of JA3-A.*5
R332, R333	R332	R333		
	Fit	**DNF**		**P10_0 is used as CN1_4PIN of pin header CN1.*2**
	DNF	Fit		P18_0 is used as CN1_4PIN of pin header CN1.*1, *6
R334, R335, R336	R334	R335	R336	
	Fit	**DNF**	**DNF**	**P18_0 is used as RS485_TXD3 of the RS485 interface.*1, *6**
	DNF	Fit	DNF	P18_0 is used as JA2_16PIN of JA2-A.*1, *6, *7
	DNF	DNF	Fit	P18_0 is used as JA2_17PIN of JA2-A.*1, *6, *8

R337, R338	R337		R338		
	Fit		**DNF**		**P18_2 is used as JA2_16PIN of JA2-A.**[*1, *7]
	DNF		Fit		P18_2 is used as JA2_17PIN of JA2-A.[*1, *8]
R339, R340, R341, R245	R339	R340	R341	R245	
	Fit	**DNF**	**DNF**	**Fit**	**P10_1 is used as CN1_5PIN of pin header CN1[*2], and P17_7 is used as RXD of RS485.[*1]**
	Fit	DNF	Fit	DNF	P10_1 is used as CN1_5PIN of pin header CN1[*2], and P17_7 is used as JA2_15PIN of JA2-A.[*1]
	DNF	Fit	DNF	DNF	P17_7 is used as CN1_5PIN of pin header CN1.[*1]
R238	**Fit**				**AN000 is used as an input of potentiometer R144.**
	DNF				AN000 is used as the 9-pin analog input of JA1-A.

Notes:
1. SW8-9 = OFF (XSPI1_OPTION_SEL = H) must also be set.
2. SW8-7 = OFF (ECAT0_OPTION_SEL = H) must also be set.
3. These settings cannot be made at the same time.
4. Pins 1-2 in CN32 must be short-circuit (3.3-V power supply to VCC1833_3).
5. Pins 1-2 in CN17 must be short-circuit (3.3-V power supply to VCC1833_2).
6. These settings cannot be made at the same time.
7. These settings cannot be made at the same time.
8. These settings cannot be made at the same time.
9. SW3-1 = OFF must also be set.

7. User Circuits

This chapter describes the circuits on the board for each of its functions.

The initial state of this board at the time of shipment is indicated by the **text in bold blue type** in the "Settings of Configuration Circuits" column of each of the signal connection tables. Refer to the details on the configuration circuits in chapter 6.

7.1 Reset Circuit

A reset signal can be generated by the power-on reset IC and RES switch on the board. Figure 7-1 shows the configuration of the reset circuit.

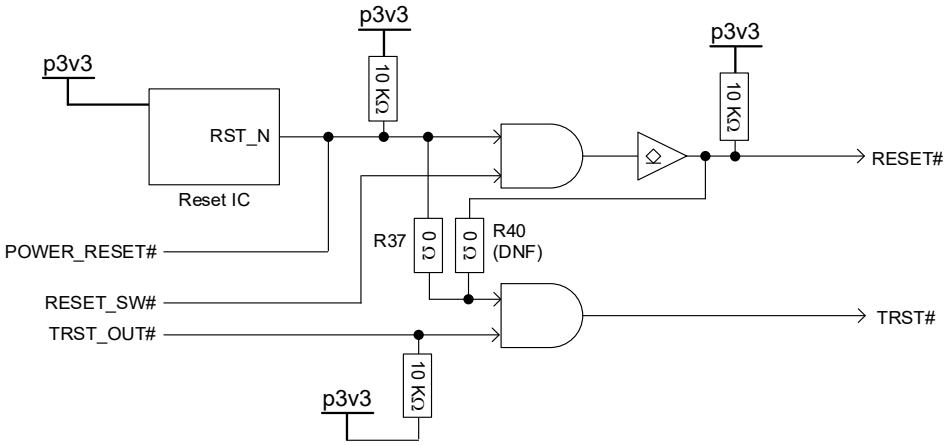


Figure 7-1 Configuration of Reset Circuit

7.2 Clock Circuit

Figure 7-2 shows the clock circuit for the RZ/T2L on this board. Table 7-1 lists the oscillators mounted on the board.

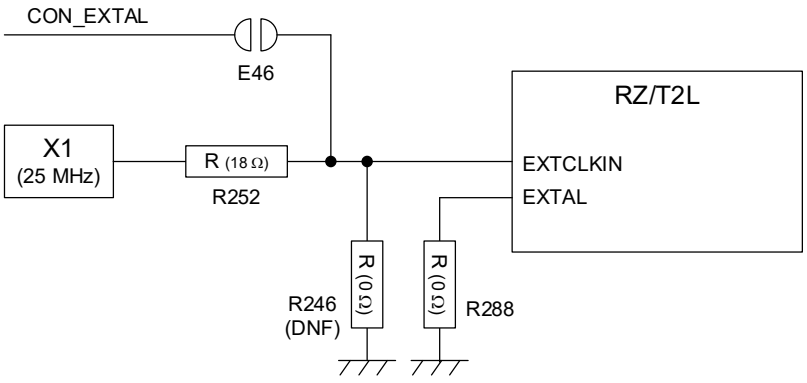


Figure 7-2 Configuration of Clock Circuit

Table 7-1 List of Oscillators

Oscillator	Function or Intended Use	State as Shipped	Frequency
X1	Main clock for the RZ/T2L (oscillator)	Mounted	25 MHz
X2	Main clock for the RL78/G1C	Mounted	12 MHz

7.3 Switches

This board is equipped with four push switches and six DIP switches in addition to the power switch described in section 2.2. Table 7-2 lists the functions and signal connections of the four push switches. Table 7-3 lists the functions and signal connections of DIP switch SW3, which is provided for user control.

Among the DIP switches, SW4 is used for setting the mode of the RZ/T2L, and SW5 to SW8 are used for selecting the functions of the signal lines. Refer to section 6.2 in which the switches are explained as part of the configuration circuitry of this board.

Table 7-2 Signal Connections of Push Switches

Switch	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
RES	Reset switch	RES#*1	N5	—
SW1	Switch for user control. Connected to IRQ6.	P14_2*2	K11	**CN32: 1-2, SW4-7: OFF**
SW2	Switch for user control. Connected to IRQ7.	P16_3	G14	—
NMI	Switch for user control. Connected to NMI.	P16_2*2	G13	**CN32: 1-2, SW4-7: OFF, E32: Short-circuit**

Notes: 1. Connected via the reset circuit.
2. Connected via the bus switch IC.

Table 7-3 Signal Connections of DIP Switch SW3 for User Control

Switch	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
SW3-1	Connected to P01_6 for user control	P01_6	C2	—
SW3-2	Connected to P04_1 for user control	P04_1*	F1	**R197: Fit**
SW3-3	Connected to P14_1 for user control	P14_1	M14	—
SW3-4	Connected to P14_3 for user control	P14_3	L13	—

Note: Connected via a 0-Ω resistor for function selection.

7.4 LEDs

This board is equipped with 14 LEDs. Table 7-4 lists the functions, colors, and signal connections of LEDs.

Table 7-4 Signal Connections of LEDs

LED	Color	Function or Intended Use	MPU		Settings of Configuration Circuits
			Port	Pin	
POWER	Green	Indicator of the 3.3-V power-supply line	—	—	—
LED0_ESC_RUN	Green	User LED or EtherCAT LED (RUN)	P21_3*1	C7	**SW8-10: OFF, CN18: Short-circuit**
LED1	Yellow	User LED	P17_6*2	F12	**SW7-6: ON**
LED2_ESC_ERR	Red	User LED or EtherCAT LED (ERR)	P20_3	C8	—
LED3	Red	User LED	P18_1*2	D14	**SW7-10: ON**
LED4_ESC_IN	Green	User LED or EtherCAT LED (IN: LINKACT0)	P21_6*1	A7	**SW8-10: OFF, CN23: Short-circuit**
LED5_ESC_OUT	Green	User LED or EtherCAT LED (OUT: LINKACT1)	P20_4	A9	—
LED6	Yellow	Indicator of J-Link® OB	—	—	—
LED built in CN14	Green	EtherCAT port 0 LED (Link)	—	—	—
LED built in CN14	Yellow	EtherCAT port 0 LED (Activity)	—	—	—
LED built in CN13	Green	EtherCAT port 1 LED (Link)	—	—	—
LED built in CN13	Yellow	EtherCAT port 1 LED (Activity)	—	—	—
LED built in CN7	Green	Ethernet port LED (Link)	—	—	—
LED built in CN7	Yellow	Ethernet port LED (Activity)	—	—	—

Notes: 1. Connected via the bus switch IC. If the factory settings are used, P21_3 can be used for controlling LED0_ESC_RUN and P21_6 can be used for controlling LED4_ESC_IN.
2. Connected via DIP switch SW7. If the factory settings are used, P17_6 can be used for controlling LED1 and P18_1 can be used for controlling LED3.

7.5 Potentiometer

On this board, a 10-kΩ single-rotation potentiometer for evaluating the ADC is connected to AN000 (pin A13) of the RZ/T2L. Figure 7-3 shows the configuration of the potentiometer circuit.

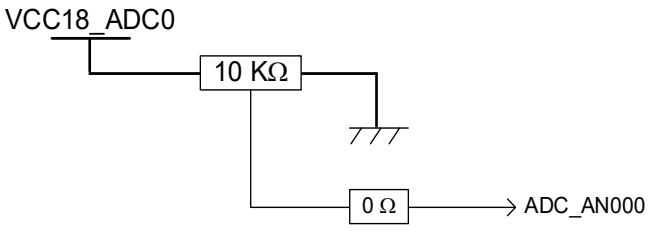


Figure 7-3 Configuration of Potentiometer Circuit

A potentiometer is installed to provide an easy way of supplying a variable analog input to the microprocessor. Note in advance that it will not guarantee the accuracy of the A/D converter.

7.6 Pmod™

This board is equipped with two connectors for Digilent Pmod™ interfaces so that compatible Pmod™ modules can be connected and evaluated. PMOD1 (J26) supports the type 2A and 6A Pmod™ interfaces and PMOD2 (J25) supports type 3A. Figure 7-4 shows the configuration of the Pmod™ interface circuits, and Table 7-5 and Table 7-6 list the signal connections.

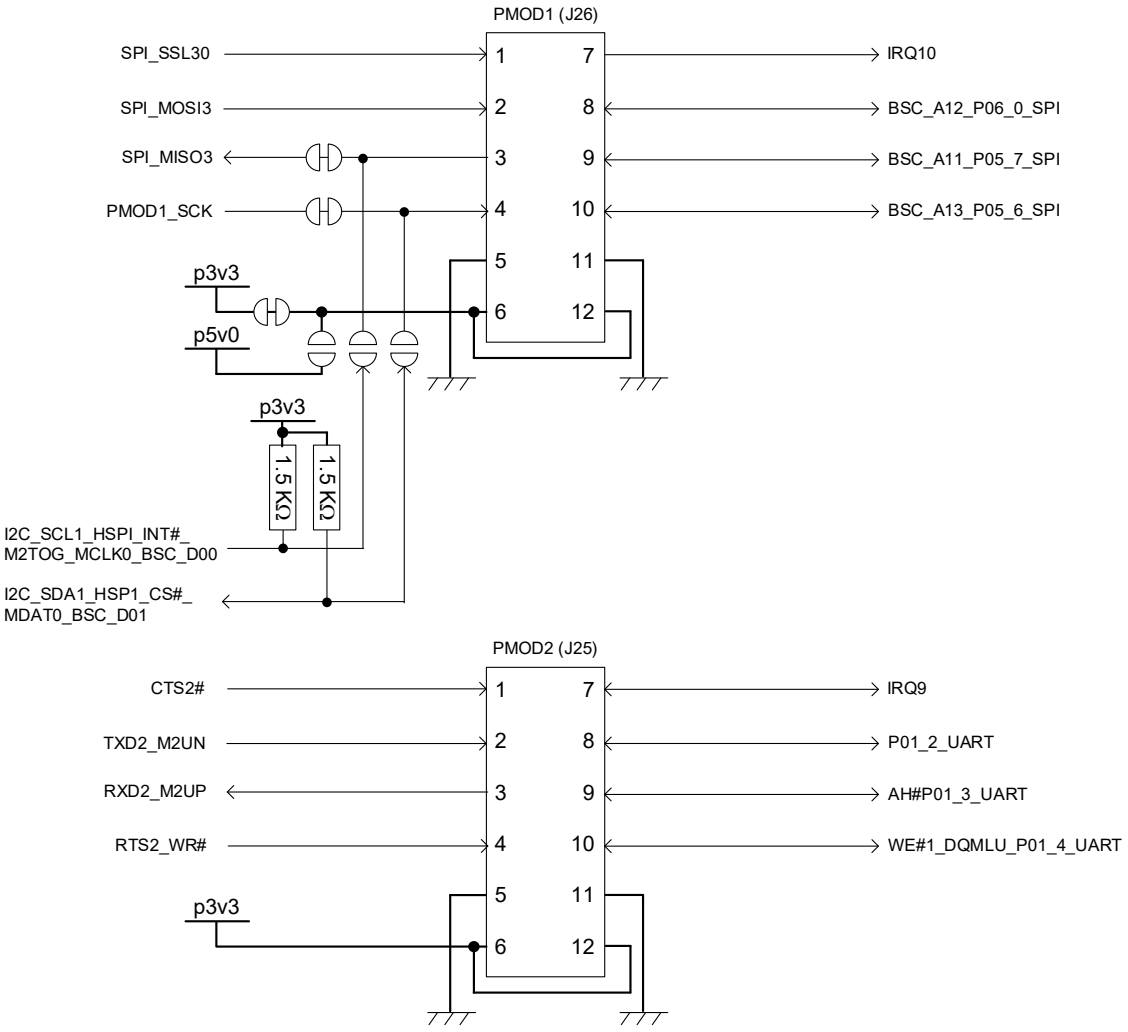


Figure 7-4 Configuration of Pmod™ Interface Circuits

Table 7-5 Signal Connections of PMOD1 Connector (J26)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	SPI_SSL30	P02_3*1	D1	SW6-6: ON
2	SPI_MOSI3	P02_2*1	E2	SW6-2: ON
3	SPI_MISO3	P02_0*1	D2	SW5-7: ON, **E23: Short-circuit**
	I2C_SCL1_HSPI_INT#_M2TOG_MCLK0_BSC_D00	P21_1*2, *3	A8	**SW8-10: OFF**, E2: Short-circuit
4	PMOD1_SCK	P01_7*1	B1	SW5-2: ON, **E24: Short-circuit**
	I2C_SDA1_HSP1_CS#_MDAT0_BSC_D01	P21_2*3	B8	**SW8-10: OFF**, E3: Short-circuit
5	GROUND	—	—	—
6	p3v3	—	—	**E1: Open-circuit,** **E25: Short-circuit**
	p5v0*3			E1: Short-circuit, E25: Open-circuit
7	IRQ10	P18_1*1	D14	SW7-7: ON
8	BSC_A12_P06_0_SPI	P06_0*2	G1	**SW8-8: OFF**
9	BSC_A11_P05_7_SPI	P05_7*2	H4	**SW8-8: OFF**
10	BSC_A13_P05_6_SPI	P05_6*2	G2	**SW8-8: OFF**
11	GROUND	—	—	—
12	p3v3	—	—	**E1: Open-circuit,** **E25: Short-circuit**
	p5v0*3			E1: Short-circuit, E25: Open-circuit

Notes: 1. Connected via DIP switches SW5, SW6, and SW7.
2. Connected via the bus switch IC.
3. To change the function, the setting of a solder bridge jumper has to be changed.

Table 7-6 Signal Connections of PMOD2 Connector (J25)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	CTS2#	P01_0*	D3	CN17: 1-2, SW4-6: OFF
2	TXD2_M2UN	P08_7*	M1	**SW8-7: OFF**
3	RXD2_M2UP	P08_5*	L2	**SW8-7: OFF**
4	RTS2_WR#	P00_3*	A3	CN17: 1-2, SW4-6: OFF
5	GROUND	—	—	—
6	p3v3	—	—	—
7	IRQ9	P08_6*	M2	**SW8-7: OFF**
8	P01_2_UART	P01_2*	B3	CN17: 1-2, SW4-6: OFF
9	AH#P01_3_UART	P01_3*	A2	CN17: 1-2, SW4-6: OFF
10	WE#1_DQMLU_P01_4_UART	P01_4*	E4	CN17: 1-2, SW4-6: OFF
11	GROUND	—	—	—
12	p3v3	—	—	—

Note: Connected via the bus switch IC.

Note that the pin assignment for a Digilent Pmod™ connector differs in terms of numbering from that for a typical connector. Figure 7-5 shows the pin assignment for a Pmod™ connector. For details, refer to the Digilent Pmod™ Interface Specification.

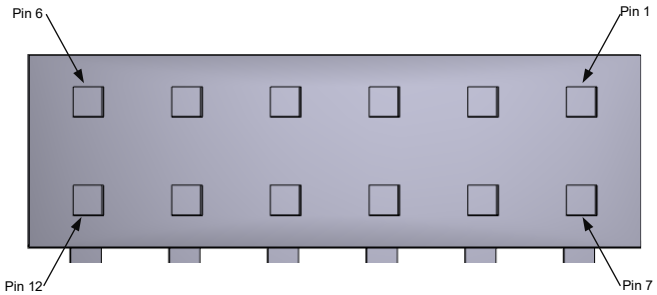


Figure 7-5 Pin Assignment for a Digilent Pmod™ Connector (Viewed from the Direction of Insertion)

7.7 Grove®

This board is equipped with two connectors for Grove® interfaces so that compatible Grove® modules can be connected and evaluated. Figure 7-6 shows the configuration of the Grove® interface circuits and Figure 7-7 shows the pin assignment for a Grove® connector. Table 7-7 and Table 7-8 list the signal connections.

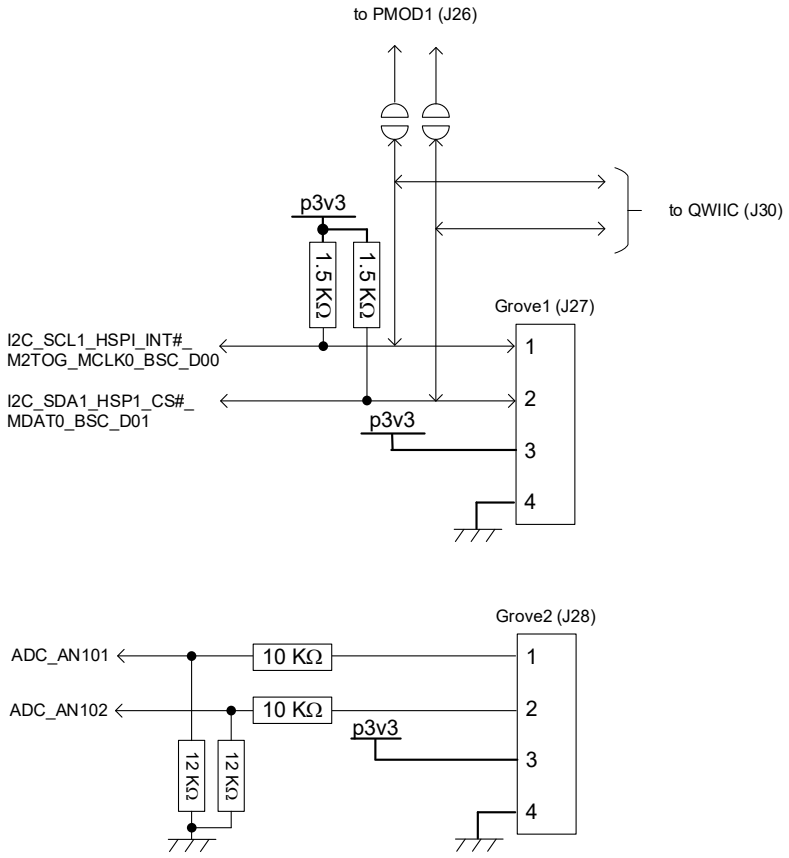


Figure 7-6 Configuration of Grove® Interface Circuits

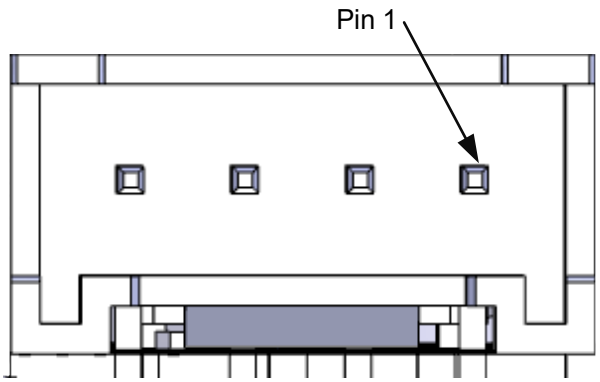


Figure 7-7 Pin Assignment for a Grove® Connector (Viewed from the Direction of Insertion)

Table 7-7 Signal Connections of Grove®1 Connector (J27)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	I2C_SCL1_HSPI_INT#_M2TOG_MCLK0_BSC_D00	P21_1*	A8	SW8-10: OFF
2	I2C_SDA1_HSP1_CS#_MDAT0_BSC_D01	P21_2*	B8	SW8-10: OFF
3	p3v3	—	—	—
4	GROUND	—	—	—

Note: Connected via the bus switch IC and shared with QWIIC® and other interfaces.

Table 7-8 Signal Connections of Grove®2 Connector (J28)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	ADC_AN101	AN101	B11	—
2	ADC_AN102	AN102	C10	—
3	p3v3	—	—	—
4	GROUND	—	—	—

7.8 QWIIC®

This board is equipped with a connector for the QWIIC® interface so that a compatible QWIIC® module can be connected and evaluated. Figure 7-8 shows the pin assignment for a QWIIC® connector, and Table 7-9 lists the signal connections.

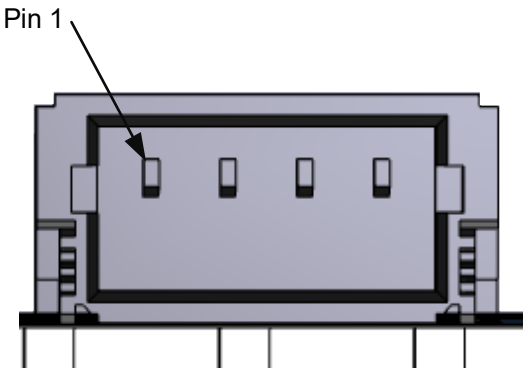


Figure 7-8 Pin Assignment for a QWIIC® Connector (Viewed from the Direction of Insertion)

Table 7-9 Signal Connections of QWIIC® Connector (J30)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	GROUND	—	—	—
2	p3v3	—	—	—
3	I2C_SDA1_HSP1_CS#_MDAT0_BSC_D01	P21_2*	B8	**SW8-10: OFF**
4	I2C_SCL1_HSPI_INT#_M2TOG_MCLK0_BSC_D00	P21_1*	A8	**SW8-10: OFF**

Note: Connected via the bus switch IC and shared with Grove®2 and other interfaces.

7.9 mikroBUS™

This board is equipped with two connectors for mikroBUS™ interfaces so that compatible mikroBUS™ modules can be connected and evaluated. Figure 7-9 shows the configuration of the mikroBUS™ interface circuits, and Table 7-10 and Table 7-11 list the signal connections.

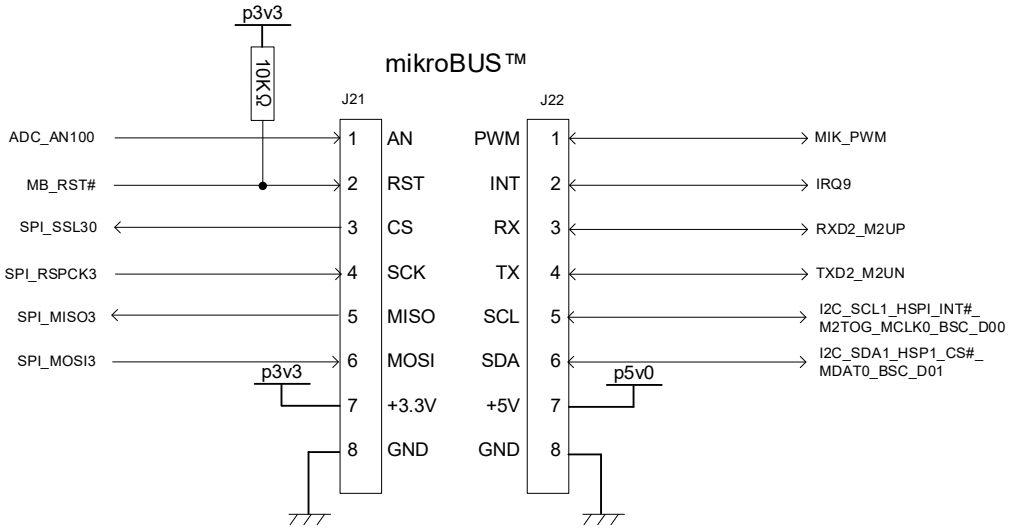


Figure 7-9 Configuration of mikroBUS™ Interface Circuits

Table 7-10 Signal Connections of mikroBUS™ Connector (J21)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	ADC_AN100	AN100	A11	—
2	MB_RST#	P18_3*1	D13	SW8-9: OFF, R89: Fit
3	SPI_SSL30	P02_3*2	D1	SW6-6: ON
4	SPI_RSPCK3	P01_7*2	B1	SW5-3: ON
5	SPI_MISO3	P02_0*2	D2	SW5-7: ON
6	SPI_MOSI3	P02_2*2	E2	SW6-2: ON
7	p3v3	—	—	—
8	GROUND	—	—	—

Notes: 1. Connected via the bus switch IC and shared with Grove®2 and other interfaces.
2. Connected via DIP switches SW5, SW6, and SW8.

Table 7-11 Signal Connections of mikroBUS™ Connector (J22)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	MIK_PWM	P17_6*1	F12	SW7-4: ON
2	IRQ9	P08_6*2	M2	**SW8-7: OFF**
3	RXD2_M2UP	P08_5*2	L2	**SW8-7: OFF**
4	TXD2_M2UN	P08_7*2	M1	**SW8-7: OFF**
5	I2C_SCL1_HSPI_INT#_M2TOG_MCLK0_BSC_D00	P21_1*2	A8	**SW8-10: OFF**
6	I2C_SDA1_HSP1_CS#_MDAT0_BSC_D01	P21_2*2	B8	**SW8-10: OFF**
7	p5v0	—	—	—
8	GROUND	—	—	—

Notes: 1. Connected via DIP switch SW7.
2. Connected via the bus switch IC and shared with Grove®2 and other interfaces.

7.10 USB-to-Serial Conversion

This board is equipped with a USB connector (CN16) for terminal output and a RL78/G1C for USB-to-serial conversion. Figure 7-10 shows the configuration of the USB-to-serial conversion circuit, and Table 7-12 lists the signal connections.

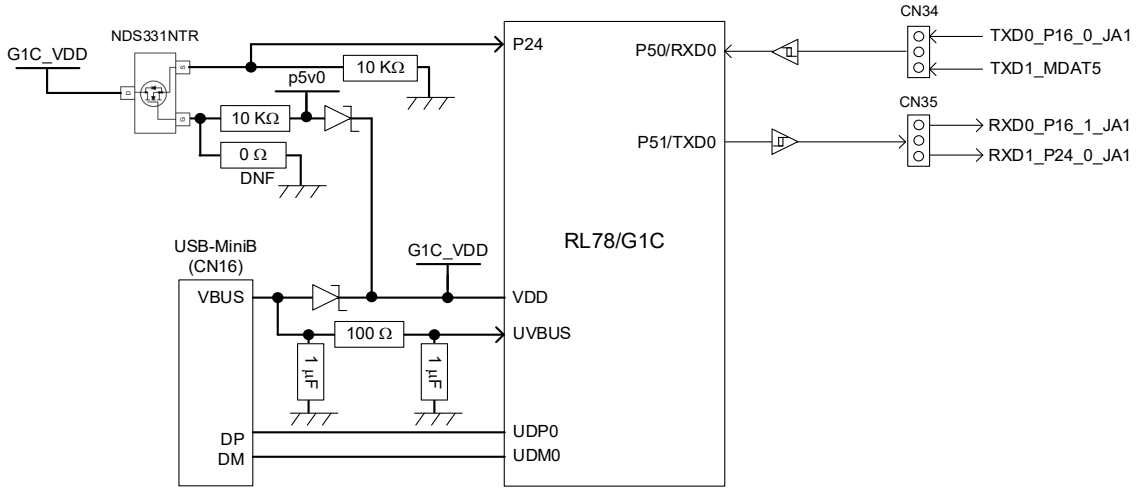


Figure 7-10 Configuration of USB-to-Serial Conversion Circuit

Table 7-12 Signal Connections of USB-to-Serial Conversion

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
TXD0_P16_0_JA1	Transmission of UART data for USB-to-serial conversion	P16_0*	G12	**CN32: 1-2, SW4-7: OFF, CN34: 1-2**
TXD1_MDAT5		P24_2*	C5	CN17: 1-2, SW4-6: OFF, CN34: 2-3
RXD0_P16_1_JA1	Reception of UART data for USB-to-serial conversion	P16_1*	G11	**CN32: 1-2, SW4-7: OFF, CN35: 1-2**
RXD1_P24_0_JA1		P24_0*	D5	CN17: 1-2, SW4-6: OFF, CN35: 2-3

Note: Connected via the bus switch IC.

When the USB connector (CN16) for terminal output is first connected to a PC, the PC will search for a driver. A driver with the standard specification that has been installed on the PC should be used. If no driver has been installed, download the driver installer from the following URL:

https://www.renesas.com/document/rsk-usb-serial-driver?language=en

7.11 CAN

This board is equipped with a CAN transceiver (U10) and a CAN interface connector (J33) so that the CAN module of the RZ/T2L can be connected and evaluated. Figure 7-11 shows the configuration of the CAN interface circuit, and Table 7-13 lists the signal connections.

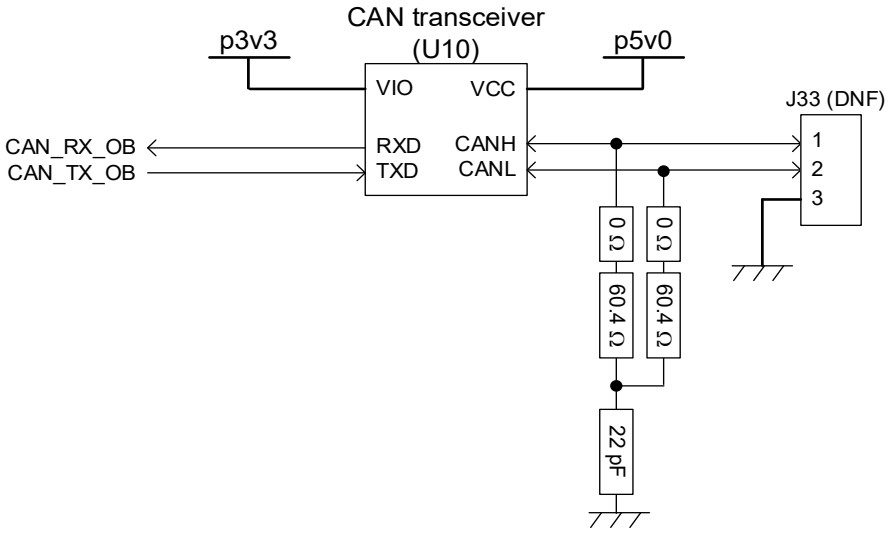


Figure 7-11 Configuration of CAN Interface Circuit

Table 7-13 Signal Connections of CAN

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
CAN_TX_OB	Transmission of CAN data	P02_2*	E2	**SW6-1: ON**
CAN_RX_OB	Reception of CAN data	P01_7*	B1	**SW5-1: ON**

Note: Connected via DIP switches SW5 and SW6.

7.12 Ethernet, EtherCAT

When running any Ethernet software, do so with the use of a unique MAC address. A sticker indicating the unique MAC address that was assigned by Renesas is affixed to the CPU board (top side) to ensure full compatibility in the case of connection to other Renesas hardware modules.

An EtherCAT ID number is required to execute the EtherCAT slave controller software. Please use SW3 as required.

This board is equipped with three Ethernet PHY devices and Ethernet connectors (CN7, CN13, and CN14) so that the Ethernet and EtherCAT interface of the RZ/T2L can be evaluated. Figure 7-12 shows the configuration of the Ethernet and EtherCAT circuits. Table 7-14, Table 7-15, and Table 7-16 list the signal connections. Table 7-17 shows initial settings by hardware strapping of the PHY chips.

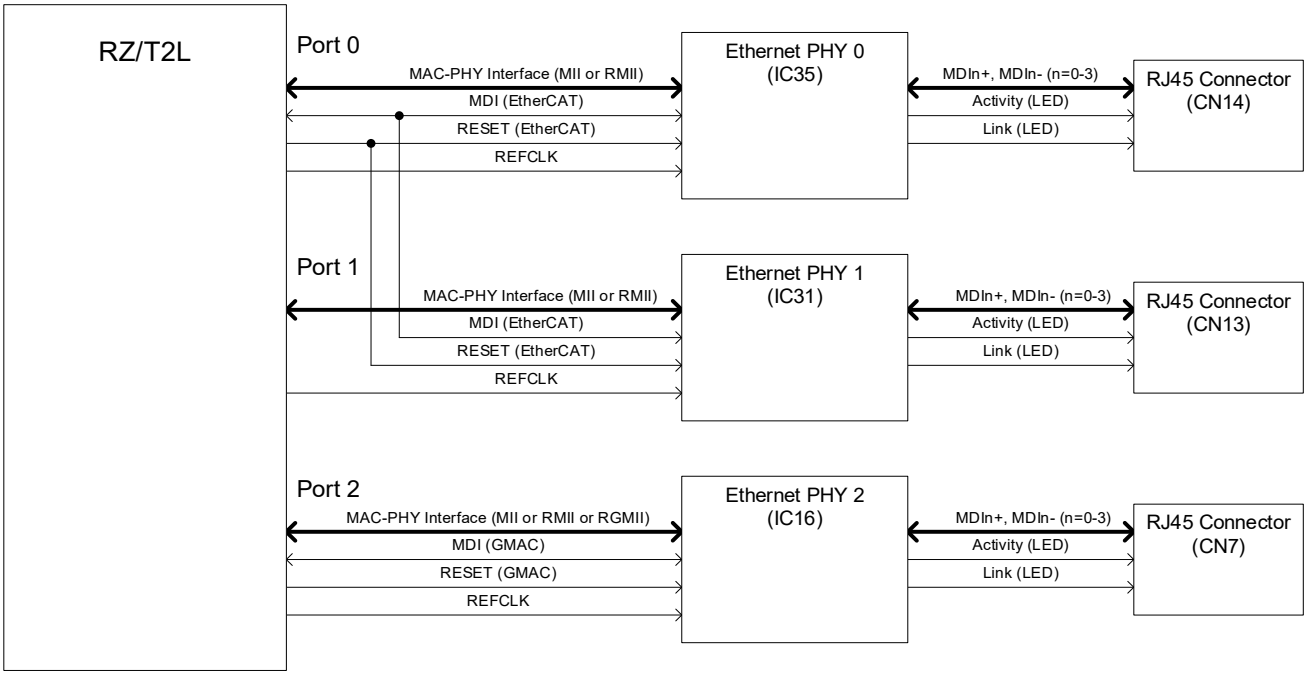


Figure 7-12 Configuration of Ethernet, EtherCAT Circuits

Table 7-14 Signal Connections of EtherCAT Port 0 (ETH0)

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
ETH0_TXCLK	MII: Transmit clock of port 0	P09_7*1	M4	SW8-7: ON
ETH0_TXEN	MII: Transmit data enable/disable error of port 0	P10_0*1	N4	SW8-7: ON
ETH0_TXD0	MII: Transmit data 0 of port 0	P09_6*1	P2	SW8-7: ON
ETH0_TXD1	MII: Transmit data 1 of port 0	P09_5*1	N3	SW8-7: ON
ETH0_TXD2	MII: Transmit data 2 of port 0	P09_4*1	L4	SW8-7: ON
ETH0_TXD3	MII: Transmit data 3 of port 0	P09_3*1	N2	SW8-7: ON
ETH0_RXCLK	MII: Receive clock of port 0	P08_6*1	M2	SW8-7: ON
ETH0_RXDV	MII: Receive data enable/disable error of port 0	P08_5*1	L2	SW8-7: ON
ETH0_RXD0	MII: Receive data 0 of port 0	P10_1*1	L5	SW8-7: ON
ETH0_RXD1	MII: Receive data 1 of port 0	P10_2*1	M5	SW8-7: ON
ETH0_RXD2	MII: Receive data 2 of port 0	P10_3*1	P3	SW8-7: ON
ETH0_RXD3	MII: Receive data 3 of port 0	P08_4*1	L3	SW8-7: ON
ETH0_REFCLK	MII: Clock output of port 0 (25 MHz)	P09_1*1	M3	SW8-7: ON
ETH0_RXER	MII: Receive data error of port 0	P09_2*1	N1	SW8-7: ON
ETH0_INT#	PHY0 interrupt input	P02_0*2	D2	SW5-6: ON
ETH0_LINK	EtherCAT PHY0 link status	P10_4*3	P4	**R321: Fit**
ESC_MDC	EtherCAT MDI: Clock	P08_7*1	M1	SW8-7: ON
ESC_MDIO	EtherCAT MDI: Data	P09_0*1	K5	SW8-7: ON
ESC_RESETOUT#	EtherCAT reset output	P13_4*3	M12	**R328: Fit**

Notes: 1. Connected via the bus switch IC.
2. Connected via DIP switch SW5.
3. Connected via a 0-Ω resistor for function selection.

Table 7-15 Signal Connections of EtherCAT Port 1 (ETH1)

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
ETH1_TXCLK	MII: Transmit clock of port 1	P06_4*1	H1	SW8-8: ON
ETH1_TXEN	MII: Transmit data enable/disable error of port 1	P06_5*1	J2	SW8-8: ON
ETH1_TXD0	MII: Transmit data 0 of port 1	P06_3*1	J4	SW8-8: ON
ETH1_TXD1	MII: Transmit data 1 of port 1	P06_2*1	H2	SW8-8: ON
ETH1_TXD2	MII: Transmit data 2 of port 1	P05_7*1	H4	SW8-8: ON
ETH1_TXD3	MII: Transmit data 3 of port 1	P06_0*1	G1	SW8-8: ON
ETH1_RXCLK	MII: Receive clock of port 1	P07_3*1	K3	SW8-8: ON
ETH1_RXDV	MII: Receive data enable/disable error of port 1	P07_2*1	K2	SW8-8: ON
ETH1_RXD0	MII: Receive data 0 of port 1	P06_6*1	J3	SW8-8: ON
ETH1_RXD1	MII: Receive data 1 of port 1	P06_7*1	J1	SW8-8: ON
ETH1_RXD2	MII: Receive data 2 of port 1	P07_0*1	K1	SW8-8: ON
ETH1_RXD3	MII: Receive data 3 of port 1	P07_1*1	K4	SW8-8: ON
ETH1_REFCLK	MII: Clock output of port 1 (25 MHz)	P06_1*1	H3	SW8-8: ON
ETH1_RXER	MII: Receive data error of port 1	P05_6*1	G2	SW8-8: ON
ETH1_INT#	PHY1 interrupt input	P02_3*2	D1	SW6-5: ON
ETH1_LINK	EtherCAT PHY1 link status	P05_5*2	G3	SW7-1: ON
ESC_MDC	EtherCAT MDI: Clock	P08_7*1	M1	SW8-8: ON
ESC_MDIO	EtherCAT MDI: Data	P09_0*1	K5	SW8-8: ON
ESC_RESETOUT#	EtherCAT reset output	P13_4*3	M12	**R328: Fit**

Notes: 1. Connected via the bus switch IC.
2. Connected via DIP switches SW6 and SW7.
3. Connected via a 0-Ω resistor for function selection.

Table 7-16 Signal Connections of Ethernet Port (ETH2)

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
ETH2_TXCLK	RGMII: Transmit clock of port 2	P00_6*1	D4	**CN17: 2-3, SW4-6: ON**
ETH2_TXEN	RGMII: Transmit data enable/disable error of port 2	P00_2*1	C4	**CN17: 2-3, SW4-6: ON**
ETH2_TXD0	RGMII: Transmit data 0 of port 2	P01_5*1	B2	**CN17: 2-3, SW4-6: ON**
ETH2_TXD1	RGMII: Transmit data 1 of port 2	P01_4*1	E4	**CN17: 2-3, SW4-6: ON**
ETH2_TXD2	RGMII: Transmit data 2 of port 2	P01_3*1	A2	**CN17: 2-3, SW4-6: ON**
ETH2_TXD3	RGMII: Transmit data 3 of port 2	P01_2*1	B3	**CN17: 2-3, SW4-6: ON**
ETH2_RXCLK	RGMII: Receive clock of port 2	P24_1*1	A4	**CN17: 2-3, SW4-6: ON**
ETH2_RXDV	RGMII: Receive data enable/disable error of port 2	P00_1*1	B4	**CN17: 2-3, SW4-6: ON**
ETH2_RXD0	RGMII: Receive data 0 of port 2	P23_7*1	B5	**CN17: 2-3, SW4-6: ON**
ETH2_RXD1	RGMII: Receive data 1 of port 2	P24_0*1	D5	**CN17: 2-3, SW4-6: ON**
ETH2_RXD2	RGMII: Receive data 2 of port 2	P24_2*1	C5	**CN17: 2-3, SW4-6: ON**
ETH2_RXD3	RGMII: Receive data 3 of port 2	P00_0*1	E5	**CN17: 2-3, SW4-6: ON**
ETH2_REFCLK	RGMII: Clock output of port 2 (25 MHz)	P00_3*1	A3	**CN17: 2-3, SW4-6: ON**
ETH2_INT#	PHY2 interrupt input	P22_1*2	D6	**SW8-10: OFF,** SW8-5: ON
GMAC_MDC	GMAC MDI: Clock	P01_1*1	C3	**CN17: 2-3, SW4-6: ON**
GMAC_MDIO	GMAC MDI: Data	P01_0*1	D3	**CN17: 2-3, SW4-6: ON**
GMAC_RESET OUT#	GMAC reset output	P22_3*2	A5	**SW8-1: ON**

Notes: 1. Connected via the bus switch IC.
2. Connected via DIP switch SW8.

Table 7-17 Initial Settings by Hardware Strapping of the PHY Chips

Items of PHY Initial Settings	Contents of PHY Initial Settings
CLKOUT	Disabled
Managed or unmanaged	Unmanaged mode
CLK delay	2.0 ns
Link advertisement	PHY0, PHY1: 10 BT, HDX forced mode, autoneg OFF PHY2: 10/100/1000 FDX/HDX, autoneg ON
MAC interface	RGMII mode
Selection of GMII/MII or RGMII/RMII	PHY0, PHY1: MII or RMII mode PHY2: MII, RMII, or RGMII mode
PHY address	PHY0 (IC35): 0 PHY1 (IC31): 1 PHY2 (IC16): 2
Enabling of forced 1000-BT mode	Not set

7.13 USB

This board is equipped with a USB type-A connector (CN10) and a mini-B connector (CN11). The USB function of the RZ/T2L can be used for either a USB host interface or a USB function interface (both cannot be used at the same time).

Figure 7-13 shows the configuration of the USB circuit, and Table 7-18 lists the signal connections.

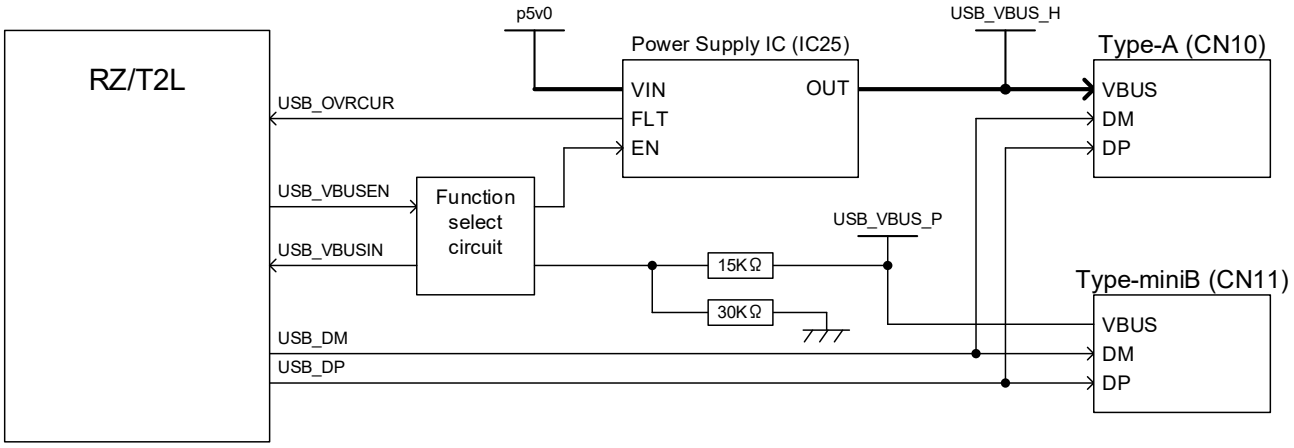


Figure 7-13 Configuration of USB Circuit

Table 7-18 Signal Connections of USB

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
USB_DP	Input/output of D+ data	USB_DP	P10	—
USB_DM	Input/output of D- data	USB_DM	P9	—
USB_VBUSIN	Signal detecting connection/disconnection of USB cable	P07_4*1	L7	**R199: Fit**
USB_VBUSEN	VBUS power enable signal	P22_3*2	A5	SW8-3: ON
USB_OVRCUR	Overcurrent signal	P17_5	F14	—

Notes: 1. Connected via a 0-Ω resistor for function selection.
2. Connected via DIP switch SW8.

7.14 Memory

This board has OctaFlash, HyperRAM, Quad SPI flash memory, and EEPROM as memory. An SPI expansion connector (CN28) is also connected to xSPI1.

Figure 7-14 shows the configuration of memory circuits, and Table 7-19 lists the memories. Table 7-20, Table 7-21, and Table 7-22 list the signal connections for each memory, and Table 7-23 lists the signal connections for the SPI expansion connector.

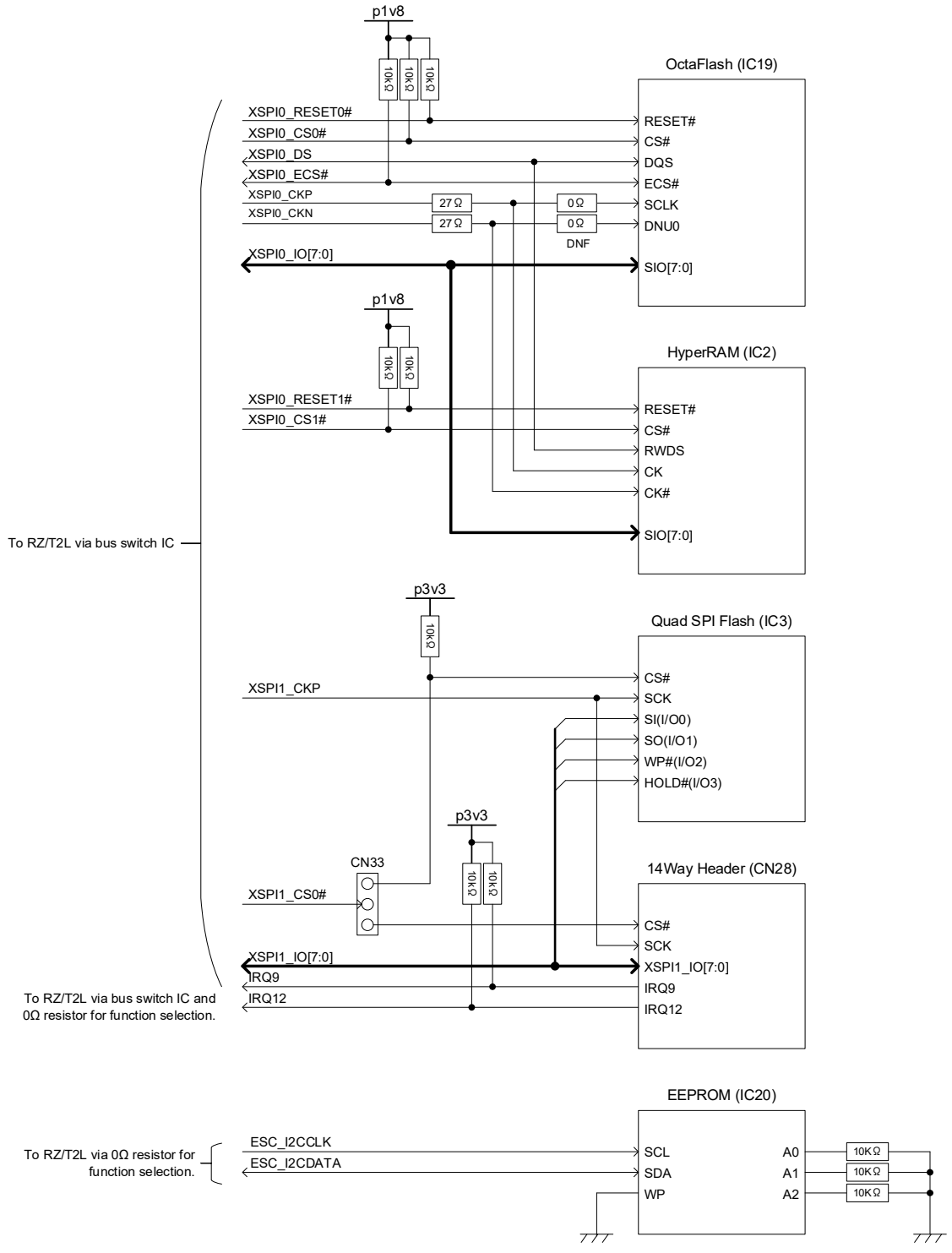


Figure 7-14 Configuration of Memory Circuits

Table 7-19 List of Memories

Device	Location	Controller	Address Space
OctaFlash (512 Mbits)	IC19	XSPI0_CS0	60000000h to 63FFFFFFh (64 Mbytes)
HyperRAM (64 Mbits)	IC2	XSPI0_CS1	64000000h to 647FFFFFh (8 Mbytes)
Quad SPI flash memory (128 Mbits)	IC3	XSPI1_CS0*	68000000h to 68FFFFFFh (16 Mbytes)
EEPROM (16 Kbits)	IC20	I2C or EtherCAT	—

Note: Also connected to pin header CN28.

Table 7-20 Signal Connections of OctaFlash and HyperRAM

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
XSPI0_RESET0#	Output of CS0 reset for XSPI0	P16_1*	G11	CN32: 2-3, SW4-7: ON
XSPI0_CS0#	CS0 output for XSPI0	P15_7*	H14	CN32: 2-3, SW4-7: ON
XSPI0_DS	DS input/output for XSPI0	P14_4*	K13	CN32: 2-3, SW4-7: ON
XSPI0_ECS#	ECS input for XSPI0	P14_2*	K11	CN32: 2-3, SW4-7: ON
XSPI0_CKP	CKP output for XSPI0	P14_6*	K14	CN32: 2-3, SW4-7: ON
XSPI0_CKN	CKN output for XSPI0	P14_5*	L14	CN32: 2-3, SW4-7: ON
XSPI0_RESET1#	Output of CS1 reset for XSPI0	P16_2*	G13	CN32: 2-3, SW4-7: ON
XSPI0_CS1#	CS1 output for XSPI0	P16_0*	G12	CN32: 2-3, SW4-7: ON
XSPI0_IO7	Input/output of data 7 for XSPI0	P15_6*	H11	CN32: 2-3, SW4-7: ON
XSPI0_IO6	Input/output of data 6 for XSPI0	P15_5*	H12	CN32: 2-3, SW4-7: ON
XSPI0_IO5	Input/output of data 5 for XSPI0	P15_4*	H13	CN32: 2-3, SW4-7: ON
XSPI0_IO4	Input/output of data 4 for XSPI0	P15_3*	J11	CN32: 2-3, SW4-7: ON
XSPI0_IO3	Input/output of data 3 for XSPI0	P15_2*	J14	CN32: 2-3, SW4-7: ON
XSPI0_IO2	Input/output of data 2 for XSPI0	P15_1*	J13	CN32: 2-3, SW4-7: ON
XSPI0_IO1	Input/output of data 1 for XSPI0	P15_0*	J12	CN32: 2-3, SW4-7: ON
XSPI0_IO0	Input/output of data 0 for XSPI0	P14_7*	K12	CN32: 2-3, SW4-7: ON

Note: Connected via the bus switch IC.

Table 7-21 Signal Connections of Quad SPI Flash Memory

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
XSPI1_CS0#	CS0 output for XSPI1	P18_2*	D12	**SW8-9: ON, CN33: 1-2**
XSPI1_CKP	CKP output for XSPI1	P17_7*	E13	**SW8-9: ON**
XSPI1_IO3	Input/output of data 3 for XSPI1	P17_4*	E12	**SW8-9: ON**
XSPI1_IO2	Input/output of data 2 for XSPI1	P17_3*	F13	**SW8-9: ON**
XSPI1_IO1	Input/output of data 1 for XSPI1	P17_0*	F11	**SW8-9: ON**
XSPI1_IO0	Input/output of data 0 for XSPI1	P18_0*	E14	**SW8-9: ON**

Note: Connected via the bus switch IC.

Table 7-22 Signal Connections of EEPROM

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
ESC_I2CCLK	I2CCLK output for EtherCAT	P13_2*	L9	**R324: Fit**
ESC_I2CDATA	I2CDATA input/output for EtherCAT	P13_3*	L10	**R326: Fit**

Note: Connected via a 0-Ω resistor for function selection.

Table 7-23 Signal Connections of SPI Expansion Connector (CN28)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	GROUND	—	—	—
2	IRQ12	P09_7*1, *2	M4	**SW8-7: OFF,** R202: Fit
3	XSPI1_CKP	P17_7*1	E13	**SW8-9: ON**
4	XSPI1_CS0#	P18_2*1	D12	**SW8-9: ON**, CN33: 2-3
5	XSPI1_IO7	P18_6*1	B14	**SW8-9: ON**
6	XSPI1_IO6	P18_5*1	C13	**SW8-9: ON**
7	XSPI1_IO5	P18_4*1	C14	**SW8-9: ON**
8	XSPI1_IO4	P18_3*1	D13	**SW8-9: ON**
9	XSPI1_IO3	P17_4*1	E12	**SW8-9: ON**
10	XSPI1_IO2	P17_3*1	F13	**SW8-9: ON**
11	XSPI1_IO1	P17_0*1	F11	**SW8-9: ON**
12	XSPI1_IO0	P18_0*1	E14	**SW8-9: ON**
13	IRQ9	P08_6*1	M2	**SW8-7: OFF**
14	p3v3	—	—	—

Notes: 1. Connected via the bus switch IC.
2. Connected via a 0-Ω resistor for function selection.

7.15 RS485 Interface

This board is equipped with an RS485 transceiver (IC27) and an RS485 interface connector (CN12). Figure 7-15 shows the configuration of the RS485 interface circuit, Table 7-24 lists the signal connections of the connector, and Table 7-25 lists the ports to be used.

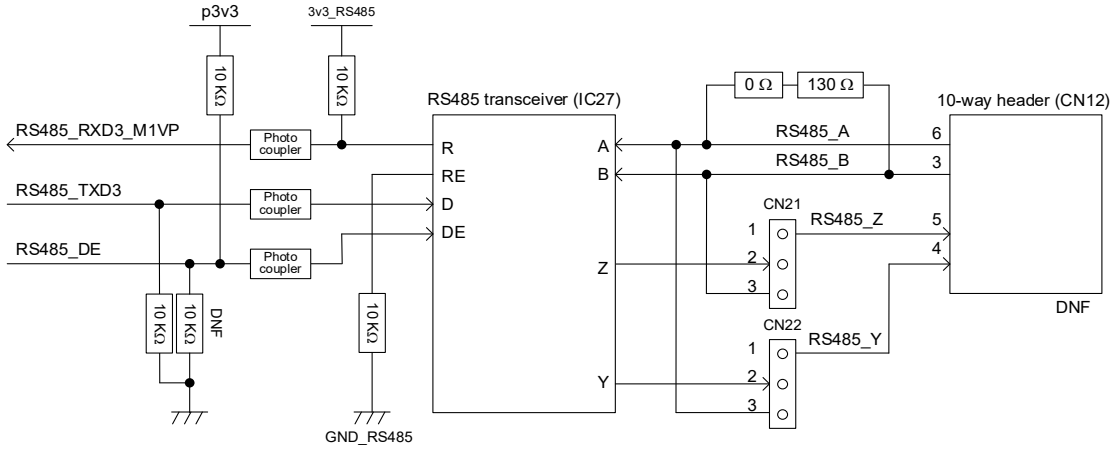


Figure 7-15 Configuration of RS485 Interface Circuit

Table 7-24 Signal Connections of RS485 Interface Connector (CN12)

Pin	Signal Name	Pin	Signal Name
1	NC	2	NC
3	RS485_B	4	RS485_Y
5	RS485_Z	6	RS485_A
7	NC	8	NC
9	NC	10	NC

Table 7-25 Ports Used with the RS485 Interface

Signal Name	Function or Intended Use	MPU		Settings of Configuration Circuits
		Port	Pin	
RS485_RXD3_M1VP	Reception of SCI3 data	P17_7*1, *2	E13	SW8-9: OFF, **R245: Fit**
RS485_DE3	SCI3 driver enable signal	P18_3*1, *2	D13	SW8-9: OFF, **R88: Fit**
RS485_TXD3	Transmission of SCI3 data	P18_0*1, *2	E14	SW8-9: OFF, **R334: Fit**

Notes: 1. Connected via the bus switch IC.
2. Connected via a 0-Ω resistor for function selection.

7.16 Serial Host Interface

This board is equipped with a connector (CN27) for the serial host interface, and the serial host interface of the RZ/T2L can be evaluated by connecting the connector to an external host CPU. Table 7-26 lists the signal connections of the serial host interface connector (CN27).

Table 7-26 Signal Connections of Serial Host Interface Connector (CN27)

Pin	Signal Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	GROUND	—	—	—
2	I2C_SCL1_HSPI_INT#_M2TOG_MCLK0_BSC_D00	P21_1*1	A8	**SW8-10: OFF**
3	P18_6	P18_6	B14	—
4	I2C_SDA1_HSP1_CS#_MDAT0_BSC_D01	P21_2*1	B8	**SW8-10: OFF**
5	HSPI_IO7_M2POE_BSC_D08	P22_1*1, *2	D6	**SW8-10: OFF, SW8-4: ON**
6	HSPI_IO6_MDAT3_BSC_D07	P22_0*1	C6	**SW8-10: OFF**
7	HSPI_IO5_MCLK3_BSC_D06	P21_7*1	B6	**SW8-10: OFF**
8	ESC_LINKACT0_HSPI_IO4_BSC_D05	P21_6*1	A7	**SW8-10: OFF**
9	HSPI_IO3_MCLK2_BSC_D04	P21_5*1	B7	**SW8-10: OFF**
10	ESC_LED0_RUN_HSPI_IO2_BSC_D02	P21_3*1	C7	**SW8-10: OFF**
11	P18_4	P18_4	C14	—
12	P18_5	P18_5	C13	—
13	MBX_HINT#_MDAT1_BSC_D03	P21_4*1	D7	**SW8-10: OFF**
14	p3v3	—	—	—

Notes: 1. Connected via the bus switch IC.
2. Connected via DIP switch SW8.

7.17 Pin Headers

In addition to the aforementioned circuits, this board is equipped with two pin headers CN1 and CN3. Table 7-27 and Table 7-28 list the signal connections of the pin headers.

Table 7-27 Signal Connections of Pin Header (CN1)

Pin	Function Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	GROUND	—	—	—
2	ENCIFCK1	P09_6*2	P2	**SW8-7: OFF**
3	ENCIFOE1	P09_7*1, *2	M4	**SW8-7: OFF, R201: Fit**
	DE3	P18_3*1, *2	D13	SW8-9: OFF, R90: Fit
4	ENCIFDO1	P10_0*1, *2	N4	**SW8-7: OFF, R332: Fit**
	TXD3	P18_0*1, *2	E14	SW8-9: OFF, R333: Fit
5	ENCIFDI1	P10_1*1, *2	L5	**SW8-7: OFF, R339: Fit**
	RXD3	P17_7*1, *2	E13	SW8-9: OFF, R340: Fit
6	DUEI1	P06_7*2	J1	**SW8-8: OFF**
7	GROUND	—	—	—
8	SI1#/HDSL1_CLK1	P07_1*2	K4	**SW8-8: OFF**
9	TST_OUT1	P07_0*2	K1	**SW8-8: OFF**
10	HDSL1_LINK	P05_5*3	G3	**SW7-3: ON**
11	HDSL1_SMPL	P06_6*2	J3	**SW8-8: OFF**
12	HDSL1_SEL1	P07_2*2	K2	**SW8-8: OFF**
13	HDSL1_MISO1	P07_3*2	K3	**SW8-8: OFF**
14	HDSL1_MOSI1	P08_4*2	L3	**SW8-7: OFF**
15	GROUND	—	—	—
16	HDSL1_CLK2	P17_4*2	E12	SW8-9: OFF
17	HDSL1_SEL2	P09_3*2	N2	**SW8-7: OFF**
18	HDSL1_MISO2	P09_4*2	L4	**SW8-7: OFF**
19	HDSL1_MOSI2	P09_5*2	N3	**SW8-7: OFF**
20	3.3 V	—	—	—

Notes: 1. Connected via a 0-Ω resistor for function selection.
2. Connected via the bus switch IC.
3. Connected via DIP switch SW7.

Table 7-28 Signal Connections of Pin Header (CN3)

Pin	Function Name	MPU		Settings of Configuration Circuits
		Port	Pin	
1	5V	—	—	—
2	3.3V	—	—	—
3	MCLK5	P24_1*2	A4	CN17: 1-2, SW4-6: OFF
4	MDAT5	P24_2*2	C5	CN17: 1-2, SW4-6: OFF
5	MCLK4	P13_2*1	L9	R325: Fit
6	MDAT4	P13_3*1	L10	R327: Fit
7	MCLK3	P21_7*2	B6	**SW8-10: OFF**
8	MDAT3	P22_0*2	C6	**SW8-10: OFF**
9	GROUND	—	—	—
10	GROUND	—	—	—
11	5V	—	—	—
12	3.3V	—	—	—
13	MCLK2	P21_5*2	B7	**SW8-10: OFF**
14	MDAT2	P15_6*2	H11	**CN32: 1-2, SW4-7: OFF**
15	MCLK1	P22_2*2	A6	**SW8-10: OFF**
16	MDAT1	P21_4*2	D7	**SW8-10: OFF**
17	MCLK0	P21_1*2	A8	**SW8-10: OFF**
18	MDAT0	P21_2*2	B8	**SW8-10: OFF**
19	GROUND	—	—	—
20	GROUND	—	—	—

Notes: 1. Connected via a 0-Ω resistor for function selection.
2. Connected via the bus switch IC.

7.18 Application Headers

This board is equipped with five application headers JA1-A, JA2-A, JA3-A, JA5-A, and JA6. They are not mounted at the time of shipment.

Table 7-29 to Table 7-33 list the signal connections of the application headers.

Table 7-29 Signal Connections of Application Header (JA1-A)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	5V	CON_5V	—	—	—
2	0V	GROUND	—	—	—
3	3.3V	CON_3V3	—	—	—
4	0V	GROUND	—	—	—
5	AVCC	CON_AVCC	—	—	—
6	AVSS	CON_AVSS	—	—	—
7	AVREF	CON_AVREF	—	—	—
8	ADTRG	ADTRG1#	P18_1*3	D14	SW7-8: ON
9	ADC0	ADC_AN000	—	A13	—
10	ADC1	ADC_AN001	—	B12	—
11	ADC2	ADC_AN002	—	A12	—
12	ADC3	ADC_AN003	—	C11	—
13	DAC0	NC	NC	NC	—
14	DAC1	NC	NC	NC	—
15	IO_0	P01_1_JA1	P01_1*1	C3	CN17: 1-2, SW4-6: OFF
16	IO_1	P14_1_JA1_DIP_SW3_18	P14_1	M14	—
17	IO_2	P14_3_JA1_DIP_SW4_18	P14_3	L13	—
18	IO_3	P14_4_JA1	P14_4*1	K13	**CN32: 1-2, SW4-7: OFF**
19	IO_4	TXD0_P16_0_JA1	P16_0*1	G12	**CN32: 1-2, SW4-7: OFF**
20	IO_5	RXD0_P16_1_JA1	P16_1*1	G11	**CN32: 1-2, SW4-7: OFF**
21	IO_6	P23_7_JA1	P23_7*1	B5	CN17: 1-2, SW4-6: OFF
22	IO_7	RXD1_P24_0_JA1	P24_0*1	D5	CN17: 1-2, SW4-6: OFF
23	IRQd/IRQAEC/M2_HSIN0	SW1_IRQ6	P14_2*1	K11	**CN32: 1-2, SW4-7: OFF**
24	IIC_EX	NC	NC	NC	—
25	IIC_SDA	ESC_I2CDATA	P13_3*2	L10	**R326: Fit**
26	IIC_SCL	ESC_I2CCLK	P13_2*2	L9	**R324: Fit**

Notes: 1. Connected via the bus switch IC.
2. Connected via a 0-Ω resistor for function selection.
3. Connected via DIP switch SW7.

Table 7-30 Signal Connections of Application Header (JA2-A)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	RESET	RESET#	—	N5	—
2	EXTAL	CON_EXTAL	—	N6	R252: DNF, E46: Short-circuit
3	NMI	SW_NMI_NMI_JA2	P16_2*1	G13	**CN32: 1-2, SW4-7: OFF**
4	Vss1	GROUND	—	—	—
5	WDT_OVF	NC	NC	NC	—
6	SCIaTX	CAS#_TXD5	P15_1*1	J13	**CN32: 1-2, SW4-7: OFF**
7	IRQa/WKUP/M1_HSIN0	IRQ1	P07_4*2	L7	R200: Fit
8	SCIaRX	CKE_RXD5	P15_0*1	J12	**CN32: 1-2, SW4-7: OFF**
9	IRQb/M1_HSIN1	SW2_IRQ7	P16_3	G14	—
10	SCIaCK	A22_SCK5	P14_7*1	K12	**CN32: 1-2, SW4-7: OFF**
11	M1_UD	NC	NC	NC	—
12	CTSaRTSa	RAS#_CTS5#/RTS5#	P15_2*1	J14	**CN32: 1-2, SW4-7: OFF**
13	M1_UP	M1_UP	P17_6*3	F12	SW7-5: ON
14	M1_UN	M1_UN	P18_1*3	D14	SW7-9: ON
15	M1_VP	JA2_15PIN	P17_7*1, *2	E13	SW8-9: OFF, **R341: Fit**
16	M1_VN	JA2_16PIN	P18_0*1, *2	E14	SW8-9: OFF, R335: Fit
			P18_2*1, *2	D12	SW8-9: OFF, **R337: Fit**
17	M1_WP	JA2_17PIN	P18_2*1, *2	D12	SW8-9: OFF, R338: Fit
			P18_0*1, *2	E14	SW8-9: OFF, R336: Fit
18	M1_WN	MB_RST#_M1WN_DE3	P18_3*1	D13	SW8-9: OFF
19	TimerOut0	NC	NC	NC	—
20	TimerOut1	NC	NC	NC	—
21	TimerIn0	NC	NC	NC	—
22	TimerIn1	NC	NC	NC	—
23	IRQc/M1_EncZ/1_HSIN2	M1_ENCZ	P01_6*2	C2	**R195: Fit**
24	M1_POE	M1_POE	P17_3*1	F13	SW8-9: OFF
25	M1_TRCCLK	M1_TRCCLK_33	P13_5	L12	—
26	M1_TRDCLK	M1_TRDCLK_33	P13_6	M13	—

Notes: 1. Connected via the bus switch IC.
2. Connected via a 0-Ω resistor for function selection.
3. Connected via DIP switch SW7.

Table 7-31 Signal Connections of Application Header (JA3-A)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	A0	BSC_A00_33_HDSL1_MISO1	P07_3*1	K3	**SW8-8: OFF**
2	A1	BSC_A01_HDSL1_SEL1	P07_2*1	K2	**SW8-8: OFF**
3	A2	BSC_A02_SI1#/HDSL1_CLK1	P07_1*1	K4	**SW8-8: OFF**
4	A3	BSC_A03_TST_OUT1	P07_0*1	K1	**SW8-8: OFF**
5	A4	BSC_A04_DUEI1	P06_7*1	J1	**SW8-8: OFF**
6	A5	BSC_A05_HDSL1_SMPL	P06_6*1	J3	**SW8-8: OFF**
7	A6	BSC_A06	P06_5*1	J2	**SW8-8: OFF**
8	A7	BSC_A07	P06_4*1	H1	**SW8-8: OFF**
9	A8	BSC_A08	P06_3*1	J4	**SW8-8: OFF**
10	A9	BSC_A09	P06_2*1	H2	**SW8-8: OFF**
11	A10	BSC_A10	P06_1*1	H3	**SW8-8: OFF**
12	A11	BSC_A11_P05_7_SPI	P05_7*1	H4	**SW8-8: OFF**
13	A12	BSC_A12_P06_0_SPI	P06_0*1	G1	**SW8-8: OFF**
14	A13	BSC_A13_P05_6_SPI	P05_6*1	G2	**SW8-8: OFF**
15	A14	BSC_A14	P05_5*3	G3	SW7-2: ON
16	A15	BSC_A15	P02_3*3	D1	SW6-7: ON
17	D0	I2C_SCL1_HSPI_INT#_M2TOG_MCLK0_BSC_D00	P21_1*1	A8	**SW8-10: OFF**
18	D1	I2C_SDA1_HSP1_CS#_MDAT0_BSC_D01	P21_2*1	B8	**SW8-10: OFF**
19	D2	ESC_LED0_RUN_HSPI_IO2_BSC_D02	P21_3*1	C7	**SW8-10: OFF**
20	D3	MBX_HINT#_MDAT1_BSC_D03	P21_4*1	D7	**SW8-10: OFF**
21	D4	HSPI_IO3_MCLK2_BSC_D04	P21_5*1	B7	**SW8-10: OFF**
22	D5	ESC_LINKACT0_HSPI_IO4_BSC_D05	P21_6*1	A7	**SW8-10: OFF**
23	D6	HSPI_IO5_MCLK3_BSC_D06	P21_7*1	B6	**SW8-10: OFF**
24	D7	HSPI_IO6_MDAT3_BSC_D07	P22_0*1	C6	**SW8-10: OFF**
25	RDn	RD#_JA3_TXD2_JA6	P00_2*1	C4	CN17: 1-2, SW4-6: OFF
26	WR/SDWE	RTS2_WR#	P00_3*1	A3	CN17: 1-2, SW4-6: OFF
27	CSa	CS5#	P00_6*1	D4	CN17: 1-2, SW4-6: OFF
28	CSb	BSC_CS3#_33	P14_5*1	L14	**CN32: 1-2, SW4-7: OFF**
29	D8	HSPI_IO7_M2POE_BSC_D08	P22_1*1, *3	D6	**SW8-10: OFF, SW8-4: ON**
30	D9	MCLK1_BSC_D09	P22_2*1	A6	**SW8-10: OFF**
31	D10	BSC_D10	P22_3*3	A5	SW8-2: ON
32	D11	BSC_D11	P15_3*1	J11	**CN32: 1-2, SW4-7: OFF**
33	D12	BSC_D12	P15_4*1	H13	**CN32: 1-2, SW4-7: OFF**
34	D13	BSC_D13	P15_5*1	H12	**CN32: 1-2, SW4-7: OFF**
35	D14	D14_MDAT2	P15_6*1	H11	**CN32: 1-2, SW4-7: OFF**
36	D15	BSC_D15	P10_4*2	P4	R322: Fit
37	A16	BSC_A16	P02_2*3	E2	SW6-3: ON

38	A17	P02_1_BSC_A17	P02_1	C1	-
39	A18	BSC_A18	P02_0*3	D2	SW5-8: ON
40	A19	BSC_A19	P01_7*3	B1	SW5-4: ON
41	A20	BSC_A20	P01_6*2	C2	R196: Fit
42	A21	BSC_A21	P14_6*1	K14	**CN32: 1-2, SW4-7: OFF**
43	A22	A22_SCK5	P14_7*1	K12	**CN32: 1-2, SW4-7: OFF**
44	SDCLK	BSC_CKIO	P04_1*2	F1	R198: Fit
45	CSc/Wait	BSC_WAIT#	P13_4*2	M12	R329: Fit
46	ALE/SDCKE	JA3_46PIN	P15_0*1, *2	J12	**CN32: 1-2, SW4-7: OFF, R330: Fit**
			P01_3*1, *2	A2	CN17: 1-2, SW4-6: OFF, R331: Fit
47	HWRn/DQMH	WE#1_DQMLU_P01_4_UART	P01_4*1	E4	CN17: 1-2, SW4-6: OFF
48	LWRn/DQML	BSC_DQMLL_WE0#	P01_5*1	B2	CN17: 1-2, SW4-6: OFF
49	CAS	CAS#_TXD5	P15_1*1	J13	**CN32: 1-2, SW4-7: OFF**
50	RAS	RAS#_CTS5#/RTS5#	P15_2*1	J14	**CN32: 1-2, SW4-7: OFF**

Notes: 1. Connected via the bus switch IC.
2. Connected via a 0-Ω resistor for function selection.
3. Connected via DIP switches SW5, SW6, SW7, and SW8.

Table 7-32 Signal Connections of Application Header (JA5-A)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	ADC4	ADC_AN100	—	A11	—
2	ADC5	ADC_AN101	—	B11	—
3	ADC6	ADC_AN102	—	C10	—
4	ADC7	ADC_AN103	—	B10	—
5	CAN1TX	CAN_TX0_JA5	P02_2*2	E2	SW6-4: ON
6	CAN1RX	CAN_RX0_JA5	P01_7*2	B1	SW5-5: ON
7	CAN2TX	CAN_TX1_JA5	P02_0*2	D2	**SW5-9: ON**
8	CAN2RX	CAN_RX1_JA5	P02_3*2	D1	**SW6-8: ON**
9	IRQe/M2_EncZ/M2HSIN1	M2ENCZ_RXD0_JA6	P10_3*1	P3	**SW8-7: OFF**
10	IRQf/M2_HSIN2	NC	NC	NC	—
11	M2_UD	NC	NC	NC	—
12	M2_Uin	NC	NC	NC	—
13	M2_Vin	NC	NC	NC	—
14	M2_Win	NC	NC	NC	—
15	M2_Toggle	I2C_SCL1_HSPI_INT#_M2TOG_MCLK0_BSC_D00	P21_1*1	A8	**SW8-10: OFF**
16	M2_POE	HSPI_IO7_M2POE_BSC_D08	P22_1*1, *2	D6	**SW8-10: OFF, SW8-4: ON**
17	M2_TRCCLK	M2_MTCLKC	P13_7*3	L11	—
18	M2_TRDCLK	M2_TRDCLK	P14_0*3	N14	—
19	M2_UP	RXD2_M2UP	P08_5*1	L2	**SW8-7: OFF**
20	M2_Un	TXD2_M2UN	P08_7*1	M1	**SW8-7: OFF**
21	M2_VP	M2_VP	P09_0*1	K5	**SW8-7: OFF**
22	M2_Vn	M2_VN	P09_2*1	N1	**SW8-7: OFF**
23	M2_WP	M2_WP	P09_1*1	M3	**SW8-7: OFF**
24	M2_Wn	M2WN_HDSL1_SEL2	P09_3*1	N2	**SW8-7: OFF**

Notes: 1. Connected via the bus switch IC.
2. Connected via DIP switches SW5, SW6, and SW8.
3. Connected via the level shifter IC.

Table 7-33 Signal Connections of Application Header (JA6)

Pin	Function Name	Signal Name	MPU		Settings of Configuration Circuits
			Port	Pin	
1	DREQ	DREQ_HDSL1_MOSI2	P09_5*1	N3	**SW8-7: OFF**
2	DACK	DACK_ENCIFOE1_IRQ12	P09_7*1	M4	**SW8-7: OFF**
3	TEND	TEND	P15_7*1	H14	**CN32: 1-2, SW4-7: OFF**
4	STBYn	NC	NC	NC	—
5	RS232TX	NC	NC	NC	—
6	RS232RX	NC	NC	NC	—
7	SCIbRX	RXD2	P00_1*1	B4	CN17: 1-2, SW4-6: OFF
8	SCIbTX	RD#_JA3_TXD2_JA6	P00_2*1	C4	CN17: 1-2, SW4-6: OFF
9	SCIcTX	TXD0_JA6	P10_2*1	M5	**SW8-7: OFF**
10	SCIbCK	SCK2	P00_0*1	E5	CN17: 1-2, SW4-6: OFF
11	SCIcCK	SCK0	P10_4*2	P4	R323: Fit
12	SCIcRX	M2ENCZ_RXD0_JA6	P10_3*1	P3	**SW8-7: OFF**
13	M1_Toggle	M1TOG_HDSL1_MOSI1	P08_4*1	L3	**SW8-7: OFF**
14	M1_Uin	MTIOC5U	P18_4*1	C14	SW8-9: OFF
15	M1_Vin	MTIOC5V	P18_5*1	C13	SW8-9: OFF
16	M1_Win	MTIOC5W	P18_6*1	B14	SW8-9: OFF
17	EXT_USB_VBUS	NC	NC	NC	—
18	Reserved	NC	NC	NC	—
19	EXT_USB_BATT	NC	NC	NC	—
20	Reserved	NC	NC	NC	—
21	EXT_USB_CHG	NC	NC	NC	—
22	Reserved	NC	NC	NC	—
23	Unregulated_VCC	NC	NC	NC	—
24	Vss	GROUND	—	—	—

Notes: 1. Connected via the bus switch IC.
2. Connected via a 0-Ω resistor for function selection.

8. Developing Code

8.1 Overview

The following methods for debugging code for this device are available.

- Connect the CPU board to a PC via J-Link® OB, which is a development tool from Segger and mounted on the CPU board.
- Connect the CPU board to a PC via an emulator from a given company.

For more details on individual emulators, refer to the Web sites of the manufacturers.

8.2 Supported Modes

This CPU board supports a variety of boot modes. The possible mode settings are shown in section 6.2.1. For detailed information on the microprocessor, such as operating modes and registers, refer to the RZ/T2L Group User's Manual: Hardware.

Mode settings should only be changed while the power is turned off to avoid causing damage to the microprocessor.

8.3 Address Spaces

For details on the usable address spaces determined by the operating mode of the microprocessor, refer to the RZ/T2L Group User's Manual: Hardware.

9. Precautions for use

9.1 Product Restrictions

This board has restrictions shown in Table 9-1. Whether your board has the restrictions or not can be identified by a control number. The control number is written on a part number sticker shown in Fig. 9-1.

Table 9-1 Restriction of RSK+RZT2L

No.	Control Number	Title	Restriction Overview
1	No Control Number	Restriction on RZ/T2L mode setting	When the signal function selection switch SW8-8 is set to ON, the MD2 to MD0 are set to "L" regardless of the settings of the mode setting switches SW4-1 to SW4-3.

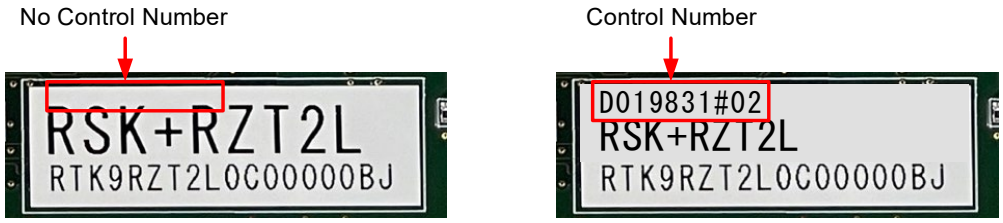


Figure 9-1 Part Number Sticker (Affixed to Soldered Side)

9.1.1 Product Restrictions 1, Restriction on RZ/T2L mode setting

Content

When a reset is released with setting the signal function selection switch SW8-8 to ON (ETH1-related signals are selected by a bus switch IC41) to use EtherCAT Port1 (ETH1), the MD2 to MD0 are ”L" regardless of the settings of the mode setting switches SW4-1 to SW4-3 and RZ/T2L boots in xSPI0 boot mode (x1 boot serial flash).

Workaround

When using EtherCAT Port1 (ETH1) with a boot mode except xSPI0 boot mode (x1 boot serial flash), refer to Table 9−2 and implement one of the following workarounds (1) to (3).

Table 9-2 Workaround for each boot mode

MD[2:0]	Boot Mode	Workaround	Remark
0 (L,L,L)	xSPI0 boot mode (x1 boot serial flash)	Unnecessary*1	
1 (L,L,H)	xSPI0 (x8 boot serial flash)	Incompatible*2	
2 (L,H,L)	16bit bus boot mode (NOR flash)	Incompatible*2	
3 (L,H,H)	Serial host interface boot mode	(2) or (3)	
4 (H,L,L)	xSPI1 boot mode (x1 boot serial flash)	(1) or (3)	(1) is impossible to be applied when a debugger is not connected
5 (H,L,H)	SCI (UART) boot mode	(2) or (3)	
6 (H,H,L)	USB boot mode	(2) or (3)	

Notes: 1. No workaround is required for this boot mode.
2. This boot mode cannot be used with this board.

(1) Perform the following steps using the debugger
   a. Start the debugger with SW8-8 turned OFF and download a program.
   b. Change SW8-8 to ON before running the program.
   d. Run the program.
   Also see "Appendix. How to Debug FSP Project with Flash Boot Mode" in a document R01AN6434EJXXXX.
(2) Boot with SW8-8 turned OFF, and change SW8-8 to ON while waiting to receive a program sent from the PC.
(3) Replace resistors R27, R29, and R30 with 1kΩ

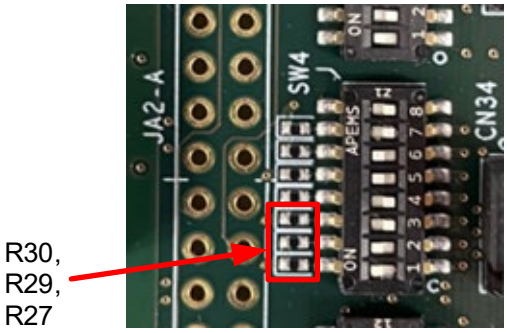


Figure 9-2 Mounting position of resistors R27, R29, and R30

10. Additional Information

Technical Support

For details on the RZ/T2L microprocessors, refer to the RZ/T2L Group User's Manual: Hardware.

Online technical support and information are available from this Web page: https://www.renesas.com/.

Technical Contact Details

America: techsupport.america@renesas.com

Europe: https://www.renesas.com/en-eu/support/contact.html

Global & Japan: https://www.renesas.com/support/contact.html

General information on Renesas microprocessors can be found on the Renesas website at: https://www.renesas.com/

Design and Manufacturing Information

The design and manufacturing information for this board "Renesas Starter Kit+ for RZ/T2L Design Package" is available from https://www.renesas.com/rskrzt2l.

- File Name：rskplus-rzt2l-v2-designpackage.zip
- Connects

Table 10-1 Renesas Starter Kit+ for RZ/T2L Design Package Contents

File Type	Content	File/Folder Name
File (txt)	Readme	Readme for schematic.txt
File (PDF)	Schematics	rskplus-rzt2l-rev1.10-schematic.pdf
File (PDF)	Mechanical Drawing	rskplus-rzt2l-rev1.00-mechdwg.pdf
File (PDF)	3D Drawing	rskplus-rzt2l-rev1.00-3d.pdf
File (xlsx)	BOM	rskplus-rzt2l-MP_rev1.10-BOM.xlsx
Folder	Manufacturing Files	rskplus-rzt2l-Manufacturing Files
Folder	Design Files	rskplus-rzt2l-Design Files - Cadence

Trademarks

Grove® is a registered trademark of Seed Technologies Corp. Ltd.

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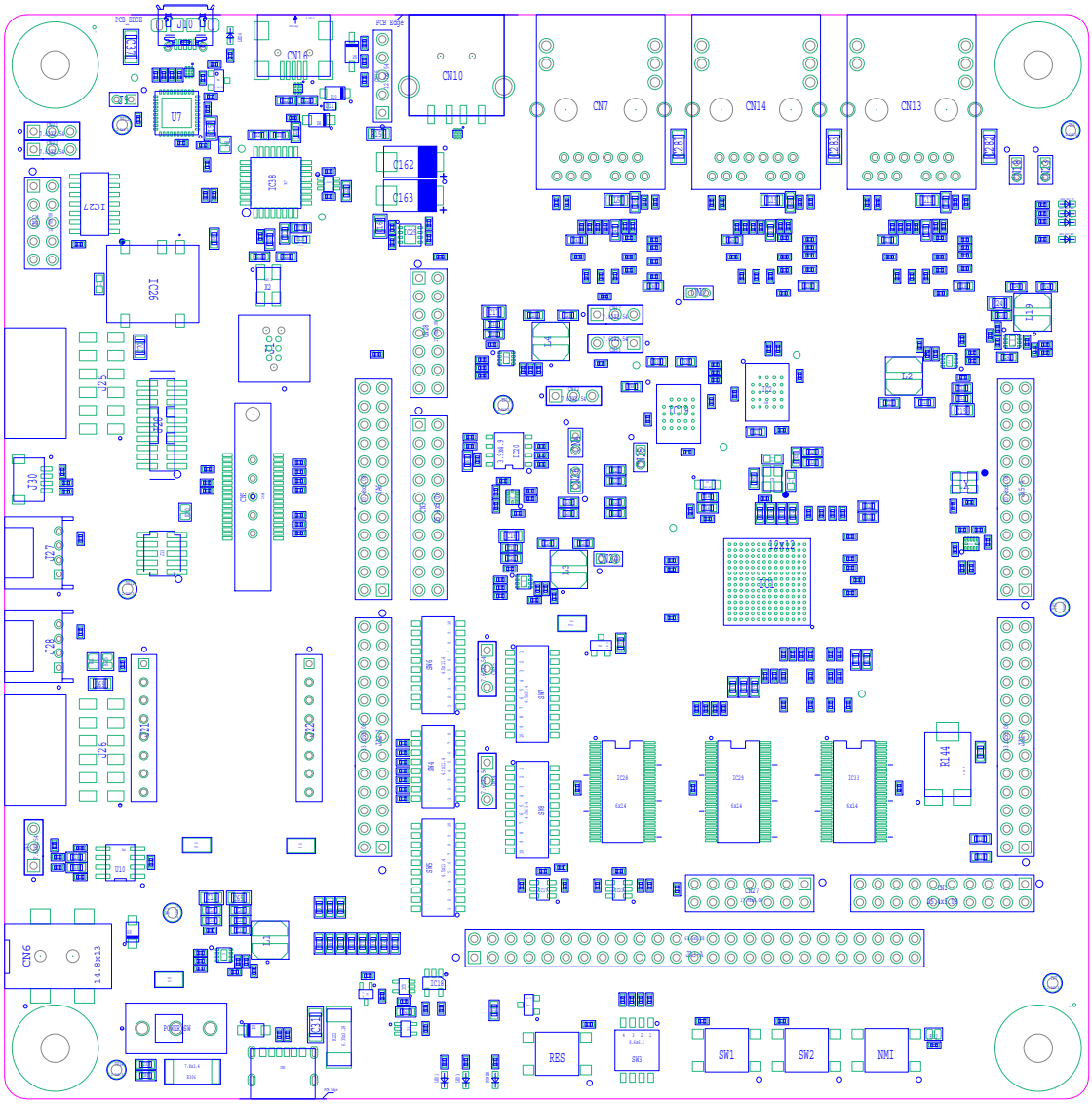
11. Appendix

The arrangements of individual components on this board are shown in this appendix.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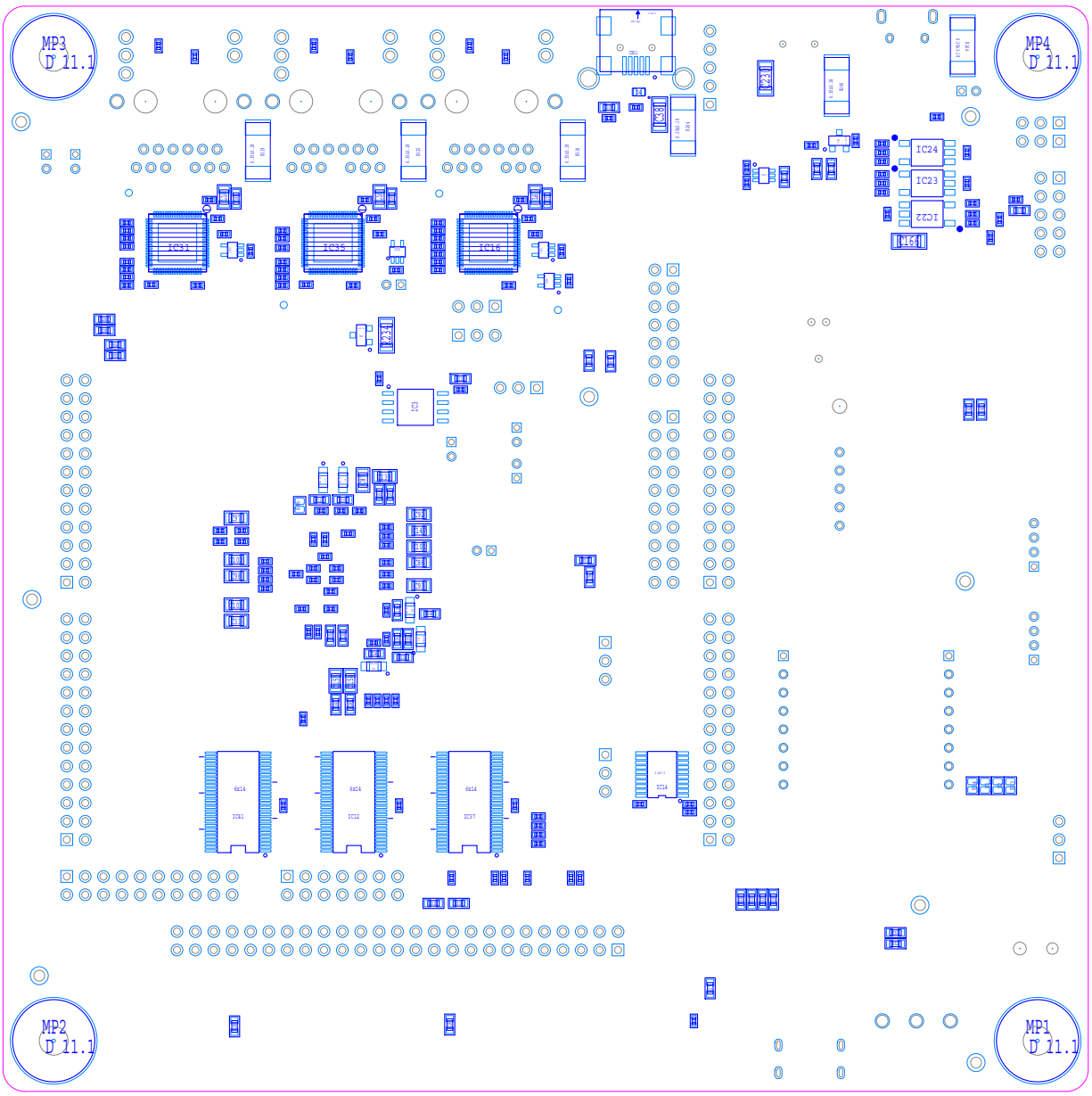
CN14
CN13
CN10
CN16
CN6
SW1
SW2
NMI
RBS
C162
C163
U7


MP3
D 11.1
MP4
D 11.1
MP2
D 11.1
MP1
D 11.1
IC24
IC23
IC22
IC31
IC35
IC16
IC1
IC41
IC12
IC17
IC14

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Rev.	Date	Description	
		Page	Summary
1.00	Dec.16.22	—	First edition issued
1.10	Mar.29.23	44 88	- Note 3 added to Table 6-1 - Added 9. Precautions for use, and moved the chapter numbers accordingly
1.20	Apr.28.23	5 90	- Deleted descriptions related to Schematics from the "How to use this manual" table. - Added Design and Manufacturing Information to 10 Additional Information
1.21	Jul.10.24	15	- Corrected typographical error in Figure 3-2

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