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April 1st, 2010
Renesas Electronics Corporation

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User's Manual

R0P3219TR001MRK

General Infomation Manual

Renesas M32192 µT-Engine Board Set

Renesas Electronics
www.renesas.com

Rev.1.00 2005.10

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Preface

Thank you very much for purchasing the R0P3219TR001MRK (hereafter, M32192 µT-Engine), the µT-Engine board set incorporating the Renesas M32192.
The M32192 µT-Engine is a board set for software evaluation that incorporates the 32-bit microcontroller M32192 made by Renesas Technology. This product is manufactured to µT-Engine specification.
This manual describes mainly specifications of the M32192 µT-Engine and how to set it up. For information on the software supplied with it, please refer to on-line manuals for each product. The latest versions of the related documents are available from the Renesas Technology Corp Web site (http://www.renesas.com/).

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Definitions of Signal Words

In both the user's manual and on the product itself, several icons are used to insure proper handling of this product and also to prevent injuries to you or other persons, or damage to your properties.
This chapter describes the precautions which should be taken in order to use this product safely and properly. Be sure to read this chapter before using this product.

⚠	This symbol represents a warning about safety. It is used to arouse caution about a potential danger that will possibly inflict an injury on persons. To avoid a possible injury or death, please be sure to observe the safety message that follows this symbol.
⚠ **DANGER**	**DANGER** indicates an imminently dangerous situation that will cause death or heavy wound unless it is avoided. However, there are no instances of such danger for the product presented in this user's manual.
⚠ **WARNING**	**WARNING** indicates a potentially dangerous situation that will cause death or heavy wound unless it is avoided.
⚠ **CAUTION**	**CAUTION** indicates a potentially dangerous situation that will cause a slight injury or a medium-degree injury unless it is avoided.
CAUTION	**CAUTION** with no safety warning symbols attached indicates a potentially dangerous situation that will cause property damage unless it is avoided.
IMPORTANT	This is used in operation procedures or explanatory descriptions to convey exceptional conditions or cautions to the user.

In addition to the five above, the following are also used as appropriate.

△means WARNING or CAUTION.
Example:  CAUTION AGAINST AN ELECTRIC SHOCK

⃠means PROHIBITION.
Example:  DISASSEMBLY PROHIBITED

●means A FORCIBLE ACTION.
Example:  UNPLUG THE POWER CABLE FROM THE RECEPTACLE.

⚠ WARNING

Warnings for AC Power Supply:

- If the attached AC power cable does not fit the receptacle, do not alter the AC power cable and do not plug it forcibly. Failure to comply may cause electric shock and/or fire.
- The AC adapter included this product is designed to be used in Japan. Do not use the adapter outside Japan.
- If this product is plugged into the same AC outlet that has another equipment connected to it, make sure the power supply voltage and power supply current are not overloaded. The rated voltage and current of this product is shown on its AC adapter nameplate.
- Do not connect the included AC adapter to any other product.

- If you smell a strange odor, hear an unusual sound, or see smoke coming from this product, then disconnect power immediately by unplugging the AC power cable from the outlet. Do not use this as it is because of the danger of electric shock and/or fire.

Warnings to Be Taken for This Product:

- Do not disassemble or modify this product. Personal injury due to electric shock may occur if this product is disassembled and modified.
- Make sure nothing falls into the cooling fan on the top panel, especially liquids, metal objects, or anything combustible.

Warning for Installation:

- Do not set this product in water or areas of high humidity. Make sure that the product does not get wet. Spilling water or some other liquid into the product may cause unrepairable damage.
- Please use this product in doors.

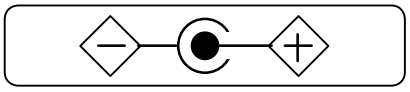
Warning for Use Environment:

- This equipment is to be used in an environment with a maximum ambient temperature of 35°C. Care should be taken that this temperature is not exceeded.

⚠ CAUTION

Cautions for AC Adapter:

- Before installing this equipment or connecting it to other equipment, disconnect the AC power cable from its outlet to prevent injury or accident.
- The DC plug on the included AC adapter has the below polarity.



About the Power-on Sequence:

- Once the power is turned off, wait for about 10 seconds before turning it back on again.

About Handling of the Product:

- Handle the product with caution, taking care not to apply strong mechanical shock to the product by dropping or letting it fall down.
- Do not touch the communication interface connector pins or other connector pins directly with your hand. Static electricity from your body may break down the internal circuit of the product.
- Do not pull the product by the cable connecting to a board in it. Do not hold down a board while you pull the other end of it. The cable may break.
- Do not use inch-sized screws for the product. All of the screws used in it are the ISO type (metric size). When replacing screws, be sure to use the same type of screw that is currently used.

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For user registration, please contact your local distributor.

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1. Overview

1.1 Product Outline

The M32192 µT-Engine is a board set for software evaluation that incorporates the 32-bit microcontroller M32192 made by Renesas Technology. This product is manufactured to µT-Engine specifications.

The CPU board M3T-M32192UT-CPU can be connected to the Renesas µT-Engine extension board by stacking one on top of another, for functional extension of the CPU board.

1.2 System Configuration

Figure 1.2.1 shows an example system configuration of the M32192 µT-Engine.

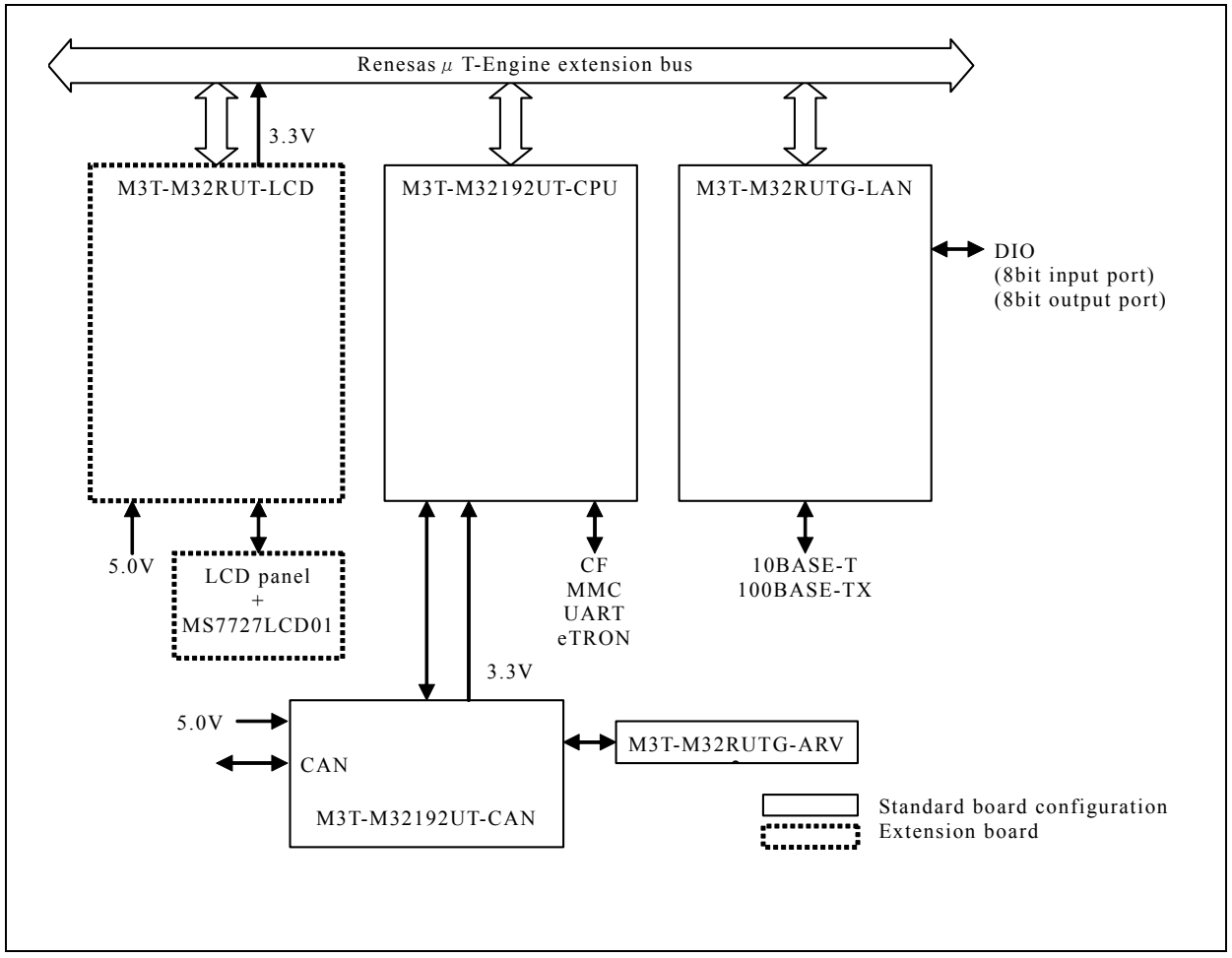


Figure 1.2.1 Example System Configuration of the M32192 µT-Engine

- For the standard board configuration, connect the AC adapter to the CAN board M3T-M32192UT-CAN to supply the power for the system.
- To use the optional extension LCD board M3T-M32RUT-LCD, connect the AC adapter to the M3T-M32RUT-LCD to supply the power for the system.

1.3 Package Components

Table 1.3.1 lists the package components of the M32192 µT-Engine.

Table 1.3.1 Package Components of the M32192 µT- Engine

Item		Quantity
µT-Engine board set	CPU board M3T-M32192UT –CPU	1
	CAN board M3T-M32192UT -CAN	1
	Extension LAN board M3T-M32RUTG-LAN	1
AR camera board M3T-M32RUTG-ARV2		1
JTAG emulator limited version for the M32100T-EZ-E type (Usable for only the R0P3219TR001MRK)		1
AC adapter KSW523 (DC 5.0 V 2.3 A output) * USX315-05 (5.0 V DC, 2.5 A output)		1
Serial cable for RS-232C (D-SUB 9-pin--15-pin)		1
CD-ROM T-kernel, T-monitor, and M32100T-EZ-E interfaces, software, sample programs, and manuals)		1

1.4 External Specifications

1.4.1 CPU Board

Table 1.4.1 lists external specifications of the M3T-M32192UT-CPU.

Table 1.4.1 External Specifications of the M3T-M32192UT-CPU

Item	Description
CPU	M32192F8VWG made by Renesas - Input clock: 20 MHz - CPU operating clock: 160 MHz - Bus operating clock: 40 MHz (BCLK) - Internal flash ROM: 1 MB - Internal RAM: 176 KB - Package: 175-pin FBGA
Memory	BS616LV8010FC-55 made by BSI - External SRAM: 1 MB (4-wait access) - Accessed on only 16-bit bus
	AT25T1024N-10SI-2.7 made by ATMEL - External serial ROM: 128 KB (accessed through the M32192 I/O port) - Used to store the configuration data for the control PLD. - Accessed by operating on the M32192 ports.
Control PLD	APEX20K60EFC144-2 made by ALTERA - Controls the interrupt controller, compact flash, MMC, etc. - PLD logic serially written to the M32192 through I/O ports.
CompactFlash interface	3.3 V compact flash slot: 31 5620 050 716 871 made by Kyocera Elco Co., Ltd. - Card power supply control available.
MMC interface	3.3 V MultiMediaCard slot: 10 5738 009 300 862 made by Kyocera Elco Co., Ltd. - Card power supply control available.
eTRON card interface	eTRON card slot: 00 5036 006 071 862 made by Kyocera Elco Co., Ltd. - Clock supply and reset control available.
Debug serial interface	RS-232C connector for debugging: RMC-EA15MY-OM15-MC1 made by Honda Tsushin Kogyo Co., Ltd. - Connects SIO3 of the M32192 (TxD and RxD only).
Real-time clock	DS1302Z made by DALLAS - Comes with battery backup.
Connector	Extension bus connector: 24 5603 14 0202 861 made by Kyocera Elco Co., Ltd. - Connects the address, data, and bus control signals of the M32192.
	Extension CAN signal connector: FX8C-60P-SV made by Hirose Electric Co., Ltd. - Connects the peripheral ports of the M32192
LED	- LED (2 pcs.)
Switch	- RESET switch (1 pc.) - INT switch (1 pc.) - DIP switch (1 pc., 4-pole)
Power supply	- Designed to operate with the 3.3 V power supply from the extension CAN signal connector or extension bus connector.
External dimensions	- Dimensions: 60 mm x 85 mm - Board assembling form: 8-layered, double-sided assembly

1.4.2 CAN Board

Table 1.4.2 lists external specifications of the M3T-M32192UT-CAN.

Table 1.4.2 External Specifications of the M3T-M32192UT-CAN

Item	Description
Connectors	Extension CAN signal connector: FX8C-60S-SV5 made by Hirose Electric Co., Ltd. - Connects the peripheral ports of the M32192; 2.54-mm-pitch through-holes also available.
	CAN communication connector: 00 8261 0361 10 806 made by Kyocera Elco Co., Ltd. - 3-terminal jumper pin (2 pcs.)
	AR camera board connector: FH12-20S-0.5SH made by Hirose Electric Co., Ltd. - Connected via FFC (Sumi-Card)
Power supply	- Designed to operate with the 5.0 V power supply from the DC power supply input connector (input voltage range: 4.5--5.5 V). EIAJ voltage class 2; outside negative, inside positive - Generates 3.3 V and 5.0 V supply voltages using a regulator.
External dimensions	- Dimensions: 60 mm x 85 mm - Board assembling form: 4-layered, double-sided assembly

1.4.3 AR Camera Board

Table 1.4.3 lists external specifications of the M3T-M32RUTG-ARV2.

Table 1.4.3 External Specifications of the M3T-M32RUTG-ARV2

Item	Description
AR camera	M64286E-800 made by Renesas - Number of effective pixels 640(H) x 480(V), VGA resolution
Connector	AR camera board connector: FH12-20S-0.5SH made by Hirose Electric Co., Ltd. - Connected via FFC (Sumi-Card)
	AR camera module connector: 24FLZ-SM1-TB made by JST
Power supply	- Designed to operate with the 3.3 V power supply from the AR camera board connector. - Generates 2.85 V and 1.8 V supply voltages using a regulator.
External dimensions	- Dimensions: 40 mm x 35 mm - Board assembling form: 4-layered, double-sided assembly

1.4.4 Extension LAN Board

Table 1.4.4 lists external specifications of the M3T-M32RUTG-LAN.

Table 1.4.4 External Specifications of the M3T-M32RUTG-LAN

Item	Description
LAN controller	LAN91C111-NC made by SMSC - 100BASE-TX/10BASE-T compatible, PHY built-in type
Control PLD	- EPM7032AETC44-7 made by ALTERA - Controls extension bus signals.
Connector	- Extension bus connector: 14 5603 14 0202 861 made by Kyocera Elco Co., Ltd.
	- RJ-45 connector with LED: RJHS-5081 made by Amphenol Corporation
	- Connector for SDI emulator: HIF3FC-10PA-2.54DS made by Hirose Electric Co., Ltd.
	- AR camera board connector (unused)
	- Parallel interface connector: HIF3FC-20PA-2.54DS made by Hirose Electric Co., Ltd.
Power supply	- Designed to operate with the 3.3 V power supply from the extension bus connector.
External dimensions	- Dimensions: 60 mm x 85 mm - Board assembling form: 6-layered, double-sided assembly

1.5 Functional Blocks

Figure 1.5.1 shows the functional blocks of the M32192 µT- Engine.

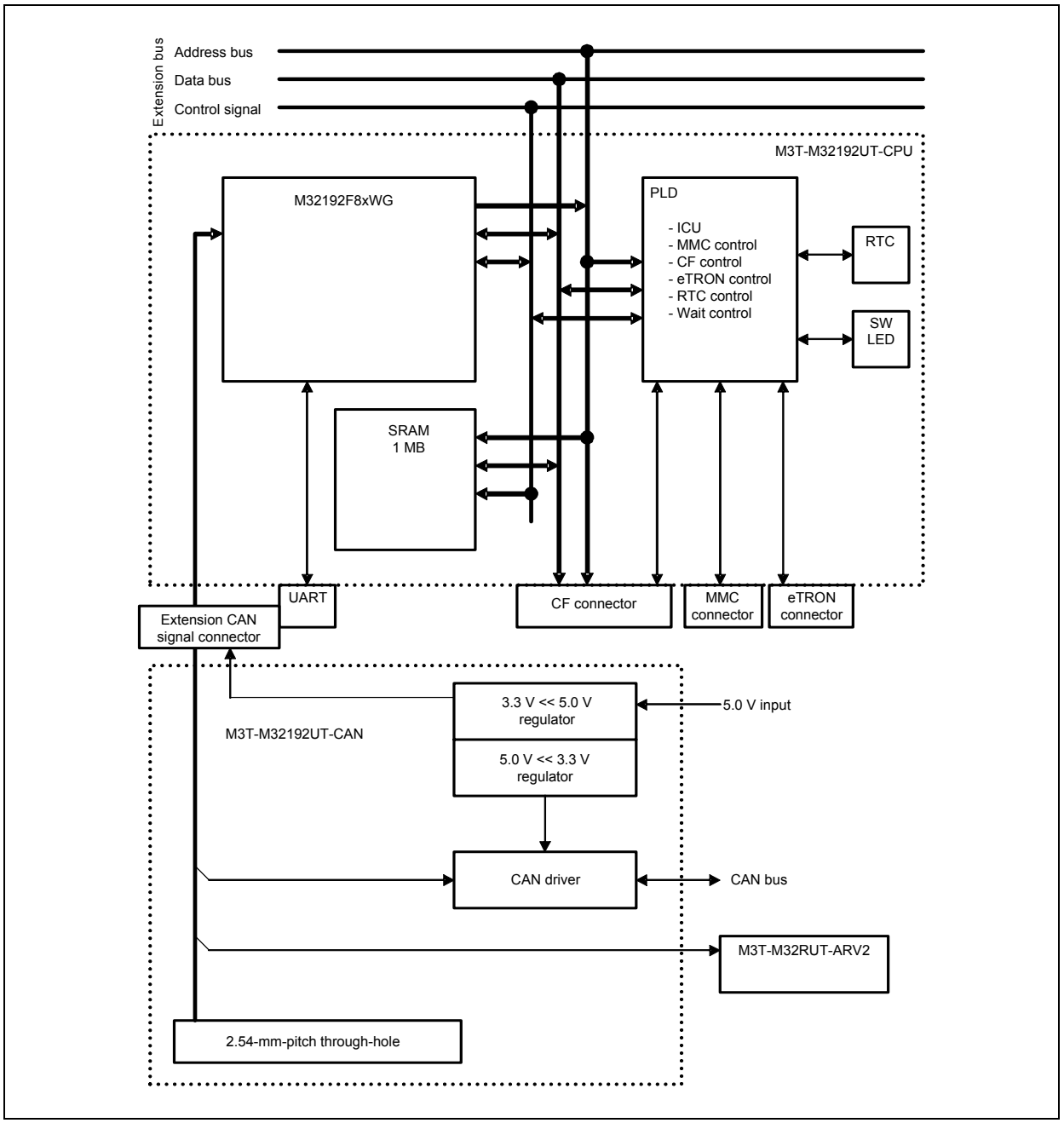


Figure 1.5.1 Functional Blocks of the M32192 µT-Engine

1.6 Address Map

Figure 1.6.1 shows an address map of the M32192 in the M32192 µT- Engine.
For details about the control PLD area, refer to the "3. Functional Description of the Control PLD" on page 30.

M32192 Address	CS	External extension mode
H'0000_0000 : H'000F_FFFF	-	M32192 internal ROM area (1 MB)
H'0010_0000 : H'001F_FFFF	CS0 area (7 MB)	External SRAM area (1 MB)
H'0020_0000 : H'0027_FFFF		Control PLD area (512 KB)
H'0028_0000 : H'002F_FFFF		CompactFlash Area (512 KB)
H'0030_0000 : H'007F_FFFF		Use of this area prohibited
H'0080_0000 : H'0080_3FFF	-	SFR area (16 KB)
H'0080_4000 : H'0082_FFFF		M32192 internal RAM area (176 KB)
H'0083_0000 : H'00FF_FFFF		Use of this area prohibited
H'0100_0000 : H'010F_FFFF	CS1 area (8 MB)	Extension LAN board reserved area (1 MB)
H'0110_0000 : H'011F_FFFF		Extension BlueTooth board reserved area (1 MB)
H'0120_0000 : H'012F_FFFF		Extension FPGA board reserved area (1 MB)
H'0130_0000 : H'013F_FFFF		Extension LCD board reserved area (1 MB)
H'0140_0000 : H'017F_FFFF		LCD controller reserved area (4 MB)
H'0180_0000 : H'01FF_FFFF	-	Use of this area prohibited
H'0200_0000 : H'027F_FFFF	CS2 area (8 MB)	Unused area (8 MB)
H'0280_0000 : H'02FF_FFFF	-	Use of this area prohibited
H'0300_0000 : H'037F_FFFF	CS3 area (8 MB)	Unused area (8 MB)
H'0380_0000 : H'03FF_FFFF	-	Use of this area prohibited

Figure 1.6.1 Address Map of the M32192

2. Functional Specifications

2.1 The CPU

2.1.1 Outline of the M32192

The CPU board M3T-M32192UT-CPU incorporates a 32-bit single-chip RISC microcomputer with internal flash ROM, or the M32192F8VWG, that operates with a clock frequency of up to 160 MHz.

The M32192 is built around Renesas's original high-performance and compact 32-bit RISC core with internal 176-KB RAM and 1-MB flash ROM included, and contains a single-precision FPU fully compliant with the IEEE754 standard to implement exact floating-point arithmetic. With the software to control the operation of the Full-CAN controller (compliant with CAN Specification 2.0B active) and other peripheral functions stored in its large-capacity flash ROM, the CPU can realize high-function/high-performance arithmetics and control, allowing the user to configure applications for any desired embedded equipment easily.

2.1.2 CPU Pin Functions in the M3T-M32192UT-CPU

(1) Dedicated pins

Table 2.1.1 lists the M32192-only pin functions in the M3T-M32192UT-CPU. The pins enclosed in parentheses are available on only the 175-pin FBGA.

Table 2.1.1 M32192-only Pin Functions

Group	Pin name	Use
Power supply	VCCE	Connects to 3.3 V power supply (4 pins)
	VCCER	Connects to 3.3 V power supply (1 pin)
	EXCVCC	Connects to 1µF capacitor (2 pins)
	VCC-BUS	Connects to 3.3 V power supply (2 pins)
	VDDE	Connects to 3.3 V power supply (1 pin)
	EXCVDD	Connects to 1µF capacitor (1 pin)
	VSS	Connects to GND (12 pins)
Clock	XIN	Inputs 20 MHz clock
	XOUT	Open
Reset	RESET#	Inputs reset signal
Mode	MOD0-MOD2	Fixed to external extension mode
	(VDCMODE1)	Fixed low
Flash	FP	Fixed high (no protect)
Interrupt controller	SBI#	Fixed high (unused)
A-D converter	AD0IN0-AD0IN15	Fixed low (unused)
	AVCC0	Connects to 3.3 V
	AVSS0	Connects to GND
	VREF0	Connects to 3.3 V
JTAG/SDI	JTMS	Connects to SDI connector via an extension bus
	JTCK/NBDCLK	Connects to SDI connector via an extension bus
	JTRST	Connects to SDI connector via an extension bus
	JTDI/NBDSYNC#	Connects to SDI connector via an extension bus
	JTDO/NBDEVENT#	Connects to SDI connector via an extension bus
	(SDIVCC)	Open
	(JDBI/TESTJDBI)	Fixed high
	(JTRCLK)	Open
	(JTRSYNC)	Open
	(JEVENT0, JEVENT1)	Open
	(JTRDATA0-JTRDATA7)	Open

(2) Programmable ports

Table 2.1.2 lists the programmable port functions of the M32192 in the M3T-M32192UT-CPU.

Table 2.1.2 Programmable Port Functions of the M32192 (1/2)

Pin name	Used function	Function description	Extension CAN signal	Extension bus
P70/CLKOUT/WR#/BCLK	BCLK	Connect 40 MHz to the external device	Unconnected	Connection/setting not changeable
P124/TCLK0/A9/DD3	A9	Connect the address bus to the external device	Unconnected	Connection/setting not changeable
P125/TCLK1/A10/DD2	A10			
P224/A11/CS2#	A11			
P225/A12/CS3#	A12			
P46/A13/TIN10	A13			
P47/A14/TIN11	A14			
P30/A15/TIN4/DD16	A15			
P31/A16/TIN5/DD17	A16			
P32/A17/TIN6/DD18	A17			
P33/A18/TIN7/DD19	A18			
P34/A19/TIN30/DD20	A19			
P35/A20/TIN31/DD21	A20			
P36/A21/TIN32/DD22	A21			
P37/A22/TIN33/DD23	A22			
P20/A23/DD24	A23			
P21/A24/DD25	A24			
P22/A25/DD26	A25			
P23/A26/DD27	A26			
P24/A27/DD28	A27			
P25/A28/DD29	A28			
P26/A29/DD30	A29			
P27/A30/DD31	A30			
P00/DB0/TO21/DD0	DB0	Connect the data bus to the external device	Unconnected	Connection/setting not changeable
P01/DB1/TO22/DD1	DB1			
P02/DB2/TO23/DD2	DB2			
P03/DB3/TO24/DD3	DB3			
P04/DB4/TO25/DD4	DB4			
P05/DB5/TO26/DD5	DB5			
P06/DB6/TO27/DD6	DB6			
P07/DB7/TO28/DD7	DB7			
P10/DB8/TO29/DD8	DB8			
P11/DB9/TO30/DD9	DB9			
P12/DB10/TO31/DD10	DB10			
P13/DB11/TO32/DD11	DB11			
P14/DB12/TO33/DD12	DB12			
P15/DB13/TO34/DD13	DB13			
P16/DB14/TO35/DD14	DB14			
P17/DB15/TO36/DD15	DB15			
P41/BLW#/BLE#	BLW#	Control the bus via control PLD	Unconnected	Connection/setting not changeable
P42/BHW#/BHE#	BHW#			
P43/RD#	RD#			
P44/CS0#/TIN8	CS0#			
P45/CS1#/TIN9	CS1#			
P71/WAIT#	WAIT#	Control EXREADY# from CF and external bus via control PLD	Unconnected	Connection/setting not changeable

Table 2.1.2 Programmable Port Functions of the M32192 (2/2)

Pin name	Used function	Function description	Extension CAN signal	Extension bus
P150/TIN0/CLKOUT/WR#	TIN0	Input FPGAINT from control PLD	Unconnected	Unconnected
P103/TO11/TIN24	TIN24	Input EXINT from extension bus	Unconnected	Connection/setting not changeable
P132/TIN18/DIN2	TIN18	Input INT2# from extension bus		
P72/HREQ#/TIN27	TIN27	Input INT3# from extension bus		
P61	P61	Connect to serial ROM for control PLD	Unconnected	Unconnected
P62	P62	Connect to CONF_DONE of control PLD		
P63	P63	Connect to CONFIG# of control PLD		
P73/HACK#/TIN26	P73	Connect to DATA0 of control PLD		
P153/TIN3/WAIT#	P153	Connect to STATUS# of control PLD		
P74/RTDTXD/TXD3/NBDD0	TXD3	Connect to debug serial connector	Unconnected	Unconnected
P75/RTDRXD/RXD3/NBDD1	RXD3			
P100/TO8	P100	Connect to eTRON card power control circuit	Unconnected	Unconnected
P82/TXD0/TO26	-	Connect to the extension CAN signal connector and extension bus connector	Connection/setting changeable	Connection/setting changeable
P83/RXD0/TO25	-			
P84/SCLKI0/SCLKO0/TO24	-			
P85/TXD1/TO23	P85			
P86/RXD1/TO22	P86			
P87/SCLKI1/SCLKO1/TO21	P87			
P93/TO16/SCLKI5/SCLKO5	-			
P94/TO17/TXD5/DD15	-			
P95/TO18/RXD5/DD14	-			
P96/TO19/DD13	-			
P97/TO20/DD12	-	Connect to the extension CAN signal connector	Connection/setting changeable	Unconnected
P101/TO9/CRX0	-			
P102/TO10/CTX0	-			
P76/RTDACK/CTX1/NBDD2	-			
P77/RTDCLK/CRX1/NBDD3	-			
P126/TCLK2/CS2#/DD1	-			
P127/TCLK3/CS3#/DD0	-			
P110/TO0/TO29/DD11	-			
P111/TO1/TO30/DD10	-			
P112/TO2/TO31/DD9	-			
P113/TO3/TO32/DD8	-			
P114/TO4/TO33/DD7	DD7			
P115/TO5/TO34/DD6	DD6			
P116/TO6/TO35/DD5	DD5			
P117/TO7/TO36/DD4	DD4			
P104/TO12/TIN25/DD3	DD3			
P105/TO13/SCLKI4/SCLKO4 /DD2	DD2			
P106/TO14/TXD4/DD1	DD1			
P107/TO15/RXD4/DD0	DD0			
P130/TIN16/PWMOFF0/DIN0	DIN0			
P131/TIN17/PWMOFF1/DIN1	DIN1			
P133/TIN19/DIN3	DIN3			
P134/TIN20/TXD3/DIN4	-			
P135/TIN21/RXD3	-			
P136/TIN22/CRX1	CRX1			
P137/TIN23/CTX1	CTX1			
P174/TXD2/TO28	-			
P175/RXD2/TO27	-			
P220/CTX0/HACK#	CTX0			
P221/CRX0/HREQ#	CRX0			

2.1.3 Interrupt Sources

Table 2.1.3 lists the interrupt sources of the M32192 in the M3T-M32192UT-CPU.

Table 2.1.3 Interrupt Sources of the M32192

Interrupt No.	Interrupt request signal	Interrupt source
TIN0	FPGAINT from control PLD	Interrupt request from CF, MMC, eTRON card, or INT_SW
TIN24	EXINT from extension bus	Interrupt request from extension LAN board M3T-M32RUT-LAN
TIN18	INT2# from extension bus	Interrupt request from extension LCD board M3T-M32RUT-LCD
TIN27	INT3# from extension bus	Reserved

Note that SBI#, TIN4(P30)-TIN7(P33), TIN8(P44)-TIN11(P47), and TIN30(P34)-TIN33(P37) cannot be used.

2.1.4 Wait Controller Settings

Table 2.1.4 lists settings made to the M32192 wait controller in the M3T-32192UT-CPU.

Table 2.1.4 M32192 Wait Controller Settings

CS signal	Device	Base	Size	WAIT	CWAIT	SWAIT	RECOV	IDLE	Bus width
CS0#	External SRAM	H'0010 0000	1 MB	4	0	0	1	1	16-bit
	Control PLD	H'0020 0000	512 KB						
	CompactFlash	H'0028 0000	512 KB						
CS1#	Extension LAN board	H'0100 0000	1 MB	4	0	0	1	1	16-bit
	Extension BlueTooth board	H'0110 0000	1 MB						
	Extension FPGA board	H'0120 0000	1 MB						
	Extension LCD board	H'0130 0000	5 MB						
CS2#	Unused	H'0200 0000	8 MB						
CS3#	Unused	H'0300 0000	8 MB						

The following shows how settings are made actually.

```
// CS0 area chip select controller initialization
CS0WTCR = 0x43;                    /* WAIT=4, CWAIT=0, SWAIT=0, RECOV=1, IDLE=1 */

// CS1 area chip select controller initialization
CS1WTCR = 0x43;                    /* WAIT=4, CWAIT=0, SWAIT=0, RECOV=1, IDLE=1 */
```

2.2 Memory

Table 2.2.1 lists the memory devices incorporated in the M3T-M32192UT-CPU.

Table 2.2.1 Memory List

Type	Base	Size	Bus width	Remarks
Internal flash ROM	H'0000 0000	1 MB	32-bit	1-wait access
Internal RAM	H'0080 4000	176 KB	32-bit	0-wait access
External SRAM	H'0010 0000	1 MB	16-bit	4-wait access
External serial ROM	-	128 KB	-	Access by operating the port of M32192

2.3 Control PLD

The APEX20K60EFC144-2 made by ALTERA is incorporated for use as control PLD in the M3T-M32192UT-CPU.

The functions listed below are implemented by the control PLD. For details, refer to the "3. Functional Description of the Control PLD" on page 30.

- CompactFlash control
- MultiMediaCard control
- Interrupt controller
- Peripheral I/O controller
- CRC calculation circuit
- Real-time clock control
- eTRON card control

2.4 CompactFlash Interface

The M3T-M32192UT-CPU incorporates one compact flash card slot (Type II).

The compact flash control signals are generated by the control PLD. In addition, a hot-line insertion/removal buffer and a power supply control IC are incorporated, enabling a CompactFlash card to be inserted or removed while the power is on.

2.5 MMC Interface

The M3T-M32192UT-CPU incorporates one MMC (MultiMediaCard) slot.

The MMC control signals are generated by the control PLD. In addition, a hot-line insertion/removal buffer and a power supply control IC are incorporated, enabling an MMC to be inserted or removed while the power is on.

The CPU board and MMC are interfaced in MMC mode, with the interface comprised of bidirectional command and data signals and a transfer clock. Furthermore, a CRC calculation circuit is implemented by the control PLD, so that CRC7 ($X^7 + X^3 + 1$) and CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) are supported.

2.6 eTRON Card Interface

The M3T-M32192UT-CPU incorporates one eTRON card slot.
The eTRON card control signals are generated by the control PLD.
The CPU board and eTRON card are interfaced by means of the following communication method.

- UART method
- Data length: 8 bits
- Transfer rule: Direct/inverse
- Start bit: 1 bit
- Parity bit: 1 bit
- _SHDN pin Can be controlled from the programmable port P100

Table 2.6.1 eTRON Card Power Supply

P100	Function
eTRON interface	When P100 = 1, the power for the eTRON card interface IC is on.
	When P100 = 0, the power for the eTRON card interface IC is off.

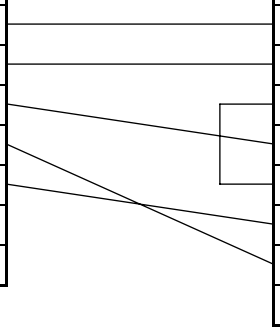
IMPORTANT

- To avoid possible shorting of power supply, do not insert or remove the eTRON card while the power is on.

2.7 Debug Serial Interface

The M3T-M32192UT-CPU incorporates a 15-pin connector for RS-232C serial communication, enabling serial communication to be performed at a rate of up to 115,200 bps (MCU maximum: 250.000bps).
The UART signals are provided using P74/TXD3 and P75/RXD3 of the M32192.
The following shows a connection of the serial cable included with the product. The connector used on the host machine side is a D-SUB 9-pin female connector.

M3T-32192UT -CPU	
Pin No.	Signal name
1	GND
2	TxD
3	RxD
4	GND
5	RTS
6	CTS
7	GND
8-15	Reserved



Host machine	
Pin No.	Signal name
1	DCD
2	RxD
3	TxD
4	DTR
5	GND
6	DSR
7	RTS
8	CTS
9	RI

Figure 2.7.1 Debug serial diagram

2.8 Real-time Clock

The M3T-M32192UT-CPU incorporates the DS1302Z made by DALLAS as its real-time clock, which allows the date and time to be preserved by battery backup using a lithium battery.
The real-time clock control signals are generated by the control PLD.
The real-time clock and devices are interfaced using a CSIO communication method.

2.9 Power Supply Circuit

2.9.1 Power Supply Circuit

The M3T-M32192UT-CPU, in a standard board configuration, operates with the 3.3 V power supply input from the extension CAN signal connector. When the system has the extension LCD board M3T-M32RUT-LCD connected, the CPU board operates with the 3.3 V power supply input from the extension bus connector.

Figure 2.9.1 shows a power supply block diagram for the standard board configuration.

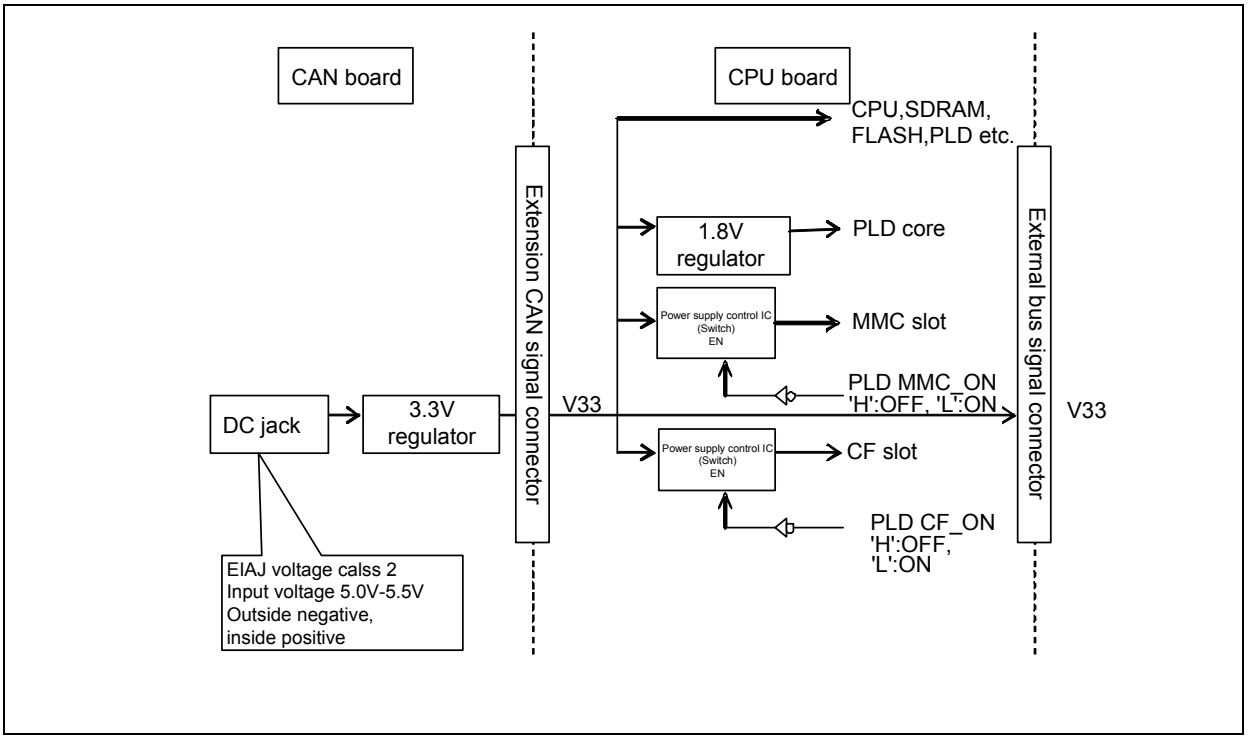


Figure 2.9.1 Power supply block diagram for the standard board configuration

2.9.2 DC Jack Input Power Supply

The table below shows specifications of the input power supply for this product that is supplied from the DC jack. When not using the AC adapter included with this product, use a power supply that conforms to the specifications shown here.

Table 2.9.1 DC Jack Input

Plug	EIAJ5320A, voltage class 2
Input voltage	5.0 V to 5.5 V
Plug polarity	Outside negative, inside positive

2.10 Clock Module

The M32192 has a 20 MHz clock module connected to its Xin.

Make sure the CPU is operated at a clock frequency of 160 MHz or less, and that the buses are operated at a clock frequency of 40 MHz or less.

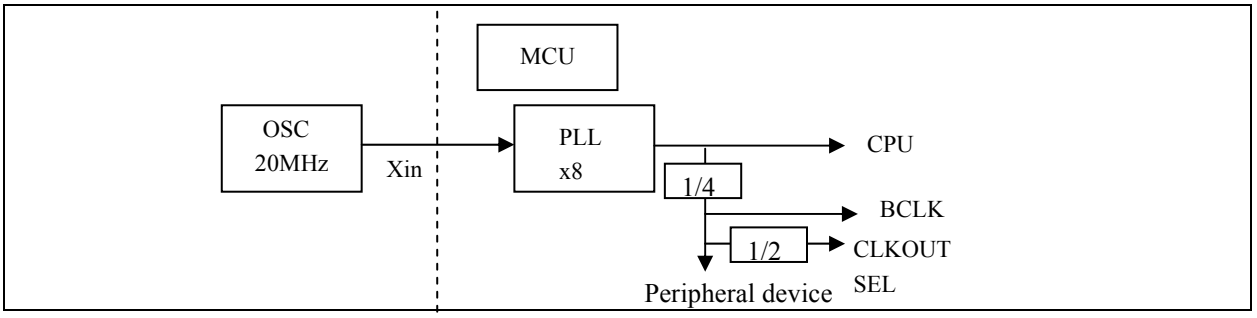


Table 2.10.1 Clock module

2.11 Reset Module

There are several reset inputs to the M32192, including power-on reset by a reset IC, reset by a reset switch, and a reset from the emulator that is applied via the extension bus connector.

Figure 2.11.1 shows a reset block diagram.

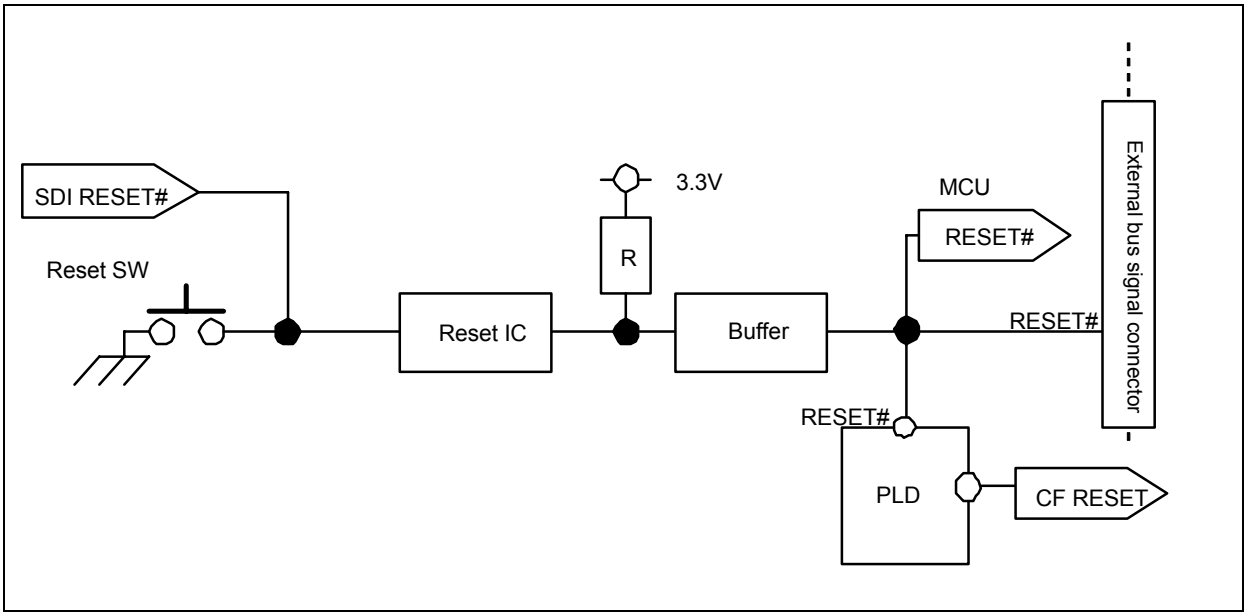


Figure 2.11.1 Reset Circuit Block Diagram

2.12 INT Switch Module

The M3T-M32192UT-CPU board has an interrupt-detectable INT switch mounted on it. This switch is connected to the INTSW# pin of the PLD, enabling INT switch input to be detected by an interrupt. The power supply block diagram is shown in Figure 2.12.1.

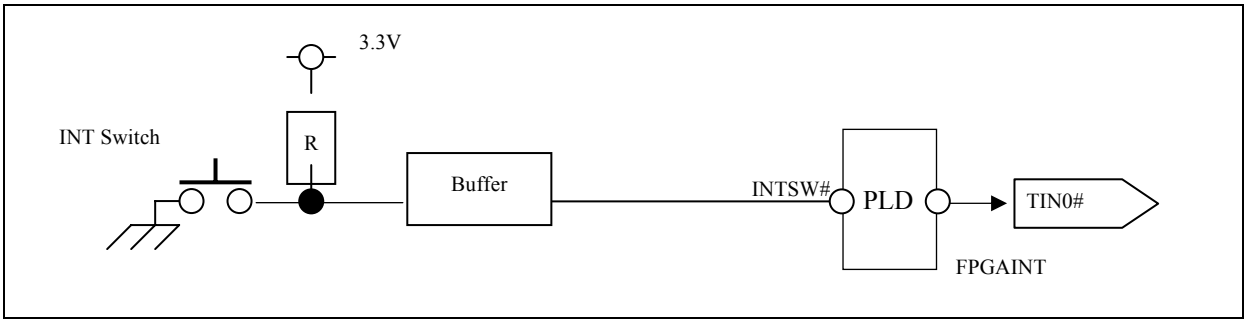


Figure 2.12.1 Power supply block diagram

2.13 Extension Bus Connector

The M3T-M32192UT-CPU incorporates one extension bus connector. The functionality of the M32912 can be extended by connecting an extension board to it via the extension bus connector. For details, refer to “4. Extension Board Specifications” on page 90.

2.14 Extension CAN Signal Connector

The M3T-M32192UT-CPU and M3T-M32192UT-CAN are connected with an extension CAN signal connector. Through-holes for extension CAN signals are provided by EXT1 and EXT2 on the M3T-M32192UT-CAN board. Table 2.14.1 lists signal assignments of the extension CAN signal connector.

Table 2.14.1 Signal Assignments of the Extension CAN Signal Connector

No.	Signal name	Through-hole No.	No.	Signal name	Through-hole No.
1	V33	*1	31	P114/TO4/TO33/DD7	EXT2-5
2	V33		32	P115/TO5/TO34/DD6	EXT2-6
3	GND	*2	33	P116/TO6/TO35/DD5	EXT2-7
4	GND		34	P117/TO7/TO36/DD4	EXT2-8
5	GND		35	P104/TO12/TIN25/DD3	EXT2-9
6	GND		36	P105/TO13/SCLK14/SCLKO4/DD2	EXT2-10
7	GND		37	P106/TO14/TXD4/DD1	EXT2-11
8	GND		38	P107/TO15/RXD4/DD0	EXT2-12
9	P82/TXD0/TO26	EXT1-5	39	P130/TIN16/PWMOFF0/DIN0	EXT2-13
10	P83/RXD0/TO25	EXT1-6	40	P131/TIN17/PWMOFF1/DIN1	EXT2-14
11	P84/SCLKI0/SCLKO0/TO24	EXT1-7	41	P133/TIN19/DIN3	EXT2-15
12	P85/TXD1/TO23	EXT1-8	42	NC	EXT2-16
13	P86/RXD1/TO22	EXT1-9	43	P134/TIN20/TXD3/DIN4	EXT2-17
14	P87/SCLKI1/SCLKO1/TO21	EXT1-10	44	P135/TIN21/RXD3	EXT2-18
15	P93/TO16/SCLKI5/SCLKO5	EXT1-11	45	P136/TIN22/CRX1	EXT2-19
16	P94/TO17/TXD5/DD15	EXT1-12	46	P137/TIN23/CTX1	EXT2-20
17	P95/TO18/RXD5/DD14	EXT1-13	47	P174/TXD2/TO28	EXT2-21
18	P96/TO19/DD13	EXT1-14	48	P175/RXD2/TO27	EXT2-22
19	P97/TO20/DD12	EXT1-15	49	P220/CTX0/HACK#	EXT2-23
20	P101/TO9/CRX0	EXT1-16	50	P221/CRX0/HREQ#	EXT2-24
21	P102/TO10/CTX0	EXT1-17	51	RESET#	EXT2-25
22	P76/RTDACK/CTX1/NBDD2	EXT1-18	52	GND	*2
23	P77/ RTDCLK/CRX1/ NBDD3	EXT1-19	53	GND	
24	P126/TCLK2/CS2#/DD1	EXT1-20	54	GND	
25	P127/TCLK3/CS3#/DD0	EXT1-21	55	GND	
26	NC	EXT1-22	56	GND	
27	P110/TO0/TO29/DD11	EXT1-23	57	GND	
28	P111/TO1/TO30/DD10	EXT1-24	58	GND	
29	P112/TO2/TO31/DD9	EXT1-25	59	V33	*1
30	P113/TO3/TO32/DD8	EXT1-26	60	V33	

*1: V33 is connected to EXT1-1, 2, 29, and 30, and to EXT2-1, 2, 29, and 30.

*2: GND is connected to EXT1-3, 4, 27, and 28, and to EXT2-3, 4, 26, 27, and 28.

2.15 CAN Communication Connector

The M3T-M32192UT-CAN incorporates two CAN communication connectors.
Table 2.15.1 lists signal assignments of the CAN communication connector.

Table 2.15.1 Signal Assignments of the CAN Communication Connector

CAN1		CAN2	
Pin No.	Signal name	Pin No.	Signal name
1	CANL1	1	CANL2
2	GND	2	GND
3	CANH1	3	CANH2

2.16 AR Camera Board Connector

The M3T-M32192UT-CAN and M3T-M32RUT-ARV2 are connected with an AR camera board connector.
Table 2.16.1 lists signal assignments of the AR camera board connector.

Table 2.16.1 Signal Assignments of the AR Camera Board Connector

Pin No.	Function	Used port
1	SCL	P87 (OE control)
2	SDA	P85 (OE control)/P86
3	VDS	P130
4	HDS	P131
5	PCK	P132
6	DGND	
7	Y0	P114/DD7
8	Y1	P115/DD6
9	Y2	P116/DD5
10	Y3	P117/DD4
11	DGND	
12	Y4	P124/DD3
13	Y5	P125/DD2
14	Y6	P126/DD1
15	Y7	P127/DD0
16	3.3V	
17	CKI(13.5MHz)	
18	3.3V	
19	RST#(RESET#)	
20	DGND	

2.17 LAN Interface

The M3T-M32RUT-LAN incorporates the LAN91C111-NC made by SMSC as an Ethernet controller. This controller is outlined below.

- Supports 10/100 Mbps.
- Supports Full/Half Duplex.
- Contains 8-KB SRAM for use as a transmit/receive buffer.
- 16-bit bus size.
- Reference clock for PHY and MAC: 25 MHz

For details on how to use the controller, refer to the user's manual for the LAN91C111-NC.

2.18 SDI Interface

The M3T-M32RUT-LAN incorporates one 10-pin SDI interface connector allowing to connect an SDI emulator. Table 2.18.1 lists signal assignments of the SDI emulator connector.

Table 2.18.1 Signal Assignments of the SDI Emulator Connector

Pin No.	Signal name
1	TCK
2	GND
3	TDI
4	TDO
5	TMS
6	TRST#
7	NC
8	NC
9	3.3V
10	RST#

Table 2.18.2 lists the functions of JP1.

Table 2.18.2 Functions of JP1

Setting	Signal name
Short	SDI connector enabled All of the SDI connectors mounted on other extension boards (e.g., SDI connector on the M3T-M32RUT-EXT) must be disabled. Only one SDI connector in the system can be enabled at a time.
Open	SDI connector disabled

2.19 Parallel Interface

The M3T-M32RUT-LAN incorporates one 20-pin connector which is capable of 8-bit parallel input/output.
Table 2.19.1 lists signal assignments of the parallel interface connector.

Table 2.19.1 Signal Assignments of the Parallel Interface Connector

Pin No.	Signal name	I/O	Remarks
1	DO0	OUT	33Ω of serial resistor installed
2	DO1	OUT	33Ω of serial resistor installed
3	DO2	OUT	33Ω of serial resistor installed
4	DO3	OUT	33Ω of serial resistor installed
5	DO4	OUT	33Ω of serial resistor installed
6	DO5	OUT	33Ω of serial resistor installed
7	DO6	OUT	33Ω of serial resistor installed
8	DO7	OUT	33Ω of serial resistor installed
9	GND		
10	GND		
11	DI0	IN	47kΩ of pull-up resistor installed
12	DI1	IN	47kΩ of pull-up resistor installed
13	DI2	IN	47kΩ of pull-up resistor installed
14	DI3	IN	47kΩ of pull-up resistor installed
15	DI4	IN	47kΩ of pull-up resistor installed
16	DI5	IN	47kΩ of pull-up resistor installed
17	DI6	IN	47kΩ of pull-up resistor installed
18	DI7	IN	47kΩ of pull-up resistor installed
19	GND		
20	GND		

Output ports (DO0-DO7) hold the values written in bytes to the address H’0108 0000.
The values of input ports (DI0-DI7) can be read out in bytes from the address H’0108 0000.

3. Functional Description of the Control PLD

3.1 Function Pins

Table 3.1.1 lists the pin functions of the control PLD.

Table 3.1.1 Pin Functions of the Control PLD (1/2)

Category	Pin name	Type	Function
Power supply	VCCIO	-	3.3V power supply
	VSSIO	-	GND
	VCCINT	-	1.8V power supply
	VSSINT	-	GND
Clock	BCLK	Input	40MHz of bus clock
Reset	RESET#	Input	System reset
Address bus	A1_[11:19]	Input	M32192 address bus A[11:19]
	A2_[22:30]	Input	M32192 address bus A[22:30]
Data bus	D[0:15]	Input/ output	M32192 data bus D[0:15]
Bus control	CS0#, CS1#	Input	M32192 chip select
	RD#	Input	M32192 read
	BHW#, BLW#	Input	M32192 write
	WAIT#	Output	Wait request to M32192
	FPGAINT	Output	Interrupt request to M32192
External bus control	EXREADY#	Input	READY# from extension bus
	BUS_RD#	Output	Extension bus read
	BUS_BHW#, BUS_BLW#	Output	Extension bus write
	BUS_CS#	Output	Extension bus chip select
	BUSSEL#	Output	Extension bus data I/O control
	SRAM_CS#	Output	External SRAM chip select
	SRAM_WE#	Output	External SRAM write
	SRAM_UB#, SRAM_LB#	Output	External SRAM byte select
CompactFlash controller	CF_ON#	Output	CF power supply control
	CFRESET	Output	CF reset
	CFCE1#, CFCE2#	Output	CF selection and valid byte location
	CFIORD#	Output	Controls output of CF I/O memory space read data
	CFIOWR#	Output	Controls writing of CF I/O memory space write data
	CFOE#	Output	Controls output of CF read data
	CFWE#	Output	Controls writing of CF write data
	CFBUFOE#	Output	Controls OE of insert/remove buffer for CE (except data)
	CFDBUFOE#	Output	Controls OE of insert/remove buffer for CE (data)
	CFWAIT#	Input	CF wait request
	CFIREQ#	Input	CF interrupt request
	CFCD1#, CFCD2#	Input	Detects hot plug status of CF
MMC controller	MMC_ON#	Output	Controls MMC power supply
	MMCCLK	Output	Clock for MMC command/data transmit
	MMCCS	Output	MMC chip select
	MMCCD	Input	Detects inserted/removed status of MMC
	MMCWP	Input	Detects MMC write protect
	MMCCMD	Input/ output	MMC command output/response input
	MMCDAT0	Input/ output	MMC I/O data

Table 3.1.1 Pin Functions of the Control PLD (2/2)

Category	Pin name	Type	Function
eTRON card controller	eTCRST#	Output	eTRON card reset signal
	eTCCLK	Output	eTRON card data transfer clock
	eTCDIO	Input/ output	eTRON card transmit/receive data
Real-time clock	RTCRST#	Output	RTC reset signal
	RTCSCLK	Output	RTC data transmit clock
	RTCIO	Input/ output	RTC command/data I/O
Others	INTSW#	Input	Push switch input
	SW1, SW2	Input	Dip switch input
	LED1, LED2	Output	LED ON control signal

3.2 Internal Register Address Map

Figure 3.2.1 shows an address map of the internal registers of the control PLD.

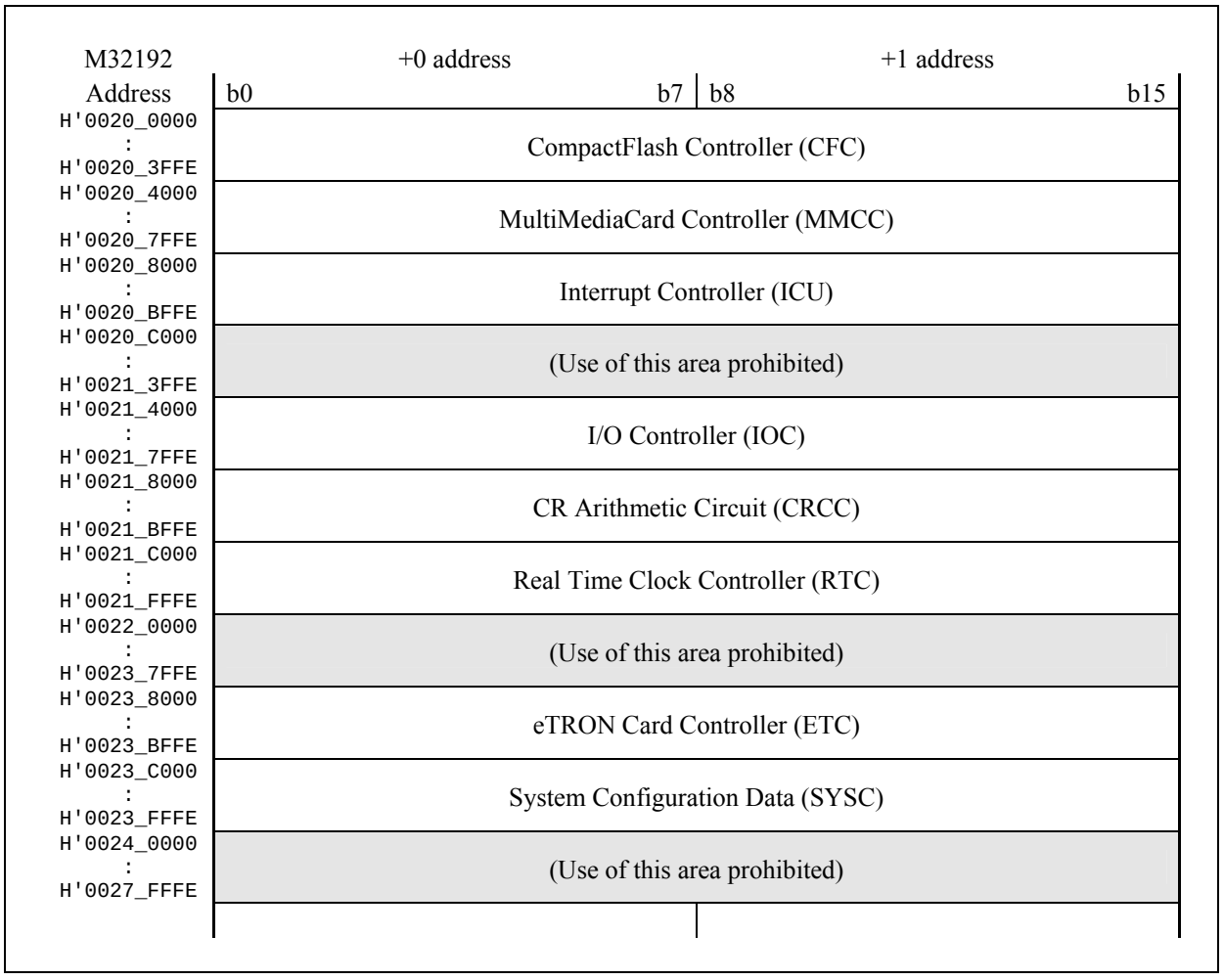


Figure 3.2.1 Address Map of the Internal Registers of the Control PLD

3.3 Access Timing

Figure 3.3.1 shows the timing with which the control PLD is accessed from the M32192.

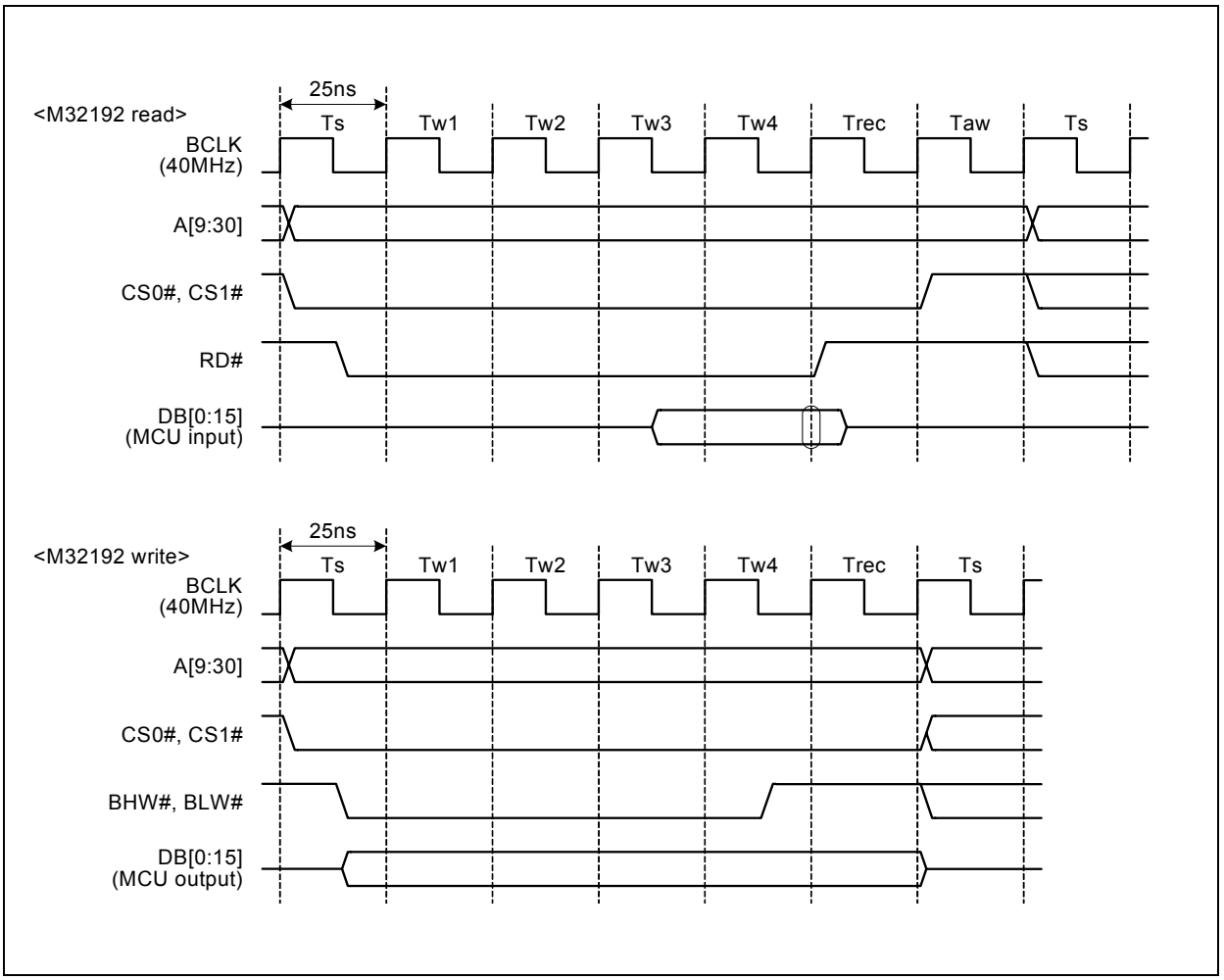


Figure 3.3.1 Timing for M32192 Access to Control PLD

3.4 CompactFlash Controller (CFC)

3.4.1 Outline of the CFC

The PLD incorporates a CompactFlash controller.

CompactFlash is mapped into the CS0# area of the M32192, and CompactFlash control signals are generated by decoding the M32192 address and control signals in the PLD.

Furthermore, this controller exercises card detection to support hot-line insertion/removal of the card.

Table 3.4.1 lists the outline of the CFC

Table 3.4.1 Outline of the CFC

Item	Outline
Control slot	1 slot
Slot size	2 KB
Support memory space	Attribute memory space Common memory space I/O memory space
Access timing control	Depends on how M32192 CS0# is set
CompactFlash access	Controlled by decoding the M32192 address and control signals
Card detection	Card insertion/removal detected by CFCD1# and CFCD2#
Card power supply control	Available
Access mode	Attribute access Memory access I/O access

3.4.2 CFC Related Registers

Figure 3.4.1 shows CFC register mapping, with each register detailed in the pages that follow. If data is written to any use-prohibited area, device operation cannot be guaranteed.

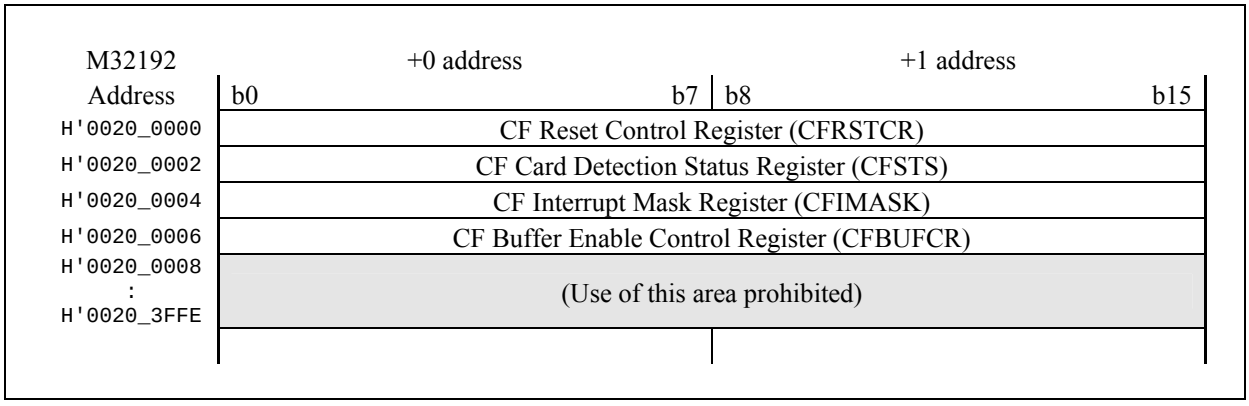


Figure 3.4.1 CFC Register Mapping

3.4.3 CFC Reset Control Register

■ CFC Reset Control Register (CFRSTCR) <Address: H'0020 0000>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
							OEO								CFRST
0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

<When reset: H'0100>

b	Bit name	Function	R	W
0-6	No function assigned.		0	-
7	OEO CFOE# output data bit	0: Output a low from CFOE# 1: Output according to CF access control	R	W
8-14	No function assigned.		0	-
15	CFRST CompactFlash resetting bit	0: Output a low from CFRESET 1: Output a high from CFRESET	R	W

(1) CFOE# output data bit, OEO (b7)

This bit controls CFOE# output.

If this bit is cleared to 0, the CFOE# signal output for CompactFlash is always driven low.

If this bit is set to 1, the CFOE# signal is output in conformity with access control by the M32192.

(2) CompactFlash reset bit, CFRST (b15)

This bit sets the reset state of CompactFlash.

Clearing this bit to 0 outputs a low from the CFRESET pin.

Setting this bit to 1 outputs a high from the CFRESET pin.

3.4.4 CF Card Detection Status Register

■ CF Card Detection Status Register (CFSTS) <Address: H'0020 0002>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
															CFDET
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	? Note

<When reset: H'000?>

b	Bit name	Function	R	W
0-14	No functions assigned.		0	-
15	CFDET CompactFlash detection status bit	0: No card exists in the slot 1: Card exists in the slot	R	-

Note: The initial value varies depending on whether a card is inserted in place.

(1) CompactFlash detection status bit, CFDET (b15)

This bit indicates whether a CompactFlash card is inserted into the slot.

This bit is set to 1 when a CompactFlash card is inserted into the slot.

This bit is cleared to 0 when a CompactFlash card is removed from the slot.

3.4.5 CF Interrupt Mask Register

■ CF Interrupt Mask Register (CFIMASK) <Address: H'0020 0004>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
															CFMSK
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<When reset: H'0000>

b	Bit name	Function	R	W
0-14	No functions assigned.		0	-
15	CFMSK CompactFlash card inserted/removed interrupt enable bit	0: Disable card inserted/removed interrupt 1: Enable card inserted/removed interrupt	R	W

(1) CompactFlash card inserted/removed interrupt enable bit, CFMSK (b15)

This bit selects whether or not to enable the card inserted/removed interrupt.

If this bit is cleared to 0, no interrupts are generated even when insertion or removal of a card is detected.

If this bit is set to 1, an interrupt request to the M32192 is generated when insertion or removal of a card is detected.

3.4.6 CF Buffer Enable Control Register

■ CF Buffer Enable Control Register (CFBUFCR) <Address: H'0020 0006>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
															BUFEN
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

<When reset: H'0001>

b	Bit name	Function	R	W
0-14	No functions assigned.		0	-
15	BUFEN CompactFlash buffer enable bit	0: Output a low from the CFBUFOE# pin 1: Output a high from the CFBUFOE# pin	R	W

(1) CompactFlash buffer enable bit, BUFEN (b15)

This bit can only be set when a CompactFlash card is inserted in place (CFDET = 1).

Clearing this bit to 0 outputs a low from the CFBUFOE# pin.

Setting this bit to 1 outputs a high from the CFBUFOE# pin.

If the card is removed when this bit = 0, CFBUFOE# changes state from low to high and this bit is set to 1.

CompactFlash can only be accessed from the M32192 when BUFEN = 0.

3.4.7 Card Configuration Register Address Mapping

Table 3.4.2 lists card configuration register address mapping in the attribute memory.

Table 3.4.2 Card Configuration Register Address Mapping

M32192 address	A15	A16	A17		A18		A19	A20	A21-A30	Register
Card signal	CE2#	CE1#	IORD#	IOWR#	OE#	WE#	REG#	A0	A10-A1	
H'0029 4200	1	0	1	1	0	1	0	0	010 0000 000	Configuration Option Register Read
H'0029 4200	1	0	1	1	1	0	0	0	010 0000 000	Configuration Option Register Write
H'0029 4202	1	0	1	1	0	1	0	0	010 0000 001	Card Status Register Read
H'0029 4202	1	0	1	1	1	0	0	0	010 0000 001	Card Status Register Write
H'0029 4204	1	0	1	1	0	1	0	0	010 0000 010	Pin Replacement Register Read
H'0029 4204	1	0	1	1	1	0	0	0	010 0000 010	Pin Replacement Register Write
H'0029 4206	1	0	1	1	0	1	0	0	010 0000 011	Socket and Copy Register Read
H'0029 4206	1	0	1	1	1	0	0	0	010 0000 011	Socket and Copy Register Write

3.4.8 CF-ATA Drive Register Address Mapping

The following describes the method for accessing the ATA drive register set incorporated in the CompactFlash Controller. There are two access methods: continuous I/O mode and memory mapped mode.

Table 3.4.3 and Table 3.4.4 list memory mapped mode (index = “0”) and continuous I/O mode (index = “1”) address mapping, respectively

Table 3.4.3 Memory Mapped Mode (Index = 0) Address Mapping

M32192 address	A15	A16	A17		A18		A19	A20	A21-A30	Register
Card signal	CE2#	CE1#	IORD#	IOWR#	OE#	WE#	REG#	A0	A10-A1	
H’0028 5000	0	0	1	1	0	1	1	0	000 0000 000	Read Data*
H’0028 5000	0	0	1	1	1	0	1	0	000 0000 000	Write Data*
H’0029 5800	1	0	1	1	0	1	1	1	000 0000 000	Error
H’0029 5800	1	0	1	1	1	0	1	1	000 0000 000	Features
H’0028 5002	0	0	1	1	0	1	1	0	000 0000 001	Sector No, Sector Count*
H’0028 5002	0	0	1	1	1	0	1	0	000 0000 001	Sector No, Sector Count*
H’0028 5004	0	0	1	1	0	1	1	0	000 0000 010	Cylinder High, Cylinder Low*
H’0028 5004	0	0	1	1	1	0	1	0	000 0000 010	Cylinder High, Cylinder Low*
H’0029 5006	1	0	1	1	0	1	1	0	000 0000 011	Select Card/Head
H’0029 5006	1	0	1	1	1	0	1	0	000 0000 011	Select Card/Head
H’0029 5806	1	0	1	1	0	1	1	1	000 0000 011	Status
H’0029 5806	1	0	1	1	1	0	1	1	000 0000 011	Command
H’0029 500E	1	0	1	1	0	1	1	0	000 0000 111	Alt Status
H’0029 500E	1	0	1	1	1	0	1	0	000 0000 111	Device Ctl
H’0029 580E	1	0	1	1	0	1	1	1	000 0000 111	Drive Address

Note: For those marked with an asterisk (*), the valid data of the M32192 resides on D0-D15. For others, the valid data resides on D0-D7.

Table 3.4.4 Continuous I/O Mode (Index = 1) Address Mapping

M32192 address	A15	A16	A17		A18		A19	A20	A21-A30	Register
Card signal	CE2#	CE1#	IORD#	IOWR#	OE#	WE#	REG#	A0	A10-A1	
H’0028 2000	0	0	0	1	1	1	0	0	000 0000 000	Read Data*
H’0028 2000	0	0	1	0	1	1	0	0	000 0000 000	Write Data*
H’0029 2800	1	0	0	1	1	1	0	1	000 0000 000	Error
H’0029 2800	1	0	1	0	1	1	0	1	000 0000 000	Features
H’0028 2002	0	0	0	1	1	1	0	0	000 0000 001	Sector No, Sector Count*
H’0028 2002	0	0	1	0	1	1	0	0	000 0000 001	Sector No, Sector Count*
H’0028 2004	0	0	0	1	1	1	0	0	000 0000 010	Cylinder High, Cylinder Low*
H’0028 2004	0	0	1	0	1	1	0	0	000 0000 010	Cylinder High, Cylinder Low*
H’0029 2006	1	0	0	1	1	1	0	0	000 0000 011	Select Card/Head
H’0029 2006	1	0	1	0	1	1	0	0	000 0000 011	Select Card/Head
H’0029 2806	1	0	0	1	1	1	0	1	000 0000 011	Status
H’0029 2806	1	0	1	0	1	1	0	1	000 0000 011	Command
H’0029 200E	1	0	0	1	1	1	0	0	000 0000 111	Alt Status
H’0029 200E	1	0	1	0	1	1	0	0	000 0000 111	Device Ctl
H’0029 280E	1	0	0	1	1	1	0	1	000 0000 111	Drive Address

Note: For those marked with an asterisk (*), the valid data of the M32192 resides on D0-D15. For others, the valid data resides on D0-D7.

3.4.9 Relationship between the M32192 Address and CompactFlash Address

The M32192 is a big endian microcomputer, whereas CompactFlash is defined in little endian. The CompactFlash used by µT-Engine has byte endians connected in reverse, upper byte for lower byte and vice versa, assuming data exchanges with a PC and other little endian systems. Therefore, the M32192 and CompactFlash have the following relationship with respect to the read/write addresses.

Table 3.4.5 lists the relationship of addresses between the M32192 and CompactFlash.

Table 3.4.5 Relationship of Addresses between the M32192 and CompactFlash

M32192 address	+0 address	+1 address
H'xxxx xxx0	CompactFlash +0 address	CompactFlash +1 address
H'xxxx xxx2	CompactFlash +2 address	CompactFlash +3 address
H'xxxx xxx4	CompactFlash +4 address	CompactFlash +5 address
: :	: :	: :

3.5 MultiMediaCard Controller (MMCC)

3.5.1 Outline of the MMCC

The control PLD internally contains an MMC (MultiMediaCard) controller.

The protocol it supports is MMC mode, where only a single-block transfer (CMD17) is supported for data read/write. In addition, the control PLD internally contains a CRC calculation circuit, which when combined with the MMCC, enables the control PLD to support high-speed data transfer.

3.5.2 MultiMediaCard Controller Related Registers

Figure 3.5.1 shows MMCC register mapping, with reach register detailed in the pages that follow. Note that if data is written to any use-prohibited area, device operation cannot be guaranteed.

M32192 Address	+0 address b0 – b7	+1 address b8 – b15
H'0020_4000	MMC Control Register (MMCCR)	
H'0020_4002	MMC Mode Register (MMCMOD)	
H'0020_4004	(Use of this area prohibited)	
H'0020_4006	MMC Status Register (MMCSTS)	
H'0020_4008	(Use of this area prohibited)	
H'0020_400A	MMC Baud Rate Register (MMCBAUR)	
H'0020_400C	MMC Command Byte Count Register (MMCCMDBCUT)	
H'0020_400E	MMC Data Byte Count Register (MMCDTBCUT)	
H'0020_4010	MMC Detection Register (MMCDET)	
H'0020_4012	MMC Write Protect Register (MMCWP)	
H'0020_4014 : H'0020_4FFE	(Use of this area prohibited)	
H'0020_5000 : H'0020_5200	MMC Write Data Memory (514 Bytes)	
H'0020_5202 : H'0020_5FFE	(Use of this area prohibited)	
H'0020_6000 : H'0020_6200	MMC Read Data Memory (514 Bytes)	
H'0020_6202 : H'0020_6FFE	(Use of this area prohibited)	
H'0020_7000 : H'0020_7004	MMC Command Data Memory (6 Bytes)	
H'0020_7006 : H'0020_701E	MMC Response Data Memory (26 Bytes)	
H'0020_7020 : H'0020_7FFE	(Use of this area prohibited)	

Figure 3.5.1 MMCC Register Mapping

3.5.3 MMC Control Register

■ MMC Control Register (MMCCR) <Address: H'0020 4000>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
							CLR							CMDEN	DTEN
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-6	No functions assigned.		0	-
7	CLR MMC initialization bit	0: No operation 1: Initialize the MMC	R	W
8-13	No functions assigned.		0	-
14	CMDEN Command transfer enable bit	- For write 0: Has no effect 1: Start command transfer - For read 0: Command/response transfer not in progress 1: Command/response transfer in progress now	R	W
15	DTEN Data transfer enable bit	- For write 0: Has no effect 1: Start data transfer - For read 0: Data transfer not in progress 1: Data transfer in progress now	R	W

(1) MMC initialization bit, CLR (b7)

Setting this bit to 1 initializes the MMC related registers and all of the internal registers of the MMC controller. Even when this bit is set to 1, the value in it is not retained.

(2) Command transfer enable bit, CMDEN (b14)

Setting this bit to 1 starts a command transfer to the MMC.

This bit also indicates the status of command/response transfer operation.

(3) Data transfer enable bit, DTEN (b15)

Setting this bit to 1 starts a data transfer to the MMC.

The MMC Mode Register is used to select between data read and write.

This bit also indicates the status of data transfer operation.

3.5.4 MMC Mode Register

■ MMC Mode Register (MMCMOD) <Address: H'0020 4002>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
							DMY								DSEL
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-6	No functions assigned.		0	-
7	DMY Dummy data transfer select bit	0: Do not receive dummy data 1: Transmit dummy clock	R	W
8-14	No functions assigned.		0	-
15	DSEL MMC data transfer select bit	0: Receive data 1: Transmit data	R	W

Note: This register can only be set while MMCC data transfer is idle (data transfer enable bit = 0).

(1) Dummy data transfer select bit, DMY (b7)

This bit selects dummy data receive (or dummy clock transmit) function.

(2) MMC Data transfer select bit, DSEL (b15)

This bit selects to transmit or receive MMC data.

When DMY bit = 1 and DSEL bit = 0, given bytes of transfer data as set in the MMC data byte counter register are received. When receiving dummy data, the start and stop bits in the data supplied to MMCDAT are not detected.

3.5.5 MMC Status Register

■ MMC Status Register (MMCSTS) <Address: H'0020 4006>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
													CRCSTS		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-12	No functions assigned.		0	-
13-15	CRCSTS MMC data CRC status bits	The CRC status of MMC data when it was written in these bits.	R	W

(1) MMC data CRC status bits, CRCSTS (b13-b15)

These bits hold the CRC status of MMC data when the MMC data was written to memory. After read out these bits, write "000" by the software to initialize the status.

3.5.6 MMC Baud Rate Register

■ MMC Baud Rate Register (MMCBAUR) <Address: H'0020 400A>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
								MMCBAUR							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-7	No functions assigned.		0	-
8-15	MMCBAUR Baud rate setting bits	These bits set a baud rate.	R	W

Note: This register can only be set while MMC is idle (MMCCR = H'0000).

(1) Baud rate setting bits, MMCBAUR (b8-b15)

The system clock (BCLK) is divided by n + 1 where n = value set by these bits.

<Transfer clock>

The "divided by n + 1" count source is further divided by 2 to become the transfer clock. The transfer clock is output from the MMCCLK pin to external devices.

Figure 3.5.2 shows the equation to calculate the value to be set in the MMC baud rate register. Table 3.5.1 shows an example of how to set the MMC baud rate register.

$$\text{Value to be set in the MMC baud rate register (MMCBAUR)} = \frac{f(BCLK)}{\text{baud rate} \times 2} - 1$$

$$\text{Baud rate} = \frac{f(BCLK)}{2 \times (\text{MMCBAUR} + 1)}$$

Figure 3.5.2 Equation to Calculate the Value to be Set in the MMC Baud Rate Register

Table 3.5.1 Example MMC Baud Rate Settings (when f(BCLK) = 40 MHz)

MMCBAUR	Baud rate (MHz)	MMCBAUR	Baud rate (MHz)
0 (H'0000)	20.0000	12 (H'000C)	1.5385
1 (H'0001)	10.0000	13 (H'000D)	1.4286
2 (H'0002)	6.6667	14 (H'000E)	1.3333
3 (H'0003)	5.0000	15 (H'000F)	1.2500
4 (H'0004)	4.0000	16 (H'0010)	1.1765
5 (H'0005)	3.3333	17 (H'0011)	1.1111
6 (H'0006)	2.8571	18 (H'0012)	1.0526
7 (H'0007)	2.5000	19 (H'0013)	1.0000
8 (H'0008)	2.2222	20 (H'0014)	0.9524
9 (H'0009)	2.0000	21 (H'0015)	0.9091
10 (H'000A)	1.8182	22 (H'0016)	0.8696
11 (H'000B)	1.6667	23 (H'0017)	0.8333

3.5.7 MMC Command Byte Count Register

■ MMC Command Byte Count Register (MMCCMDBCUT) <Address: H'0020 400C>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
											CBCUT				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-10	No functions assigned.		0	-
11-15	CBCUT Transfer byte count setting bits	Transfer byte count value	R	W

Note: If this register is accessed for write while command/response data transfer is in progress, device operation cannot be guaranteed.

(1) Transfer byte count setting bits, CBCUT (b11-b15)

These bits set a total number of bytes of command and response data to be transmitted or received. The transfer byte count set in this register is decremented each time one byte of data is transferred and the data transfer finishes when the count reaches 0.

If the set value of the MMC command byte count register is H'0001, one byte of data is transferred; if the set value is H'17, 23 bytes of data are transferred.

3.5.8 MMC Data Byte Count Register

■ MMC Data Byte Count Register (MMCDTBCUT) <Address: H'0020 400E>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
						DBCUT									
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-5	No functions assigned.		0	-
6-15	DBCUT Transfer byte count setting bits	Transfer byte count value	R	W

Note: If this register is accessed for write while data transfer is in progress, device operation cannot be guaranteed.

(1) Transfer byte count setting bits, DBCUT (b6-b15)

These bits set a number of bytes of data to be transmitted or received. The transfer byte count set in this register is decremented each time one byte of data is transferred and the data transfer finishes when the count reaches 0.

During data write, the count indicates the number of data to be transmitted; during data read, it indicates the number of data to be received.

If the set value of the MMC data byte count register is H'0001, one byte of data is transferred; if the set value is H'202, 514 bytes of data are transferred.

3.5.9 MMC Detection Register

■ MMC Detection Register (MMCDET) <Address: H'0020 4010>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
															MMCDET
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	? Note

<Reset: H'000?>

b	Bit name	Function	R	W
0-14	No functions assigned.		0	-
15	MMCDET MMC detection status bit	0: MMC exists in slot 1: No MMC exists in slot	R	-

Note: The initial value varies depending on whether an MMC is inserted in place.

(1) MMC detection status bit, MMCDET (b15)

This bit indicates whether an MMC is inserted in the slot.

This bit is cleared to 0 if an MMC is inserted into the slot.

This bit is set to 1 if an MMC is removed from the slot.

An MMC must be inserted into or removed from the slot when the card power supply is on.

3.5.10 MMC Write Protect Detection Register

■ MMC Write Protect Detection Register (MMCWP) <Address: H'0020 4012>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
															MMCWP
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	? Note

<Reset: H'000?>

b	Bit name	Function	R	W
0-14	No functions assigned.		0	-
15	MMCWP MMC write protect status bit	0: MMC is write protected 1: MMC is not write protected	R	-

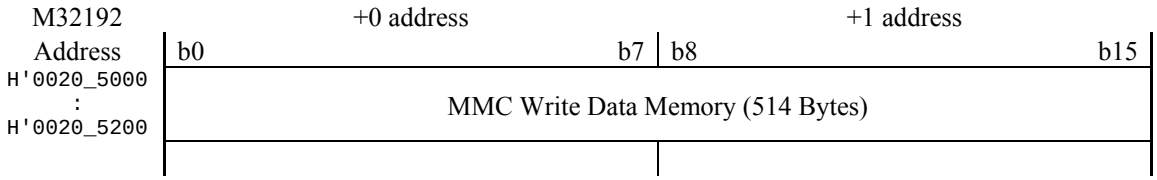
Note: The initial value varies depending on whether an MMC is write protected.

(1) MMC write protect status bit, MMCWP (b15)

This bit indicates whether an MMC is write protected.

This bit is set to 1 if an MMC is not write protected, and is cleared to 0 if the card is write protected.

3.5.11 MMC Write Data Memory



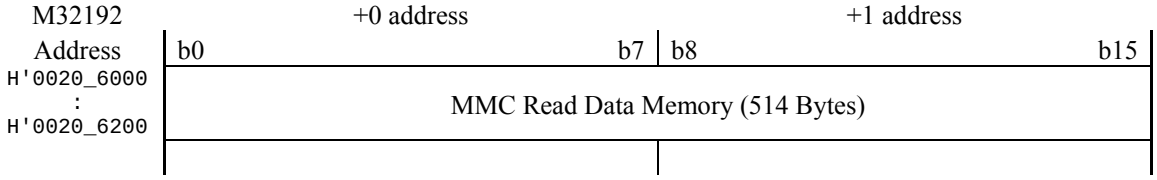
<Reset: Indeterminate>

b	Bit name	Function	R	W
0-15	Write data bits	Write data is written to these bits.	-	W

(1) Write data bits (b0-b15)

These bits are used to set the write data and CRC code to be written to the MMC. The data must be set beginning with the start address (H'0020 5000). For writing data to the PLD, note that the PLD can only be accessed in 16 bits. When setting odd number of bytes of data, set dummy data on the lower byte side.

3.5.12 MMC Read Data Memory



<Reset: Indeterminate>

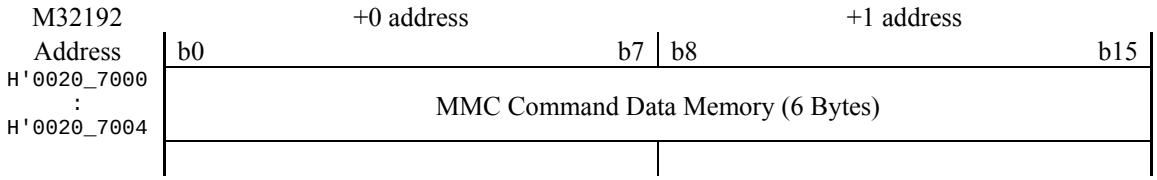
b	Bit name	Function	R	W
0-15	Read data bits	Read data is stored in these bits.	R	-

(1) Read data bits (b0-b15)

These bits are used to read data from an MMC.

The received data is set here sequentially beginning with the start address (H'0020 6000). The MMC read data memory is read-only memory, so that no data can be written to this memory area.

3.5.13 MMC Command Data Memory



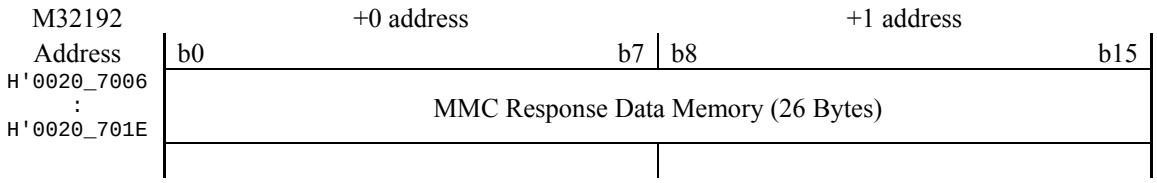
<Reset: Indeterminate>

b	Bit name	Function	R	W
0-15	Command data bits	Command data is written to these bits.	-	W

(1) Command data bits (b0-b15)

These bits are used to set the command data and CRC code to be written to the MMC. The data must be set beginning with the start address (H'0020 7000).

3.5.14 MMC Response Data Memory



<Reset: Indeterminate>

b	Bit name	Function	R	W
0-15	Response data bits	Response data is stored in these bits.	R	-

(1) Response data bits (b0-b15)

These bits are used to read the response data received from an MMC. The received data is set here sequentially beginning with the start address (H'0020 7006).

The MMC response data memory is read-only memory, so that no data can be written to this memory area.

3.5.15 Description of MMCC Operation

I MMCC data transfer rate (baud rate)

The data transfer rate of the MMCC (baud rate) is determined by the transfer clock used.

The system clock (BCLK) is divided by n + 1 where n = value set by the MMC baud rate register. The “divided by n + 1” count source is further divided by 2 to become the transfer clock.

$$\text{Baud rate (MHz)} = \frac{f(\text{BCLK})}{(\text{set value of the MMC baud rate register} + 1) \times 2}$$

II MMC command transfer operation

(1) Setting the command data

Write the command data to be transmitted to the MMC command data memory.

(2) Command transfer start condition

A command transfer operation is started by setting the command transfer enable bit (CMDEN) to 1.

(3) End of command transfer

When command transmission and response reception finish, CMDEN is automatically cleared, with command transfer processing thereby completed.

III MMC data transfer operation

<Writing data to MMC>

(1) Setting the write data

Write the data to be transmitted to the MMC write data memory and the MMC Write Data CRC Register.

(2) Data transfer start condition

A data transfer operation is started by setting the MMC data transfer select bit (DSEL) to 1 and then the data transfer enable bit (DTEN) to 1.

(3) End of data transfer

After data transmission, CRC status reception and ready status detection, the DTEN bit is automatically cleared, with data transfer processing thereby completed.

<Reading data from MMC>

(1) Data reception start condition

A data receive operation is started by setting the MMC data select bit (DSEL) to 0 and then the data transfer enable bit (DTEN) to 1.

(2) End of data transfer

After data reception, the DTEN bit is automatically cleared, with data transfer processing thereby completed.

3.6 Interrupt Controller (ICU)

3.6.1 Outline of the ICU

The PLD contains an Interrupt Controller (ICU) that manages interrupt requests.

The ICU has six maskable interrupt sources for interrupt requests from the internal peripheral I/O and external devices. These interrupt sources each are assigned one of nine priority levels for managing interrupt requests by priority resolution. If multiple interrupt requests with the same priority level occur at the same time, they are resolved by the fixed priority that is predetermined in hardware. Interrupt requests accepted by the PLD are output to TIN0 of the M32192 as an active-high signal.

Table 3.6.1 lists the outline of the ICU.

Table 3.6.1 Outline of the ICU

Item	Outline
Interrupt source	8 sources
Priority management	Managed by 9 priority levels including interrupt-disabled

3.6.2 ICU Related Registers

Figure 3.6.1 shows ICU register mapping, with reach register detailed in the pages that follow. Note that if data is written to any use-prohibited area, device operation cannot be guaranteed.

M32192 Address	+0 address b0 – b7	+1 address b8 – b15
H'0020_8000	(Use of this area prohibited)	
H'0020_8002	Interrupt Status Register (ICUISTS)	
H'0020_8004	Interrupt Request Register 0 (ICUIREQ0)	
H'0020_8006 : H'0020_8102	(Use of this area prohibited)	
H'0020_8104	External Pin CFIREQ# Interrupt Control Register (ICUCR3)	
H'0020_8106	CF Card Insertion Interrupt Control Register (ICUCR4)	
H'0020_8108	CF Card Removal Interrupt Control Register (ICUCR5)	
H'0020_810A	External Pin INTSW# Interrupt Control Register (ICUCR6)	
H'0020_810C : H'0020_8112	(Use of this area prohibited)	
H'0020_8114	MMC Insert/Remove Interrupt Control Register (ICUCR11)	
H'0020_8116	(Use of this area prohibited)	
H'0020_8118	eTRON Card Error Interrupt Control Register (ICUCR13)	
H'0020_811A	eTRON Card Receive Interrupt Control Register (ICUCR14)	
H'0020_811C	eTRON Card Transmit Interrupt Control Register (ICUCR15)	
H'0020_811E : H'0020_BFFE	(Use of this area prohibited)	

Figure 3.6.1 ICU Related Register Mapping

3.6.3 Interrupt Status Register

■ Interrupt Status Register (ICUSTS) <Address: H'0020 8002>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
VECB					ISN										
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-3	VECB Vector base bits	M32192 address A20-A23 in EIT vector entry is set	R	W
4	No functions assigned.		0	-
5-9	ISN Interrupt source number bits	00000: No interrupt 00001: Interrupt source 1 00010: Interrupt source 2 00011: Interrupt source 3 : : 11110: Interrupt source 30 11111: Interrupt source 31	R	-
10-14	No functions assigned.		0	-

The interrupt status register is used to identify the interrupt source of an interrupt request to be accepted.
When this register is read out in interrupt handler processing, the ICU recognizes that the M32192 has accepted the interrupt request and drives FPGAINT low. Since this register is not a status register to indicate interrupt requests, do not read it twice in one session of interrupt handler processing. The ISN bits are automatically cleared to '0000' by a read of this register.

(1) Vector base bits, VECB (b0-b3)

These bits may be used to set the start address A[20:23] of the software vector table corresponding to each interrupt source, to reduce the interrupt handler processing load in software. Note that setting these bits does not affect operation of the ICU or the M32192 itself.

(2) Interrupt source number bits, ISN (b5-b9)

These bits indicate the interrupt source number that has the highest priority among the currently requested interrupt sources. The value of these bits is always updated, even when interrupts to the M32192 are enabled (FPGAINT signal = high). Therefore, if an interrupt request with higher priority than that of the currently indicated one occurs before the interrupt status register is read, the interrupt source number of that higher priority interrupt request will be referenced. When the interrupt status register is read in the interrupt handler, the interrupt request which has had its interrupt source number read out at that point in time is assumed to have been accepted, so that the FPGAINT signal to the M32192 is asserted high.

Inspect the value of these bits in software to identify the interrupt source that generated the interrupt request, before proceeding to the appropriate handler processing.

A combined use of these bits with the vector base bits (VECB) allows to reference the user-defined vector table directly.

Table 3.6.2 lists the supported interrupt sources.

Table 3.6.2 List of Interrupt Sources

Interrupt source No.	Interrupt source	Interrupt source No.	Interrupt source
0	No interrupt source	16	(Reserved)
1	(Reserved)	17	(Reserved)
2	(Reserved)	18	(Reserved)
3	CFIREQ# (CF external pin)	19	(Reserved)
4	CF card insertion	20	(Reserved)
5	CF card removal	21	(Reserved)
6	INTSW# (external pin)	22	(Reserved)
7	(Reserved)	23	(Reserved)
8	(Reserved)	24	(Reserved)
9	(Reserved)	25	(Reserved)
10	(Reserved)	26	(Reserved)
11	MMC insertion/removal	27	(Reserved)
12	(Reserved)	28	(Reserved)
13	eTRON card error	29	(Reserved)
14	eTRON card receive	30	(Reserved)
15	eTRON card transmit	31	(Reserved)

3.6.4 Interrupt Request Registers 0

■ Interrupt Request Register 0 (ICUIREQ0) <Address: H'0020 8004>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
			IREQ3	IREQ4	IREQ5	IREQ6					IREQ11		IREQ13	IREQ14	IREQ15
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-2	No functions assigned.		0	-
3	IREQ3 Interrupt source 3 interrupt request bit	0: External pin CFIREQ# interrupt not requested 1: External pin CFIREQ# interrupt requested	R	-
4	IREQ4 Interrupt source 4 interrupt request bit	0: CF card insertion interrupt not requested 1: CF card insertion interrupt requested	R	-
5	IREQ5 Interrupt source 5 interrupt request bit	0: CF card removal interrupt not requested 1: CF card removal interrupt requested	R	-
6	IREQ6 Interrupt source 6 interrupt request bit	0: External pin INTSW# interrupt not requested 1: External pin INTSW# interrupt requested	R	-
7-10	No functions assigned.		0	-
11	IREQ11 Interrupt source 11 interrupt request bit	0:MMC insert/remove interrupt not requested 1:MMC insert/remove interrupt requested	R	-
12	No functions assigned.		0	-
13	IREQ13 Interrupt source 13 interrupt request bit	0:eTRON card error interrupt not requested 1:eTRON card error interrupt requested	R	-
14	IREQ14 Interrupt source 14 interrupt request bit	0:eTRON card receive interrupt not requested 1:eTRON card receive interrupt requested	R	-
15	IREQ15 Interrupt source 15 interrupt request bit	0:eTRON card transmit interrupt not requested 1:eTRON card transmit interrupt requested	R	-

(1) Interrupt source 'n' interrupt request bits IREQ3-IREQ6, IREQ11, IREQ13-IREQ15 (b3-b6, b11, b13-b15)

When an interrupt request is generated by one of the mapped interrupt sources, the corresponding IREQ bit is set to 1. This bit is cleared to 0 under the following conditions:

[For edge-sensed interrupts]

- Cleared to 0 when the interrupt status register is read out while FPGAINT is asserted high.
- Cleared to 0 when the interrupt request bit (IREQ) in the corresponding interrupt control register is set to 1.

[For level-sensed interrupts]

- Cleared to 0 when the interrupt request is dropped by the interrupt source that generated it. No data can be written to these bits. These bits are mirror bits of the IREQ bits of each interrupt control register.

3.6.5 Interrupt Control Registers

- External Pin CFIREQ# Interrupt Control Register (ICUCR3) <Address: H'0020 8104>
- CF Card Insertion Interrupt Control Register (ICUCR4) <Address: H'0020 8106>
- CF Card Removal Interrupt Control Register (ICUCR5) <Address: H'0020 8108>
- External Pin INTSW# Interrupt Control Register (ICUCR6) <Address: H'0020 810A>
- MMC Insert/Remove Interrupt Control Register (ICUCR11) <Address: H'0020 8114>
- eTRON Card Error Interrupt Control Register (ICUCR13) <Address: H'0020 8118>
- eTRON Card Receive Interrupt Control Register (ICUCR14) <Address: H'0020 811A>
- eTRON Card Transmit Interrupt Control Register (ICUCR15) <Address: H'0020 811C>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
			IEN				IRQ			ISMOD			ILEVEL		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'1007>

b	Bit name	Function	R	W
0-2	No functions assigned.		0	-
3	IEN Interrupt request acceptance enable bit	0: Disable interrupt request acceptance 1: Enable interrupt request acceptance	R	W
4-6	No functions assigned.		0	-
7	IREQ Interrupt request bit	[For read] 0: Interrupt not requested 1: Interrupt requested [For write] 0: Has no effect 1: Clear interrupt request	R	*
8, 9	No functions assigned.		0	-
10, 11	ISMOD Input sense mode select bits	00: Falling edge sense 01: Low level sense 10: Rising edge sense 11: High level sense	R	W
12	No functions assigned.		0	-
13-15	ILEVEL Interrupt priority level select bits	000: Interrupt priority level 0 001: Interrupt priority level 1 010: Interrupt priority level 2 011: Interrupt priority level 3 100: Interrupt priority level 4 101: Interrupt priority level 5 110: Interrupt priority level 6 111: Interrupt priority level 7 (interrupts disabled)	R	W

Note: The asterisk (*) in the W column denotes: writing 0 has no effect; writing 1 clears the bit.

Note: Interrupt request input sense modes for interrupt requests from the PLD internal peripheral I/O are shown below.

<<Rising edge sense>>
CF card removal interrupt
<<Falling edge sense>>
CF card insertion interrupt
<<High level sense>>
eTRON card error interrupt, eTRON card receive interrupt, eTRON card transmit interrupt

(1) Interrupt request acceptance enable, IEN (b3)

This bit enables or disables acceptance of interrupt requests.
Clearing this bit to 0 disables interrupt requests to the Interrupt Controller from being accepted, so that even when an interrupt request to the Interrupt Controller occurs, the interrupt request bit (IREQ) is not set to 1. However, if this bit is cleared to 0 while the interrupt request bit remains set to 1, the interrupt request bit is not cleared.
Setting this bit to 1 enables interrupt requests to the Interrupt Controller to be accepted, so that when an interrupt request to the Interrupt Controller occurs, the interrupt request bit (IREQ) is set to 1.

(2) Interrupt request bit, IREQ (b7)

This bit is set to 1 when an interrupt request from one of the interrupt sources occurs while interrupt request acceptance is enabled (IEN = 1).
Although this bit is set irrespective of the value set by the interrupt priority level select bits (ILEVEL), whether an interrupt request to the M32192 is actually output depends on priority resolution that is determined according to ILEVEL.
The following shows conditions under which the interrupt request bit is cleared to 0.

[For edge-sensed interrupts]

- Cleared to 0 when the Interrupt Status Register is read out while FPGAINT is asserted high.
- Cleared to 0 when this bit is set by writing 1 in software.

[For level-sensed interrupts]

- Cleared to 0 when the interrupt request is dropped by the interrupt source that generated it.

If the interrupt request bit is cleared to 0 in software at the same time it is set to 1 for an interrupt request generated, the latter has priority, so that the bit is set.

(3) Input sense mode select bits, ISMOD (b10-b11)

These bits are effective in only the ICUCR3.
These bits select interrupt acceptance input sense mode.

(4) Interrupt priority level select bits, ILEVEL (b13-b15)

These bits set the interrupt priority level of each interrupt source.

Table 3.6.3 shows the relationship between ILEVEL values and priority levels.

Note: Even when ILEVEL = '111' (interrupts disabled), the interrupt request bit is set when an interrupt request is generated.

Table 3.6.3 ILEVEL Values and Priority Levels

Set value of ILEVEL	Priority level	External pin FPGAINT status
0	High	Outputs a high when selected interrupt request is sent to the M32192
1	↑	
2	|	
3	|	
4	|	
5	↓	
6	Low	
7	Interrupts disabled	Always low.

Note: This applies when IREQ = 1.

Whether interrupt requests from FPGAINT are finally accepted by the M32192 should be determined by the Interrupt Controller in the M32192.

3.6.6 Hardware Priority and Interrupt Sources

Table 3.6.4 shows the hardware priority of each interrupt source and the timing at which interrupt requests from the respective interrupt sources are generated.

Table 3.6.4 Hardware Priority and Interrupt Request Timing

Interrupt source	Hardware priority	Interrupt request generation timing
External pin CFIREQ#	High	When active edge or level on external CFIREQ# pin is detected
CF card insertion	↑	When CompactFlash card is inserted
CF card removal	|	When CompactFlash card is removed
External pin INTSW#	|	When active edge or level on external INTSW# pin is detected
MMC insertion/removal	|	When MMC is inserted or removed
eTRON card error	|	When error occurred in communication with eTORN card
eTRON card receive	↓	When data is received from eTORN card
eTRON card transmit	Low	When eTORN card transmit buffer is emptied

3.6.7 Description of Interrupt Operation

[Interrupt requests to the M32192]

Interrupt requests from the PLD internal peripheral I/O and external pins are compared for priority resolution with the ILEVEL set by the interrupt control register (and with the fixed hardware priority). The selected interrupt request is forwarded to the M32192 by outputting a high from the FPGAINT pin.

However, if multiple interrupt requests occur at the same time, their priority is resolved following the procedure described below to determine which interrupt request should be output to the M32192.

(1) Priority levels set by ILEVEL in the respective interrupt control registers are compared to select the highest priority interrupt request.

(2) If two or more of these interrupt requests have the same ILEVEL value, they are resolved according to the fixed hardware priority, and the highest priority interrupt request is forwarded to the M32192.

There are following interrupt priority and interrupt mask settings:

<Setting interrupt priority for each interrupt source>

Set the ILEVEL in each interrupt control register. (Set ILEVEL = ‘111’ to disable the interrupt.)

<Controlling external interrupts to the M32192>

Set the ILEVEL bits in the interrupt control register for the external pin TIN0 of the M32192.

3.7 I/O Controller (IOC)

3.7.1 Outline of the IOC

The PLD contains an I/O Controller (IOC).

The IOC controls the MMC and CF power supplies, LEDs, switches, external bus signal and external SRAM.

3.7.2 IOC Related Registers

Figure 3.7.1 shows IOC register mapping, with reach register detailed in the pages that follow. Note that if data is written to any use-prohibited area, device operation cannot be guaranteed.

M32192 Address	+0 address b0 – b7	+1 address b8 – b15
H'0021_4000	Card Power Supply Control Register (CDPCR)	
H'0021_4002	LED Control Register (LEDCR)	
H'0021_4004	Switch Status Register (SWSTS)	
H'0021_4006 : H'0021_4012	(Use of this area prohibited)	
H'0021_4014	CS1 Wait Control (CS1WCR)	
H'0021_4016 : H'0021_7FFE	(Use of this area prohibited)	

Figure 3.7.1 IOC Register Mapping

3.7.3 Card Power Supply Control Register

■ Card Power Supply Control Register (CDPCR) <Address: H'0021 4000>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
														CDP1	CDP0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-13	No functions assigned.		0	-
14	CDP1 MMC power supply control bit	0: Output a high from MMC_ON# pin 1: Output a low from MMC_ON# pin	R	W
15	CDP0 CompactFlash power supply control bit	0: Output a high from CF_ON# pin 1: Output a low from CF_ON# pin	R	W

Note: This register can only be accessed for write when a CF or MMC is inserted in place.

(1) MMC power supply control bit, CDP1 (b14)

This bit sets the output level at the MMC_ON# pin.

Setting this bit to 1 outputs a low from the MMC_ON# pin, in which case the power for the MMC to be supplied.

Setting this bit to 0 outputs a high from the MMC_ON# pin, causing the power for the MMC is not supplied.

(2) CompactFlash power supply control bit, CDP0 (b15)

This bit sets the output level at the CF_ON# pin.

Setting this bit to 1 outputs a high from the CF_ON# pin, causing the power for the CF to be supplied.

Setting this bit to 0 outputs a low from the CF_ON# pin, in which case the power for the CF is not supplied.

3.7.4 LED Control Register

■ LED Control Register (LEDCR) <Address: H'0021 4002>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
														LED2	LED1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

<Reset: H'0003>

b	Bit name	Function	R	W
0-13	No functions assigned.		0	-
14	LED2 LED2 control bit	0: Turn LED2 off 1: Turn LED2 off	R	W
15	LED1 LED1 control bit	0: Turn LED1 off 1: Turn LED1 on	R	W

(1) LED2 control bit, LED2 (b14)

This bit sets the output level at the LED2 pin.

Setting this bit to 1 outputs a low from the LED2 pin, causing LED2 to turn on.

Setting this bit to 0 outputs a high from the LED2 pin, causing LED2 to turn off.

(2) LED1 control bit, LED1 (b15)

This bit sets the output level at the LED1 pin.

Setting this bit to 1 outputs a low from the LED1 pin, causing LED1 to turn on.

Setting this bit to 0 outputs a high from the LED1 pin, causing LED1 to turn off.

3.7.5 Switch Status Register

■ Switch Status Register (IOSWSTS) <Address: H'0021 4004>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
						SW2	SW1								
0	0	0	0	0	0	?	?	0	0	0	0	0	0	0	0

<Reset: H'0?00>

b	Bit name	Function	R	W
0-5	No functions assigned.		0	-
6	SW2 SW2 status bit	0: SW2 is at OFF state 1: SW2 is at ON state	R	-
7	SW1 SW1 status bit	0: SW1 is at OFF state 1: SW1 is at ON state	R	-
8-15	No functions assigned.		0	-

Note: The initial value varies depending on whether the switch is on or off.

(1) SW2 status bit, SW2 (b6)

Check this bit to determine the SW2 status.

This bit is set to 1 when SW2 is on, and is cleared to 0 when the switch is off.

(2) SW1 status bit, SW1 (b7)

Check this bit to determine the SW1 status.

This bit is set to 1 when SW1 is on, and is cleared to 0 when the switch is off.

3.7.6 CS1 Wait Control Register

■ CS1 Wait Control Register (CS1WCR) <Address: H'0021 4014>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
								WAIT1							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-7	No functions assigned.		0	-
8-11	WAIT1 CS1 wait cycles select bits	0000: 0 wait 0001: 1 wait : : 1111: 15 wait	R	W
12-15	No functions assigned.		0	-

(1) CS1 wait cycles select bits, WAIT1 (b8-b11)

These bits are used to set the number of wait cycles for the CS1 area.

Make sure the same value as set by the CS1 control register (CS1WTCR) of the M32192 (i.e., 4 wait cycles) is set in this register.

Figures 3.7.2 and 3.7.3 show the timing with which the CS1 area is accessed for read and write.

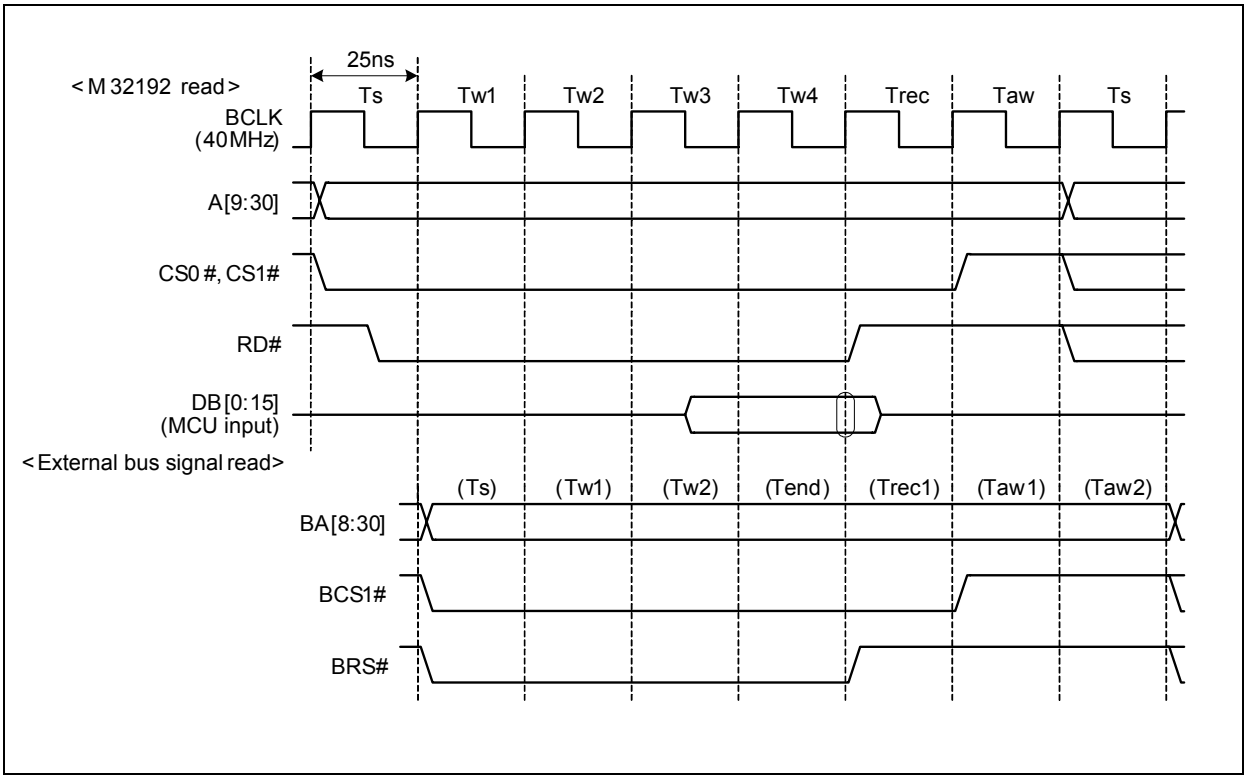


Figure 3.7.2 CS1 Area Read Timing

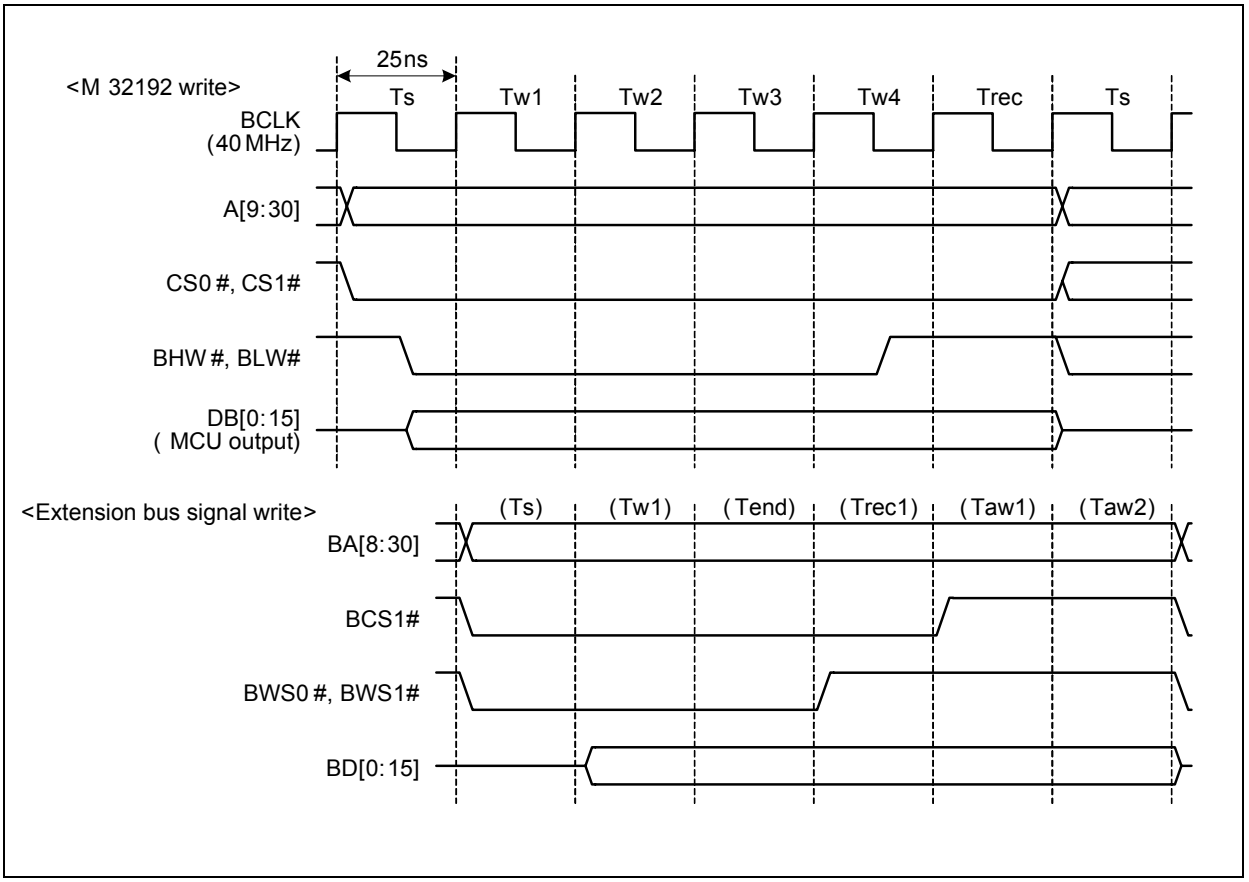


Figure 3.7.3 CS1 Area Write Timing

3.8 CRC Calculation Circuit (CRCC)

3.8.1 Outline of the CRCC

The PLD contains a CRC Calculation Circuit. CRC (Cyclic Redundancy Check) is a method for detecting errors in communication data by comparing the CRC code derived from the communication data by processing it with a generator polynomial and the CRC check data transmitted from the other side.

The CRC Calculation Circuit allows to generate this CRC code.

The following lists the supported generator polynomials:

- CRC-7 (X^7+X^3+1): CRC7
- CRC-CCITT ($X^{16}+X^{12}+X^5+1$): CRC16
- CRC-16 ($X^{16}+X^{15}+X^2+1$): CRC16A

3.8.2 CRCC Related Registers

Figure 3.8.1 shows CRCC register mapping, with each register detailed in the pages that follow. If data is written to any use-prohibited area, device operation cannot be guaranteed.

M32192 Address	+0 address b0 – b7	+1 address b8 – b15
H'0021_8000	CRC7 Data Register (CRC7DATA)	
H'0021_8002	CRC7 Data Input Register (CRC7INDATA)	
H'0021_8004	CRC16 Data Register (CRC16DATA)	
H'0021_8006	CRC16 Data Input Register (CRC16INDATA)	
H'0021_8008	CRC16A Data Register (CRC16ADATA)	
H'0021_800A	CRC16A Data Input Register (CRC16AINDATA)	
H'0021_800C : H'0021_BFFE	(Use of this area prohibited)	

Figure 3.8.1 CRC Register Mapping

3.8.3 CRC7 Data Register

■ CRC7 Data Register (CRC7DATA) <Address: H'0021 8000>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
									CRC7D						
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-8	No functions assigned.		0	-
9-15	CRC7D CRC7 data bits	These bits store the CRC7 calculation result.	R	W

(1) CRC7 data bits, CRC7D (b9-b15)

These bits are used to store the calculation result obtained based on the CRC7 generator polynomial (X^7+X^3+1).

3.8.4 CRC7 Data Input Register

■ CRC7 Data Input Register (CRC7INDATA) <Address: H'0021 8002>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
								CRC7IN							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-7	No functions assigned.		0	-
8-15	CRC7IN CRC7 input data bits	These bits store the data on which to perform CRC7 calculation.	R	W

(1) CRC7 input data bits, CRC7IN (b8-b15)

These bits are used to set the target data on which CRC7 calculation is to be performed.

When data is written to this register, CRC code is produced based on the written data and the content of the CRC7 data register, with the result written to the CRC7 data register.

3.8.5 CRC16 Data Register

■ CRC16 Data Register (CRC16DATA) <Address: H'0021 8004>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
CRC16D															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-15	CRC16D CRC16 data bits	These bits store the CRC16 calculation result.	R	W

(1) CRC16 data bits, CRC16D (b0-b15)

These bits are used to store the calculation result obtained based on the CRC16 generator polynomial ($X^{16}+X^{12}+X^5+1$).

3.8.6 CRC16 Data Input Register

■ CRC16 Data Input Register (CRC16INDATA) <Address: H'0021 8006>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
								CRC16IN							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-7	No functions assigned.		0	-
8-15	CRC16IN CRC16 input data bits	These bits store the data on which to perform CRC16 calculation.	R	W

(1) CRC16 input data bits, CRC16IN (b8-b15)

These bits are used to set the target data on which CRC 16 calculation is to be performed.

When data is written to this register, CRC code is produced based on the written data and the content of the CRC16 data register, with the result written to the CRC16 data register.

3.8.7 CRC16A Data Register

■ CRC16A Data Register (CRC16ADATA) <Address: H'0021 8008>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
CRC16AD															
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-15	CRC16AD CRC16A data bits	These bits store the CRC16A calculation result.	R	W

(1) CRC16A data bits, CRC16AD (b0-b15)

These bits are used to store the calculation result obtained based on the CRC16A generator polynomial ($X^{16}+X^{15}+X^2+1$).

3.8.8 CRC16A Data Input Register

■ CRC16A Data Input Register (CRC16AINDATA) <Address: H'0021 800A>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
								CRC16AIN							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-7	No functions assigned.		0	-
8-15	CRC16AIN CRC16A input data bits	These bits store the data on which to perform CRC16A calculation.	R	W

(1) CRC16A input data bits, CRC16AIN (b8-b15)

These bits are used to set the target data on which CRC16A calculation is to be performed.

When data is written to this register, CRC code is generated in the CRC16A data register based on the written data and the content of the CRC16A data register.

3.8.9 About the CRC Calculation

- The data to be transmitted is assumed to be a high-order polynomial.
  Example: H'A1 = b'01010001 → x6 + x4 + 1

- Divided by checking polynomial P(x), and the remainder (BCC: Block Check Character) is made the CRC.
  <Example of CRC checking polynomial>
  CRC-7: P(x) = x7 + x3 + 1
  CRC-CCITT: P(x) = x16 + x12 + x5 + 1

■ Calculation on the transmitting side

(1) The transmit data is transformed into polynomial M(x).
(2) The highest-order xk of the generator polynomial P(x) and M(x) are multiplied together to produce xkM(x).
(3) xkM(x) is divided by P(x).
(4) The remainder of this division is the CRC code.
(0+0=0, 1+0 =1, 0-1=1, 0+1=1, 1+1 = 0, 1-0=1)
Note, however, that the above division is performed using modulo-2 arithmetic.

■ Calculation on the receiving side

(1) If the received data has CRC code included in it, it is divided by generator polynomial P(x). If the remainder is 0, the received data is considered normal. If it cannot be divided without a remainder, the received data is considered erratic.

3.8.10 Operation of the CRC Calculation Circuit

The following describes operation of the CRC calculation circuit. Figure 3.8.2 shows an example operation of the CRC calculation circuit.

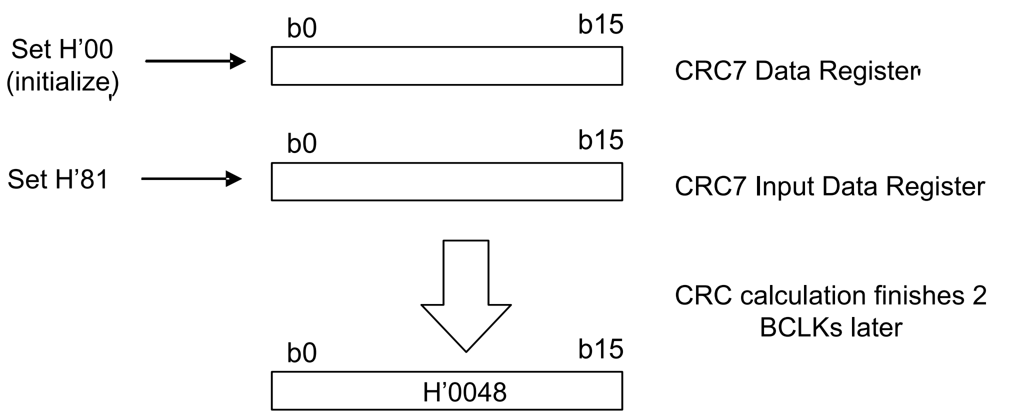
■ CRC7 calculation

(1) Set the initial value H’00 in the CRC7 data register.

(2) When one byte of data is written to the CRC7 input data register, CRC code is generated in the CRC7 data register based on the written data and the content of the CRC7 data register. CRC code generation for one byte of data finishes in 2 BCLKs.

(3) To perform CRC calculation on consecutive bytes of data, proceed to write the next data to the CRC7 input data register.

(4) The content of the CRC7 data register obtained after all of the data to be calculated have been written to the CRC7 input data register, is the CRC code.



The data H’81 when represented in binary is (b’1000 0001), so that CRC code derived from generator polynomial X7 + X3 + 1 is the remainder of (b’1000 0001) x 2^7 divided by (b’1000 1001) using modulo-2 arithmetic.

```
                                        1000    1000
1000    1001   ) 100    0000    1000    0000
                 100    0100    1000    0000
                 -------------------------------
                        100     0000    0000
                        100     0100    1000
                 -------------------------------
                                100     1000
```

Therefore, the CRC code is (b’100 1000).

Figure 3.8.2 Example Operation of the CRC Calculation Circuit

3.9 Real Time Clock Controller (RTCC)

3.9.1 Outline of the RTCC

The PLD contains a RTCC for the control of real-time clock ICs. Specifically, the RTCC controls resetting a real-time clock IC, as well as reading/writing commands and data to and from the real-time clock IC.
Table 3.9.1 outlines the RTCC.

Table 3.9.1 Outline of the RTCC

Item	Outline
Reset control	Reset control by an output port
Transfer clock	Internal clock (system clock BCLK)
Data format	Transfer data length: 16 bits, fixed Order of transfer: MSB first
Baud rate	105468-27000000 bps

3.9.2 RTCC Related Registers

Figure 3.9.1 shows RTCC register mapping, with each register detailed in the pages that follow. If data is written to any use-prohibited area, device operation cannot be guaranteed.

M32192 Address	+0 address b0	b7	+1 address b8	b15
H'0021_C000	RTC Control Register (RTCCR)			
H'0021_C002	RTC Baud Rate Register (RTCBAUR)			
H'0021_C004	RTC Write Data Register (RTCWRDATA)			
H'0021_C006	RTC Read Data Register (RTCRDDATA)			
H'0021_C008	RTCRST Output Register (RTCRSTODT)			
H'0021_C00A : H'0021_FFFE	(Use of this area prohibited)			

Figure 3.9.1 RTCC Register Mapping

3.9.3 RTC Control Register

■ RTC Control Register (RTCCR) <Address: H'0021 C000>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
														WREN	RDEN
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-13	No functions assigned.		0	-
14	WREN Write enable bit	- For write 0: <Has no effect> 1: Start writing - For read 0: Write operation not in progress 1: Write operation in progress now	R	W
15	RDEN Read enable bit	- For write 0: <Has no effect> 1: Start reading - For read 0: Read operation not in progress 1: Read operation in progress now	R	W

Note: Only writing 1 is effective.

(1) Write enable bit, WREN (b14)

Setting this bit to 1 causes the RTCC to start writing to the real-time clock IC.
This bit also indicates the status of write operation to the real-time clock IC.

(2) Read enable bit, RDEN (b15)

Setting this bit to 1 causes the RTCC to start reading from the real-time clock IC.
This bit also indicates the status of read operation from the real-time clock IC.

3.9.4 RTC Baud Rate Register

■ RTC Baud Rate Register (RTCBAUR) <Address: H'0021 C002>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
								RTCBAUR							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-7	No functions assigned.		0	-
8-15	RTCBAUR Baud rate setting bits	Set a baud rate	R	W

Note: This register can only be set while the RTC is idle (both WREN and RDEN = 0).

(1) Baud rate setting bits, RTCBAUR (b8-b15)

The system clock (BCLK) is divided by n + 1 where n = value set by these bits.

The "divided by n + 1" count source is further divided by 2 to become the transfer clock. The transfer clock is output from the RTCSCLK pin to external devices.

Figure 3.9.2 shows the equation to calculate the value to be set in the RTC baud rate register. And Table 3.9.2 lists the example of setting the RTC baud rate.

$$\text{Value to be set in the RTC baud rate register (RTCBAUR)} = \frac{f\,(BCLK)}{\text{Baud rate} \times 2} - 1$$

$$\text{Baud rate} = \frac{f\,(BCLK)}{2 \times (\text{RTCBAUR} + 1)}$$

Figure 3.9.2 Equation to Calculate the Value to Be Set in the RTC Baud Rate Register

Table 3.9.2 Example for Setting the RTC Baud Rate: f(BCLK)=40MHz

RTCBAUR	Baud rate (MHz)	RTCBAUR	Baud rate (MHz)
0 (H'0000)	20.0000	12 (H'000C)	1.5385
1 (H'0001)	10.0000	13 (H'000D)	1.4286
2 (H'0002)	6.6667	14 (H'000E)	1.3333
3 (H'0003)	5.0000	15 (H'000F)	1.2500
4 (H'0004)	4.0000	16 (H'0010)	1.1765
5 (H'0005)	3.3333	17 (H'0011)	1.1111
6 (H'0006)	2.8571	18 (H'0012)	1.0526
7 (H'0007)	2.5000	19 (H'0013)	1.0000
8 (H'0008)	2.2222	20 (H'0014)	0.9524
9 (H'0009)	2.0000	21 (H'0015)	0.9091
10 (H'000A)	1.8182	22 (H'0016)	0.8696
11 (H'000B)	1.6667	23 (H'0017)	0.8333

3.9.5 RTC Write Data Register

■ RTC Write Data Register (RTCWRDATA) <Address: H'0021 C004>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
WRDATA								WRADR							
?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

<Reset: Indeterminate>

b	Bit name	Function	R	W
0-7	WRDATA Write data bits	Write the write data to these bits.	R	W
8-15	WRADR Write address bits	Write the write address to these bits.	R	W

(1) Write data bits, WRDATA (b0-b7)

Set the write data for the RTC IC in these bits.

(2) Write address bits, WRADR (b8-b15)

Set the write address of the RTC IC in these bits.

The data set in the RTC write data register is transferred to the RTC transmit shift register by setting the write enable bit to 1.

Table 3.9.3 shows the relationship between the write data and WRADR.

Table 3.9.3 Relationship between the Write Data and WRADR

Data	WRADR	Data	WRADR
Seconds	H'80	Month	H'88
Minutes	H'82	Day of the week	H'8A
Hours	H'84	Year	H'8C
Day	H'86		

<<To write "30 seconds" data>>

(1) Write H'3080 to this register.

(2) Set the write enable bit to 1.

(3) Wait until the write operation finishes (write enable bit cleared to 0).

For details, refer to the DS1302 User's Manual.

3.9.6 RTC Read Data Register

■ RTC Read Data Register (RTCRDDATA) <Address: H'0021 C006>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
RDDATA								RDADR							
?	?	?	?	?	?	?	?	?	?	?	?	?	?	?	?

<Reset: Indeterminate>

b	Bit name	Function	R	W
0-7	RDDATA Read data bits	Read data is stored in these bits.	R	-
8-15	RDADR Read address bits	Write the read address to these bits.	R	W

(1) Read data bits, RDDATA (b0-b7)

These bits are used to read out the read data from the RTC IC.

The read data input through the RTCIO pin is received in the RTC read shift register. The received data is transferred from the RTC read shift register to these read data bits after the receive operation has finished.

Note that the read data bits are read-only bits, and no data can be written to these bits.

(2) Read address bits, RDADR (b8-b15)

Set the read address of the RTC IC in these bits.

The address set in the RTC read data register is transferred to the RTC transmit shift register by setting the read enable bit to 1, and then the data from the RTC IC is written to the read data bits.

Table 3.9.4 shows the relationship between the read data and RDADR.

Table 3.9.4 Relationship between the Read Data and RDADR

Data	RDADR	Data	RDADR
Seconds	H'81	Month	H'89
Minutes	H'83	Day of the week	H'8B
Months	H'85	Year	H'8D
Day	H'87		

<<To read "seconds" data>>

(1) Write H'0081 to this register.

(2) Set the read enable bit to 1.

(3) Wait until the read operation finishes (read enable bit cleared to 0).

(4) The 8 high-order bits read from the read data register indicates a "seconds" value.

For details, refer to the DS1302 User's Manual.

3.9.7 RTCRST Output Register

■ RTCRST Output Register (RTCRSTODT) <Address: H'0021 C008>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
															RSTO
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-14	No functions assigned.		0	-
15	RSTO RTCRST# pin output bit	0: Output a low from RTCRST# pin 1: Output a high from RTCRST# pin	R	W

(1) RTCRST# pin output bit, RSTO (b15)

This bit is used to set the output level of the RTCRST# pin.

When this bit is cleared to 0, a low is output from the RTCRST# pin to reset the RTC IC.

When this bit is set to 1, a high is output from the RTCRST# pin to reset the RTC IC.

3.10 eTRON Card Controller (ETC)

3.10.1 Outline of the ETC

The control PLD internally contains an eTRON card interface.
The eTRON card interface has the following communication method adapted for it.

- UART method
- Data length: 8 bits
- Transfer rule: Direct/inverse
- Start bit: 1 bit
- Parity bit: 1 bit

The transmit/receive data of the eTRON card is checked for errors by parity.
When a parity error is detected when receiving data, the ETC controller outputs a low to the eTCDIO pin for 1 etu (elementary time unit: 1-bit transfer time) 0.5 etu after it finished receiving the parity bit.
When an error is received from the card after the ETC controller finished sending a parity bit during transmission, it resends the data repeatedly until the data can be transferred normally.
When transmission and reception are enabled at the same time while no cards are inserted in place, the ETC controller can receive the data it itself transmitted.

3.10.2 ETC Related Registers

Figure 3.10.1 shows the ETC register mapping, with each register detailed in the pages to follow. Note that if any use-inhibited area is accessed for write, the device operation cannot be guaranteed.

M32192 Address	+0 address b0 – b7	+1 address b8 – b15
H'0023_8000	ETC Control Register (ETCCR)	
H'0023_8002	(Use of this area prohibited)	
H'0023_8004	ETC Mode Register (ETCMOD)	
H'0023_8006	ETC Status Register (ETCSTS)	
H'0023_8008	ETC Interrupt Control Register (ETCINTCR)	
H'0023_800A	ETC Baud Rate Register (ETCBAUR)	
H'0023_800C	ETC Transmit Buffer Register (ETCTXB)	
H'0023_800E	ETC Receive Buffer Register (ETCRXB)	
H'0023_8010 : H'0023_BFFE	(Use of this area prohibited)	

Figure 3.10.1 ETC Register Mapping

3.10.3 ETC Control Register

■ ETC Control Register (ETCCR) <Address: H'0023 8000>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
							RST							RXEN	TXEN
0	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0

<Reset: H'0102>

b	Bit name	Function	R	W
0-6	No functions assigned.		0	-
7	RST eTRON card reset bit	- For write 0: <Has no effect> 1: Start writing - For read 0: Reset operation not in progress 1: Reset operation in progress now	R	W
8-13	No functions assigned.		0	-
14	RXEN Receive enable bit	0: Disable reception 1: Enable reception	R	W
15	TXEN Transmit enable bit	0: Disable transmission 1: Enable transmission	R	W

(1) eTRON card reset bit, RST (b7)

Setting this bit to 1 initializes the ETC related registers and all of the internal registers of the ETC controller, at which time the eTRON card reset signal is asserted low for a period of 400 eTCCLK cycles. The reset signal is released back high 400 cycles later, at which time this bit is cleared to 0.

When reset, eTCCLK is initialized to 3.375 MHz.

(2) Receive enable bit, RXEN (b14)

Setting this bit to 1 enables data reception from the eTRON card.

(3) Transmit enable bit, TXEN (b15)

Setting this bit to 1 enables data transmission to the eTRON card.

3.10.4 ETC Mode Register

■ ETC Mode Register (ETCMOD) <Address: H'0023 8004>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
											DIR				
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-10	No functions assigned.		0	-
11	DIR Transfer rule select bit	0: Direct rule transfer 1: Inverse rule transfer	R	W
12-15	No functions assigned.		0	-

Note: This register cannot be accessed for write when communication with the eTRON card is underway.

(1) Transfer rule select bit, DIR (b11)

This bit is used to select a data transfer rule (direct or inverse).

When this bit is cleared to 0, data is transferred in even parity beginning with the LSB side (bit 15 of the ETC transmit buffer register). Therefore, data is transferred in order of bit 15, bit 14,..., bit 9, and bit 8 of the ETC transmit buffer register, with a 1 representing the high level and a 0 representing the low level.

When this bit is set to 1, data is transferred in odd parity beginning with the MSB side (bit 0 in the ETC transmit buffer register). Therefore, data is transferred in order of bit 8, bit 9,..., bit 14, and bit 15 of the ETC transmit buffer register, with a 1 representing the low level and a 0 representing the high level.

Figure 3.10.2 shows an example data transfer (0xAC) performed according to each transfer rule.

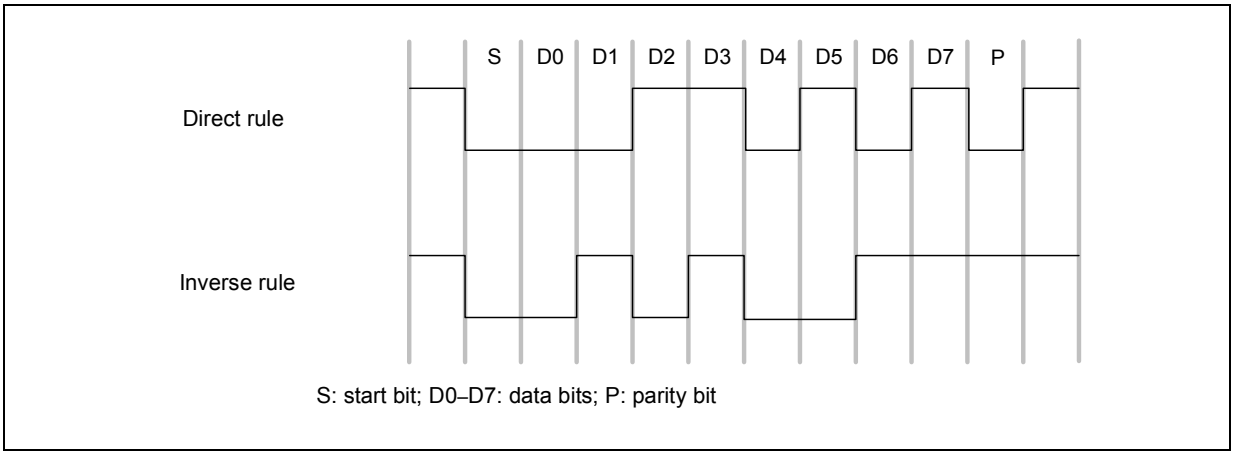


Figure 3.10.2 Example Data Transfer (0xAC) by Each Transfer Rule

3.10.5 ETC Status Register

■ ETC Status Register (ETCSTS) <Address: H'0023 8006>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
						RXSC	TXSC	ESSTS	PERR	OERR			RXCP	TXCP	TEMP
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-5	No functions assigned.		0	-
6	RXSC Receive shift register status flag	0: Not receiving data 1: Receiving data now	R	-
7	TXSC Transmit shift register status flag	0: Not transmitting data 1: Transmitting data now	R	-
8	ESSTS Error signal status flag	0: No error 1: Error found	R	*
9	PERR Receive parity error flag	0: No error 1: Error found	R	*
10	OERR Receive overrun error flag	0: No error 1: Error found	R	*
11, 12	No functions assigned.		0	-
13	RXCP Reception completed flag	0: No data exists in the receiver buffer register 1: Data exists in the receiver buffer register	R	-
14	TXCP Transmission completed flag	0: Data exists in the transmit shift register 1: No data exists in the transmit shift register	R	-
15	TEMP Transmit buffer empty flag	0: Data exists in the transmit buffer 1: No data exists in the transmit buffer	R	-

Note: The asterisk (*) in the W column denotes that writing a 0 only is effective.

(1) Receive shift register status flag, RXSC (b6)

This bit allows the operating status of the receive shift register to be referenced. The following shows the conditions under which this bit is set or cleared.

The set/clear timing of this bit has a finite time lag after the set or clear condition is detected. If this bit is to be referenced after disabling data reception, this time lag should be taken into consideration, providing a time allowance equal to approximately 1 transfer data bit.

- Set condition
  The bit is set to 1 when the start bit is detected (falling edge of data bit).
- Clear condition
  The bit is cleared to 0 when the ETC controller finished receiving the parity bit.

(2) Transmit shift register status flag, TXSC (b7)

This bit allows the operating status of the transmit shift register to be referenced. The following shows the conditions under which this bit is set or cleared.

The set/clear timing of this bit has a finite time lag after the set or clear condition is detected. If this bit is to be referenced after disabling data transmission, this time lag should be taken into consideration, providing a time allowance equal to approximately 1 transfer data bit.

- Set condition
  The bit is set to 1 when the start bit is detected (falling edge of data bit).
- Clear condition
  The bit is cleared to 0 a finite time equal to 2 transfer data bits after the ETC controller transmitted the parity bit.

(3) Error signal status flag, ESSTS (b8)

This bit indicates the status of the error signal returned from the receiver side during data transmission. The following shows the conditions under which this bit is set or cleared.

- Set condition
  The bit is set to 1 when a signal indicating a parity error is sent from the receiver side.
- Clear condition
  The bit is not automatically cleared in hardware. Write 0 to clear it.

(4) Receive parity error flag, PERR (b9)

This bit allows the status of the receive parity error occurring in the received data. The following shows the conditions under which this bit is set or cleared.

- Set condition
  The bit is set to 1 when a parity error is detected during data reception. In this case, serial data consisting of 0’s is transmitted for a 1 clock period.
- Clear condition
  The bit is not automatically cleared in hardware. Write 0 to clear it.

(5) Receive overrun error flag, OERR (b10)

An overrun error is assumed when while received data exists in the receive buffer register and receive shift register, the ETC controller starts receiving the next receive data. The following shows the conditions under which this bit is set or cleared.

- Set condition
  The bit is set to 1 when an overrun error is detected during data reception.
- Clear condition
  The bit is not automatically cleared in hardware. Write 0 to clear it.

(6) Reception completed flag, RXCP (b13)

This bit allows to inspect whether data is present in the receive buffer register. The following shows the conditions under which this bit is set or cleared.

- Set condition
  The bit is set to 1 when valid received data has been transferred from the receive shift register to the receive buffer register.
- Clear condition
  The bit is cleared to 0 by reading data out of the receive buffer register. Note that the bit is not cleared by reading out the status register.

(7) Transmission completed flag, TXCP (b14)

This bit allows to inspect whether data is present in the transmit shift register. The following shows the conditions under which this bit is set or cleared.
If this bit is cleared to 0, it means that the transmit shift register contains some data which has not been transmitted yet.
If this bit is set to 1, it means that the transmit shift register does not contain any data.

- Set condition
  If one of the following conditions is met when the ETC controller has finished sending data from the transmit shift register, no transmit data is transferred from the transmit buffer register to the transmit shift register, so that the transmit shift register becomes empty, in which case the bit is set to 1.
  - No data exists in the transmit buffer register (TEMP = 1).
  - The transmit enable bit (TXEN in the ETC control register) is 0.
- Clear condition
  The bit is cleared to 0 when transmit data has been transferred from the transmit buffer register to the transmit shift register.

(8) Transmit buffer empty flag, TEMP (b15)

This bit allows to inspect whether data is present in the transmit buffer register. The following shows the conditions under which this bit is set or cleared.
If this bit is cleared to 0, it means that the transmit buffer register contains some data which has not been transferred to the transmit shift register yet.
If this bit is set to 1, it means that the transmit buffer register does not contain any data.

- Set condition
  The bit is set to 1 when transmit data has been transferred from the transmit buffer register to the transmit shift register.
- Clear condition
  The bit is cleared to 0 by writing to the transmit buffer register.

3.10.6 ETC Interrupt Control Register

■ ETC Interrupt Control Register (ETCINTCR) <Address: H'0023 8008>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
												EREN	RXIEN		TEMPIEN
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

<Reset: H'0000>

b	Bit name	Function	R	W
0-11	No functions assigned.		0	-
12	ERIEN Error-generated interrupt enable bit	0: Disable interrupt 1: Enable interrupt	R	W
13	RXIEN Reception-completed interrupt enable bit	0: Disable interrupt 1: Enable interrupt	R	W
14	No functions assigned.		0	-
15	TEMPIEN Transmit buffer empty interrupt enable bit	0: Disable interrupt 1: Enable interrupt	R	W

(1) Error-generated interrupt enable bit, ERIEN (b12)

This bit specifies whether the relevant interrupt should be enabled when an error occurs during data transmission or reception.

If this bit is set to 0, the interrupt is disabled. If this bit is set to 1, the interrupt is enabled.

The following shows the cases in which such an error may occur.

- During data transmission
  When an error signal is returned
- During data reception
  When an overrun error occurred or when a parity error occurred

(2) Reception-completed interrupt enable bit, RXIEN (b13)

This bit specifies whether the relevant interrupt should be enabled when a receive operation has terminated normally, with the data placed in the receive buffer register.

If this bit is set to 0, the interrupt is disabled. If this bit is set to 1, the interrupt is enabled.

(3) Transmit buffer empty interrupt enable bit, TEMPIEN (b15)

This bit specifies whether the relevant interrupt should be enabled when the transmit data buffer is emptied.

If this bit is set to 0, the interrupt is disabled. If this bit is set to 1, the interrupt is enabled.

3.10.7 ETC Baud Rate Register

■ ETC Baud Rate Register (ETCBAUR) <Address: H'0023 800A>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
ETCBAUR															
0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

<Reset: H'0007>

b	Bit name	Function	R	W
0-15	ETCBAUR Baud rate setting bits	Set a baud rate.	R	W

Note: This register can only be set while the ETC is inactive (ETCCR = H'0000).

(1) Baud rate setting bits, ETCBAUR (b0-b15)

The system clock (BCLK) divided by 2 x (n + 1) where 'n' is the value set by this bit becomes the clock that is input to the clock for the eTRON card (eTCCLK). The value of this eTCCLK is divided by 382, which yields the baud rate used for data transfer. After reset, eTCCLK is 3.1215 MHz, and the baud rate is 8,181 bps.
Figure 3.10.3 shows the equation to calculate the value to be set in the ETC baud rate register.

$$\text{ETC baud rate register setting value (ETCBAUR)} = \frac{f(BCLK)}{\text{Baud rate} \times 764} - 1$$

$$\text{Baud rate} = \frac{f(BCLK)}{764 \times (\text{ETCBAUR} + 1)}$$

Figure 3.10.3 Equation to Calculate the ETC Baud Rate Register Setting Value

Table 3.10.1 Example of ETC Baud Rate Setting where f(BCLK) = 40 MHz

ETCBAUR	Baud rate (bps)	ETCBAUR	Baud rate (bps)
0 (H'0000)	52356.0	99 (H'0063)	523.6
1 (H'0001)	26178.0	499 (H'01F3)	104.7
2 (H'0002)	17452.0	999 (H'03E7)	52.4
3 (H'0003)	13089.0	4999 (H'1387)	10.5
4 (H'0004)	10471.2	9999 (H'270F)	5.2
5 (H'0005)	8726.0	65535 (H'FFFF)	0.8
6 (H'0006)	7479.4		
7 (H'0007)	6544.5		
8 (H'0008)	5817.3		
9 (H'0009)	5235.6		
10 (H'000A)	4759.6		
11 (H'000B)	4363.0		

3.10.8 ETC Transmit Buffer Register

■ ETC Transmit Buffer Register (ETCTXB) <Address: H'0023 800C>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
								ETCTXB							
0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

<Reset: H'00??>

b	Bit name	Function	R	W
0-7	No functions assigned.		0	-
8-15	ETCTXB Transmit data bits	Write transmit data to these bits.	R	W

(1) Transmit data bits, ETCTXB (b8-b15)

These bits are used to set the data to be transmitted.

When all of the following conditions are met, the data set in the ETC transmit buffer register is transferred to the ETC transmit shift register.

- The transmit enable bit (bit 15 in the ETC control register) is 1.
- Data exists in the ETC transmit buffer register (TEMP in the ETC status register = 0).
- No data exists in the ETC transmit shift register (TXCP in the ETC status register = 1 or the ETC controller has just finished transmitting the data of the ETC transmit shift register).

3.10.9 ETC Receive Buffer Register

■ ETC Receive Buffer Register (ETCRXB) <Address: H'0023 800E>

b0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	b15
								ETCRXB							
0	0	0	0	0	0	0	0	?	?	?	?	?	?	?	?

<Reset: H'00??>

b	Bit name	Function	R	W
0-7	No functions assigned.		0	-
8-15	ETCRXB Received data bits	Received data is stored in these bits.	R	-

(1) Receive data bits, ETCRXB (b8-b15)

These bits are used to read out the received data.

If while receive operation is enabled (RXEN in the ETC Status Register = 1) all bits of the received data have been placed in the ETC receive shift register and no data exists in the ETC receive buffer register, the received data is transferred from the ETC receive shift register to the ETC receive buffer register.

The ETC receive buffer register is a read-only register, so that no data can be written into it.

3.10.10 ETC Access Timing

(1) Data transmission

Figure 3.10.4 shows ETC transmit timing.

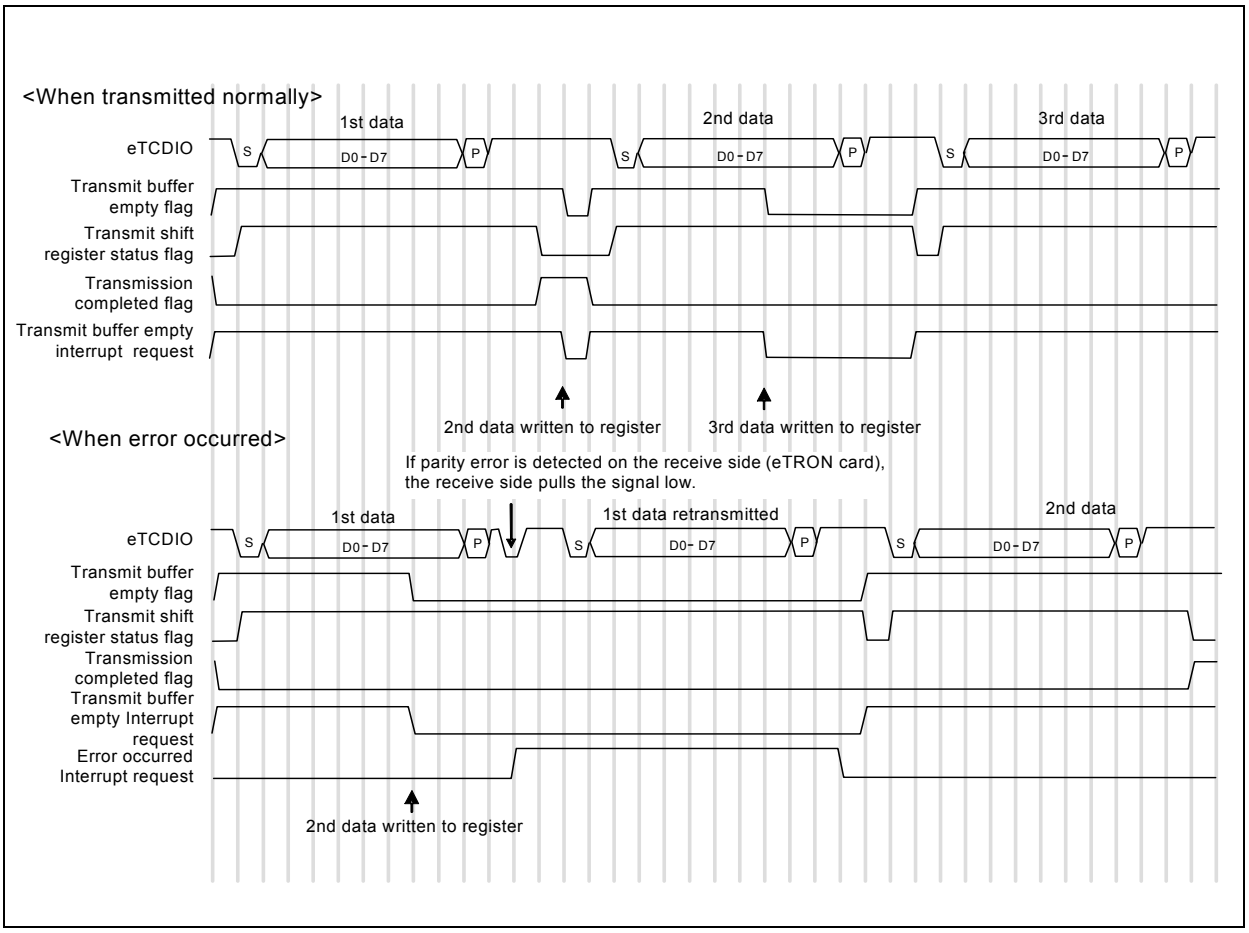


Figure 3.10.4 ETC Transmit Timing

(2) Data reception

Figure 3.10.5 shows ETC receive timing.

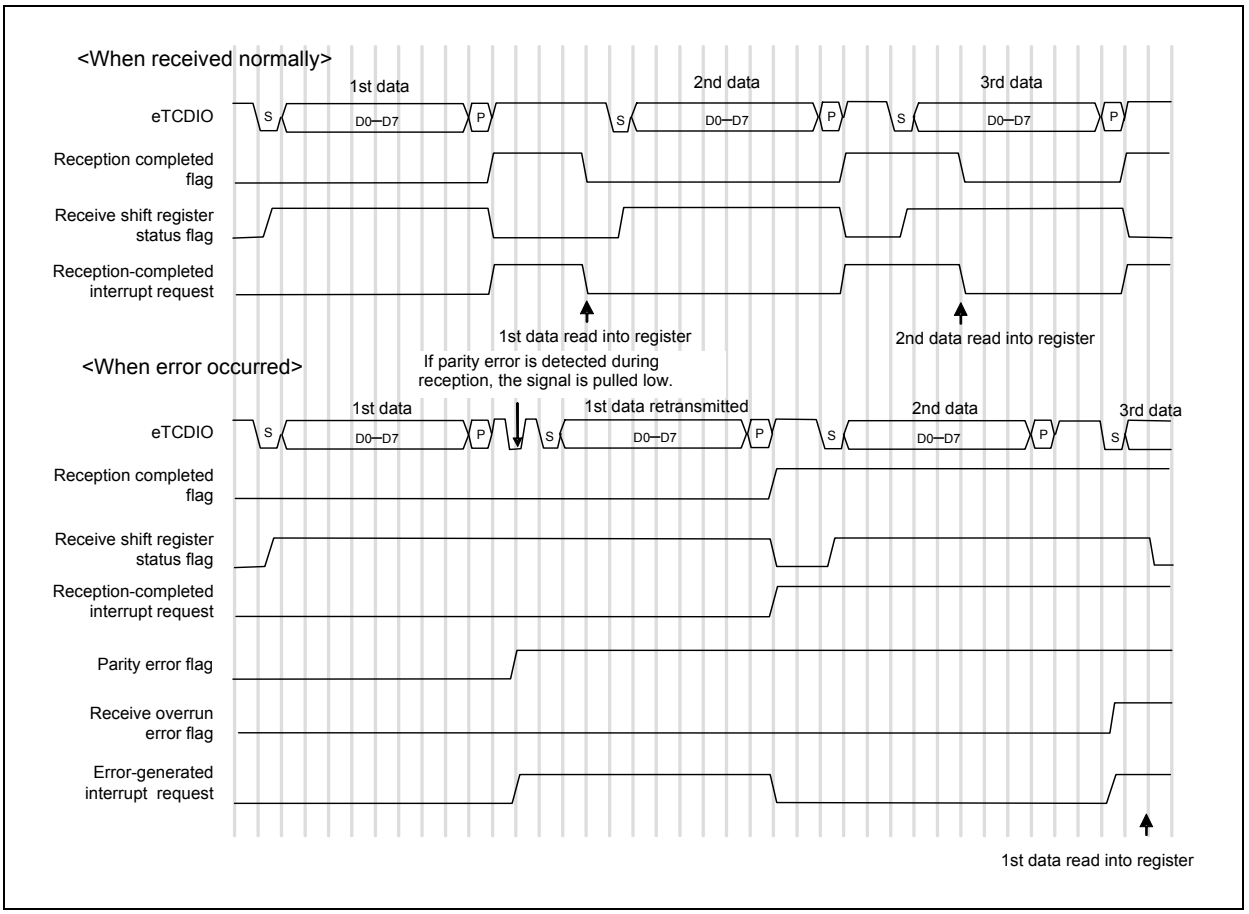


Figure 3.10.5 ETC Receive Timing

3.11 System Configuration Data (SYSC)

The control PLD has stored in it the data indicating the M3T-M32192UT-CPU version, PLD updated date, and PLD version. This data can be read out as internal ROM data of the PLD. The stored data is represented by ASCII code.

Figure 3.11.1 shows an address map of the system configuration data.

M32192 Address	+0	+1	+2	+3	+4	+5	+6	+7	+8	+9	+A	+B	+C	+D	+E	+F
H'0023_C000	M	3	T	-	M	3	2	1	9	2	U	T	(sp)	C	*	*
H'0023_C010	D	a	t	e	:	X	X	-	X	X	-	X	X	*	*	*
H'0023_C020	V	e	r	.	:	Y	Y	.	Y	Y	.	Y	Y	*	*	*
H'0023_C030 : H'0023_FFFE	(Use of this area prohibited)															

Note 1: “(sp)” denotes a space (H'20 for ASCII code).
Note 2: The asterisk (*) denotes H’00.
Note 3: X contains a date (yy-mm-dd) (e.g., 04-09-01).
Note 4: Y contains a PLD version number (e.g., 01.00.00).

Figure 3.11.1 System Configuration Data Address Map

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4. LAN Extension Board

4.1 External Specifications

Table 4.1.1 lists external specifications of the M3T-M32RUT-LAN Rev.B.

Table 4.1.1 External Specifications of the M3T-M32RUT-LAN Rev.B

Item	Content
Compatible µT-Engine board	R0P3219TR001MRK from Renesas Technology
Control PLD	ALTERA EP20K60EFC144-2 - Operating clock: EXCLK (BCLK) LAN controller access control - Interrupt controller - DIO controller
LAN controller	SMSC: LAN91C111 - Operating clock: XTAL1 = 25 MHz
Power supply	3.3 V DC supplied from the extension bus
Interface connector	- Extension bus connector: Kyocera Elco 10 5603 14 0202 861 - LAN interface connector: Amphenol RJHS-5381
External dimensions	Dimensions: 60 mm x 85 mm; Mounting: 6-layered double-sided mount

4.2 Functional Blocks

Figure 4.2.1 shows the functional blocks of the M3T-M32RUT-LAN Rev.B.

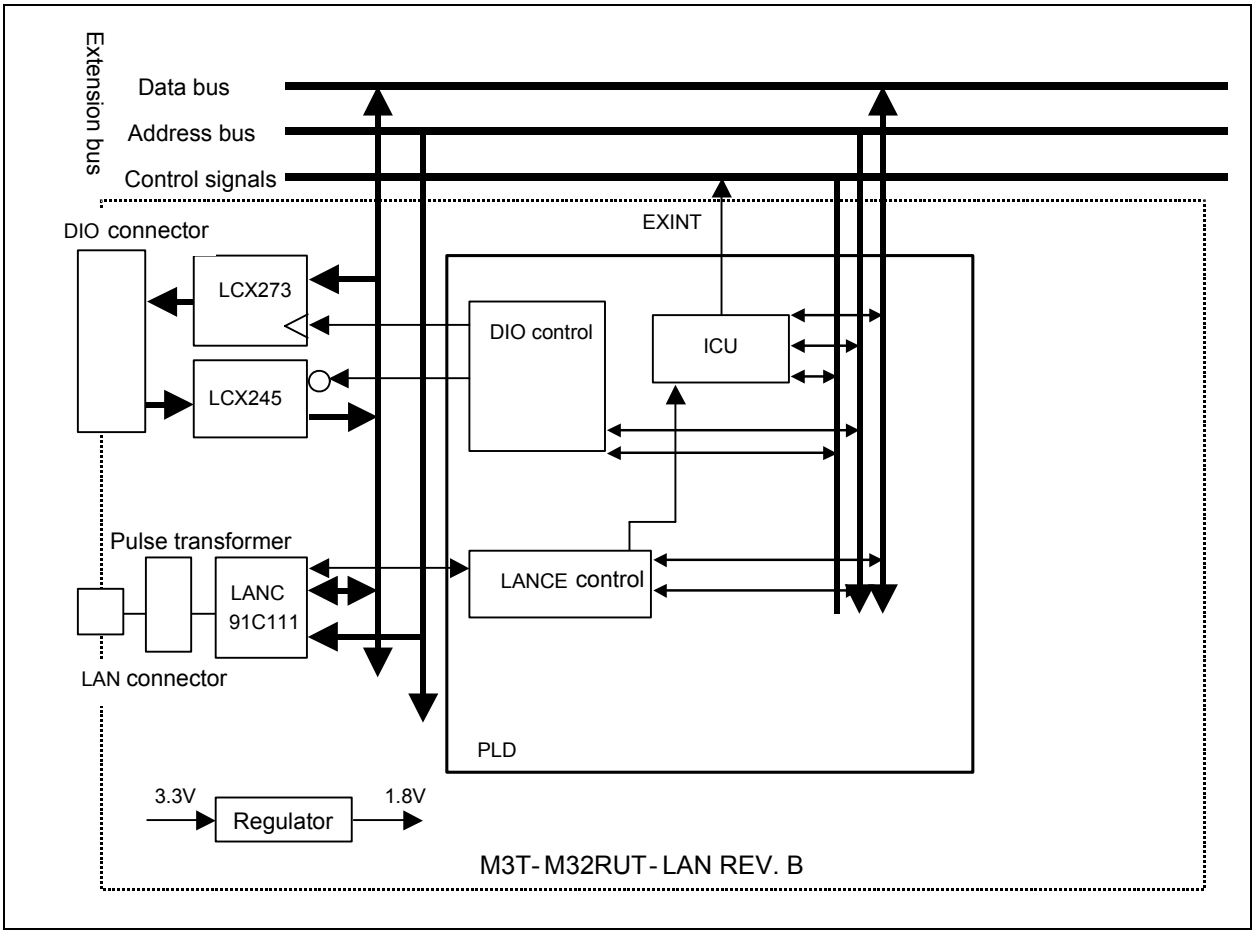

Figure 4.2.1 Functional blocks of the M3T-M32RUT-LAN Rev.B

4.3 Mapping of the LAN Extension Board Space

Figure 4.3.1 shows mapping of the LAN board space.

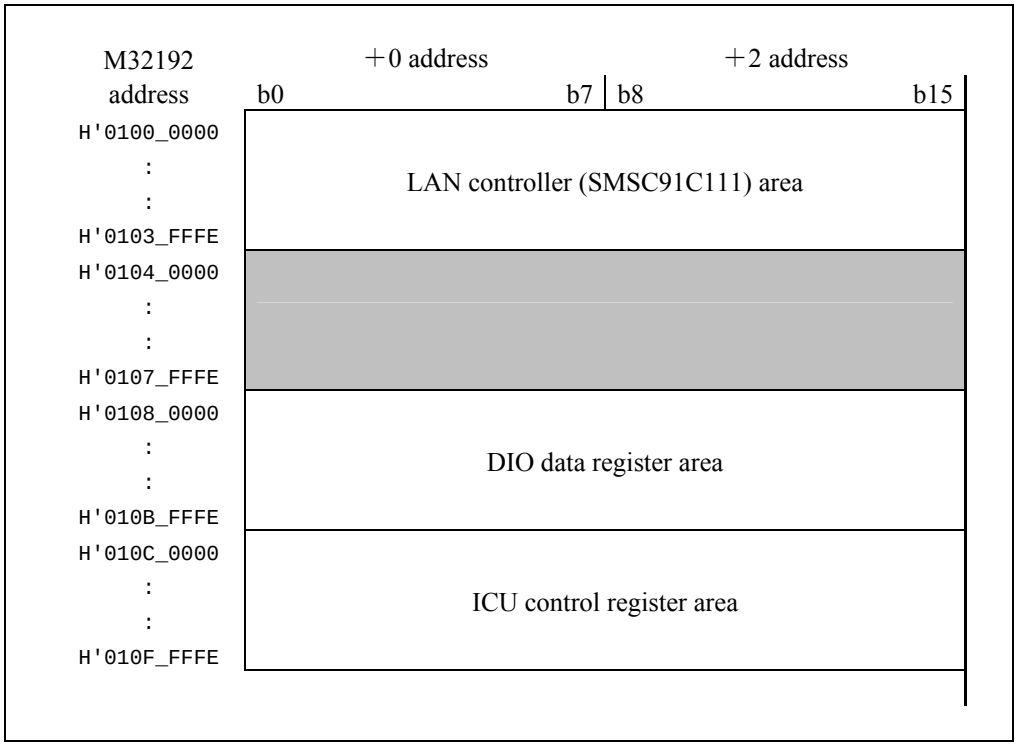

Figure 4.3.1 Mapping of the LAN board space

4.4 Outline of the PLD

4.4.1 Device Overview

The PLD on the M3T-M32RUT-LAN Rev.B is a large-scale PLD that controls the peripheral I/O devices. For this PLD, the EP20K60E, or the APEX20K family device made by ALTERA, is used to control LAN access and DIO access. Table 4.1 lists specifications of the device (ALTERA EP20K60EFC144-2).

Table 4.1 Specifications of the Device (ALTERA EP20K60EFC144-2)

Item	Content
Internal power supply voltage	1.8V
External pin power supply voltage	3.3V
Number of standard gates	60,000
Number of system gates	162,000
Number of logic elements	2,560
Number of RAM bits	32,768
Speed grade	-2
Package	144-pin FBGA (20 mm x 20 mm)
Number of I/O pins	93

4.4.2 Functional Outline

Table 4.2 lists the functional outline of the PLD on the M3T-M32RUT-LAN Rev.B.

Table 4.2 Functional Outline of the PLD

Functional block	Outline
LAN controller access control	Generates access control signals for the LAN controller (LAN91C111).
DIO controller access control	Generates output port latch clock signal and input port enable signal.

4.5 DIO

4.5.1 Outline of the DIO

The DIO consists of an input-only 8-bit and an output-only 8-bit parallel port.

Reading the DIO data register permits the input port value of the DIO connector to be read out. Writing to the DIO data register permits data to be forwarded to the output port of the DIO connector.

4.5.2 DIO Related Register List

Figure 4.4 lists the registers associated with the DIO. If the use-prohibited area is accessed for write, the device operation cannot be guaranteed.

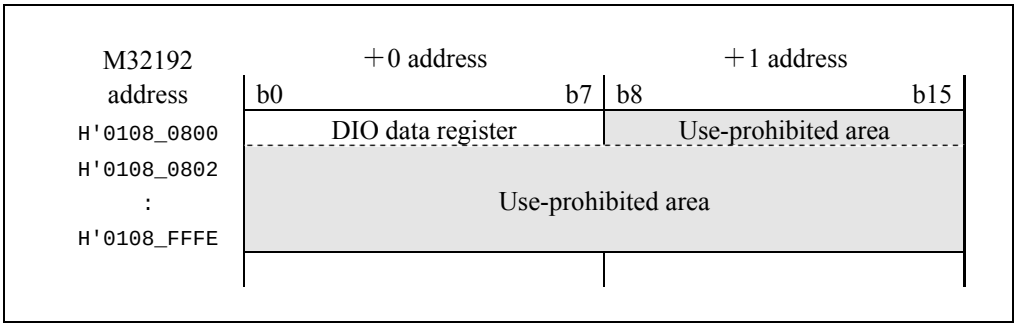

Figure 4.4 DIO related register list

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5. Extension Board Specifications

5.1 Outline of the Extension Board

The term “extension board” is a generic name for the daughter boards used for functional extension, which is connected to the system via the extension bus connector of the CPU board M3T-M32192UT-CPU. By connecting the M32192 address bus, data bus, bus control signals, and I/O ports of the extension bus connector with the user’s hardware IP, the M3T-M32192UT-CPU can be used as a component to verify and execute the hardware IP.

5.2 Extension Bus Connectors

5.2.1 Type Names of Extension Bus Connectors

The extension bus connectors shown below are used to connect an extension board with the CPU board by stacking one on top of another. There are two types of extension bus connectors, PLUG and RECE. The CPU board has only the RECE-type connector mounted on it. To connect an extension board with the CPU board by stacking one on top of another, prepare the PLUG-type connector on the CPU board side and the RECE-type connector on the other side of the extension board. The manufacturer names and type numbers of extension bus connectors are shown below.

- PLUG: 14 5603 14 0202 861 made by Kyocera Elco Co., Ltd.
- RECE: 24 5603 14 0202 861 made by Kyocera Elco Co., Ltd.

This extension bus connector comes in the same external form for both T-Engine and µT-Engine, but has different signal assignments for each. For this reason, the connector uses a key structure (internal concave and convex) to prevent erroneous insertion.
The key structure can be identified by a key code (xxxx part in 24 5603 14 xxxx). The key code "0202" is used for the M3T-M32192UT. The connectable key codes for this extension bus connector are "0202" and "0000" (master connectable to all connectors).

5.2.2 Stacking of Extension Boards

Up to two extension boards can be stacked one on top of another. Pay attention to the power supply capacity of the extension board to be stacked (up to 3.3 V, 400 mA).
Figure 5.2.1 shows an example of how extension boards are stacked one on top of another.

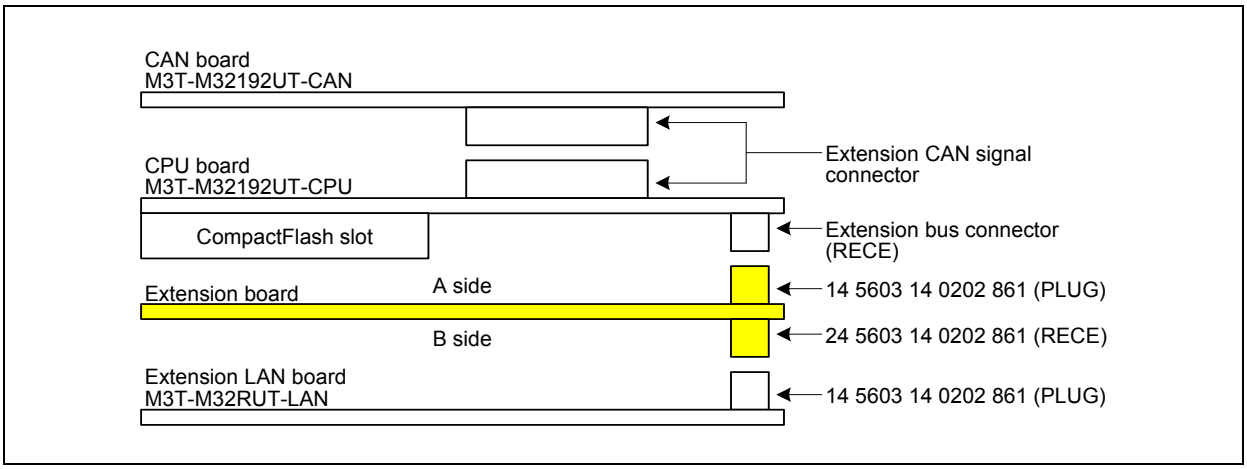

Figure 5.2.1 Example Stacking of Extension Boards

5.2.3 Board Size of the Extension Board

We recommend that the user extension board is the same size as the µT-Engine board (85 mm x 60 mm).

Do not place any part exceeding 2 mm in height on the side A (CPU board side) of the user extension board.

Do not place any part exceeding 7 mm in height on the side B (extension LAN board side) of the user extension board. However, if the extension LAN board is unused and the user extension board is connected at the bottom of the stack with only the PLUG-type connector mounted on it, parts in height of less than 15 mm can be placed on the side B.

Requirements regarding the board dimensions are stipulated below.

(1) The board thickness must be 1.6 mm.

(2) There must be board-fitting holes in diameter of 2.1 mm at the four corners of the board.
The holes must each be located at 2.5 mm from the board edge. No parts or patterns (except GND) must be placed in the range of 2.5 mm around the center of each hole.

(3) The center of the boss hole on the extension bus connector must be located at 5.5 mm from the board edge.
The center of the extension bus connector is the same as the board center.

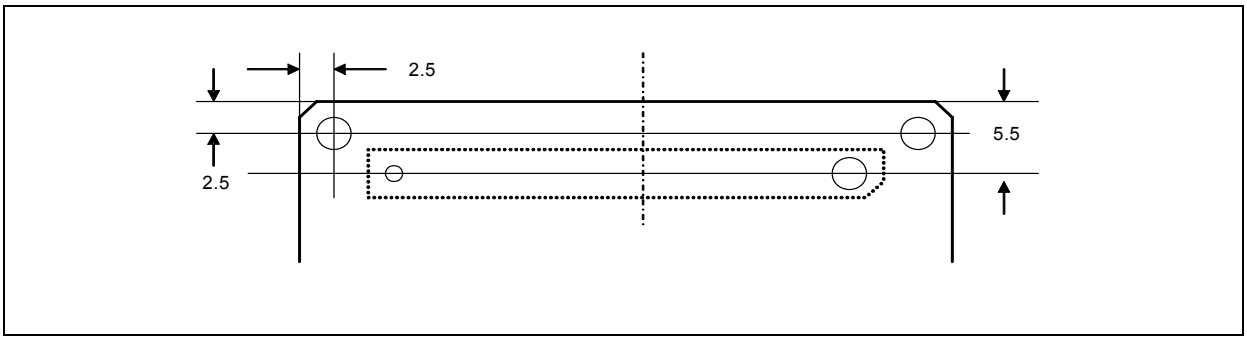

Figure 5.2.2 Peripheral Dimensions of the Extension Bus Connector

5.2.4 Mounted Direction of the Extension Bus Connector

Figure 5.2.3 shows the direction in which the extension bus connector is mounted on the board. The pin numbers here are reversed from those designated as pin numbers of a part by the connector manufacturer. So be careful with pin numbers when designing a pattern.

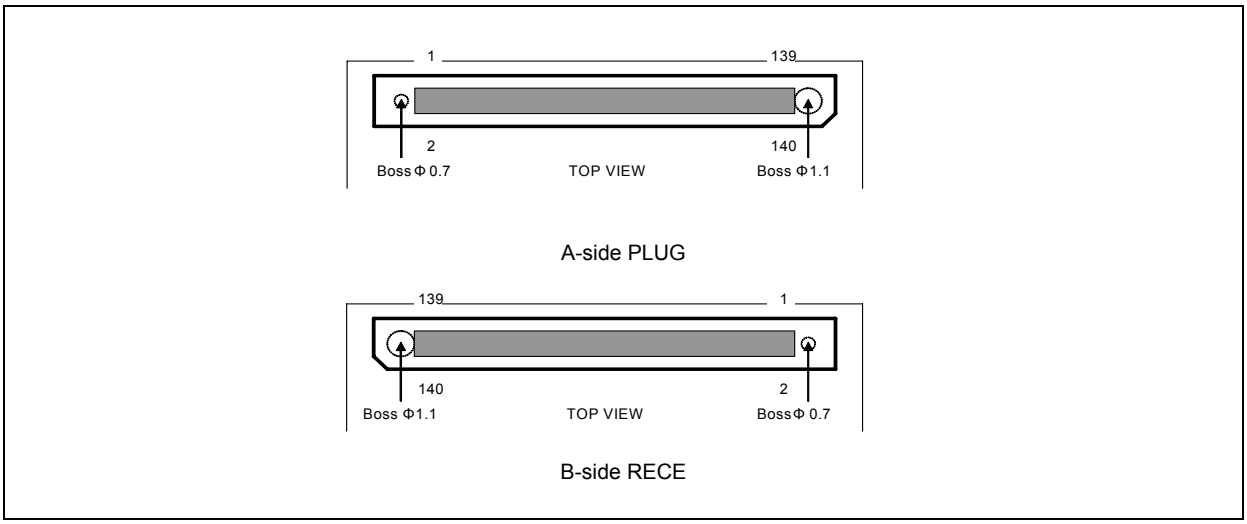

Figure 5.2.3 Mounted Direction of the Extension Bus Connector

5.3 Extension Bus Signal Assignments

Table 5.3.1 lists signal assignments of the extension bus.

Table 5.3.1 Signal Assignments of the Extension Bus (1/4)

No.	M3T-M32192UT-CPU signal name	Extension bus signal name	Signal used for extension bus board (reference)	
			M3T-M32RUT-LAN (REV.B)	M3T-M32RUT-LCD
1	GND	GND	GND	GND
2	GND	GND	GND	GND
3	GND	GND	GND	GND
4	GND	GND	GND	GND
5	V33	V33	V33	V33
6	V33	V33	V33	V33
7	V33	V33	V33	V33
8	V33	V33	V33	V33
9	JTAG_RST#	JTAG_RST#	JTAG_RST#	NC
10	TRST#	TRST#	TRST#	NC
11	TMS	TMS	TMS	NC
12	TDO	TDO	TDO	NC
13	TDI	TDI	TDI	NC
14	TCK	TCK	TCK	NC
15	GND	GND	GND	GND
16	GND	GND	GND	GND
17	P83 *2	P77	CTS2 (port)	NC
18	P85/TO23 *2	P76	ARXCLK# (timer output)	NC
19	NC	NC	NC	NC
20	NC	NC	NC	NC
21	P93 *2	P67	ARSTART (port)	NC
22	P82/TxD0 *2	P66	TXD2	NC
23	P84/SCLK0 *2	P65	SCLK2	NC
24	P86/RxD1	P64	RXD1	NC
25	P94 *2	P63	XRST# (port)	NC
26	P87/SCLK1	P62	SCLK1	NC
27	GND	GND	GND	GND
28	GND	GND	GND	GND
29	P95 *2	P27	CTS1 (port)	NC
30	NC	P26	NC	INT6 (INT for 32104)
31	NC	P25	NC	NC
32	P96 *2	P24	READ (port)	NC
33	NC	EXTPWR	NC	EXTPWR
34	NC	EXTPWR	NC	EXTPWR
35	NC	V33SB	NC	V33SB

Unused: Although patterns exist on the board, these signals are not used.

NC: No patterns exist on the board.

*1: These signals are generated by the control PLD, and not directly by the MCU.

*2: These signals are connected to the extension CAN signal connector as well. If these signals are used on the CAN board, they cannot be used on the extension board.

Table 5.3.1 Signal Assignments of the Extension Bus (2/4)

No.	M3T-M32192UT-CPU signal name	Extension bus signal mane	Signal used for extension board (reference)	
			M3T-M32RUT-LAN (REV.B)	M3T-M32RUT-LCD
36	NC	V33SB	NC	V33SB
37	GND	GND	GND	GND
38	GND	GND	GND	GND
39	P72/TIN27	INT3#	NC	NC
40	P132/TIN18/DIN2	INT2#	NC	INT2 (INT for 32700)
41	NC	BBSEL6#	NC	BBSEL6# (unused)
42	NC	BBSEL5#	NC	BBSEL5# (unused)
43	SW2	SW2	NC	NC
44	SW1	SW1	NC	NC
45	LED2	LED2	NC	NC
46	LED1	LED1	NC	NC
47	GND	GND	GND	GND
48	GND	GND	GND	GND
49	MPU_WAIT# *1	EXREADY#	EXREADY#	EXREADY#
50	P103/TO11/TIN24	EXINT	EXINT	NC
51	BUS_CS# *1	BCS1#	BCS1#	BCS1#
52	NC	BWS3#	NC	NC
53	NC	BWS2#	NC	NC
54	BUS_BLW# *1	BWS1#	BWS1#	BWS1#
55	BUS_BHW# *1	BWS0#	BWS0#	BWS0#
56	BUS_RD# *1	BRS#	BRS#	BRS#
57	GND	GND	GND	GND
58	GND	GND	GND	GND
59	GND	GND	GND	GND
60	BCLK	EXCLK	EXCLK	EXCLK
61	GND	GND	GND	GND
62	GND	GND	GND	GND
63	RESET#	RESET#	RESET#	RESET#
64	GND	GND	GND	GND
65	GND	GND	GND	GND
66	A30	BA30	BA30	BA30
67	A29	BA29	BA29	BA29
68	A28	BA28	BA28	BA28
69	A27	BA27	BA27	BA27
70	A26	BA26	BA26	BA26

Unused: Although patterns exist on the board, these signals are not used.

NC: No patterns exist on the board.

*1: These signals are generated by the control PLD, and not directly by the MCU.

*2: These signals are connected to the extension CAN signal connector as well. If these signals are used on the CAN board, they cannot be used on the extension board.

Table 5.3.1 Signal Assignments of the Extension Bus (3/4)

No.	M3T-M32192UT-CPU signal name	Extension bus signal name	Signal used for extension board (reference)	
			M3T-M32RUT-LAN (REV.B)	M3T-M32RUT-LCD
71	A25	BA25	BA25	BA25
72	A24	BA24	BA24	BA24
73	GND	GND	GND	GND
74	GND	GND	GND	GND
75	A23	BA23	BA23	BA23
76	A22	BA22	BA22	BA22
77	A21	BA21	BA21	BA21
78	A20	BA20	BA20	BA20
79	A19	BA19	BA19	BA19
80	A18	BA18	BA18	BA18
81	A17	BA17	BA17	BA17
82	A16	BA16	BA16	BA16
83	GND	GND	GND	GND
84	GND	GND	GND	GND
85	A15	BA15	BA15	BA15
86	A14	BA14	BA14	BA14
87	A13	BA13	BA13	BA13
88	A12	BA12	BA12	BA12
89	A11	BA11	BA11	BA11
90	A10	BA10	BA10	BA10
91	A9	BA9	BA9	BA9
92	GND	BA8	BA8	BA8
93	GND	GND	GND	GND
94	GND	GND	GND	GND
95	NC	BD31	NC	BD31 (unused)
96	NC	BD30	NC	BD30 (unused)
97	NC	BD29	NC	BD29 (unused)
98	NC	BD28	NC	BD28 (unused)
99	NC	BD27	NC	BD27 (unused)
100	NC	BD26	NC	BD26 (unused)
101	NC	BD25	NC	BD25 (unused)
102	NC	BD24	NC	BD24 (unused)
103	GND	GND	GND	GND
104	GND	GND	GND	GND
105	NC	BD23	NC	BD23 (unused)

Unused: Although patterns exist on the board, these signals are not used.

NC: No patterns exist on the board.

*1: These signals are generated by the control PLD, and not directly by the MCU.

*2: These signals are connected to the extension CAN signal connector as well. If these signals are used on the CAN board, they cannot be used on the extension board.

Table 5.3.1 Signal Assignments of the Extension Bus (4/4)

No.	M3T-M32192UT-CPU signal name	Extension bus signal name	Signal used for extension board (reference)	
			M3T-M32RUT-LAN (REV.B)	M3T-M32RUT-LCD
106	NC	BD22	NC	BD22 (unused)
107	NC	BD21	NC	BD21 (unused)
108	NC	BD20	NC	BD20 (unused)
109	NC	BD19	NC	BD19 (unused)
110	NC	BD18	NC	BD18 (unused)
111	NC	BD17	NC	BD17 (unused)
112	NC	BD16	NC	BD16 (unused)
113	GND	GND	GND	GND
114	GND	GND	GND	GND
115	DB15	BD15	BD15	BD15
116	DB14	BD14	BD14	BD14
117	DB13	BD13	BD13	BD13
118	DB12	BD12	BD12	BD12
119	DB11	BD11	BD11	BD11
120	DB10	BD10	BD10	BD10
121	DB9	BD9	BD9	BD9
122	DB8	BD8	BD8	BD8
123	GND	GND	GND	GND
124	GND	GND	GND	GND
125	DB7	BD7	BD7	BD7
126	DB6	BD6	BD6	BD6
127	DB5	BD5	BD5	BD5
128	DB4	BD4	BD4	BD4
129	DB3	BD3	BD3	BD3
130	DB2	BD2	BD2	BD2
131	DB1	BD1	BD1	BD1
132	DB0	BD0	BD0	BD0
133	V33	V33	V33	V33
134	V33	V33	V33	V33
135	V33	V33	V33	V33
136	V33	V33	V33	V33
137	GND	GND	GND	GND
138	GND	GND	GND	GND
139	GND	GND	GND	GND
140	GND	GND	GND	GND

Unused: Although patterns exist on the board, these signals are not used.

NC: No patterns exist on the board.

*1: These signals are generated by the control PLD, and not directly by the MCU.

*2: These signals are connected to the extension CAN signal connector as well. If these signals are used on the CAN board, they cannot be used on the extension board.

5.4 EXREADY# Input

The CPU board has an EXREADY# pin for WAIT# input from the extension board.

The EXREADY# signal should be an open-collector output to prevent collision of accesses when multiple extension boards are stacked one on top of another. This means that the EXREADY# signal is normally in the Hi-Z state and only when the CPU needs to be held waiting, it can be driven high to the CPU.

The EXREADY# signal internally is pulled low with 1 kΩ in the CPU board, and is converted to a WAIT# signal to the CPU by the control PLD.

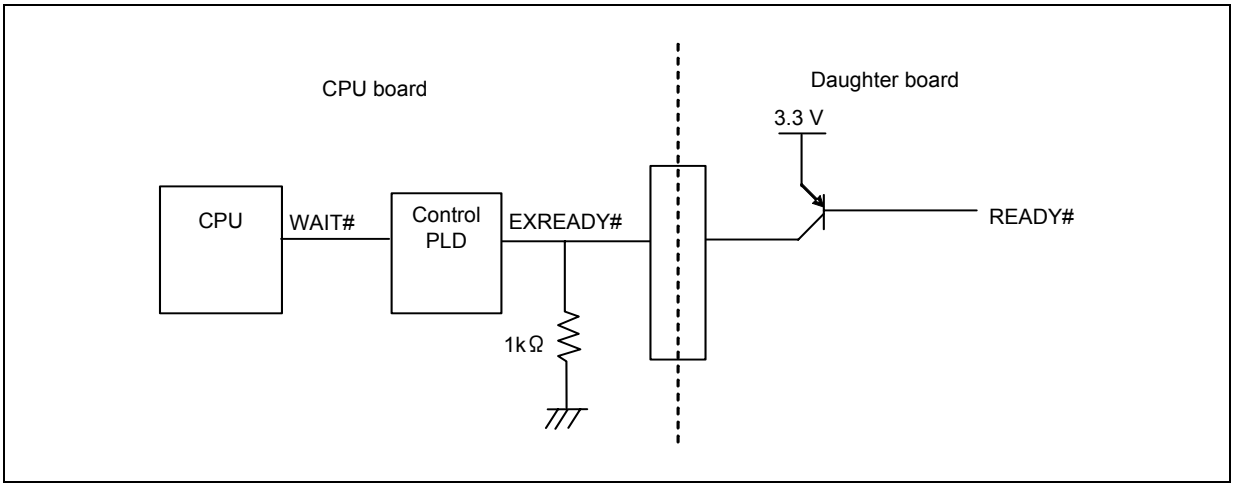

Figure 5.4.1 EXREADY# Input Circuit

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6. Mechanical Specifications

6.1 External View of the Board

6.1.1 M3T-M32192UT-CPU

Figure 6.1.1 shows an external view of the CPU board.

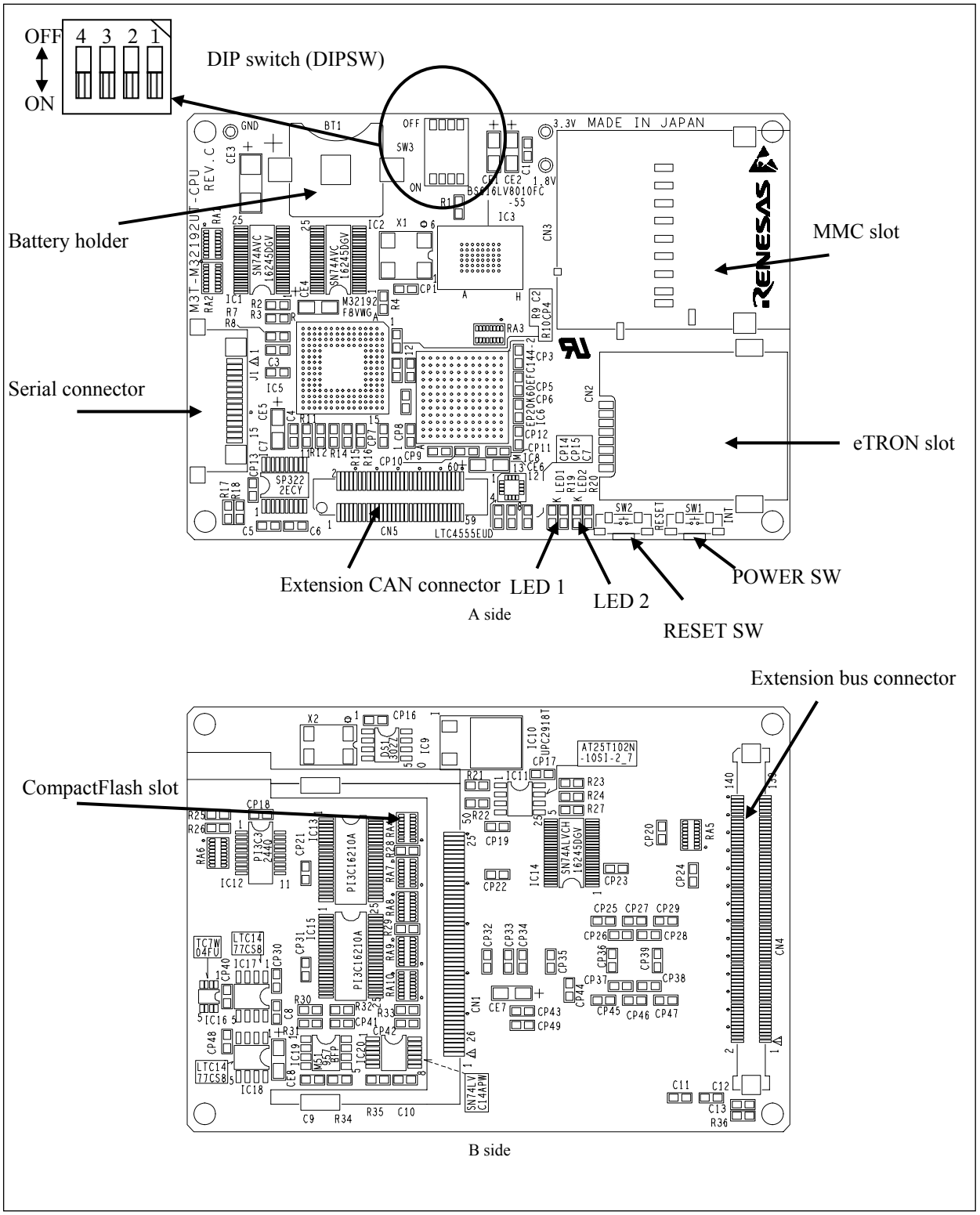

Figure 6.1.1 External View of the CPU Board

6.1.2 M3T-M32192UT-CAN

Figure 6.1.2 shows an external view of the CAN board.

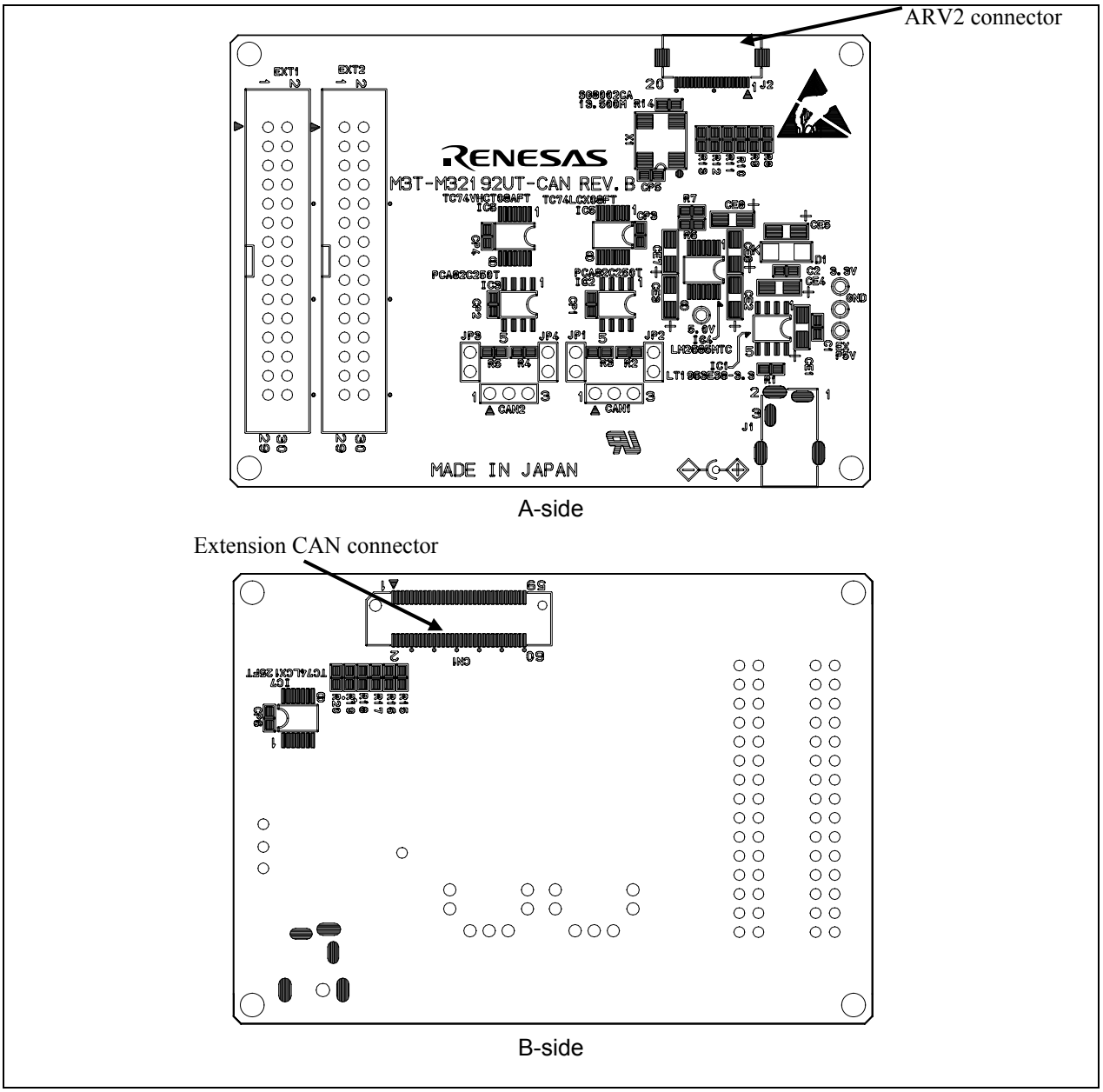

Figure 6.1.2 External View of the CAN Board

6.1.3 M3T-M32RUT-LAN

Figure 6.1.3 shows an external view of the extension LAN board.

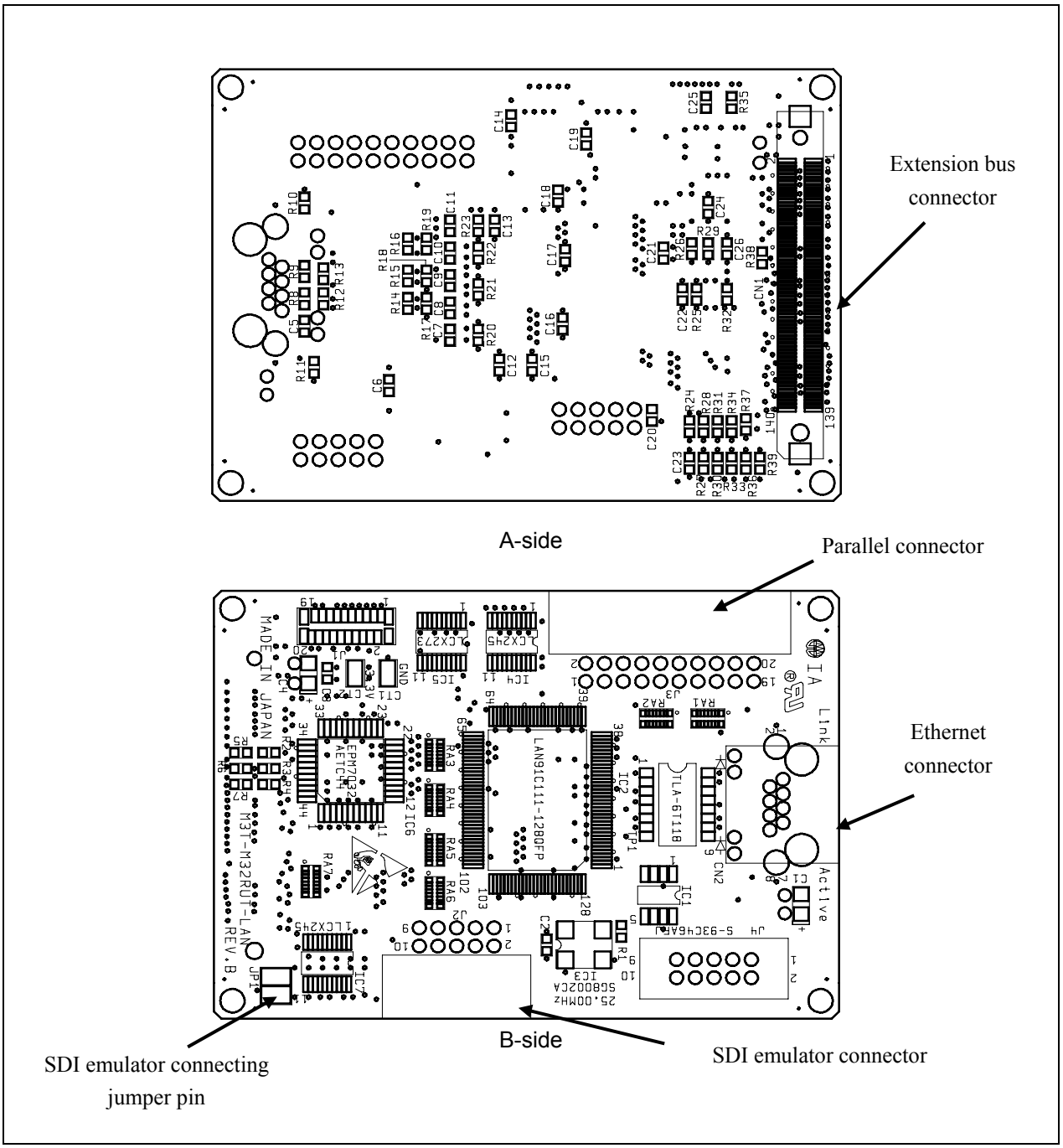

Figure 6.1.3 External View of the Extension LAN Board

6.2 Outline of Operating Parts

6.2.1 Realtime Clock Backup Battery Holder

A lithium battery with a rated voltage of 3.0 V or less can be used.

Name: BR1216, CR1216, BR1220, CR1220, CL1220, BR1225

The power of the backup battery is supplied to only the realtime clock.

When loading a battery into the battery holder, make sure it is inserted with the positive (+) side up, as shown in Figure 6.2.1.

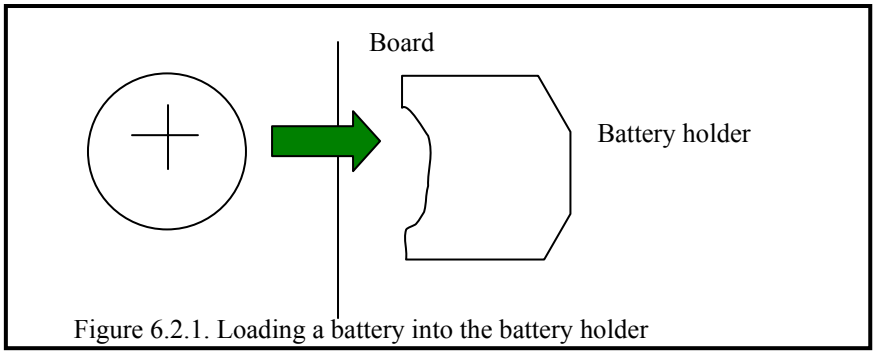

Figure 6.2.1. Loading a battery into the battery holder

To remove the battery, push the spot indicated by the arrow in Figure 6.2.2 with a nonconductive tool.

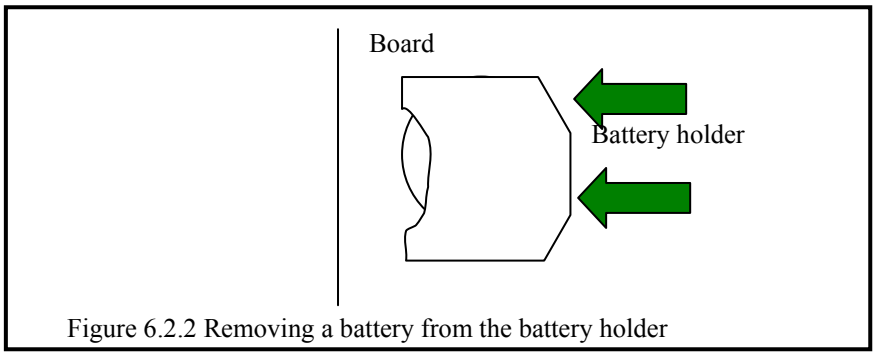

Figure 6.2.2 Removing a battery from the battery holder

6.2.2 LEDs

Two LEDs (green) are mounted on-board. These LEDs connect to the PLD. They can be turned on or off by manipulating the LEDCR register (address H'0214002) of the PLD.

6.2.3 User DIP Switch

A 4-bit DIP switch is mounted on-board.

The values of SW1 and SW2 can be read out via the IOSWSTS register (address H'00214006) of the PLD. For details, refer to Section 3.7.5, "Switch Status Register." The values of these switches themselves do not have any specific meaning. They are provided for selecting debug and startup modes of the OS.

SW3-3: Connects to the write protect pin of the EEPROM. Turning this switch on enables write protect, and turning it off disables write protect. The EEPROM contains the configuration data of the FPGA.

6.2.4 INT Switch

The INT switch connects to TIN0 of the MCU via INTSW of the FPGA. Therefore, how the device will operate when the POWER switch is pressed depends on software.

6.2.5 RESET Switch

Pressing the RESET switch generates a hardware reset to the device.

6.2.6 SDI Emulator Connecting Jumper Pin

J1 on the extension LAN board is a jumper pin for the SDI emulator to be connected. To connect the emulator to the SDI interface connector of the extension LAN board, attach the jumper pin. To connect the emulator to another extension board after attaching an SDI interface connector to that board, remove the jumper pin.

6.2.7 Ethernet Connector

To connect Ethernet to a hub, use straight cable.

The green LED indicates that a link has been established, and the yellow LED indicates that communication is active.

6.2.8 Connecting the ARV2 Board

To connect the ARV2 board, connect it and the extension CAN board with flex cable. Connect the cable to each board, as shown in Figure 6.2.3.

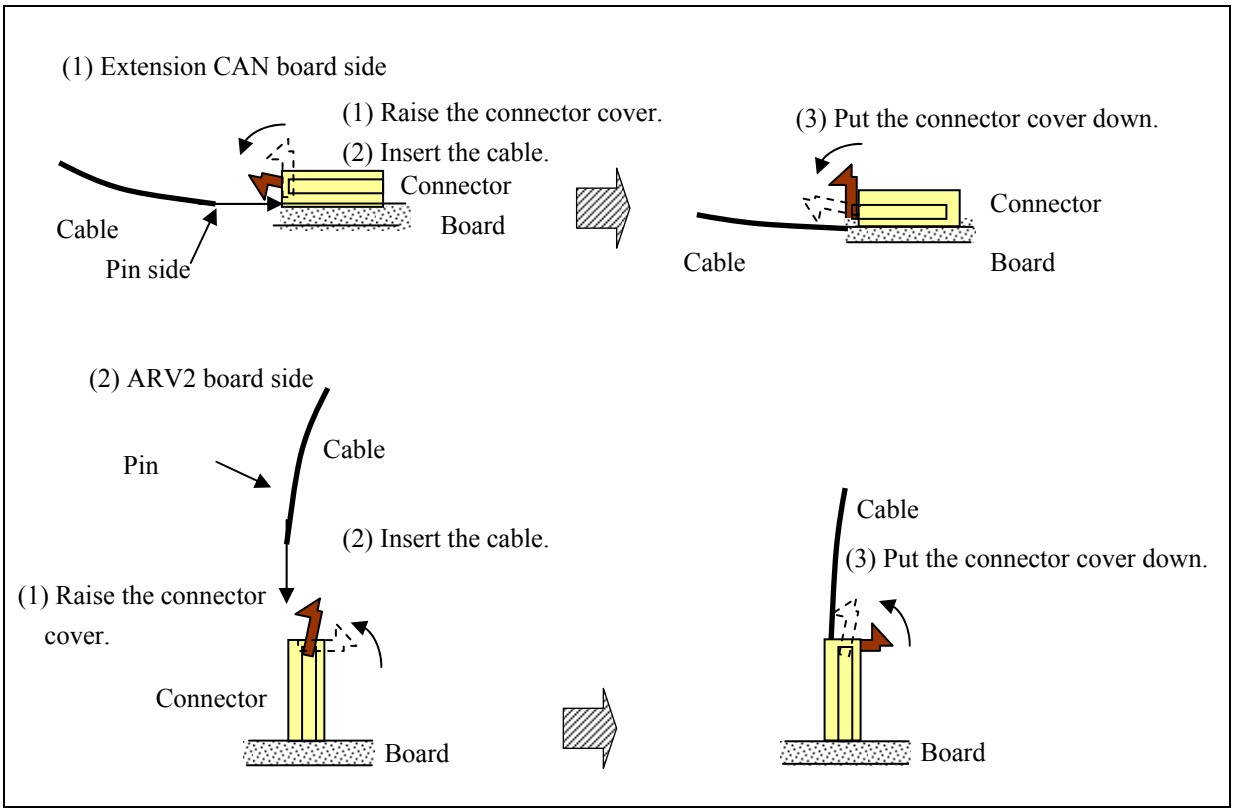

Figure 6.2.3 Connecting cable to the ARV2 board

6.2.9 Connecting the SDI Emulator

Connect the SDI connector to the SDI interface connector of the extension LAN board.

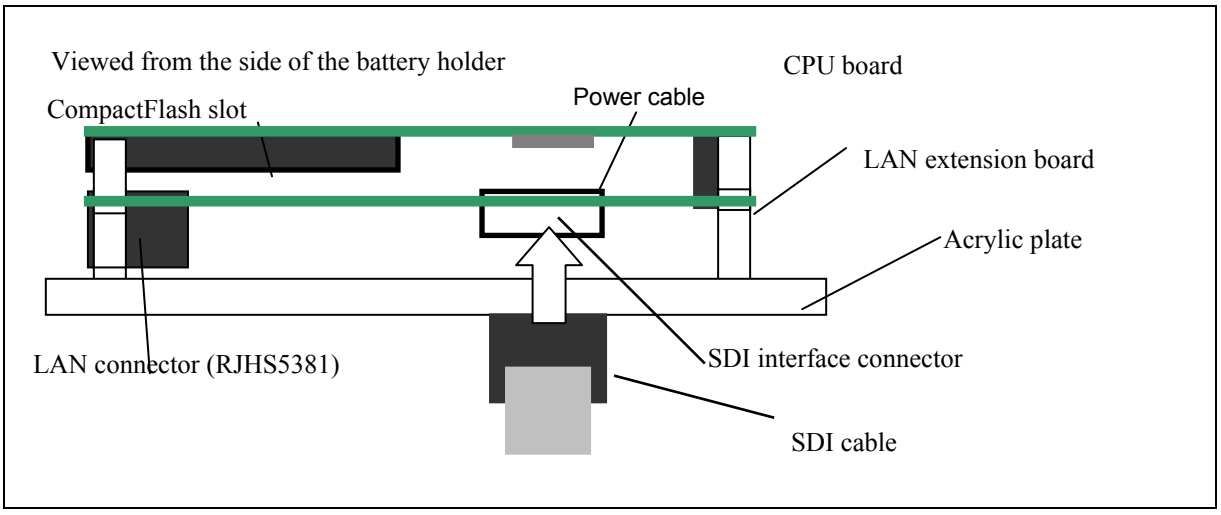

Figure 6.2.4 Connecting the SDI emulator

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