8V19N49x Hardware Design

This document provides board-level hardware design guidelines for the 8V19N49x family products (see table). The hardware design guidelines are similar for this product family. In this document, the 8V19N490 device is used for demonstration purposes.

Table 1. 8V19N49x Family

Part Number	VCO Frequency (GHz)
8V19N490, 8V19N490A, 8V19N490B, 8V19N492	~2.94912
8V19N490-19	~1.966
8V19N490-24, 8V19N491-24	~2.4576
8V19N491-36	~3.6864
8V19N492-39	~3.93216

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1. Overview

As indicated, this document provides board-level hardware design guidelines for the 8V19N49x product family. The document also recommends power rail handling, loop filter calculation, and input/output termination. A general schematic example is shown in Figure 1. A more detailed version is available upon request.

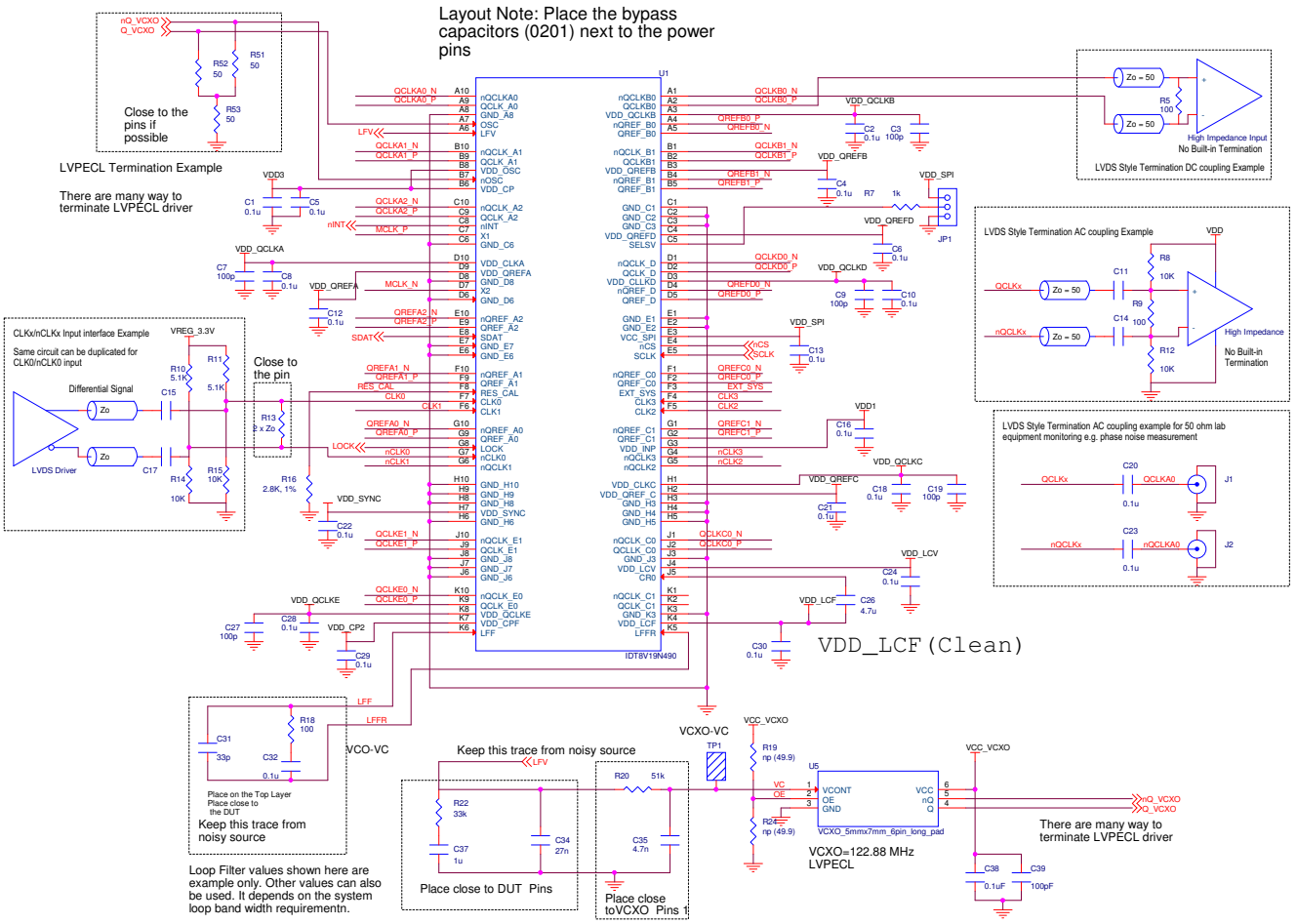

Figure 1. 8V19N490 Schematic Example

2. Power Rails

2.1 Bypass Capacitors

Bypass capacitors are required to filter out the system noise from switching power supplies and switching signal interference from other parts of the system. Figure 1 shows examples of bypass capacitors on the schematic. A PCB layout example is also available upon request. The type of bypass capacitor will depend on the noise level and noise frequencies in the system environment. The synthesizer output driver switching can also cause power rail noise. These noises can also interfere with other parts of the circuit or cause spur on other output channels.

The bypass capacitor values are usually in the range of 0.01uF to 0.1uF; however, other values can be used. Typical capacitor sizes are 0603, 0402, or 0201 with low ESR. The dielectric types typically are X5R or X7R. The smaller size allows the capacitor to be placed close to the power pin and reduces the trace length. Some capacitor vendors such as AVX provide online tools and models to provide the frequency response of the capacitors. Figure 2 to Figure 5 show the frequency response of various value capacitors provided by the capacitor supplier AVX. The frequency response plot shows that the smaller value capacitor can filter out high frequency noise and a larger value capacitor can filter out lower frequency noise. Typical power supply switching frequency can be

approximately 50KHz to 2MHz. Switching noise from other parts of the system can be varied. A combination of various values are suggested to cover low frequency and high frequency noise.

To minimize ESR between power pins and the bypass capacitors, Renesas suggests at least one bypass cap per power pin and to place these capacitors as close as possible to the power pins. Thicker trace widths between the bypass capacitor and power pin can also help reduce the ESR.

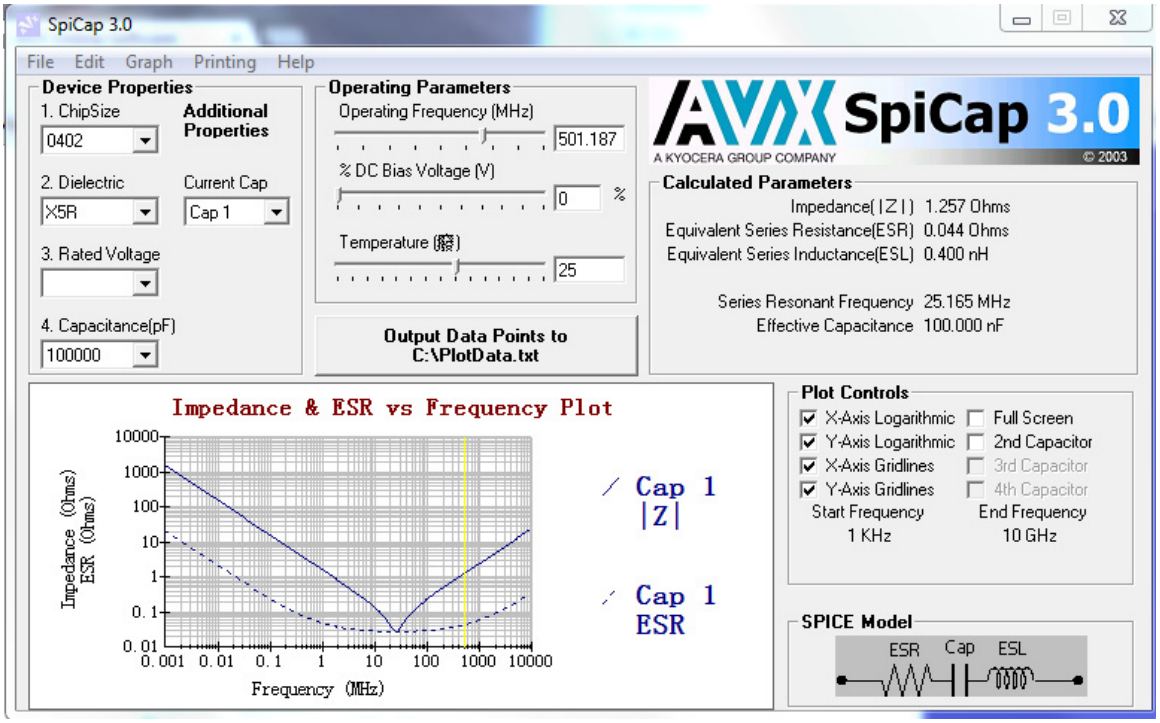

Figure 2. Example of a 100nF Bypass Capacitor Frequency Response

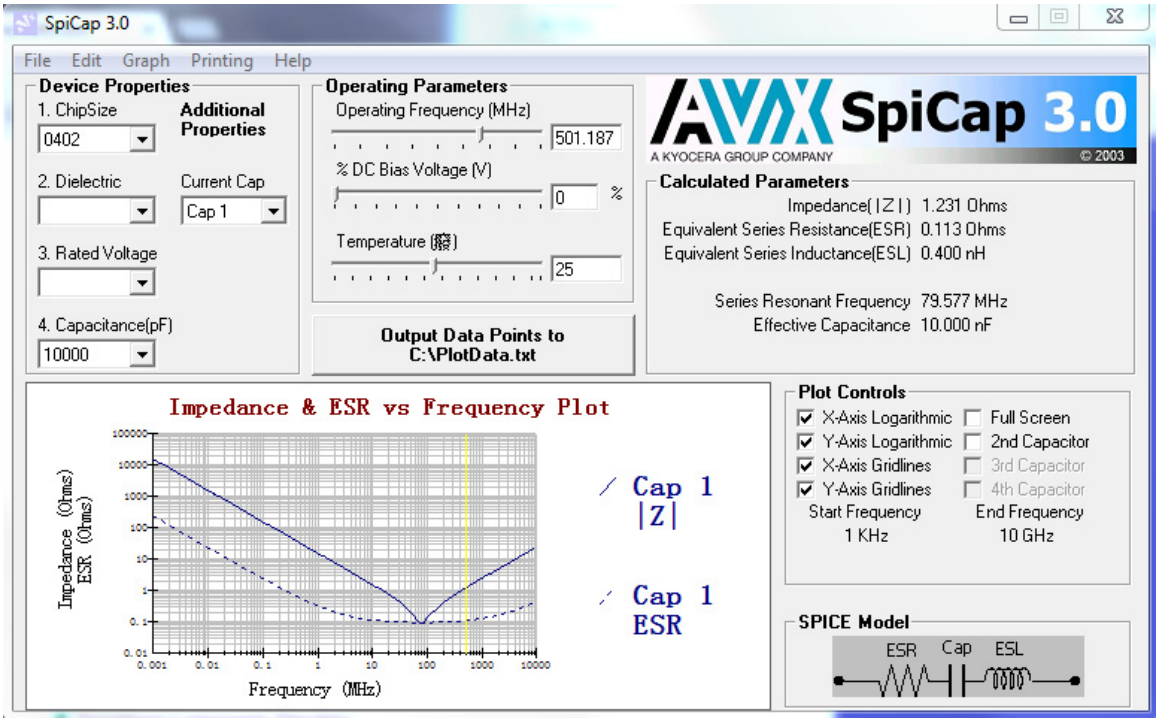

Figure 3. Example of a 10nF Bypass Capacitor Frequency Response

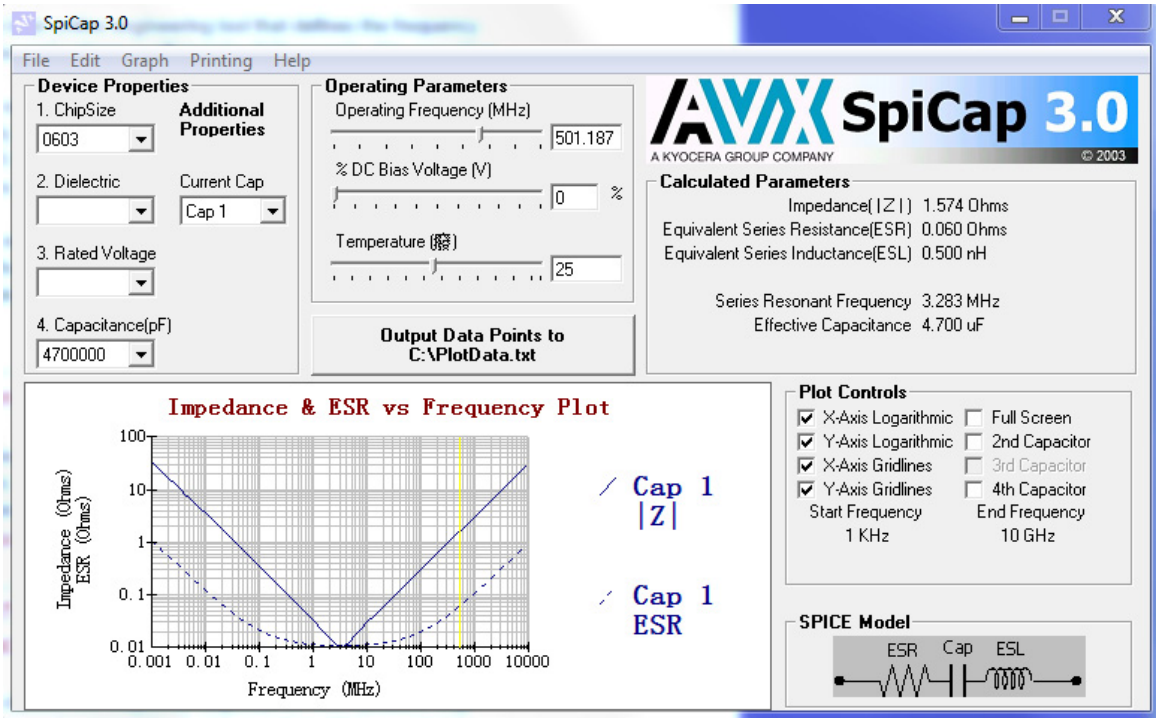

Figure 4. Example of Larger Value (4.7uF) Bypass Capacitor Frequency Response

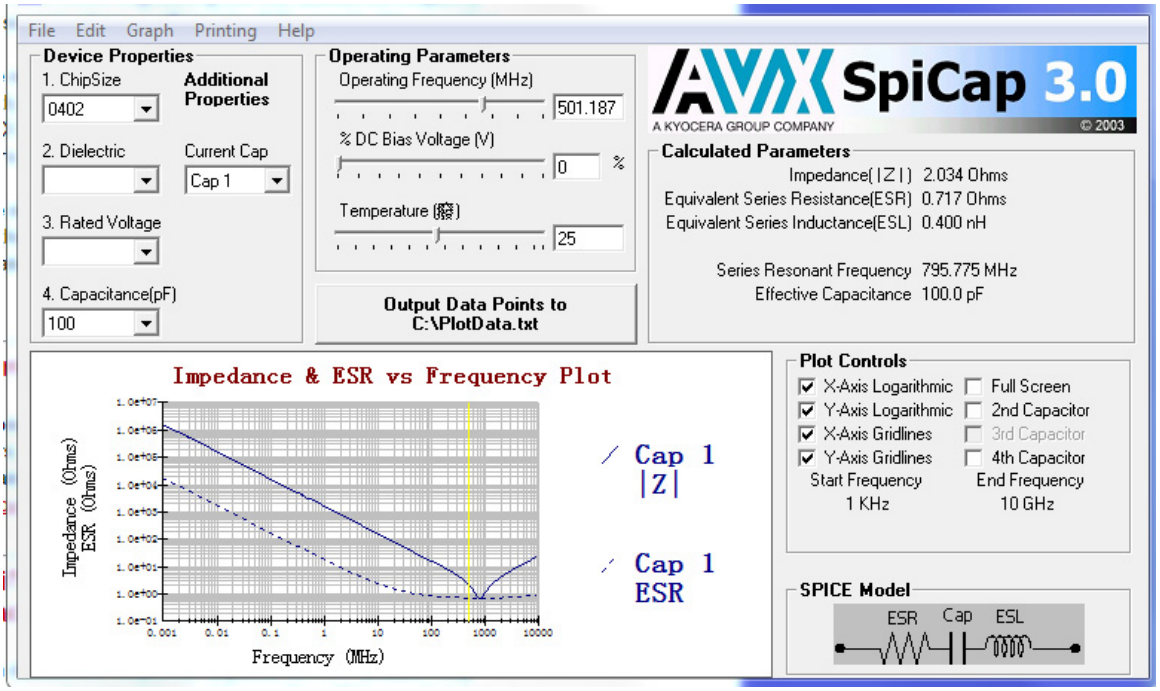

Figure 5. Example of Smaller Value (100pF) Bypass Capacitor Frequency Response

2.2 Power Supply Isolation

Analog power rails require cleaner power to optimize the jitter performance of PLLs. Most parts in the N49x family contain built-in LDOs. An external ultra-low noise LDO may not be required but it is recommended for reducing power supply noise for noise-sensitive power lines such as VDD_LCF and the external VCXO. An LDO with a noise level of less than 6uVrms from 10Hz to100kHz is recommended. This ultra-low noise LDO is mainly for the external VCXO that does not have a built-in LDO, and this affects the performance of 100Hz to 100kHz region.

It is suggested to isolate the analog power rail from other high-noise power rails. The isolation can be implemented through an RC low pass filter. The larger RC component values can reduce the cutoff frequency further and clean up lower frequency noise. For the VDDO output supplies, to reduce output frequency interference, the power rails between the output banks that operate at different output frequencies can be isolated using separate LDOs or using 1 to 2 ohm resistors if they share the same power source. Additional smaller value capacitors (e.g., 100pF) in parallel with the existing 0.1uF near the power pins can provide additional higher frequency noise filtering.

3. Loop Filter

3.1 2nd Order Loop Filter

This section provides design guidelines for a 2nd order loop filter for PLL. A typical 2nd order loop filter is displayed in Figure 6. In addition, a step-by-step calculation is provided to determine Rs, Cs, and Cp values. The required parameters for this part are also provided. A software tool for calculating the loop filter values is also available.

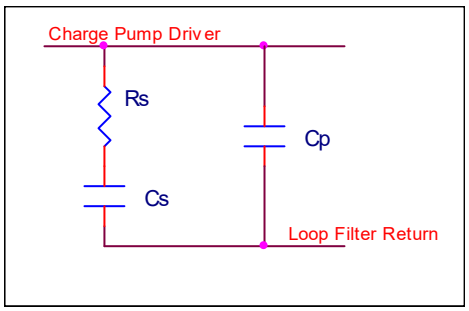

Figure 6. Typical 2nd Order Loop Filter

1. Determine the desired loop bandwidth, fc. The fc must satisfy the following condition:

$$\frac{Fpd}{fc} >> 20$$

Where,

Fpd is phase-detector input frequency.

2. Calculate Rs.

$$Rs = \frac{2 * \pi * fc * N}{Icp * Kvco}$$

Where,

Icp is charge pump current.

Kvco is VCO gain.

N is effective feedback divider.

$$N = \frac{Fvco}{Fpd}$$

Fvco is vco frequency.

Fpd is the phase detector input frequency.

3. Calculate Cs.

$$Cs = \frac{\alpha}{2 * \pi * fc * Rc}$$

Where,

α is ratio between loop bandwidth and the zero frequency at zero, α = fc / fz, recommend α to be greater than 3.

fz is frequency at zero.

4. Calculate Cp.

$$Cp = \frac{Cs}{\alpha * \beta}$$

Where,

fp is frequency at pole.

β is ratio between frequency at pole and loop bandwidth, β = fp/fc, recommend β greater than 3.

5. Verify maximum Phase Margin, PM.

$$PM = \arctan\left(\frac{b-1}{2 * \sqrt{b}}\right)$$

Where,

$$b = 1 + \frac{Cs}{Cp}$$

The PM should be greater than 50 degrees.

3.2 3rd Order Loop Filter

This section provides design guidelines for a 3rd order loop filter. A typical 3rd order loop filter is displayed in Figure 7.

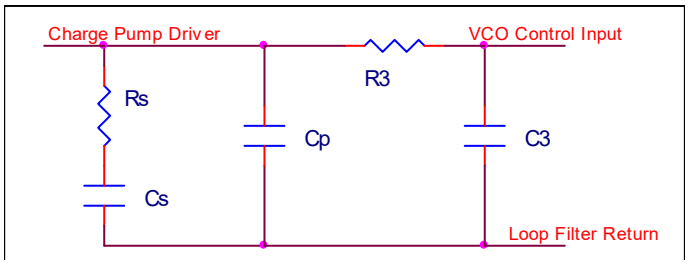

Figure 7. Typical 3rd Order Loop Filter

The Rs, Cs, and Cp can be the actual value used in the 2nd order loop filter. The following equation helps determine the 3rd order loop filter R3 and C3.

1. Pick an R3 value. Suggest R3 ~ 1.5xRs

$$C3 = \frac{Rs * Cp}{R3 * \gamma}$$

Where,

γ is ratio between the 1st pole frequency and the 2nd pole frequency. Suggest γ greater than 3.

2. The Timing Commander software tool is provided to calculate the loop filter component values. To use the spread sheet, user can enters the follow parameters:

   fc, Fpd, fvco, α and β

   The software tool will provide the component values, Rs, Cs, and Cp as result. The tool will also calculate maximum phase margin for verification.

The 3rd order loop filter, R3 and C3, are also calculated using the actual 2nd order loop filter components values.

3.3 Loop Filter Calculation Examples

3.3.1 Loop Filter for VCXO PLL

3.3.1.1 Second Order Loop Filter for the VCXO PLL

This section provides calculation examples for the VCXO PLL loop filter value. The 8V19N490 VCXO phase lock loop block diagram is displayed in Figure 8. A 2nd order loop filter for VCXO is shown in Figure 9. In this example, the reference CLK input frequency = 30.72MHz and a VCXO with output frequency of 122.88MHz is used.

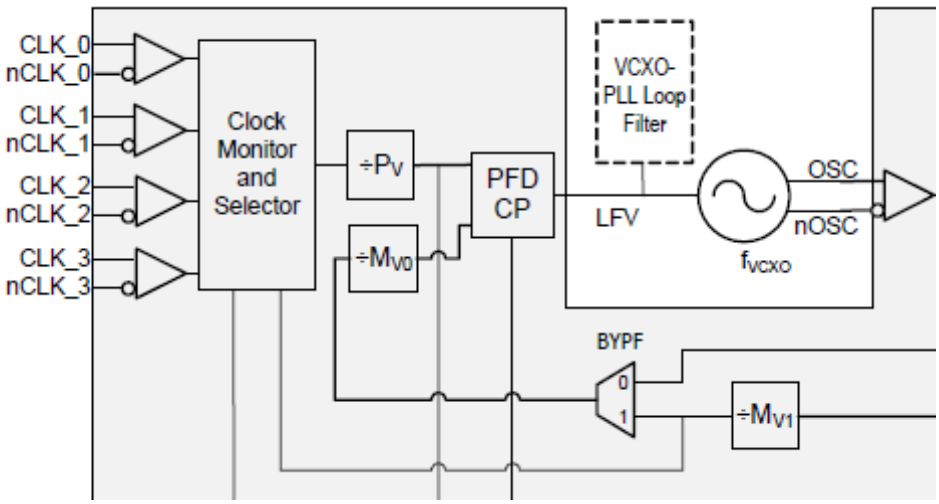

Figure 8. 8V19N490 VCXO PLL Block Diagram

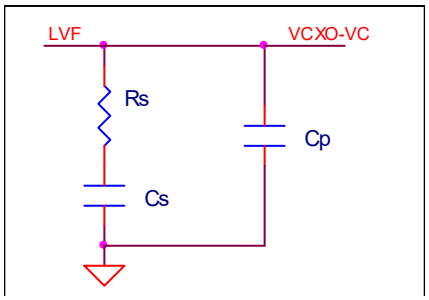

Figure 9. Typical 2nd Order Loop Filter

To calculate loop filter component values for loop bandwidth Fc = 40Hz with the reference CLK input frequency equals to 30.72MHz, set the input pre-divider Pv = 256. The phase detector input frequency Fpd = 0.12MHz. This satisfies the condition of Fpd / Fc >> 20.

The VCXO frequency Fvcxo = 122.88MHz, the effective feedback divider.

N = Mv = Fvcxo / Fpd = 1024

Rs can be calculated from the equation,

$$Rs = \frac{2 * \pi * fc * N}{Icp * Kvco}$$

Rs = 33k ohm

Kvco VCO gain can be found or derived from the VCXO datasheet. The VCO gain can also be measured from lab experiments. In this example, we use Kvco = 10kHz/V.

The 8V19N490 charge pump current can be programmed from 50uA to 1.6mA. In this example, assume the charge pump current is programmed to Icp = 800uA.

Cs can be calculated from the following equation,

$$Cs = \frac{\alpha}{2 * \pi * fc * Rc}$$

For α = 8, Cs is calculated to be 0.99uF. Cs greater than this value can be used to ensure that the α is greater than 12. For example, the actual chosen value can be 1uF from a standard capacitor value.

Cp can be calculated from the following equation,

$$Cp = \frac{Cs}{\alpha * \beta}$$

For β = 4, Cp = 31nF. Less than this value can be used for Cp to assure that the β is greater than 4 (e.g., actual chosen value Cp can be 27nF).

3.3.1.2 Third Order Loop Filter for the VCXO PLL

This section provides design guidelines for a 3rd order loop filter for the 8V19N490 VCXO PLL. A general 3rd order loop filter is displayed in Figure 10.

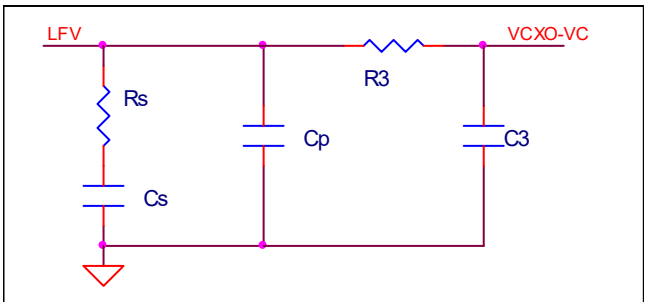

Figure 10. Typical 3rd Order Loop Filter

The Rs, Cs, and Cp are chosen standard values from the 2nd order loop filter. In this example, the chosen values are Rs = 33KOhm, Cs = 1uF, and Cp = 27nF. The following equation can help determine the 3rd order loop filter, R3 and C3.

1. Choose an R3 value. Suggest R3 ~ 1.5xRs to ~2.5xRs or greater (e.g, R3 = 51KHz is used in this example). C3 can be calculated using the following equation:

$$C3 = \frac{Rs * Cp}{R3 * \gamma}$$

2. Pick γ = 4 in this example.

C3 is calculated to be 4.37nF. A closest standard capacitor value can be used.

Table 2 shows some VCXO PLL Loop Filter examples for different VCXO frequencies. Other values can also be used to meet other specific conditions and requirements.

Table 2. Loop Filter Examples

VCXO Frequency[1]	122.88MHz	30.72MHz
VCXO Made/Model Examples	Epson,VG4513CA/CB Epson VG3225EFN* Crystek CVPD922 Crystek CHPD950 Crystek CVPD-037 Rakon RVX7050M TXC Vectron	Epson, TXC, Rakon
Typical VCXO Gain, Kvco	10k Hz/V	2.5k Hz/V
Loop Bandwidth, Fc	~40Hz	~40Hz
PDF, Phase Detector Input Frequency	120kHz	960kHz
Feedback Divider (N or Mv)	1024	32
Charge Pump Current Setting (Can be slightly Adjusted to change the loop band width)	800uA	800uA
Rs	33k Ohm	1k Ohm
Cs	1uF	10uF
Cp	27nF	330nF

Table 2. Loop Filter Examples (Cont.)

R3	51k Ohm	1.8k Ohm
C3	4.7nF	33nF

1. Other VCXO frequencies can also be used with proper loop filter and parameter setting. Below are examples of VCXO order information:
   * 122.88MHz - Epson VG3225EFN 122.88M-CJHHBA
   * 245.76MHz - Epson VG3225ENN 245.76M-CJHHMA
   * 491.52MHz - Epson VG3225ENN 491.52M-CJGHSA

3.3.2 Loop Filter for VCO PLL

The 8V19N490 VCO phase lock loop diagram is displayed in Figure 11. The Fvco frequency is 2.94912GHz. In this example, the 2949.12MHz VCO is used. A 2nd order loop filter for the VCO is shown in Figure 12.

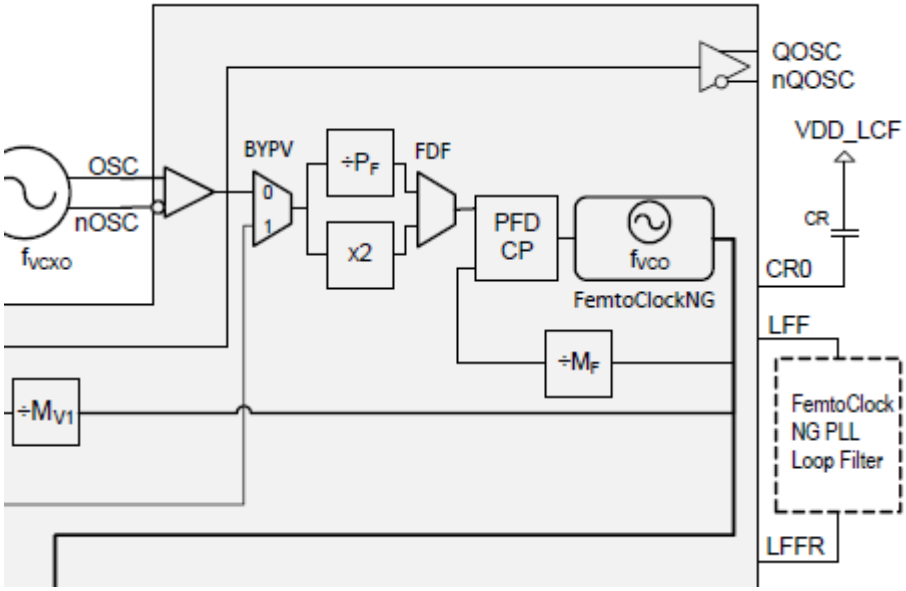

Figure 11. VCO PLL Block Diagram

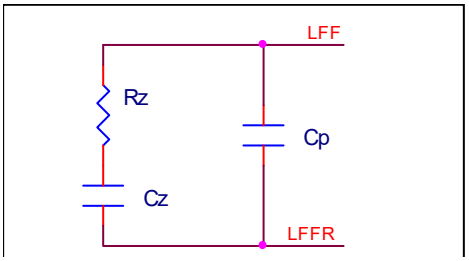

Figure 12. 2nd Order Loop Filter for the VCO

The board-level VCO 2nd order loop filter works in conjunction with the internal circuitries. A traditional loop filter calculation method may not be accurate. After simulation and actual experiment, an example of external two-pole loop filter value is provided in Table 3.

Table 3. VCO PLL 2nd Order Loop Filter Recommendation

VCXO used in the 1st PLL	122.88MHz	30.72MHz
PDF, Phase detector input frequency with doubler on	245.76MHz	61.44MHz
Feedback divider	12	48
Suggest Charge pump current setting	~ 3.2ma (typical) Suggest range setting 600ua to 6.4ma	~3.2ma (typical) Suggest range setting 600ua to 6.4ma
Rs	100 Ohm Suggest range (100 to 1k Ohm)	400 Ohm Suggest range (100 to 1k Ohm)
Cs	100nF	100nF
Cp	~ 40pF	~ 40pF

4. Input Output Interface

4.1 Input Termination for Reference Clock Input

The 8V19N490 reference clock input CLK/nCLK is a high-impedance differential receiver. The inverting input nCLK has weak bias to 1.2V. The input can accept signals from a standard 3.3V LVPECL or an LVDS driver directly without AC coupling. The board-level termination at the CLK/nCLK input is determined by the driver type. Figure 13 and Figure 14 provide examples of input interface without AC coupling. Figure 15 and Figure 16 provide examples of input driven by a differential driver with AC coupling. This section discusses only few examples; other termination topologies can also be used if desired.

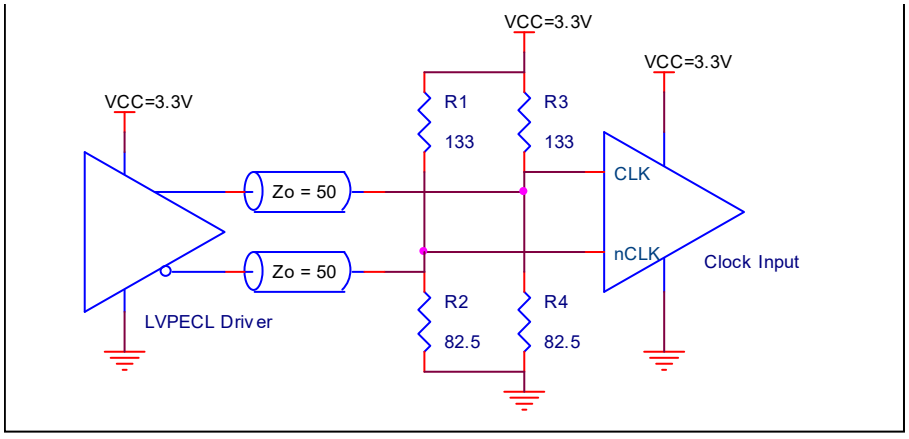

Figure 13. Input Termination Example – 8V19N490 Reference Clock Input CLK/nCLK, Driven by a 3.3V LVPECL Driver

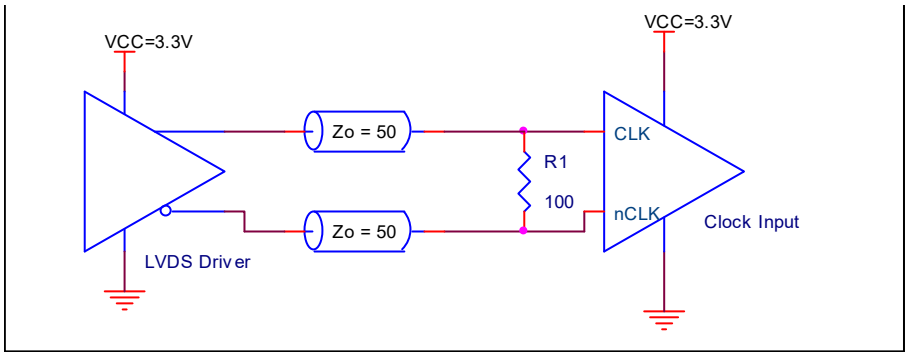

Figure 14. Input Termination Example – 8V19N490 Reference Clock Input CLK/nCLK Driven by a 3.3V LVDS Driver

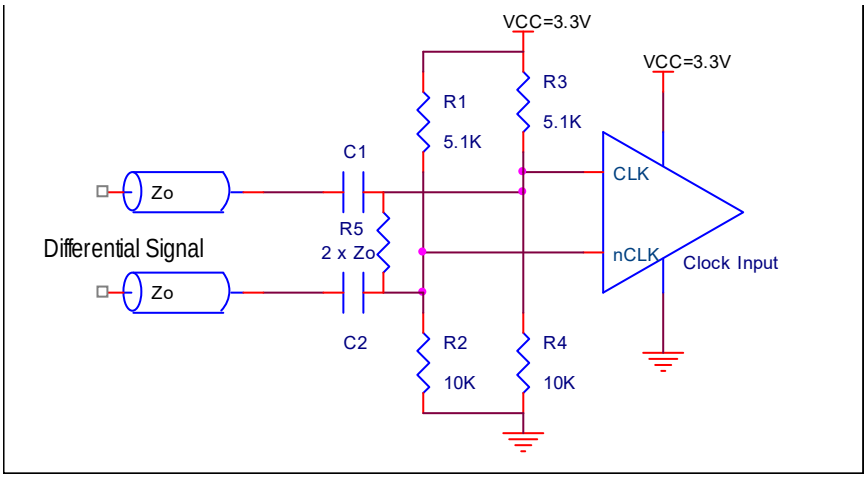

Figure 15. 8V19N490 Reference Clock Input CLK/nCLK AC Coupling Termination Example 1

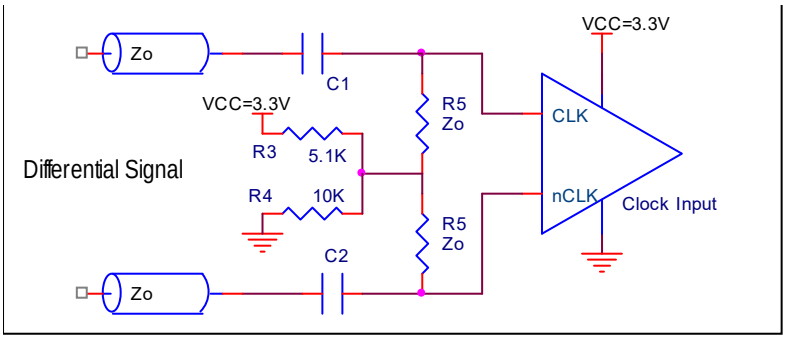

Figure 16. 8V19N490 Reference Clock Input CLK/nCLK AC Coupling Termination Example 2

4.2 Output Terminations for QCLK and QREF Drivers

The output stage of the 8V19N490 QCLK drivers can be configured to an LVPECL or LVDS style driver.

4.2.1 LVPECL Type Driver Terminations

When the output is configured to an LVPECL style driver, the driver is open-emitter type and requires a pull-down resistor for the DC current path in order for the output to switch. A standard LVPECL driver termination is displayed in Figure 17. There are many ways to terminate the LVEPCL driver. Figure 18 to Figure 21 show several examples of LVPECL style driver termination.

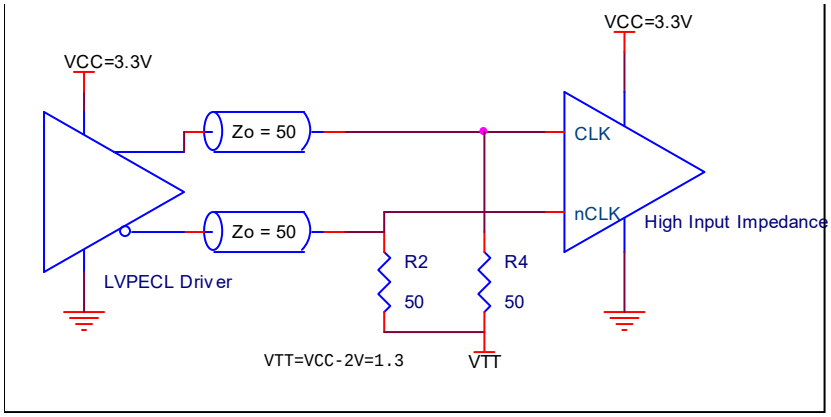

Figure 17. Standard LVEPCL 750mV Driver Termination

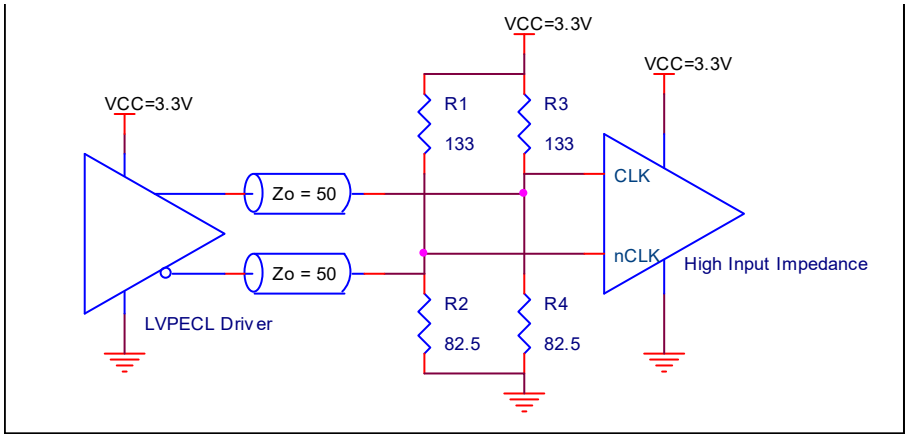

Figure 18. LVPECL 750mV Termination Example 1

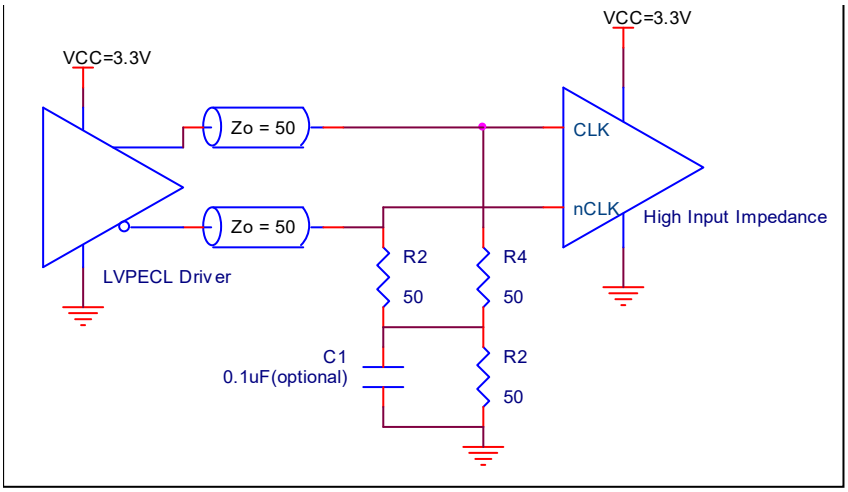

Figure 19. LVPECL 750mV Termination Example 2

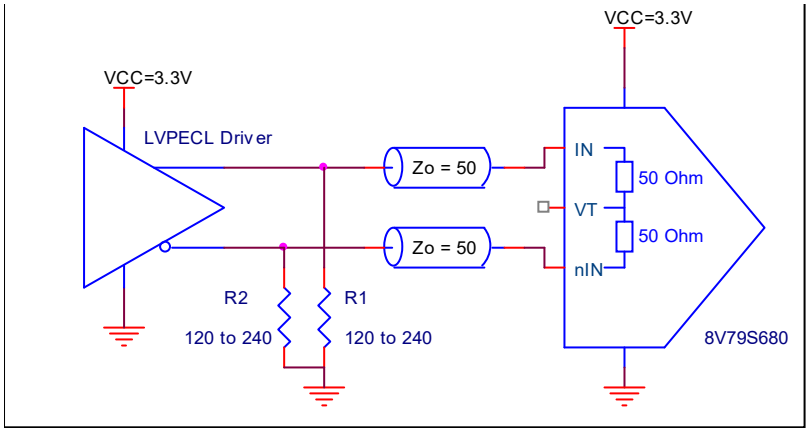

Figure 20. LVPECL Driver DC Coupling Termination for the Receiver with built-in 100 ohm termination

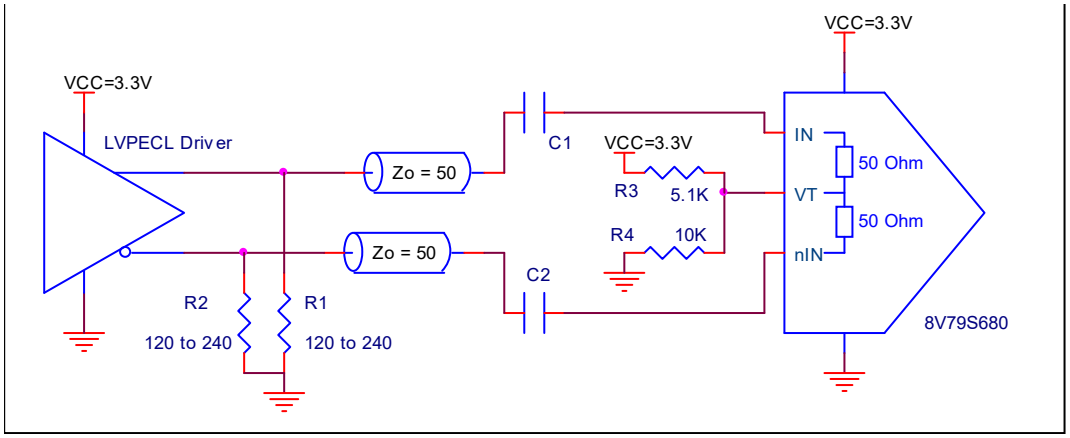

Figure 21. LVPECL Driver AC Coupling Termination for the Receiver with Built-in Termination

4.2.2 LVDS Type Driver Terminations

An LVDS type driver does not require board-level pull-down resistors. A typical termination with DC coupling for an LVDS type driver is displayed in Figure 22. A termination with AC coupling example is shown in Figure 23.

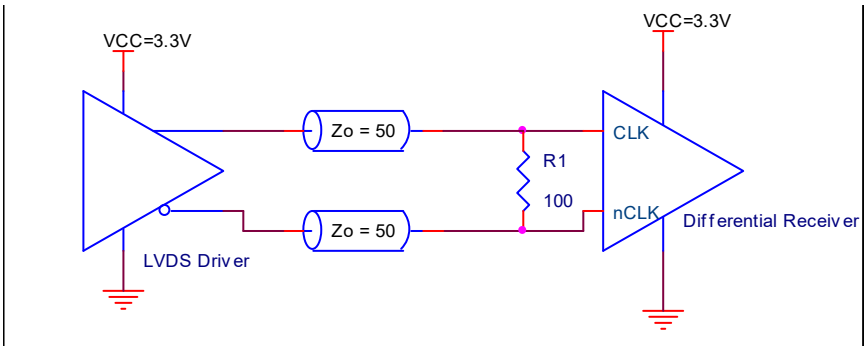

Figure 22. Typical LVDS Style Driver Termination

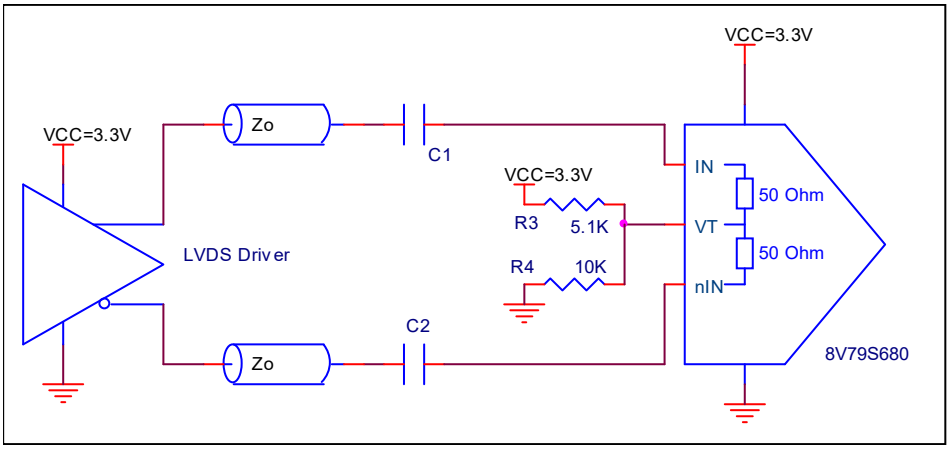

Figure 23. 8V19N490 LVDS Driver Driving a Receiver with Built-in Termination (e.g., 8V79S680/8V79S683 CLK/nCLK Input)

4.2.3 DC Coupling Interface for QREF Driver

The 8V19N49x QREF driver can be programmed to be an LVPECL or LVDS style driver. When programmed to an LVPECL style driver, the output is an open-emitter type driver and can be terminated in a similar way as the LVPECL termination (i.e., 50 Ohm to VTT or equivalence). When the QREF driver is programmed to an LVDS style driver, the driver can be terminated as an LVDS driver (i.e., 100Ohm across). The output signals are not quite same as standard LVPECL or LVDS. The amplitude can be programmed to different amplitude levels, 250mV, 500mV, 750mV, and 1000mV. The DC offset is about ~2V for both LVPECL and LVDS driver. 2V DC offset is close the standard LVPECL signal; however, 8V19N490 LVDS DC offset is about 2V which is not standard. In some applications, the receiver requires lower DC offset level with DC coupling interface. This section provides several termination solution examples to shift down the DC offset to level using the DC coupling interface.

4.2.3.1 Receiver with High Input Impedance (No Built-in Termination)

Figure 24 shows an example of a DC coupling interface. In this example, the receiver is high-input impedance without a built-in termination. The 8V19N490 driver is programmed to be an LVPECL style driver with 750mV amplitude. The DC offset level is shifted down to approximately 1.2V and the amplitude is reduced to 400mV, which is same signal of a standard LVDS level.

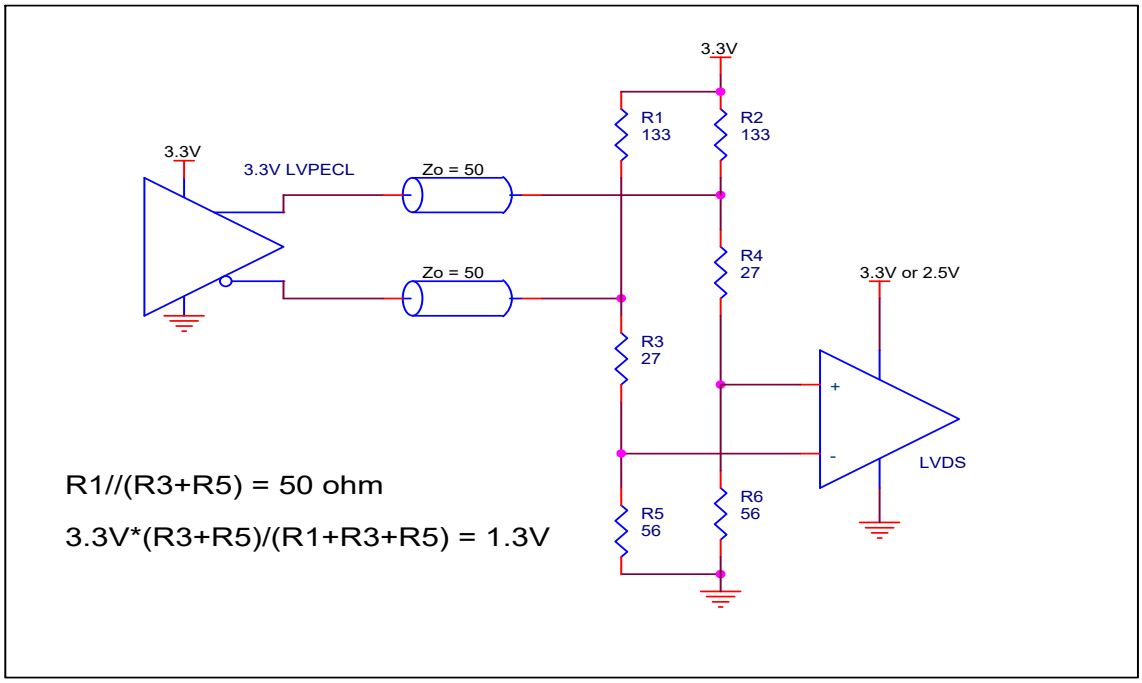

Figure 24. LVPECL 750mV to LVDS Receiver with High Input Impedance

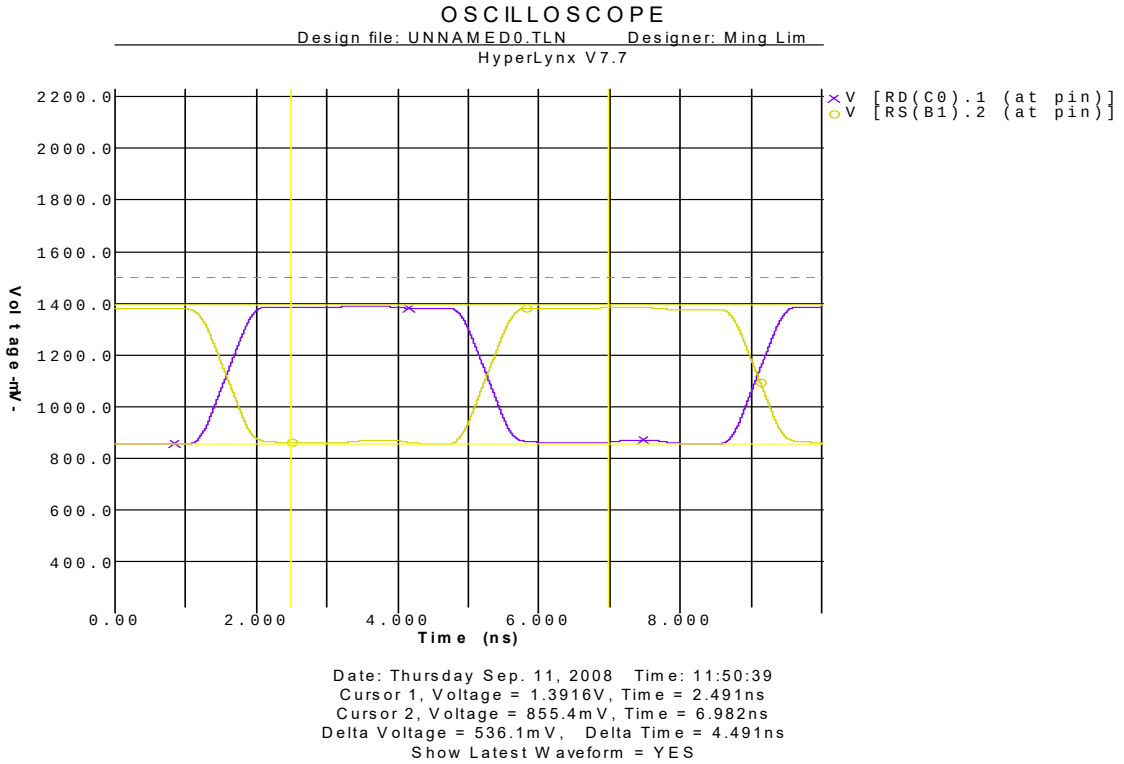

Figure 25. Simulation Waveforms at the Receiver Pins

4.2.3.2 Receiver with Built-in Termination

Figure 26 shows a receiver with built-in termination. The recommended termination for the non built-in is not feasible. The DC coupling interface example to shift down the DC offset level is displayed in Figure 27.

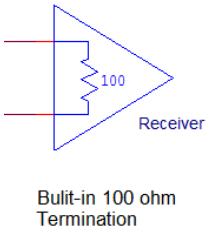

Figure 26. Receiver with Built-in 100 ohm

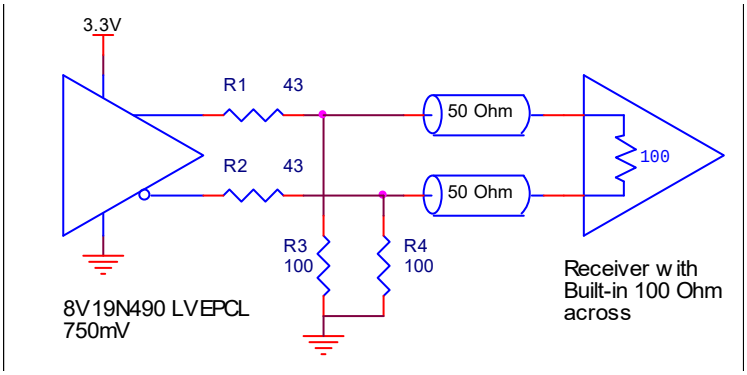

Figure 27. DC Coupling Example for Receiver with Built-in Termination

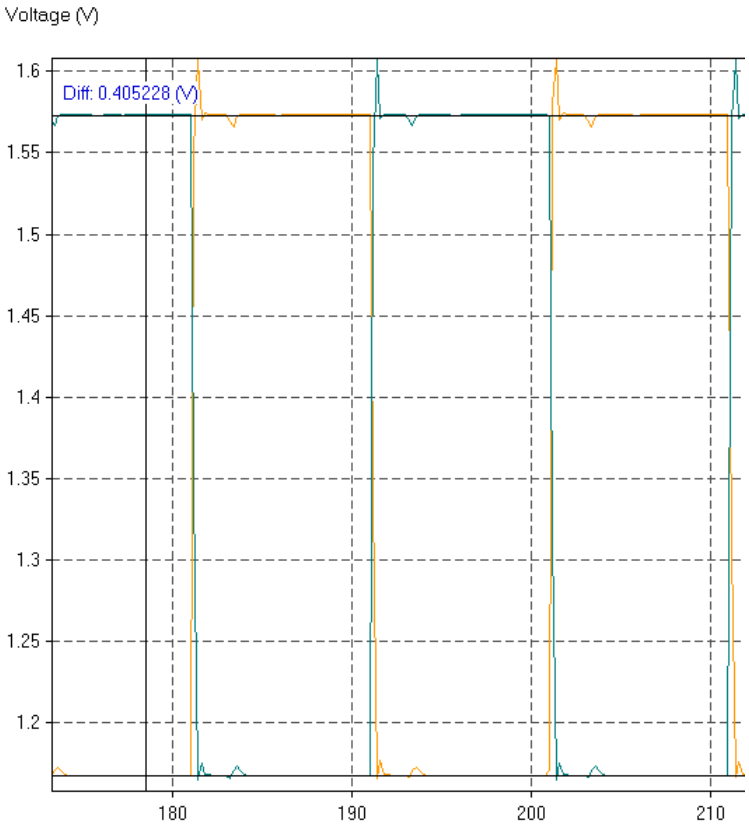

Figure 28. Simulation Waveform at the Receiver

4.2.3.3 Receiver with Built-in Termination and DC Bias

This section provides a DC coupling termination interface example to shift down the DC offset level for 8V19N490 driver. In this example, the receiver has built-in termination and built-in DC bias of 0.5V. The DC offset is required to shift close to this level.

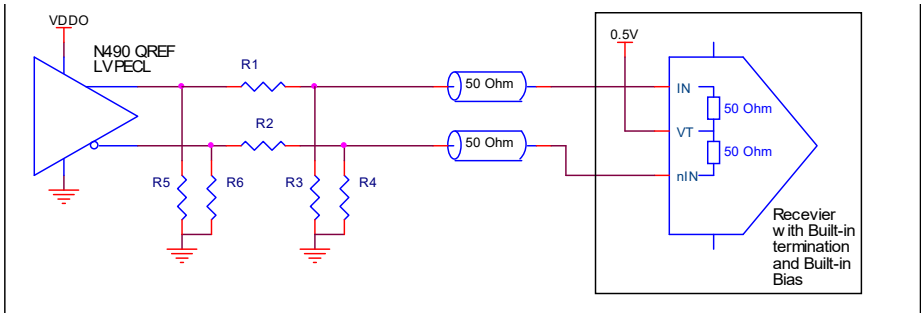

Figure 29. Interface to Receiver with Built-in Termination and Built-in DC Bias

The value of the component is shown in Table 4.

VDDO = 3.3V. The QREF output is set to LVPECL style driver and the amplitude is set to 750mV.

Table 4. Component Values

Component References	Component Values
R1	100 Ohm
R2	100 Ohm
R3	100 Ohm
R4	100 Ohm
R5	200 Ohm
R6	200 Ohm

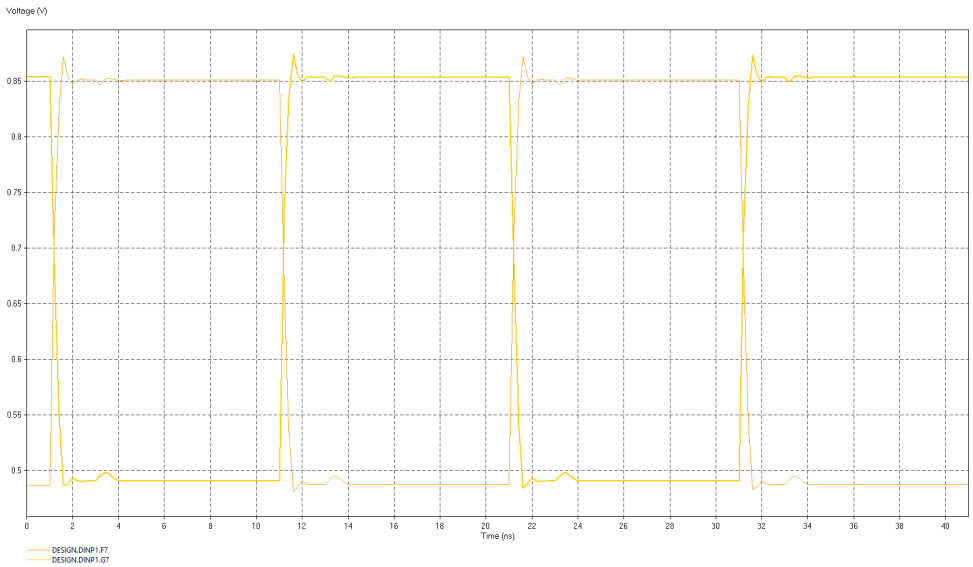

Figure 30. Simulation Waveform at the Receiver

5. Schematic Diagrams

The following schematic diagrams are available from request:

- 8V19N490 EVB schematic
- 8V19N490 EVB board layout

6. Revision History

Revision	Date	Description
1.0	Jun 3, 2021	Initial release.

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