ZL8801

Dual Phase PMBus™ ChargeMode™ Control DC/DC Digital Controller

FN8614
Rev.3.00
March 27, 2015

The ZL8801 is a dual phase digital DC/DC controller. Up to four ZL8801s (8 phases) can be operated in parallel to provide additional output current.

The ZL8801 supports a wide range of output voltages (0.54V to 5.5V) operating from input voltages as low as 4.5V up to 14V.

With its fully digital ChargeMode™ Control loop the ZL8801 can respond to a transient load step within a single switching cycle. This unique compensation-free modulation technique allows designs to meet transient specifications with minimum output capacitance, thus saving cost and board space.

Intersil's proprietary single wire DDC (Digital-DC™) serial bus enables the ZL8801 to communicate between other Intersil digital power ICs. By using the DDC, the ZL8801 achieves complex functions such as inter-IC phase current balancing, sequencing and fault spreading, eliminating complicated power supply managers with numerous external discrete components.

The ZL8801 features cycle-by-cycle overcurrent protection and protection for overvoltage, undervoltage, over-temperature and MOSFET driver under and overvoltage protection. A snapshot parametric capture feature allows users to take a snapshot of operating and fault data during normal or fault conditions.

Integrated Low Drop-Out (LDO) regulators allow the ZL8801 to be operated from a single input supply eliminating the need for additional linear regulators. A dedicated 5V VDRV LDO output can be used to power external drivers or DrMOS devices.

With full PMBus™ compliance, the ZL8801 is capable of measuring and reporting input voltage, input current, output voltage, output current as well as the device's internal temperature, an external temperature and an auxiliary voltage input.

Related Literature

- AN1948, "ZL8801-4PH-DEMO1Z Demonstration Board User Guide"
- UG005, "ZL8801-2PH-DEMO1Z Demonstration Board User Guide"
- AN1900, "USB to PMBus™ Adapter User Guide"

Features

- Unique compensation-free design – always stable
- Output voltage range: 0.54V to 5.5V
- Input voltage range: 4.5V to 14V
- 1% output voltage accuracy over line, load and temperature
- Charge mode control achieves fast transient response, reduced output capacitance and provides output stability without compensation
- Single 2-phase output, up to 8 phases with multiple devices
- Switching frequency range 200kHz to 1.33MHz
- Proprietary single wire DDC (Digital-DC) serial bus enables voltage sequencing and fault spreading with all other Intersil digital power ICs
- Tracking of an external power supply in the single 2-phase configuration
- Cycle-by-cycle inductor peak current protection
- Digital fault protection for output voltage UV/OV, input voltage UV/OV, temperature and MOSFET driver voltage
- 10-bit cycle-by-cycle average output current measurement with adjustable gain settings for sensing with high current, low DCR inductors
- 10-bit monitor ADC measures input voltage, input current, output voltage, internal, external temperature, driver voltage
- Configurable to use standalone MOSFET drivers or integrated driver-MOSFET (DrMOS) devices
- Nonvolatile memory (NVRAM) for storing operating parameters and fault events.
- PMBus™ compliant

Applications

- Servers/storage equipment
- Telecom/datacom equipment
- Power supplies (memory, DSP, ASIC, FPGA)

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	DUAL OUTPUT	DUAL PHASE	DDC CURRENT SHARE
ZL8800	Yes	Yes	No
ZL8801	No	Yes	Yes

Table of Contents

Simplified Application

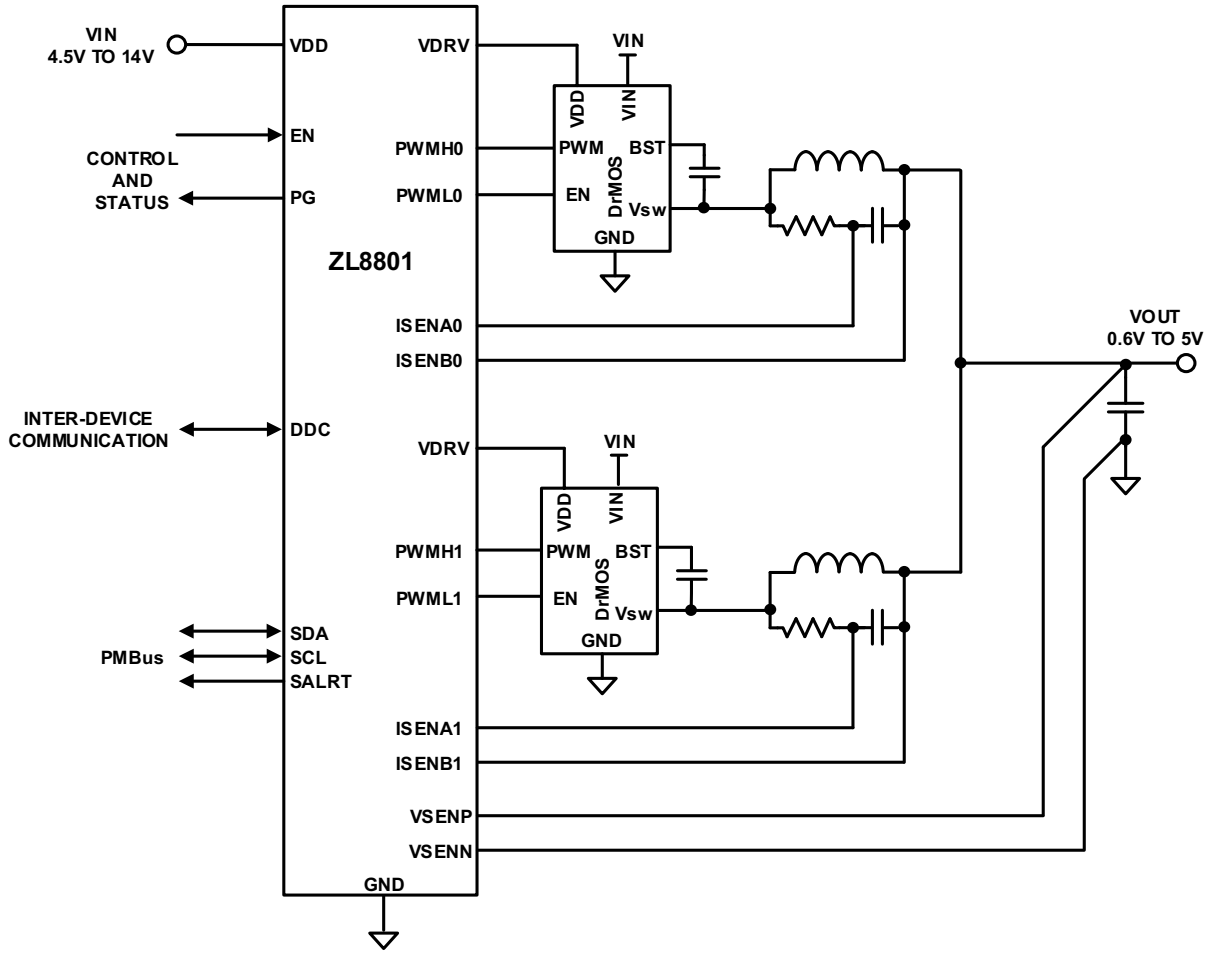


FIGURE 1. SIMPLIFIED APPLICATION

Block Diagram

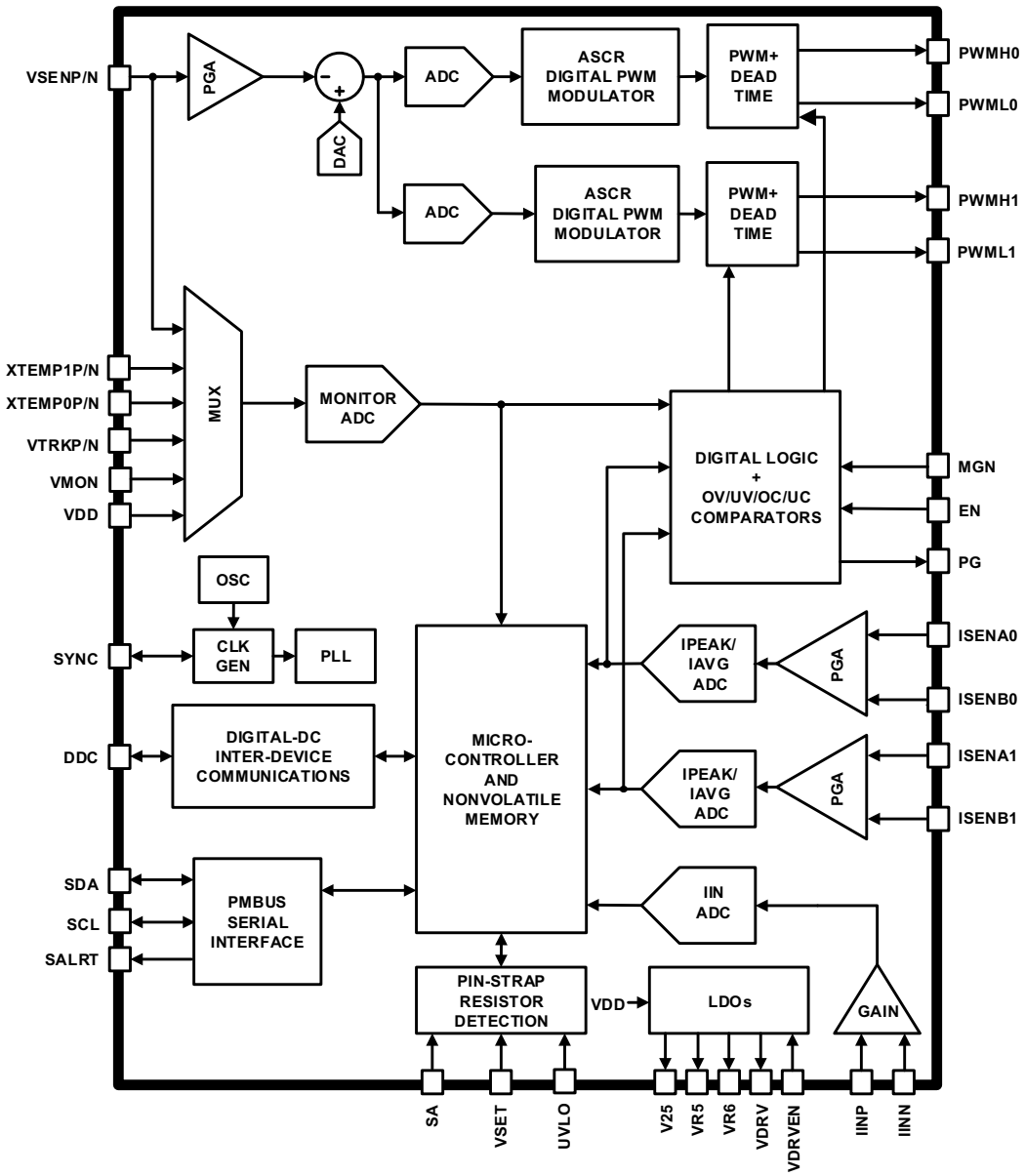


FIGURE 2. BLOCK DIAGRAM

Schematic

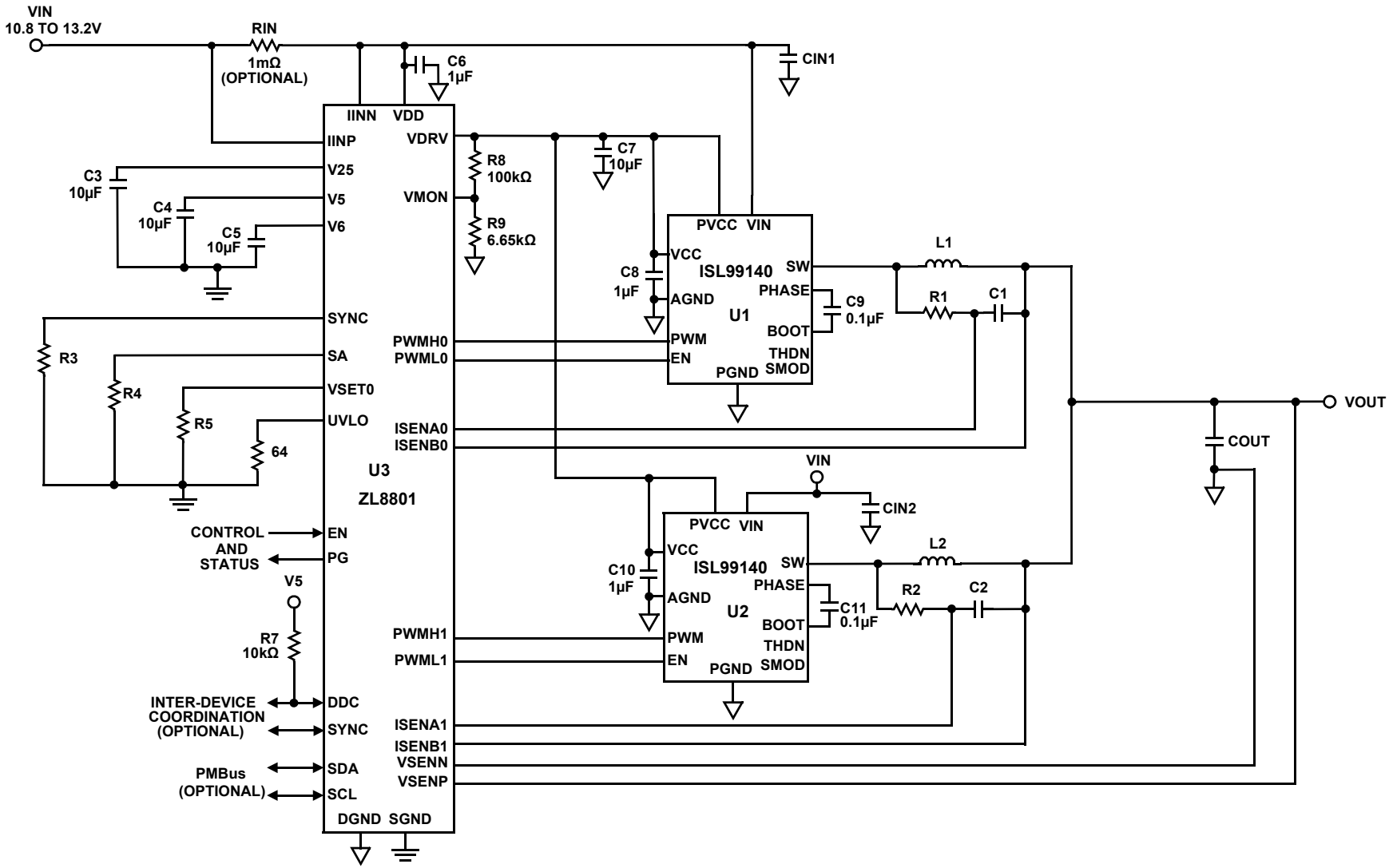
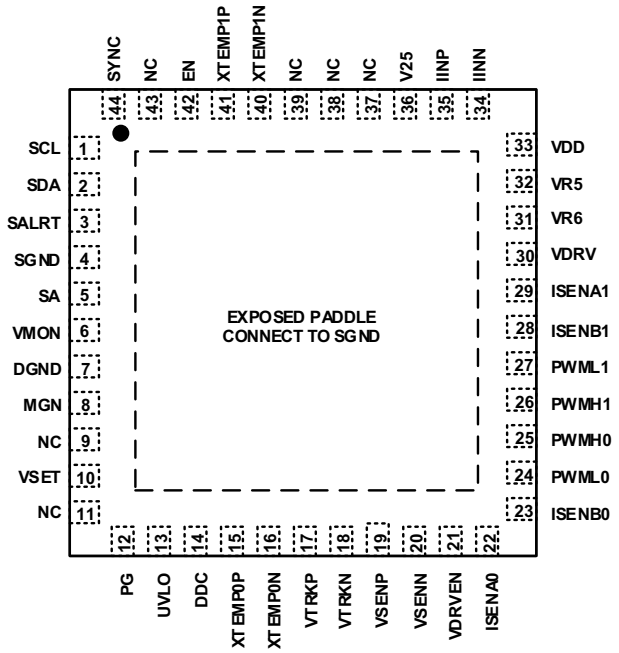


FIGURE 3. ZL8801 SCHEMATIC

Pin Configuration

ZL8801
(44 LD QFN)
TOP VIEW



Pin Description

PIN#	PIN NAME	TYPE (Note 1)	DESCRIPTION
1	SCL	I/O	Serial clock. Connect to external host and/or to other ZL devices. Requires a pull-up resistor to a 2.5V to 5.5V (recommend VR5, do not use V25) source.
2	SDA	I/O	Serial data. Connect to external host and/or to other ZL devices. Requires a pull-up resistor to a 2.5V to 5.5V (recommend VR5, do not use V25) source.
3	SALRT	O	Serial alert. Connect to external host if desired. Requires a pull-up resistor to a 2.5V to 5.5V (recommend VR5) source. If not used this pin should be left floating.
4	SGND	PWR	Connect to low impedance ground plane. Internal connection to SGND. All pin-strap resistors should be connected to SGND. SGND must be connected to DGND and PGND using a single point connection.
5	SA	M	Serial address select pin. Used to assign unique address for each individual device or to enable certain management features. See Table 3 for SMBus address options. Connect resistor to SGND.
6	VMON	I	External voltage monitoring (can be used for external driver bias (VDRV) monitoring). Requires an external 16:1 resistor divider network. Connect bottom of resistor divider network to SGND. Connect divider network to VR5 if an external voltage is not monitored.
7	DGND	PWR	Digital ground. Must connect to SGND and PGND using a single point connection.
8	MGN	I	Margin pin. High = margin high, low = margin low, float = no margin.
10	VSET	M	Output voltage selection pin. Used to set V_{OUT} and V_{OUT} max. See Table 4 for V_{OUT} pin-strap options. Default VOUT max is 115% of V_{OUT} setting, but this can be overridden via the PMBus interface with VOUT_MAX command. Connect resistor to SGND.
12	PG	O	Power-good output. Can be configured as open-drain or push-pull using the PMBus interface. Default setting is open drain.
13	UVLO	M	Undervoltage lockout selection. Sets the minimum value for V_{DD} voltage to enable V_{OUT}. See Table 6 for UVLO setting options. Pin-strapped (configured) values can be overridden by the PMBus interface. Connect resistor to SGND.
14	DDC	I/O	Single wire DDC bus (Current sharing and interdevice communication). Requires a pull-up resistor to a 2.5 to 5.5V (recommend VR5, do not use V25) source. Pull-up voltage must be present when the device is powered.
15	XTEMP0P	I	External temperature sensor input. Connect to external 2N3904 (Base Emitter junction) or equivalent embedded thermal diode. If not used connect to SGND.

Pin Description (Continued)

PIN#	PIN NAME	TYPE (Note 1)	DESCRIPTION
16	XTEMP0N	I	External temperature sensor input return. If not used connect to SGND.
17	VTRKP	I	Tracking sense positive input. Used to track an external voltage source. If not used, this pin can be left floating. Tracking is only possible in 2-phase operation. Tracking is disabled in 4-, 6- and 8-phase operation.
18	VTRKN	I	Tracking sense negative input (return). If not used, this pin can be left floating.
19	VSENP	I	Differential voltage sense feedback. Connect to positive output regulation point.
20	VSENN	I	Differential voltage sense feedback. Connect to negative output regulation point.
21	VDRVEN	I	VDRV (MOSFET Driver Bias Supply) Enable. Leave unconnected (float) or pull-up to VR5 to enable, tie to ground to disable.
22	ISENA0	I	Positive differential voltage input for phase 0 DCR current sensing. Should be routed as a pair with ISENB0. Should connect to resistor located close to output inductor. See "Current Sensing Components" on page 17.
23	ISENB0	I	Negative differential voltage input for phase 0 DCR current sensing. Should be routed as a pair with ISENA0. Should be connected to output inductor terminal. See "Current Sensing Components" on page 17.
24	PWML0	O	PWM0 Gate low signal/DrMOS enable. Configured using Bit 10 of USER_CONFIG command. Default is DrMOS operation.
25	PWMH0	O	PWM0 Gate high signal.
26	PWMH1	O	PWM1 Gate high signal.
27	PWML1	O	PWM1 Gate low signal/DrMOS enable. Configure using Bit 10 of USER_CONFIG command. Default is DrMOS operation.
28	ISENB1	I	Negative differential voltage input for phase 1 DCR current sensing. Should be routed as a pair with ISENA1. Should be connected to output inductor terminal. See "Current Sensing Components" on page 17.
29	ISENA1	I	Positive differential voltage input for phase 1 DCR current sensing. Should be routed as a pair with ISENB1. Should connect to resistor located close to output inductor. See "Current Sensing Components" on page 17.
30	VDRV	PWR	MOSFET driver bias supply regulator output. If disabled, this pin can be left floating. Decouple with a high quality 4.7µF X7R or better ceramic capacitor placed close to this pin.
31	VR6	PWR	Bypass for internal 6V reference used to power internal circuitry. Decouple with a high quality 4.7µF X7R or better ceramic capacitor placed close to this pin. Keep this net as small as possible. Do not route near switching signals.
32	VR5	PWR	Bypass for internal 5V reference used to power internal circuitry. Decouple with a high quality 4.7µF X7R or better ceramic capacitor placed close to this pin.
33	VDD	PWR	Supply voltage. Decouple with a high quality 1µF X7R or better ceramic capacitor placed close to this pin.
34	IINN	I	Input current monitor negative input. If not used connect to VDD.
35	IINP	I	Input current monitor positive input. If not used connect to VDD
36	V25	PWR	Bypass for internal 2.5V reference used to power internal circuitry. Decouple with a high quality 4.7µF X7R or better ceramic capacitor placed close to this pin
9, 11, 37, 38, 39, 43	NC		Not Connected. Leave pin floating.
40	XTEMP1N	I	External temperature sensor input for phase1. Connect to external 2N3904 (Base Emitter junction) or equivalent embedded thermal diode. If not used connect to SGND.
41	XTEMP1P	I	External temperature sensor input for phase 1 return. If not used connect to SGND.
42	EN	I	Enable input. Active signal enables PWM0 and PWM1 switching. Recommended to be tied low during device configuration. Refer to "Enable" on page 16 for additional information.
44	SYNC	M/I/O	Clock synchronization input. Used to set the frequency of the internal clock to sync to an external clock or to output internal clock. When configured as an output, this pin is push-pull and does not require a pull-up. See "Switching Frequency Setting (SYNC)" on page 14 for additional information.
PAD	SGND	PWR	Exposed thermal pad. Connect to low impedance ground plane. Internal connection to SGND.

NOTE:

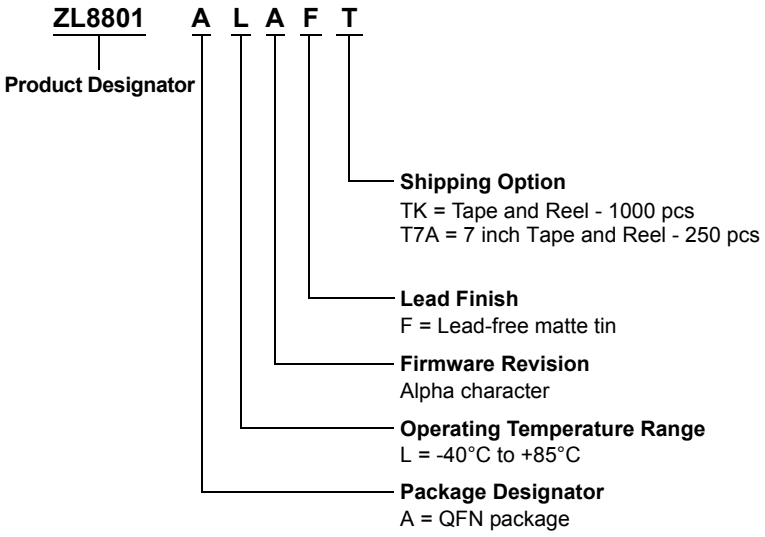
1. I = Input, O = Output, PWR = Power or Ground, M = Multi-mode pins.

Ordering Information

PART NUMBER (Notes 2, 3, 4)	PART MARKING	TEMP. RANGE (°C)	PACK METHOD	PACKAGE (RoHS Compliant)	PKG. DWG. #
ZL8801ALAFTK	8801	-40 to +85	Tape and Reel 1k	44 Ld QFN	L44.7x7B
ZL8801ALAFT7A	8801	-40 to +85	Tape and Reel 250pc	44 Ld QFN	L44.7x7B
ZL8801-2PH-DEMO1Z	2-phase Demonstration board.				
ZL8801-4PH-DEMO1Z	4-phase Demonstration board.				

NOTES:

2. Please refer to TB347 for details on reel specifications.
3. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
4. For Moisture Sensitivity Level (MSL), please see device information page for ZL8801. For more information on MSL, please see tech brief TB363



Absolute Maximum Ratings

DC Supply Voltage: VDD . . . . . -0.3V to 17V
Logic I/O Voltage: DDC, EN, MGN, PG,
SA, VDRVEN, SALRT, SCL, SDA, SYNC, UVLO,
VMON, VSET . . . . . -0.3V to 6.0V
Analog Input Voltages:
VSENP, VSENN, VTRKP, VTRKN, ISENA0, ISENA1,
ISENB0, ISENB1 . . . . . -0.3V to 6.5V
XTEMP0P, XTEMP1P . . . . . -0.3V to 6.0V
XTEMP0N, XTEMP1N . . . . . -0.3V to 0.3V
IINN, IINP . . . . . -0.3V to 17V
Logic Reference: V25 . . . . . -0.3V to 3V
Bias Supplies: VR5, VR6, VDRV . . . . . -0.3V to 6.5V
PWM Logic Outputs, PWMH0, PWMH1, PWML0, PWML1 . . . . -0.3V to 6.5V
Ground Voltage Differential (VDGND, VSGND) . . . . . -0.3V to +0.3V
ESD Ratings
Human Body Model (Tested per JESD22-A114E) 3kV
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per JESD22-C1010-D) 1kV
Latch-up (Tested per JESD78C; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
44 Ld QFN Package (Notes 6, 7)	25	1.5

Junction Temperature . . . . . -55°C to +150°C
Storage Temperature Range . . . . . -55°C to +150°C
Pb-free Reflow Profile . . . . . see TB493

Recommended Operating Conditions

Input Supply Voltage Range, VDD . . . . . 4.5V to 14V
Output Voltage Range, VOUT . . . . . 0.54V to 5.5V
Operating Junction Temperature Range, T_J . . . . . -40°C to +125°C
Ambient Temperature Range, T_A . . . . . -40°C to +85°C
5V (VR5) Supply Total Supplied Current (Note 8) 5mA
5V LDO Supply (VDRV) (Note 5) . . . . . 0 to 80mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Output current is limited by device thermal dissipation.
6. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
7. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
8. Total of current used by pull-ups to SDA, SCL, SALRT, DDC, EN, PG (including Push-pull configuration).

Electrical Specifications

V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNITS
IC INPUT AND BIAS SUPPLY CHARACTERISTICS					
I_{DD} Supply Current	f_{SW} = 200kHz		26	**50**	mA
	f_{SW} = 1.33MHz		50	**80**	mA
I_{DD} Device Disabled Current	EN = 0V, SMBus inactive, V_{DD} = 12V, f_{SW} = 1.33MHz		20	**30**	mA
VR5 Reference Output Voltage	V_{DD} > 6V, I < 5mA	**4.5**	5.0	**5.5**	V
V25 Reference Output Voltage	For reference only, VR > 3V	**2.25**	2.5	**2.75**	V
VR6 Reference Output Voltage	For reference only, V_{DD} = 12V	**5.5**	6.1	**6.6**	V
VDRV 5V Output Voltage (Note 9)	V_{DD} > 5.5V; 0 to 80mA	**4.5**	5.25	**5.5**	V
OUTPUT CHARACTERISTICS					
Output Voltage Adjustment Range	V_{IN} > V_{OUT} + 1.1V	**0.54**		**5.5**	V
Output Voltage Set-point Accuracy (Note 11)	Across line, load, temperature variation	**-1**		**1**	% V_{OUT}
Output Voltage Set-point Resolution (Note 10)	Set using PMBus™ command		±0.025		% V_{OUT}
Output Voltage Positive Sensing Bias Current	VSENP = 4V (negative = sinking)	**-100**	20	**100**	µA
Output Voltage Negative Sensing Bias Current	VSENN = 0V		20		µA
Logic Input/Output Characteristics					
Logic Input Leakage Current	Logic I/O - multi-mode pins	**-100**		**100**	nA
Logic Input Low, V_{IL}				**0.8**	V
Logic Input High, V_{IH}		**2**			V
Logic Output Low, V_{OL}	2mA sinking			**0.5**	V
Logic Output High, V_{OH}	2mA sourcing	**2.25**			V

Electrical Specifications V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNITS
PWM INPUT/OUTPUT CHARACTERISTICS					
PWM Output Low	2mA sinking			**0.5**	V
PWM Output High	2mA sourcing	**4.25**			V
OSCILLATOR AND SWITCHING CHARACTERISTICS					
Switching Frequency Range		**200**		**1334**	kHz
Switching Frequency Set-point Accuracy		**-5**		**5**	%
Minimum SYNC Pulse Width	50% to 50%	**150**			ns
Input Clock Frequency Drift Tolerance	Maximum allowed drift of external clock	**-10**		**10**	%
PMBus™ Clock Frequency (Note 12)		**100**		**400**	kHz
POWER MANAGEMENT					
SOFT-START/RAMP CHARACTERISTICS					
t_{ON} Delay/t_{OFF} Delay	Factory default		5		ms
t_{ON} Delay/t_{OFF} Delay Range	Set using PMBus™ command	**4**		**5000**	ms
t_{ON} Delay/T_{OFF} Delay Accuracy	Turn on, Turn off delay		-0/+2		ms
t_{ON} Ramp/t_{OFF} Ramp Duration	Factory default (2-phase only)		5		ms
t_{ON} Ramp/t_{OFF} Ramp Duration Range	Set using PMBus™ command (2-phase only)	**5**		**100**	ms
t_{ON} Ramp/t_{OFF} Ramp Duration Accuracy	(2-phase only)		±250		µs
TRACKING					
VTRK Input Bias Current	VTRK = 5V		70	**200**	µA
VTRK Regulation Accuracy	100% Tracking, V_{OUT} – VTRK (2-phase only)	**-2**		**2**	% V_{OUT}
POWER-GOOD					
Power-good V_{OUT} Threshold	Factory default		90		% V_{OUT}
Power-good V_{OUT} Hysteresis	Factory default		5		%
Power-good Delay Applies to turn-on only (Low-to-high transition)	Factory default		1		ms
	Set using PMBus™ command	**0**		**5000**	ms
MONITORING AND FAULT MANAGEMENT					
INPUT VOLTAGE MONITOR AND FAULT DETECTION					
VDD/VIN UVLO Threshold Range		**2.85**		**16**	V
VDD/VIN Monitor Accuracy	Full Scale (FS) = 14V		±2		% FS
VDD/VIN Monitor Resolution	Full Scale (FS) = 14V		±0.15		%
VIN UV/OV Fault Response Delay			100		µs
INPUT CURRENT					
Input Current Sense Differential Input Voltage	V_{IINP} to V_{IINN}	**0**		**20**	mV
Input Current Sense Input Offset Voltage	V_{IINP} to V_{IINN}		±100		µV
Input Current Sense Accuracy	% of Full Scale (20mV)		±5		% FS
OUTPUT VOLTAGE MONITOR AND FAULT DETECTION					
VOUT Monitor Accuracy	FS = VSET voltage (V_{OUT})	**-2**		**2**	% FS
VOUT Monitor Resolution	FS = VSET voltage (V_{OUT})		± 0.15		% FS
VOUT UV/OV Fault Response Delay			10		µs
OUTPUT CURRENT					
OUTPUT CURRENT SENSE INPUT RESOLUTION					
Low Range	±25mV Full Scale		37.5		µV
Medium Range	±35mV Full Scale		56.25		µV
High Range	±50mV Full Scale		75		µV

Electrical Specifications V_{DD} = 12V. Typical values are at T_A = +25°C. **Boldface limits apply across the operating ambient temperature range, T_A -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNITS
OUTPUT CURRENT SENSE INPUT BIAS CURRENT					
VOUT Referenced	ISENA0 or ISENA1	**-100**		**100**	nA
	ISENB0 or ISENB1	**-25**		**25**	µA
OUTPUT CURRENT SENSE MONITOR AND FAULT DETECTION					
IOUT Monitor Temperature Compensation	Factory default		3900		ppm/°C
	Configurable via PMBus™	**100**		**12700**	ppm/°C
VMON BIAS MONITOR AND FAULT DETECTION					
VMON UVLO Threshold Range	Using VMON pin with 16:1 resistor divider	**2.85**		**5**	V
VMON Accuracy (Note 13)	Full Scale (FS) = 1.15V	**-2**		**2**	% FS
VMON Resolution	Full Scale (FS) = 1.15V		±0.15		% FS
VMON UV/OV Fault Response Delay			200		µs
TEMPERATURE SENSING					
INTERNAL TEMPERATURE SENSOR					
Internal Temperature Accuracy	Tested at +100°C	-5		5	°C
Internal Temperature Resolution			1		°C
Thermal Protection Threshold (junction temperature)	Factory default		125		°C
	Configurable via PMBus™	**-40**		**125**	°C
Thermal Protection Hysteresis			15		°C
EXTERNAL TEMPERATURE SENSOR: XTEMP0 and XTEMP1					
External Temperature Accuracy			±5		°C
External Temperature Resolution			1		°C
Thermal Protection Threshold	Factory default		125		°C
	Configurable via PMBus™	**-40**		**125**	°C
Thermal Protection Hysteresis			15		°C

NOTES:

9. Output current is limited by device thermal dissipation.
10. Percentage of Full Scale (FS) with temperature compensation applied.
11. V_{OUT} measured at the termination of the VSENP and VSENN sense points.
12. For operation at 400kHz, see PMBus™ Power System Management Protocol Specification Part 1, Section 5.2.6.2 for timing parameter limits.
13. Does not include errors due to resistor divider tolerances.
14. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

ZL8801 Overview

Digital-DC Architecture Overview

The ZL8801 is an innovative mixed-signal power conversion and power management IC based on Intersil patented Digital-DC technology that provides an integrated, high performance step-down converter for a wide variety of power supply applications.

The ZL8801 DC/DC controller is a dual phase controller based on an architecture that does not require loop compensation. Adaptive algorithms enable the power converter to automatically change the operating state to increase efficiency and overall performance with no user interaction needed.

The ZL8801 is a full digital loop that achieves precise control of the entire power conversion process with no software required resulting in a very flexible device that is also very easy to use. The ChargeMode control algorithm is implemented that responds to output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers. An extensive set of power management functions are fully integrated and can be configured using simple pin connections. The user configuration can be saved in an internal nonvolatile memory (NVRAM). Additionally, all functions can be configured and monitored via the SMBus hardware interface using standard PMBus™ commands, allowing ultimate flexibility. The ZL8801 is compliant with the PMBus™ Power System Management Protocol Specification Part I and II version 1.2.

Once enabled, the ZL8801 is immediately ready to regulate power and perform power management tasks with no programming required. Advanced configuration options and real-time configuration changes are available via PMBus™ commands if desired and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated subregulation circuitry enables single supply operation from any supply between 4.5V and 14V with no bias supplies needed.

The ZL8801 can be configured by simply connecting its pins according to the tables provided in the following sections. Additionally, a comprehensive set of online tools and application notes are available to help simplify the design process. An evaluation board is also available to help the user become familiar with the device. This board can be evaluated as a standalone platform using pin configuration settings. A Windows™ based GUI is also provided to enable full configuration and monitoring capability via the SMBus interface and the included USB cable.

Power Management Overview

The ZL8801 incorporates a wide range of configurable power management features that are simple to implement with no external components. Additionally, the ZL8801 includes circuit protection features that continuously safeguard the device and load from damage due to unexpected system faults. The ZL8801 can continuously monitor input voltage and current, output voltage and current, internal temperature and the temperature of an external thermal diode. A power-good output signal is also included to enable power-on reset functionality for an external processor.

All power management functions can be configured using either pin configuration techniques described in this document or via the SMBus interface using PMBus™ commands. Monitoring parameters can also be preconfigured to provide alerts for specific conditions. “PMBus™ Command Detail” starting on page 30, contains a listing of all the PMBus™ commands supported by the ZL8801 and a detailed description of the use of each of these commands.

Multi-mode Pins

In order to simplify circuit design, the ZL8801 incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device with no programming. Most power management features can be configured using these pins. The multi-mode pins can respond to four different connections as shown in Table 2. These pins are sampled when power is applied.

Pin-strap Settings: This is the simplest implementation method, as no external components are required. Using this method, each pin can take on one of three possible states: LOW, OPEN, or HIGH. These pins can be connected to the V25 pin for logic HIGH settings (excluding VDRVEN which should be left floating or tied to VR5). Using a single pin, one of three settings can be selected.

TABLE 2. MULTI-MODE PIN CONFIGURATION

PIN TIED TO	VALUE
LOW (Logic LOW)	<0.8 VDC
OPEN (N/C)	No connection
HIGH (Logic HIGH)	>2.0 VDC
Resistor to SGND	Set by resistor value

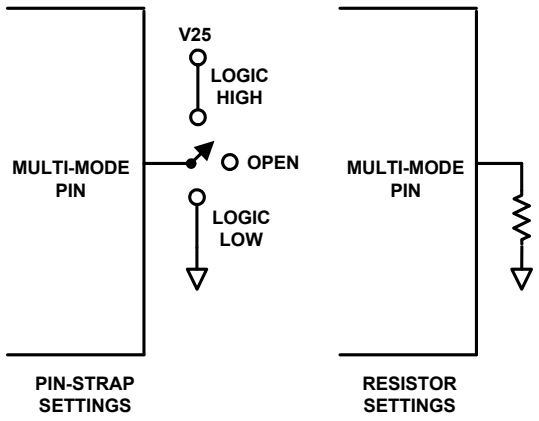


FIGURE 4. PIN-STRAP AND RESISTOR SETTING

Resistor Settings: This method allows a greater range of adjustability when connecting a finite value resistor (in a specified range) between the multi-mode pin and SGND. Standard 1% resistor values are used and only every fourth E96 resistor value is used so the device can reliably recognize the value of resistance connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

SMBus: Almost any ZL8801 function can be configured via the SMBus interface using standard PMBus™ commands. Additionally, any value that has been configured using the pin-strap or resistor setting methods can also be reconfigured and/or verified via the SMBus. The “PMBus™ Command Detail” section, starting on page 30, explains the use of the PMBus™ commands in detail.

Configurable Pins

Four operating parameters can be set using the pin-strap or resistor setting method: The SMBus address (pin 5, SA), output voltage (pin 10, VSET), switching frequency (pin 44, SYNC) and input voltage undervoltage lockout (pin 13, UVLO).

The SMBus device address and the output voltage are the only parameters that must be set by external pins. All other device parameters can be set via the SMBus. The device address is set using the SA pin. The output voltage is set using the VSET pin.

SMBus Device Address Selection (SA)

When communicating with multiple SMBus devices using the SMBus interface, each device must have its own unique address so the host can distinguish between the devices. The device address can be set according to the pin-strap options listed in Table 3. The SMBus address cannot be changed with a PMBus™ command.

TABLE 3. SMBus DEVICE ADDRESS SELECTION

RSA (kΩ)	SMBus ADDRESS	RSA (kΩ)	SMBus ADDRESS
LOW (SGND)	26h	42.2	28h
OPEN	28h	46.4	29h
10	19h	51.1	2Ah
11	1Ah	56.2	2Bh
12.1	1Bh	61.9	2Ch
13.3	1Ch	68.1	2Dh
14.7	1Dh	75	2Eh
16.2	1Eh	82.5	2Fh
17.8	1Fh	90.9	30h
19.6	20h	100	31h
21.5	21h	110	32h
23.7	22h	121	33h
26.1	23h	133	34h
28.7	24h	147	35h
31.6	25h	162	36h
34.8	26h	178	37h
38.3	27h		

Output Voltage and VOUT_MAX Selection (VSET)

The output voltage may be set to any voltage between 0.54V and 5.5V provided that the input voltage is higher than the desired output voltage by at least 1.1V. Using the pin-strap method, V_{OUT} can be set to any of the voltages shown in Table 4. The V_{OUT} can also be set using a PMBus™ command. VOUT_MAX is also determined by this pin-strap setting and is 10% greater than the VSET voltage setting. VOUT_MAX can be set higher than this pin-strap setting using the VOUT_MAX PMBus command.

TABLE 4.

RVSET (kΩ)	V_{OUT} (V)	RVSET (kΩ)	V_{OUT} (V)
LOW (SGND)	1.00	38.3	1.30
OPEN	1.20	42.2	1.40
HIGH (>2.0V)	2.50	46.4	1.50
10	0.60	51.1	1.60
11	0.65	56.2	1.70
12.1	0.70	61.9	1.80
13.3	0.75	68.1	1.90
14.7	0.80	75	2.00
16.2	0.85	82.5	2.10
17.8	0.90	90.9	2.20
19.6	0.95	100	2.30
21.5	1.00	110	2.50
23.7	1.05	121	2.80
26.1	1.10	133	3.00
28.7	1.15	147	3.30
31.6	1.20	162	4.00
34.8	1.25	178	5.00

Switching Frequency Setting (SYNC)

The device's switching frequency is set from 200kHz to 1333kHz using the pin-strap method as shown in Table 5, or by using a PMBus™ command. The ZL8801 generates the device switching frequency by dividing an internal precision 16MHz clock by integers from 12 to 80. 500kHz (n = 32) and 1000kHz (n = 16) are not recommended operating frequencies; use 533kHz (or 516kHz if setting the frequency with PMBus) and 1067kHz instead.

TABLE 5.

RSYNC (kΩ)	FREQ (kHz)	RSYNC kΩ	FREQ (kHz)
LOW (SGND)	200	23.7	471
OPEN	400	26.1	533
HIGH (>2.0V)	1067	28.7	571
10	200	31.6	615
11	222	34.8	727
12.1	242	38.3	800
13.3	267	42.2	842
14.7	296	46.4	889
16.2	320	51.1	1067
17.8	364	56.2	1143
19.6	400	61.9	1231
21.5	421	68.1	1333

The ZL8801 incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Intersil digital power devices.

The SYNC pin can also be configured as an input. When configured as an input, the device will automatically check for a clock signal on the SYNC pin each time EN is asserted. The ZL8801's oscillator will then synchronize with the rising edge of the external clock.

The incoming clock signal must be in the range of 200kHz to 1.33MHz, meet the limits given in the "Logic Input/Output Characteristics" on page 9 and must be stable when the enable pin (EN) is asserted. When using an external clock, the frequencies are not limited to discrete values as when using the internal clock. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns. In the event of a loss of the external clock signal, the output voltage may show transient overshoot or undershoot.

If loss of synchronization occurs, the ZL8801 will automatically switch to its internal oscillator and switch at its configured frequency. For this reason, it is important to configure the ZL8801 to a frequency close to the expected external clock frequency.

The SYNC pin can also be configured as an output. The device will run from its internal oscillator and will drive the SYNC pin so other devices can be synchronized to it. The output will conform to the limits given in the "Logic Input/Output Characteristics" on page 9. The SYNC pin will not be checked for an incoming clock signal while in this mode.

The switching frequency can be set to any value between 200kHz and 1.33MHz using a PMBus™ command. The available frequencies below 1.33MHz are defined by f_{SW} = 16MHz/N, where 12 ≤ N ≤ 80.

If a value other than f_{SW} = 16MHz/N is entered using a PMBus™ command, the internal circuitry will select the switching frequency value using N as a whole number to achieve a value close to the entered value. For example, if 810kHz is entered, the device will select 800kHz (N = 20).

Input Voltage Undervoltage Lockout Setting (UVLO)

The input undervoltage lockout (UVLO) prevents the ZL8801 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The input voltage undervoltage lockout threshold can be set between 2.85V and 16V using the pin-strap method as shown in Table 6. The UVLO can also be set or changed using the VIN_UV_FAULT_LIMIT command.

TABLE 6.

RUVLO (kΩ)	UVLO (V)	RUVLO (kΩ)	UVLO (V)
LOW (SGND)	Not used	46.4	7.42
OPEN	4.5	51.1	8.18
HIGH (>2.0V)	10.8	56.2	8.99
26.1	4.18	61.9	9.90
28.7	4.59	68.1	10.90
31.6	5.06	75	12.00
34.8	5.57	82.5	13.20
38.3	6.13	90.9	14.54
42.2	6.75	100	16.00

Once an input undervoltage fault condition occurs, the user may determine the desired response to the fault condition. The following input undervoltage protection response options are available:

1. Shut down and stay off until the fault has cleared and the device has been disabled and reenabled.
2. Shut down and restart continuously after a delay.

The default response from an undervoltage fault is to shut down and stay off until the fault has cleared and the device has been disabled and reenabled (see option 1).

Refer to "PMBus™ Command Detail", starting on page 30 of this document, for details on how to select specific undervoltage fault response options using the VIN_UV_FAULT_RESPONSE command.

When controlling the ZL8801 exclusively through the PMBus™, a high voltage setting for UVLO can be used to prevent the ZL8801 from being enabled until a lower voltage for UVLO is set using the VIN_UV_FAULT_LIMIT command.

Internal Bias Regulators and Input Supply Connections

The ZL8801 employs internal low dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

VR6: The VR6 LDO provides a regulated 6.1V bias supply for internal circuitry. It is powered from the VDD pin. A 4.7µF ceramic X7R filter capacitor to SGND is required at the VR6 pin. Keep this net as small as possible and avoid routing this net near any switching signals.

VR5: The VR5 LDO provides a regulated 5.1V bias supply for internal circuitry. It is powered from the VDD pin. A 4.7µF ceramic X7R filter capacitor to SGND is required at the VR5 pin. This supply may be used for to provide a pull-up supply as long as load current does not exceed 5mA.

V25: The V25 LDO provides a regulated 2.5V bias supply for the main controller circuitry. It is powered from an internal 5V node. A 4.7µF ceramic X7R filter capacitor to SGND is required at the V25 pin. The V25 supply is used to power internal IC circuitry. It should only be used externally to set pin-strap pins to the HIGH state.

VDRV: The VDRV LDO provides a regulated 5.25V bias supply for external MOSFET driver ICs or DrMOS integrated drivers/FETs. A 4.7µF ceramic X7R filter capacitor to PGND is required, however, additional capacitance will be needed as specified by the MOSFET driver or DrMOS device selected. The maximum rated output current is 80mA, but device thermal limits must be considered. The power dissipated by the VDRV supply, as shown by Equation 1.

$$(VIN - 5.25V) \times IDRV \quad \text{(EQ. 1)}$$

where IDRV is the current supplied by the VDRV bias supply. The VDRV is enabled by leaving the VDRVEN unconnected (floating) or connecting it to VR5 and is disabled by connecting VDRVEN to ground.

NOTE: The internal bias regulators, VR6, VR5 and V25, are not designed to be outputs for powering other circuitry. The multi-mode pins may be connected to the V25 pin for logic HIGH settings and the VR5 supply should be used to provide up to 5mA of pull-up current for the SDA, SCL, SALRT, DDC and PG pins.

Operation with 5V VDD: When operating the ZL8801 at voltages below 5.5V, the VR6 and VR5 supplies should be connected directly to V_{DD} for best performance. The VDRV supply should not be used; the 5V VDD supply should be used instead for powering DrMOS and MOSFET driver ICs.

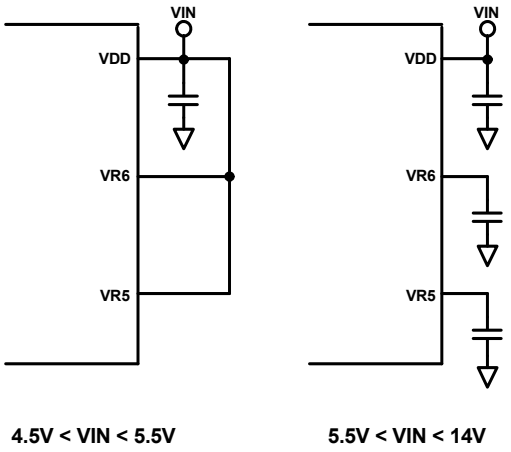


FIGURE 5.

Start-up Procedure

The ZL8801 follows a specific internal start-up procedure after power is applied to the VDD pin, as shown in Figure 6.

The device requires approximately 30ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded.

Once this process is completed, the device is ready to accept commands via the serial interface and the device is ready to be enabled. If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. Once enabled, the device requires approximately 2ms before its output voltage may be allowed to start its ramp-up process.

After the TON_DELAY period has expired, the output will begin to ramp towards its target voltage according to the preconfigured ton-rise time.

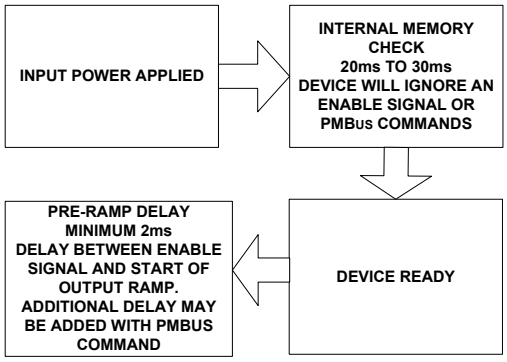


FIGURE 6. ZL8801 INTERNAL START-UP PROCEDURE

The V_{IN} should be above the ZL8801's UVLO limit (VIN_UV_FAULT_LIMIT) before the Enable pin is driven high. Following this sequence will result in the most consistent turn-on delays. When V_{IN} is first applied to the ZL8801, for example during initial PCB turn-on and test, the Enable pin must be held low by some means until the ZL8801 configuration file can be loaded. If the Enable pin is not held low, then the ZL8801 may attempt to turn-on with incorrect configuration settings, possibly causing circuit failure.

In those cases where the Enable pin cannot be held low during the initial application of power, two options are available:

1. Limit V_{IN} to 3.0V during initial testing. The ZL8801 configuration file can be loaded when V_{IN} is as low as 3V. Once the configuration file is loaded V_{IN} can be increased to the normal input voltage range.
2. Use a 100kΩ resistor to set UVLO to 16V. This will keep the ZL8801 disabled while the configuration file is loaded. Ensure that the VIN_UV_FAULT_LIMIT command is the last command in the configuration file.

TON Delay and Rise Times

In some applications, it may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. The ZL8801 gives the system designer the ability to independently control both the delay and ramp time periods.

The TON_DELAY time begins when the EN pin is asserted. The TON_DELAY time is set using the PMBus™ command TON_DELAY.

The TON-RISE time enables a precisely controlled ramp to the nominal V_{OUT} value that begins once the TON_DELAY time has expired. The ramp-up is monotonic and its slope may be precisely set using the PMBus™ command TON_RISE.

The TON_DELAY and TON_RAMP times can be set using PMBus™ commands TON_DELAY and TON_RISE over the serial bus interface. When the TON_DELAY time is set to 0ms, the device will begin its ramp after the internal circuitry has initialized.

The TON_DELAY and TON_RAMP times can be set using PMBus™ commands TON_DELAY and TON_RISE over the serial bus interface. When the TON_DELAY time is set to 0ms, the device will begin its ramp after the internal circuitry has initialized which takes approximately 2ms to complete. The TON_RISE time may be set to values less than 2ms, however the TON_RISE time should be set to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current. A lower TON_RISE time limit can be estimated using the formula as shown by Equation 2.

$$TON\_RISE = C_{OUT} * V_{OUT} \quad \text{(EQ. 2)}$$

Where C_{OUT} is the total output capacitance, V_{OUT} is the output voltage and limit is the current limit setting for the ZL8801.

When interdevice current sharing is used (4-, 6- or 8- phases), the output voltage rise time will vary by application. The rise time in this case can be adjusted using the PMBus command MULTI_PHASE_RAMP_GAIN. Higher gain values produce faster turn-on ramps. Typical MULTI_PHASE_RAMP_GAIN values range between 1 and 10; the default value is 3.

Enable

The enable pin (EN) is used to enable and disable the ZL8801. The enable pin should be held low whenever a configuration file or script is used to configure the ZL8801, or a PMBus™ command is sent that could potentially damage the application circuit. When the ZL8801 is used in a self-enabled mode, for example, when EN is tied to VR5, or to a resistor divider to V_{IN}, the user must consider the ZL8801's default factory settings. When a configuration file is used to configure the ZL8801, the factory default settings are restored to both the user and default stores in order to set the ZL8801 to an initialized state. Since the default state of the ZL8801 is to be enabled when the enable pin is high, it is possible for the ZL8801 to be enabled while the PMBus™ commands are sent to the ZL8801 during the configuration process. For this reason self-enabled mode is not recommended for the ZL8801.

Power-good

The ZL8801 provides a power-good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within 10% of the target voltage. These limits may be changed using PMBus™ commands.

A PG delay period is defined as the time from when all conditions within the ZL8801 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL8801 PG delay is set equal to 1ms. The PG delay may be set using a PMBus™ command as described in the "PMBus™ Command Summary" on page 25.

Power Management Functional Description

Output Overvoltage Protection

The ZL8801 offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VSEN pins) to a programmable threshold set to 10% higher than the target output voltage (the default setting). If the VSEN voltage exceeds this threshold, the PG pin will deassert and the device can then respond to the following options:

1. Shut down and stay off until the fault has cleared and the device has been disabled and reenabled.
2. Shut down and restart continuously after a delay.

The default response from an overvoltage fault is to shut down and stay off until the fault has cleared and the device has been disabled and reenabled (see option 1).

Refer to the "PMBus™ Command Detail" section, starting on page 30, for details on how to select specific overvoltage fault response options using the VOUT_OV_FAULT_RESPONSE command.

Output Prebias Protection

The ZL8801 provides prebiased start-up operation. An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The ZL8801 provides

prebias protection by sampling the output voltage prior to initiating an output ramp. If a prebias voltage lower than the desired output voltage is present after the TON_DELAY time, the ZL8801 starts switching with a duty cycle that matches the prebias voltage. This ensures that the ramp-up from the prebias voltage is monotonic. The output voltage is then ramped to the desired output voltage at the ramp rate set by the TON_RISE command. The resulting output voltage rise time will vary depending on the prebias voltage, but the total time elapsed from the end of the TON_DELAY time to when the TON-RISE time is complete and the output is at the desired value will match the preconfigured ramp time (see Figure 7).

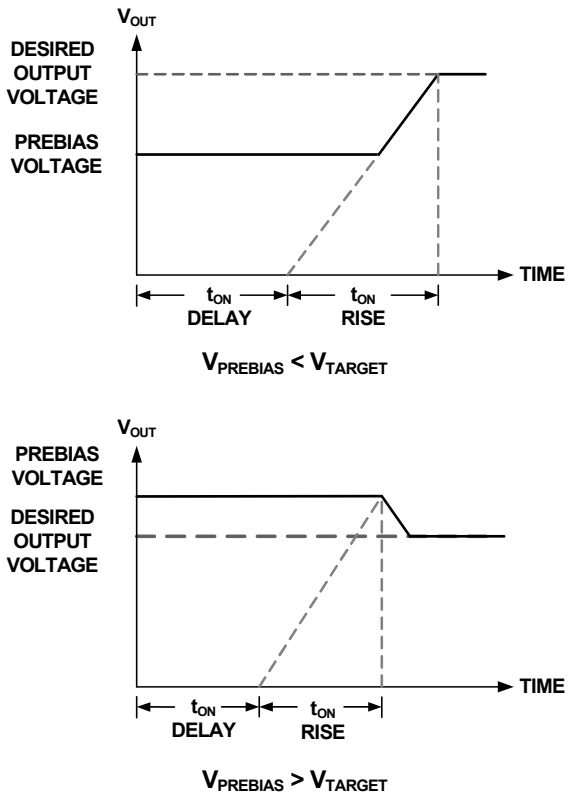


FIGURE 7. OUTPUT RESPONSES TO PREBIAS VOLTAGES

If a prebias voltage higher than the target voltage exists after the preconfigured TON-DELAY time and TON-RISE time have completed, the ZL8801 starts switching with a duty cycle that matches the prebias voltage. This ensures that the ramp down from the prebias voltage is monotonic. The output voltage is then ramped down to the desired output voltage.

If a prebias voltage higher than the overvoltage limit exists, the device will not initiate a turn on sequence and will stay off with an output OV fault recorded.

Output Overcurrent Protection

The ZL8801 can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. Once the current limit threshold has been selected (see "Current Limit Configuration" on page 18), the user may determine the desired response to the fault condition. The following overcurrent protection response options are available:

1. Shut down and stay off until the fault has cleared and the device has been disabled and reenabled.
2. Shut down and restart continuously after a delay.

The default response from an overcurrent voltage fault is to shut down and stay off until the fault has cleared and the device has been disabled and reenabled (see option 1).

Refer to the "PMBus™ Command Detail" section, starting on page 30, for details on how to select specific overcurrent fault response options using the IOUT_OC_FAULT_RESPONSE command.

CURRENT SENSING COMPONENTS

The ZL8801 uses the inductor DCR current sensing technique. Current sensing is achieved by selecting an R/C network as shown in Figure 8.

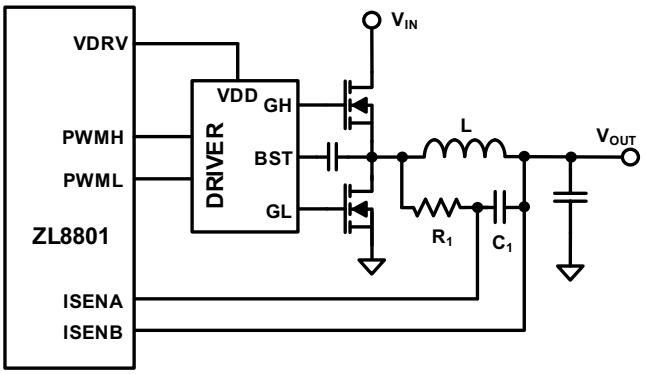


FIGURE 8. DCR CURRENT SENSING (ONLY 1 PHASE SHOWN)

For the voltage across C_1 to reflect the voltage across the DCR of the inductor, the time constant of the inductor must match the time constant of the RC network, as shown in Equation 3:

$$\tau_{RC} = \tau_{L/DCR}$$
$$R1 \cdot C1 = \frac{L}{DCR} \quad \text{(EQ. 3)}$$

For L, use the average of the nominal value and the minimum value. Include the effects of tolerance, DC bias and switching frequency on the inductance when determining the minimum value of L. Use the typical room temperature value for *DCR*.

The value of R_1 should be as small as feasible and no greater than 5kΩ for best signal-to-noise ratio. The designer should make sure the resistor package size is appropriate for the power dissipated and include this loss in efficiency calculations. In calculating the minimum value of R_1, the average voltage across C_1 (which is the average I_{OUT}, DCR product) is small and can be neglected. Therefore, the minimum value of R_1 may be approximated by Equation 4:

$$R1_{min} = \left(\frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{P_{R1}}\right) \quad \text{(EQ. 4)}$$

where P_{R1} is the maximum power dissipation specification for the resistor. Once $R1_{min}$ has been calculated, solve for the maximum value of C1 from Equation 5:

$$C1_{max} = \frac{L}{R1_{min} \cdot DCR} \quad \text{(EQ. 5)}$$

Choose the next lowest readily available value (e.g., for $C1_{max}$ = 1.86µF, C_1 = 1.5µF is a good choice). Then substitute the chosen value into the same equation and recalculate the value of R_1. Choose the 1% resistor standard value closest to this recalculated value of R_1.

Current Limit Configuration

The ZL8801 gives the power supply designer several choices for the fault response during over or undercurrent condition. The user can select the number of violations allowed before declaring fault, a blanking time and the action taken when a fault is detected. These parameters are configured using the ISENSE_CONFIG command.

The blanking time represents the time when no current measurement is taken. This is to avoid taking a reading just after a switching transition (less accuracy due to potential ringing). It is a configurable parameter from 0 to 832ns.

The ZL8801 provides an adjustable maximum full scale sensing range. Three ranges are available: ±25mV, ±35mV and ±50mV maximum input voltage.

By default, current sensing is enabled during the inductor current down slope period of the switching period (D). In applications where the steady state duty cycle is >0.5, for example a 5V to 3.3V converter, the ZL8801 can be configured to sense current during the inductor up slope period of the switching cycle (D).

The user has the option of selecting how many consecutive overcurrent readings must occur before an overcurrent fault and subsequent shutdown are initiated. Either 1, 3, 5, 7, 9, 11, 13 or 15 consecutive faults can be selected.

Once the ISENSE_CONFIG parameters have been selected, the user must select the desired current limit thresholds and the resistance of the sensing element.

The current limit thresholds are set with 4 commands:

1. **IOUT_OC_FAULT_LIMIT** – this sets the overcurrent threshold that must be exceeded by the number of consecutive times chosen in ISENSE_CONFIG.
2. **IOUT_UC_FAULT_LIMIT** – this is the same as IOUT_OC_FAULT_LIMIT, but represents the negative current that flows in the lower FET during the D' interval. Large negative currents can flow during faults such as when a higher voltage rail is shorted to a lower voltage rail.
3. **IOUT_AVG_OC_FAULT_LIMIT** – this limit is similar to IOUT_OC_FAULT_LIMIT, but the limit represents an average reading over several switching cycles. Since it is an average, the response time is slower, but the limit can be set closer to the maximum average expected output current.
4. **IOUT_AVG_UC_FAULT_LIMIT** – this limit is similar to IOUT_AVG_OC_FAULT_LIMIT, but represents the negative current that flows in the lower FET during the D' interval.

Input Current Monitor

The input current can be monitored through the IINN and IINP pins. The input current monitor input should be connected across a current sensing resistor in series with the input supply. The IINP pin is connected to the input supply side of the current sense resistor, the IINN pin is connected to the ZL8801 VDD side of the current sense resistor. Using the IIN_SCALE command, set the current sense resistor value. Select the current sense resistor value such that the maximum expected input current times the current sense resistor value does not exceed the maximum current sensing input voltage of 20mV. If this feature is not used, IINN and IINP should be tied to VDD.

Thermal Overload Protection

The ZL8801 includes an on-chip thermal sensor that continuously measures the internal temperature of the die. This thermal sensor is used to provide both over-temperature and under-temperature protection. If the over-temperature limit is exceeded, or the temperature falls below the under-temperature limit, the ZL8801 is shut down. The over-temperature and under-temperature limits are set by the OT_FAULT_LIMIT and UT_FAULT_LIMIT respectively. The ZL8801 will not attempt to restart until the temperature has fallen below the OT_WARN_LIMIT for over-temperature faults or has risen above the UT_WARN_LIMIT for under-temperature faults. The default temperature limits are +125°C and -45°C, but the user may set the limits to different values if desired. Note that setting a higher over-temperature or under-temperature limit may result in permanent damage to the device. Once the device has been disabled due to an internal temperature fault, the user may select one of the fault response options as follows:

1. Shut down and stay off until the fault has cleared and the device has been disabled and reenabled.
2. Shut down and restart continuously after a delay.

The default response from an over-temperature or under-temperature fault is to shut down and stay off until the fault has cleared and the device has been disabled and reenabled (see option 1).

Refer to the "PMBus™ Command Detail" section, starting on page 30, for details on how to select specific over-temperature or under-temperature fault response options using the OT_FAULT_RESPONSE and UT_FAULT_ RESPONSE commands.

Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications.

The ZL8801 integrates a tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. The VTRK pin is an analog input that, when tracking mode is enabled, configures the voltage applied to the VTRK pin to act as a reference for the device's output regulation. Tracking can only be used when operating as a 2-phase controller, i.e.; when the device is not part of a current sharing group.

Figure 9 illustrates the typical connection and the two tracking modes:

Coincident: This mode configures the ZL8801 to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.

Ratiometric. This mode configures the ZL8801 to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor string may be used to configure a different tracking ratio. The device that is tracking another output voltage (slave) must be set to its desired steady-state output voltage.

The master ZL8801 device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode.

The maximum tracking rise-time is 1V/ms. The slave device must be enabled before the master.

Any device that is configured for tracking mode will ignore its TON_DELAY and TON_RISE settings and its output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin.

Tracking mode can be configured by using the TRACK_CONFIG command.

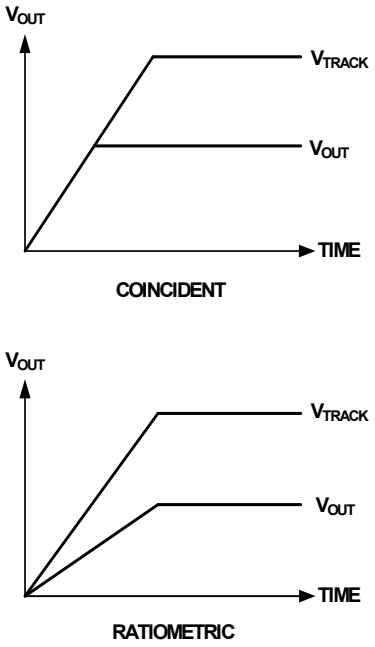


FIGURE 9. TRACKING MODES

Voltage Margining

The ZL8801 offers a simple means to vary its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. Margining is controlled through the OPERATION command.

Default margin limits of V_{OUT} ±5% are preloaded in the factory, but the margin limits can be modified through to be as high as 5.5V or as low as 0V.

Additionally, the transition rate between the nominal output voltage and either margin limit can be configured using the VOUT_TRANSITION_RATE command.

External Voltage Monitoring

The voltage monitoring (VMON) pin is available to monitor the voltage supply for the external driver IC. The VMON input must be scaled by a 16:1 ratio in order to read-back the VMON voltage correctly. A 100kΩ and 6.65kΩ resistor divider is recommended. Overvoltage and undervoltage fault thresholds can be set using MFR_VMON_OV_FAULT_LIMIT and MFR_ VMON_UV_FAULT_LIMIT commands. The response to these limits are set using the VMON_OV_FAULT_RESPONSE and VMON_ UV_FAULT_RESPONSE commands.

Once the device has been disabled due to VMON fault, the user may select one of the following fault response option:

1. Shut down and stay off until the fault has cleared and the device has been disabled and reenabled.
2. Shut down and restart continuously after a delay.

The default response from an overvoltage or undervoltage VMON fault is to shut down and stay off until the fault has cleared and the device has been disabled and reenabled (see option 1).

SMBus Communications

The ZL8801 provides a SMBus digital interface. The ZL8801 can be used with any standard 2-wire SMBus host device. In addition, the device is compatible with SMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the SMBus. The pull-up resistor may be tied to VR5 or to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that will ensure a logic 0 (typically 0.8V at the device monitoring point) given the pull-up voltage (5V if tied to VR5) and the pull-down current capability of the ZL8801 (nominally 4mA). A pull-up resistor of 10kΩ is a good value for most applications.

The SMBus Data and Clock lines should be routed with a closely coupled return or ground plane to minimize coupled interference (noise). Excessive noise on the data and clock lines that cause the voltage on these lines to cross the high and low logic thresholds of 2.0V and 0.8V respectively, will cause command transmissions to be interrupted and result in slow bus operation or missed commands. For less than 10 devices on an SMBus, a 10kΩ resistor on each line provides good performance.

The ZL8801 accepts most standard PMBus™ commands. When enabling the device with ON_OFF_CONFIG command, it is recommended that the enable pin is tied to SGND.

In addition to bus noise considerations, it is important to ensure that user connections to the SMBus are compliant to the PMBus™ command standards. Any device that can malfunction

in a way that permanently shorts SMBus lines will disable PMBus™ communications. Incomplete PMBus™ commands can also cause the ZL8801 to halt PMBus™ communications. This can be corrected by disabling, then reenabling the device.

Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Intersil digital power Digital-DC devices. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading and current sharing. The DDC pin must be pulled up to an external 3.3V or 5.0V supply, even if the ZL8801 is operating standalone. If the ZL8801 is used in a standalone circuit and will not have its DDC pin connected to any other devices, the ZL8801 DDC pin can be configured as a push-pull output using the MFR_USER_CONFIG command and the pull-up resistor can be eliminated. In addition, the DDC pin must be pulled up (or configured as a push-pull output, with the limitations listed previously) before the Enable pin is set high. The DDC pin on all Digital-DC devices that utilize sequencing, fault spreading or current sharing must be connected together. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to guarantee the rise time as shown by Equation 6:

$$\text{Rise Time} = R_{PU} * (C_{LOAD} \leq 1\mu s) \quad \text{(EQ. 6)}$$

Where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor may be tied to VR5 or to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. As a rule of thumb, each device connected to the DDC bus presents approximately 12pF of capacitive loading. The ideal design will use a central pull-up resistor that is well matched to the total load capacitance. In power module applications, the user should consider whether to place the pull-up resistor on the module or on the PCB of the end application. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that will ensure a logic 0 (typically 0.8V at the device monitoring point) given the pull-up voltage (5V if tied to VR5) and the pull-down current capability of the ZL8801 (nominally 4mA). As with SMBus data and clock lines, the DDC data line should be routed with a closely coupled return or ground plane to minimize coupled interference (noise). Excessive noise on the DDC signal can cause the voltage on this line to cross the high and low logic thresholds of 2.0V and 0.8V respectively and will cause command transmissions to be interrupted and result in slow bus operation or missed commands. For less than 10 devices on the DDC bus, a 10kΩ resistor provides good performance.

Phase Spreading

When multiple point-of-load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices have coincident rising edges. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to I_{RMS}^2 are reduced.

In order to enable phase spreading, all converters must be synchronized to the same switching clock. Configuring the SYNC pin is described in the Configuration Pin on page 6 The ZL8801 will automatically offset the phase of parallel connected ZL8801s in a current sharing group. Selecting the phase offset for the device is accomplished by selecting a device address according to Equation 7:

$$\text{Phase offset} = \text{device address} \times 45° \quad \text{(EQ. 7)}$$

This behavior is illustrated in Table 7.

TABLE 7.

ADDRESS LSB	PHASE OFFSET (°)	ADDRESS LSB	PHASE OFFSET (°)
0	0	8	0
1	45	9	45
2	90	A	90
3	135	B	135
4	180	C	180
5	225	D	225
6	270	E	270
7	315	F	315

The phase offset of each device may also be set to any value between 0° and 360° in 22.5° increments using the INTERLEAVE PMBus™ command.

Output Sequencing

A group of Intersil digital power devices may be configured to power-up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs and ASICs that require one supply to reach its operating voltage prior to another supply reaching its operating voltage in order to avoid latch-up from occurring. Multi-device sequencing can be achieved by configuring each device using the SEQUENCE PMBus™ command.

Multiple device sequencing is achieved by issuing PMBus™ commands to assign the preceding device in the sequencing chain as well as the device that will follow in the sequencing chain.

The enable (EN) pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn on of the group. Enable must be driven low to initiate a sequenced turn off of the group. The DDC pins of all devices in a sequencing group must be connected together to ensure accurate sequencing.

Sequencing can also be accomplished by connecting the enable pin of a sequel device to the power-good pin of a prequel device. Sequencing is also achieved by using the TON_DELAY and TON_RISE commands and choosing appropriate delay and rise durations such that sequel devices start after their associated prequel devices. The drawback to this method is that if a prequel device fails to start properly, its sequel device will still start and ramp on according to its delay and rise time settings. The best sequencing performance is achieved by using the SEQUENCE command and tying the Enable and DDC pins of the sequencing

group devices together. If the DDC pins of the devices are not connected together and the user depends on TON_DELAY and TOFF_DELAY values alone to ensure device sequencing, timing accuracy will suffer. This is due to the 0ms to 4ms delay variability between ZL8801 devices.

Fault Spreading

Digital-DC devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the DDC bus. The other devices on the DDC bus will shut down together if configured to do so, and will attempt to restart in their prescribed order if configured to do so.

Active Current Sharing

The PWM outputs of the ZL8801 are used in parallel to create a dual phase power rail. The device outputs will share the current equally within a few percent, assuming all external sensing element variations and tolerances are negligible. Current sensing element tolerances must be taken into account, or adjusted for using the IOUT_CAL_GAIN and IOUT_CAL_OFFSET commands in any application.

Figure 10 shows a typical connection for a dual phase converter. The ZL8801 will current share between phases without utilizing output voltage droop.

Droop resistance is used in 4-, 6- and 8-phase current sharing to add artificial resistance in the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to power train components and PCB layout.

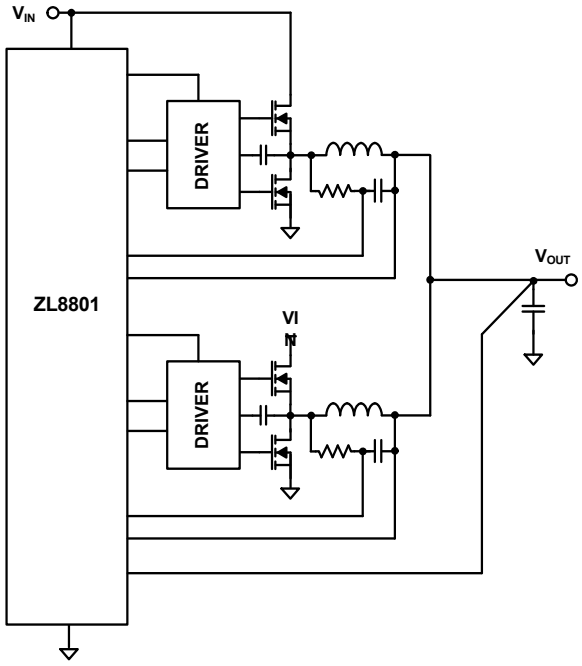


FIGURE 10. DUAL PHASE SIMPLIFIED CIRCUIT

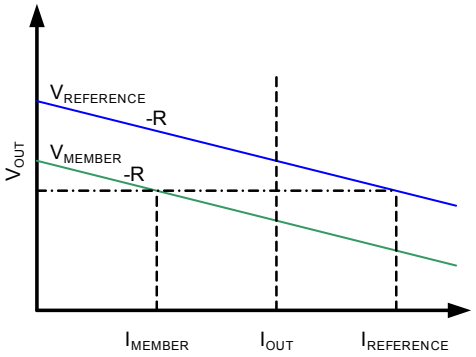


FIGURE 11. ACTIVE CURRENT SHARING

When current sharing up to 4 sets of ZL8801s (8 phases total), the ZL8801 uses a low-bandwidth, first-order digital current sharing technique to balance the unequal device output loading by aligning the load lines of member devices to a reference device.

Upon system start-up, the lowest numbered phase is defined as the reference phase and all other phases are member phases. The reference phase broadcasts its current over the DDC bus. The member phases use the reference current information to trim their reference voltages (V_{MEMBER}) to balance the current loading of each device in the system.

Figure 11 shows that, for load lines with identical slopes, the member reference voltage is increased towards the reference voltage, which closes the gap between the inductor currents.

The relation between reference and member current and voltage is given by Equation 8:

$$V_{MEMBER} = V_{OUT} + R \times \left(I_{REFERENCE} - I_{MEMBER} \right) \quad \text{(EQ. 8)}$$

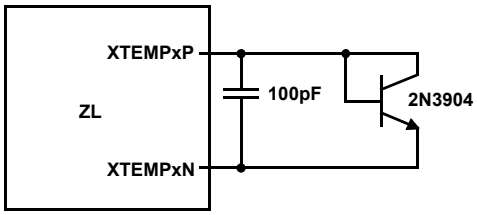
Where *R* is the value of the droop resistance.

The ISHARE_CONFIG command is used to configure the device for active current sharing. The default setting is a standalone non current sharing, two-phase device. A current sharing rail can be part of a system sequencing group.

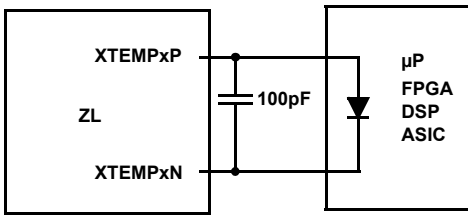
A 4-, 6- or 8-phase current sharing group must have their DDC and SYNC pins tied together in order to achieve current sensing and accurate phase offsets between current sharing phases.

Temperature Monitoring Using XTEMP Pin

The ZL8801 supports measurement of an external device temperature using either a thermal diode integrated in a processor, FPGA or ASIC, or using a discrete diode-connected 2N3904 NPN transistor. Figure 12 illustrates the typical connections required. A noise filtering capacitor, not exceeding 100pF, may be connected close to the ZL8801 XTEMP pins for long or noisy trace runs. The external temperature sensors can be used to provide the temperature reading for over-temperature and under-temperature faults. The external sensors can also be used to provide more accurate temperature compensation for inductor DCR current sensing by being placed close to the inductor. When routing the XTEMP signals between the inductor and the ZL8801, these PCB traces should be kept away from the switch node; (node connected the inductor to the MOSFET switches).



DISCRETE NPN



EMBEDDED THERMAL DIODE

FIGURE 12. EXTERNAL TEMPERATURE MONITORING

Nonvolatile Memory (NVRAM) and Security Features

The ZL8801 has internal nonvolatile memory where user configurations are stored. Integrated security measures ensure that the user can only restore the device to a level that has been made available to them. During the initialization process, the ZL8801 checks for stored values contained in its internal nonvolatile memory. The ZL8801 offers two internal memory storage units that are accessible by the user as follows:

User Store: The User Store is the most commonly used store. It provides the ability to modify certain power supply settings while still protecting the equipment from modifying values that can lead to a system level fault. The equipment manufacturer would use the User Store to achieve this goal.

Default Store: The default store is less commonly used. It provides a means to protect the circuit from damage by preventing the user from modifying certain values that are related to the physical construction of the circuit. In this case, the Original Equipment Manufacturer (OEM) would use the “Default Store” in a protected mode and allow the user to restore the device to its default settings. In this case, the “User Store” would be available to the end-user for making changes, but would restrict the user from restoring the device to the factory settings or modifying the default store.

The “User Store” takes priority over the “Default Store”. If there are no values set in the “User or Default Store”, then the device will use the pin-strap setting value.

For details regarding protection of the user and default stores, see the PASSWORD PMBus command.

DC/DC Converter Design

The ZL8801 operates as a voltage-mode, synchronous buck converter with a selectable constant frequency pulse width modulator (PWM) control scheme that uses external driver, MOSFETs, capacitors and an inductor to perform power conversion.

DUAL OUTPUT PWM PER PHASE

The ZL8801 has been designed to provide independent upper and lower FET drive signals to a 2 input MOSFET driver such as the ZL1505.

The ZL8801 utilizes adaptive deadtime control to improve the power conversion efficiency. The ZL8801 monitors the power converter’s operating conditions and continuously adjusts the turn-on and turn-off timing of the high-side and low-side driver input signals to optimize the overall efficiency of the power supply.

The ZL8801 can also be used with single-ended DrMOS integrated driver and MOSFET devices. The DrMOS device or single-ended MOSFET driver must have a fast-acting enable pin. Power supplies using DrMOS devices can be made smaller than discrete solutions utilizing separate drivers and MOSFETs, but at a slightly lower efficiency. The option to use DrMOS or drivers and discrete MOSFETs is set using the USER_CONFIG command.

Power Train Component Selection

The ZL8801 is a dual phase synchronous buck converter that uses external Drivers, MOSFETs, inductors and capacitors to perform the power conversion process. The proper selection of the external components is critical for optimized performance.

To select the appropriate external components for the desired performance goals, the power supply requirements listed in Table 8 must be known.

TABLE 8. POWER SUPPLY REQUIREMENTS

PARAMETER	EXAMPLE VALUE
Input Voltage (V_{IN})	12V
Output Voltage (V_{OUT})	1.2V
Output Current (I_{OUT})	30A
Output Voltage Ripple (V_{orip})	1% of V_{OUT}
Output Load Step (I_{ostep})	50% of I_o
Output Load Step Rate	10A/µs
Output Deviation Due to Load Step	±2%
Maximum PCB Temperature	+85°C
Desired Efficiency	90%
Other Considerations	Optimize for small size

DESIGN GOAL TRADE-OFFS

The design of the buck power stage requires several compromises among size, efficiency and cost. The inductor core loss increases with frequency, so there is a trade-off between a small output filter made possible by a higher switching frequency and getting better power supply efficiency. Size can be decreased by increasing the switching frequency at the expense of efficiency. Cost can be minimized by using through-hole inductors and capacitors; however these components are physically large.

To start the design, select a switching frequency based on Table 9. This frequency is a starting point and may be adjusted as the design progresses.

TABLE 9. CIRCUIT DESIGN CONSIDERATIONS

FREQUENCY RANGE	EFFICIENCY	CIRCUIT SIZE
200 to 400kHz	Highest	Larger
400 to 800kHz	Moderate	Smaller
800kHz to 1.33MHz	Lower	Smallest

INDUCTOR SELECTION

The output inductor selection process must include several trade-offs. A high inductance value will result in a low ripple current (ΔI_L), which will reduce output capacitance and produce a low output ripple voltage, but may also compromise output transient load performance. Therefore, a balance must be struck between output ripple and optimal load transient performance. A good starting point is to select the output inductor ripple equal to 30% to 50% of the maximum output current (I_{OUT}).

$\Delta I_L = 0.5 * I_{OUT}$

Now the output inductance can be calculated using Equation 9, where V_{IN} is the input voltage:

$$L = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{f_{sw} \times \Delta I_L} \quad \text{(EQ. 9)}$$

The average inductor current is equal to the maximum output current. The peak inductor current (I_{Lpk}) is calculated using Equation 10, where I_{OUT} is the maximum output current:

$$I_{Lpk} = I_{OUT} + \frac{I}{2} \quad \text{(EQ. 10)}$$

Select an inductor rated for the average DC current and with saturation current rating above the peak current calculated.

Once an inductor is selected, the DCR and core losses in the inductor are calculated. Use the DCR specified in the inductor manufacturer's datasheet, as shown in Equation 11:

$$P_{LDCR} = DCR \times I_{Lrms}{}^2 \quad \text{(EQ. 11)}$$

I_{Lrms} is given by Equation 12:

$$I_{Lrms} = \sqrt{I_{OUT}{}^2 + \frac{(\Delta I_L)^2}{12}} \quad \text{(EQ. 12)}$$

Where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor datasheet. Add the core loss and the ESR loss and compare the total loss to the maximum power dissipation recommendation in the inductor datasheet.

OUTPUT CAPACITOR SELECTION

Several trade-offs must also be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation (V_{step}) during transient load steps and low output voltage ripple (ΔV). However, capacitors with low ESR, such as X5R and X7R dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up or down to the new steady state output current value.

As a starting point, apportion one-half of the output ripple voltage to the capacitor ESR and the other half to capacitance, as shown in Equations 13 and 14:

$$C_{OUT} = \frac{\Delta I_L}{8 \times f_{sw} \times \frac{\Delta V}{2}} \quad \text{(EQ. 13)}$$

$$ESR = \frac{\Delta V}{2 \times \Delta I_L} \quad \text{(EQ. 14)}$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using Equation 15:

$$\Delta V = \Delta I_L \times ESR + \frac{\Delta I_L}{8 \times f_{sw} \times C_{OUT}} \quad \text{(EQ. 15)}$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the ΔV should be less than the desired maximum output ripple.

ChargeMode control achieves a fast-acting, low deviation transient response by detecting and reacting to very small variations in the output voltage. ChargeMode control performance is optimized when ΔV due to capacitor ripple is 1% or less of the output voltage.

INPUT CAPACITOR

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5V or 12V "bulk" supply from an off-line power supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This ripple (I_{inRMS}) can be determined from Equation 16:

$$I_{inRMS} = I_{OUT} \times \sqrt{D} \quad \text{(EQ. 16)}$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated above the ripple current calculated above and the maximum expected input voltage.

QL SELECTION

The bottom or lower MOSFET should be selected with the lowest possible $r_{DS(ON)}$ while maintaining the desired circuit size and cost.

Calculate the RMS current in QL as shown by Equation 17:

$$I_{QLRMS} = I_{OUT} \times \sqrt{1-D} \quad \text{(EQ. 17)}$$

Calculate the power dissipated due to $r_{DS(ON)}$ as shown in Equation 18:

$$P_{QL} = r_{DS(ON)}(I_{botrms})^2 \quad \text{(EQ. 18)}$$

NOTE: $r_{DS(ON)}$ given in the manufacturer's datasheet is measured at +25°C.

The actual $r_{DS(ON)}$ in the end-use application will be much higher. Select a candidate MOSFET and calculate the required gate drive current using Equation 19:

$$I_g = f_{SW} \times Q_g \quad \text{(EQ. 19)}$$

MOSFETs with lower $r_{DS(ON)}$ tend to have higher gate charge requirements, which increases the current and resulting power required to turn them on and off.

QH SELECTION

In addition to the $r_{DS(ON)}$ loss and gate charge loss, QH also has switching loss. Select QH with a lower gate charge, keeping in mind that QH's $r_{DS(ON)}$ will be higher as a result. As was done with QL, calculate the RMS current using Equations 20 and 21:

$$I_{QHRMS} = I_{OUT} \times \sqrt{D} \quad \text{(EQ. 20)}$$

$$P_{QH} = r_{DS(ON)}(I_{QHRMS})^2 \quad \text{(EQ. 21)}$$

Next, calculate the switching time using Equation 22:

$$t_{SW} = \frac{Q_g}{I_{DR}} \quad \text{(EQ. 22)}$$

where Q_g is the gate charge of the selected QH and I_{DR} is the peak gate drive current available from the gate drive IC.

To calculate the switching time, use the ZL1505s minimum guaranteed drive current of 3A for a conservative design. Using the calculated switching time, calculate the switching power loss in QH using Equation 23:

$$P_{swtop} = V_{INM} \times t_{sw} \times I_{OUT} \times f_{sw} \quad \text{(EQ. 23)}$$

The total power dissipated by QH is given by Equation 24:

$$P_{QHtot} = P_{QH} + P_{swtop} \quad \text{(EQ. 24)}$$

MOSFET THERMAL CHECK

Once the power dissipations for QH and QL have been calculated, the MOSFET's junction temperature can be estimated. Using the junction to case thermal resistance (R_{th}) given in the MOSFET manufacturer's datasheet and the expected maximum printed circuit board temperature, calculate the junction temperature using Equation 25:

$$T_{j\max} = T_{pcb} + (P_Q \times R_{th}) \quad \text{(EQ. 25)}$$

To calculate power losses and junction temperature rise in DrMOS devices, consult the datasheet and application notes for the DrMOS device selected.

EFFICIENCY OPTIMIZED DRIVER DEADTIME CONTROL

The ZL8801 utilizes a closed loop algorithm to optimize the deadtime applied between the gate drive signals for the top and bottom FETs. In a synchronous buck converter, the MOSFET drive circuitry must be designed such that the top and bottom MOSFETs are never in the conducting state at the same time. Potentially damaging currents flow in the circuit if both top and bottom MOSFETs are simultaneously on for periods of time exceeding a few nanoseconds. Conversely, long periods of time in which both MOSFETs are off, reduce overall circuit efficiency by allowing current to flow in their parasitic body diodes.

It is therefore advantageous to minimize this deadtime to provide optimum circuit efficiency. In the first order model of a buck converter, the duty cycle is determined by Equation 26:

$$D \approx \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 26)}$$

However, nonidealities exist that cause the real duty cycle to extend beyond the ideal. Deadtime is one of those nonidealities that can be manipulated to improve efficiency. The ZL8801 has an internal algorithm that constantly adjusts deadtime nonoverlap to minimize duty cycle, thus maximizing efficiency. This circuit will null out deadtime differences due to component variation, temperature and loading effects. This algorithm is independent of application circuit parameters such as MOSFET type, gate driver delays, rise and fall times and circuit layout. In addition, it does not require drive or MOSFET voltage or current waveform measurements. Adaptive deadtime is enabled using the DEADTIME_CONFIG PMBus™ command. Adaptive deadtime is only effective when a discrete driver (such as the ZL1505) and MOSFETs are used. When DrMOS devices are selected using USER_CONFIG, adaptive deadtime is automatically disabled. Deadtime minimum and maximum limits can be set using the DEADTIME PMBus™ command.

Monitoring via SMBus

A system controller can monitor a wide variety of different ZL8801 parameters through the SMBus interface. The device can monitor for fault conditions by monitoring the SALRT pin, which will be asserted when any number of preconfigured fault conditions occur.

The device can also be monitored continuously for any number of power conversion parameters including but not limited to the following:

- Input voltage
- Output voltage
- Input current
- Output current
- Internal junction temperature
- Temperature of an external device
- Switching frequency
- Duty cycle
- Fault status information

The PMBus™ Host should respond to SALRT as follows:

1. ZL device pulls SALRT Low.
2. PMBus™ Host detects that SALRT is now low, performs transmission with Alert Response Address to find which ZL device is pulling SALRT low.
3. PMBus™ Host talks to the ZL device that has pulled SALRT low. The actions that the host performs are up to the System Designer.

If multiple devices are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared.

Please refer to the “PMBus™ Command Detail” section, starting on page 30, for details on how to monitor specific parameters via the SMBus interface.

PMBus™ Command Summary

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
01h	OPERATION	Enable/disable, margin settings.	R/W	BIT	00h	Immediate Off, Nominal Margin
02h	ON_OFF_CONFIG	On/off configure settings.	R/W	BIT	17h	ENABLE Pin Control, Active High
03h	CLEAR_FAULTS	Clears faults.	Write	N/A	N/A	N/A
11h	STORE_DEFAULT_ALL	Stores values to default store.	Write	N/A	N/A	N/A
12h	RESTORE_DEFAULT_ALL	Restores values from default store.	Write	N/A	N/A	N/A
15h	STORE_USER_ALL	Stores values to user store.	Write	N/A	N/A	N/A
16h	RESTORE_USER_ALL	Restores values from user store.	Write	N/A	N/A	N/A
20h	VOUT_MODE	Reports VOUT_COMMAND Mode value.	Read	BIT	13h	13h, Fixed Value
21h	VOUT_COMMAND	Sets nominal V_{OUT} setpoint.	R/W	L16u		Pin-strap Setting
23h	VOUT_CAL_OFFSET	Applies offset voltage to V_{OUT} setpoint.	R/W	L16u	0000h	0V
24h	VOUT_MAX	Sets maximum V_{OUT} setpoint.	R/W	L16u		1.10 X VOUT_COMMAND Pin-strap Setting
25h	VOUT_MARGIN_HIGH	Sets V_{OUT} set point during margin high.	R/W	L16u		1.05 x VOUT_COMMAND Pin-strap Setting
26h	VOUT_MARGIN_LOW	Sets V_{OUT} setpoint during margin low.	R/W	L16u		0.95 x VOUT_COMMAND Pin-strap Setting
27h	VOUT_TRANSITION_RATE	Sets V_{OUT} transition rate during margin commands.	R/W	L11	BA00h	1V/ms
28h	VOUT_DROOP	Sets V/I slope for total rail output current (all phases combined).	R/W	L11	0000h	0mV/A
33h	FREQUENCY_SWITCH	Sets switching frequency.	R/W	L11		Pin-strap Setting
37h	INTERLEAVE	Configures phase offset during group operation.	R/W	BIT		Set by Pin-Strapped PMBus™ Address
40h	VOUT_OV_FAULT_LIMIT	Sets the V_{OUT} overvoltage fault threshold.	R/W	L16u		1.15 x VOUT_COMMAND Pin-strap Setting
41h	VOUT_OV_FAULT_RESPONSE	Sets the V_{OUT} overvoltage fault response.	R/W	BIT	80h	Disable, No Retry
44h	VOUT_UV_FAULT_LIMIT	Sets the V_{OUT} undervoltage fault threshold.	R/W	L16u		0.85 x VOUT_COMMAND Pin-strap Setting
45h	VOUT_UV_FAULT_RESPONSE	Sets the V_{OUT} undervoltage fault response.	R/W	BIT	80h	Disable, No Retry
46h	IOUT_OC_FAULT_LIMIT	Sets the I_{OUT} peak overcurrent fault threshold for each phase.	R/W	L11	DBC0h	30A

PMBus™ Command Summary (Continued)

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
4Bh	IOUT_UC_FAULT_LIMIT	Sets the I_{OUT} valley undercurrent fault threshold for each phase.	R/W	L11	D440h	-15A
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault limit.	R/W	L11	EBE8h	+125˚C
50h	OT_FAULT_RESPONSE	Sets the over-temperature fault response.	R/W	BIT	80h	Disable, No Retry
51h	OT_WARN_LIMIT	Sets the over-temperature warning limit.	R/W	L11	EB70h	+110°C
52h	UT_WARN_LIMIT	Sets the under-temperature warning limit.	R/W	L11	DC40h	-30°C
53h	UT_FAULT_LIMIT	Sets the under-temperature fault limit.	R/W	L11	E530h	-45°C
54h	UT_FAULT_RESPONSE	Sets the under-temperature fault response.	R/W	BIT	80h	Disable, No Retry
55h	VIN_OV_FAULT_LIMIT	Sets the V_{IN} overvoltage fault threshold.	R/W	L11	D380h	14V
56h	VIN_OV_FAULT_RESPONSE	Sets the V_{IN} overvoltage fault response.	R/W	BIT	80h	Disable, No Retry
57h	VIN_OV_WARN_LIMIT	Sets the V_{IN} overvoltage warning threshold.	R/W	L11	D360h	13.5V
58h	VIN_UV_WARN_LIMIT	Sets the V_{IN} undervoltage warning threshold.	R/W	L11	N/A	1.1 x VIN_UV_FAULT_LIMIT Pin-strap Setting
59h	VIN_UV_FAULT_LIMIT	Sets the V_{IN} undervoltage fault threshold.	R/W	L11	N/A	Pin-strap Setting
5Ah	VIN_UV_FAULT_RESPONSE	Sets the V_{IN} undervoltage fault response.	R/W	BIT	80h	Disable, No Retry
5Eh	POWER_GOOD_ON	Sets the voltage threshold for Power-good indication.	R/W	L16u	N/A	0.9 x VOUT_COMMAND Pin-strap Setting
60h	TON_DELAY	Sets the delay time from enable to V_{OUT} rise.	R/W	L11	CA80h	5ms
61h	TON_RISE	Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.	R/W	L11	CA80h	5ms
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of V_{OUT} fall.	R/W	L11	CA80h	5ms
65h	TOFF_FALL	Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY.	R/W	L11	CA80h	5ms
78h	STATUS_BYTE	First byte of STATUS_WORD.	Read	BIT	0000h	No Faults
79h	STATUS_WORD	Summary of critical faults.	Read	BIT	0000h	No Faults
7Ah	STATUS_VOUT	Reports V_{OUT} warnings/faults.	Read	BIT	00h	No Faults
7Bh	STATUS_IOUT	Reports I_{OUT} warnings/faults.	Read	BIT	00h	No Faults
7Ch	STATUS_INPUT	Reports input warnings/faults.	Read	BIT	00h	No Faults
7Dh	STATUS_TEMPERATURE	Reports temperature warnings/faults.	Read	BIT	00h	No Faults
7Eh	STATUS_CML	Reports Communication, memory, logic errors.	Read	BIT	00h	No Errors
80h	STATUS_MFR_SPECIFIC	Reports voltage monitoring/clock synchronization faults.	Read	BIT	00h	No Faults
88h	READ_VIN	Reports input voltage measurement.	Read	L11	N/A	N/A
89h	READ_IIN	Reports input current measurement.	Read	L11	N/A	N/A
8Bh	READ_VOUT	Reports output voltage measurement.	Read	L16u	N/A	N/A
8Ch	READ_IOUT	Reports output total current measurement.	Read	L11	N/A	N/A
8Dh	READ_TEMPERATURE_1	Reports internal temperature measurement.	Read	L11	N/A	N/A

PMBus™ Command Summary (Continued)

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
8Eh	READ_TEMPERATURE_2	Reports external temperature 0 measurement.	Read	L11	N/A	N/A
8Fh	READ_TEMPERATURE_3	Reports external temperature 1 measurement.	Read	L11	N/A	N/A
94h	READ_DUTY_CYCLE	Reports actual duty cycle.	Read	L11	N/A	N/A
95h	READ_FREQUENCY	Reports actual switching frequency.	Read	L11	N/A	N/A
98h	PMBUS_REVISION	Returns the revision of the PMBus Specification to which the device is compliant.	Read	BIT	11h	Part 1 Revision 1.2, Part 2 Revision 1.2
99h	MFR_ID	Sets a user defined identification.	R/W	ASC	N/A	<null>
9Ah	MFR_MODEL	Sets a user defined model.	R/W	ASC	N/A	<null>
9Bh	MFR_REVISION	Sets a user defined revision.	R/W	ASC	N/A	<null>
9Ch	MFR_LOCATION	Sets a user defined location identifier.	R/W	ASC	N/A	<null>
9Dh	MFR_DATE	Sets a user defined date.	R/W	ASC	N/A	<null
9Eh	MFR_SERIAL	Sets a user defined serialized identifier.	R/W	ASC	N/A	<null>
A1h	READ_IOUT0	Reports phase 0 output current.	Read	L11	N/A	N/A
A2h	READ_IOUT1	Reports phase 1 output current.	Read	L11	N/A	N/A
A8h	LEGACY_FAULT_GROUP	Configures fault group compatibility with older Intersil digital power devices.	R/W	BIT	N/A	<null>
ADh	IC_DEVICE_ID	Reports device identification information.	Block Read	CUS	49A02300h	Intersil, ZL8801
AEh	IC_DEVICE_REV	Reports device revision information.	Block Read	CUS	01000000h	Initial Release
B0h	USER_DATA_00	Sets a user defined data.	R/W	ASC	N/A	<null>
BFh	DEADTIME_MAX	Sets the max deadtime value for the adaptive deadtime.	R/W	BIT	3838h	56ns/56ns
CAh	IOUT0_CAL_GAIN	Sets impedance of phase 0 current sense circuit.	R/W	L11	AA66h	0.3mΩ
CBh	IOUT1_CAL_GAIN	Sets impedance of phase 1 current sense circuit.	R/W	L11	AA66h	0.3mΩ
CCh	IOUT0_CAL_OFFSET	Sets an offset to IOUT0 sense circuit.	R/W	L11	0000h	0A
CDh	IOUT1_CAL_OFFSET	Sets an offset to IOUT1 sense circuit.	R/W	L11	0000h	0A
CEh	MIN_VOUT_REG	Sets a minimum start-up voltage.	R/W	L11	F258h	150mV
D0h	ISENSE_CONFIG	Configures current sensing circuitry.	R/W	BIT	4204h	Downslope, 5 Fault Count, 256ns Blanking, Low Range
D1h	USER_CONFIG	Configures several user-level features.	R/W	BIT	0402h	Enable XTEMP0,1, PG Open Drain, DrMOS Enabled
D2h	IIN_CAL_GAIN	Sets the resistance of the input current sensing resistor	R/W	L11	C200h	2mΩ
D3h	DDC_CONFIG	Configures the DDC addressing and current sharing.	R/W	BIT	N/A	Set By Pin-strapped PMBus™ Address
D4h	POWER_GOOD_DELAY	Sets the delay between PG threshold and PG assertion.	R/W	L11	CA00h	4ms
D5h	MULTI_PHASE_RAMP_GAIN	Adjusts the ramp-up and ramp-down rate by setting the feedback gain.	R/W	CUS	03h	Gain of 3
D6h	INDUCTOR	Sets the inductance of both phases.	R/W	L11	B23Dh	0.56µH
D7h	VOUT_MARGIN_RATIO	% MARGIN_HIGH, LOW above/below VOUT_COMMAND.	R/W	L11	CA80h	5%
D8h	OVUV_CONFIG	Configures output voltage OV/UV fault detection.	R/W	BIT	00000000h	Low-side FET Off On Fault, 1 Violation Triggers Fault.

PMBus™ Command Summary (Continued)

CODE	COMMAND NAME	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE	DEFAULT SETTING
D9h	XTEMP_SCALE	Calibrates external temperature sensor.	R/W	L11	BA00h	1/°C
DAh	XTEMP_OFFSET	Offset calibration for external temperature sensor.	R/W	L11	0000h	No Offset
DCh	TEMPCO_CONFIG	Sets tempco settings.	R/W	BIT	27h	3900ppm/°C
DDh	DEADTIME	Sets default deadtime settings.	R/W	CUS	1010h	16ns/16ns
DEh	DEADTIME_CONFIG	Configures the adaptive deadtime optimization mode.	R/W	BIT	8888h	Adaptive Deadtime Enabled, 8ns/8ns
DFh	ASCR_CONFIG	Configures the ASCR settings.	R/W	BIT	015A0190h	ASCR Enabled, 400 Gain, 90 Residual
E0h	SEQUENCE	DDC rail sequencing configuration.	R/W	BIT	00h	Prequel and Sequel Disabled
E1h	TRACK_CONFIG	Configures voltage tracking modes.	R/W	BIT	00h	Tracking Disabled
E2h	DDC_GROUP	Configures group ID, fault spreading, OPERATION and V_{OUT}.	R/W	BIT	000000h	Ignore Broadcast, Sequenced Shutdown, Fault Spreading
E4h	DEVICE_ID	Returns the device identifier string.	Block Read	ASC	N/A	<Part Number/Die Revision/Firmware Revision>
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the I_{OUT} overcurrent fault response.	R/W	BIT	80h	Disable, No Retry
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the I_{OUT} undercurrent fault response.	R/W	BIT	80h	Disable, No Retry
E7h	IOUT_AVG_OC_FAULT_LIMIT	Sets the I_{OUT} average overcurrent fault threshold for each phase.	R/W	L11	DA80h	20A
E8h	IOUT_AVG_UC_FAULT_LIMIT	Sets the I_{OUT} average undercurrent fault threshold for each phase.	R/W	L11	D580h	-10A
E9h	MFR_USER_CONFIG	Sets options pertaining to advanced features.	R/W	BIT	0000h	Numerous Device Settings
EAh	SNAPSHOT	32 byte read-back of parametric and status values.	Block Read	BIT	N/A	<null>
EBh	BLANK_PARAMS	Indicates recently saved parameter values.	Block Read	BIT	FF...FFh	<null>
F3h	SNAPSHOT_CONTROL	Snapshot feature control command.	R/W	BIT	00h	N/A
F4h	RESTORE_FACTORY	Restores device to the hard-coded default values.	Write	N/A	N/A	N/A
F5h	MFR_VMON_OV_FAULT_LIMIT	Sets the VMON overvoltage fault threshold.	R/W	L11	D300h	12V
F6h	MFR_VMON_UV_FAULT_LIMIT	Sets the VMON undervoltage fault threshold.	R/W	L11	CA00h	4.0V
F7h	MFR_READ_VMON	Reads the VMON voltage.	Read	L11	N/A	N/A
F8h	MFR_VMON_OV_FAULT_RESPONSE	Configures the VMON overvoltage fault response.	R/W	BIT	80h	Disable, No Retry
F9h	MFR_VMON_UV_FAULT_RESPONSE	Configures the VMON undervoltage fault response.	R/W	BIT	80h	Disable, No Retry
FAh	SECURITY_LEVEL	Reports the security level.	Read	Hex	01h	Public Security Level
FBh	PRIVATE_PASSWORD	Sets the private password string.	R/W	ASC	00...00h	<null>
FCh	PUBLIC_PASSWORD	Sets the public password string.	R/W	ASC	00...00h	<null>
FDh	UNPROTECT	Identifies which commands are protected.	R/W	Custom	FF...FFh	N/A

PMBus™ User Guidelines

The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring the ZL8801 for their application. When configuring the ZL8801 in a circuit, the ZL8801 should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW and ASCCR_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been reenabled, hence the recommendation that commands that change device settings are written while the device is disabled.

SUMMARY:

All commands can be read at any time.

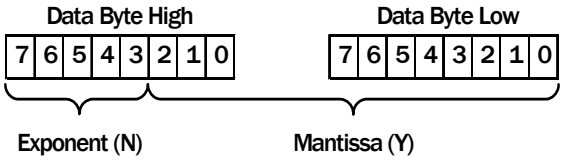
Always disable the ZL8801 when writing commands that change device settings. Exceptions to this rule are commands intended to be written while the device is enabled, for example, VOUT_MARGIN_HIGH.

To be sure a device setting change has taken effect, write the STORE_USER_ALL command, then cycle input power and reenable the device.

PMBus™ Data Formats

Linear-11 (L11)

L11 data format uses 5-bit two's compliment exponent (N) and 11-bit two's compliment mantissa (Y) to represent real world decimal value (X).



Relation between real world decimal value (X), N and Y is: $X = Y \times 2^{N}$

Linear-16 Unsigned (L16u)

L16u data format uses a fixed exponent (hardcode to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). Relation between real world decimal value (X), N and Y is: $X = Y \times 2^{-13}$

Linear-16 Signed (L16s)

L16s data format uses a fixed exponent (hardcode to N = -13h) and a 16-bit two's compliment mantissa (Y) to represent real world decimal value (X).
Relation between real world decimal value (X), N and Y is: $X = Y \times 2^{-13}$

Bit Field (BIT)

Breakdown of Bit Field is provided in "PMBus™ Command Detail" section, starting on page 30.

Custom (CUS)

Breakdown of Custom data format is provided in "PMBus™ Command Detail" section, starting on page 30. A combination of Bit Field and integer are common types of Custom data format.

ASCII (ASC)

A variable length string of text characters uses ASCII data format.

PMBus™ Command Detail

OPERATION (01h)

Definition: Sets Enable, Disable and VOUT Margin settings. Data values of OPERATION that force margin high or low only take effect when the MGN pin is left open (i.e., in the NOMINAL margin state). This command can also be monitored to read the operating state of the device on bits 7:6. Writing Immediate off will turn off the output and ignore TOFF_DELAY and TOFF_FALL settings. This command is not stored like other PMBus commands. The value read reflects the current state of the device. When this command is written, the command takes effect. If a STORE _USER_ALL written and the device is reenabled, the OPERATION settings may not be the same settings that were written before the device was reenabled.

Data Length in Bytes: 1

Data Format: BIT Field

Type: R/W

Protectable: Yes

Default Value: 00h (immediate off)

Units: N/A

COMMAND	OPERATION (01h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS 7:6	BITS 5:4	BITS 3:0 (NOT USED)	UNIT ON OR OFF	MARGIN STATE
00	00	0000	Immediate off (No sequencing)	N/A
01	00	0000	Soft-off (With sequencing)	N/A
10	00	0000	On	Nominal
10	01	0100	On	Margin Low
10	10	0100	On	Margin High

NOTE: Bit combinations not listed above may cause command errors.

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN). When Bit 0 is set to 1 (Turn-off the output immediately) TOFF_DELAY and TOFF_FALL settings are ignored.
Data Length in Bytes: 1
Data Format: BIT Field
Type: R/W
Protectable: Yes
Default Value: 17h (ENABLE pin control, active high, turn off output immediately – no ramp down)
Units: N/A

COMMAND	ON_OFF_CONFIG (02h)							
Format	BIT FIELD							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	0	0	0	1	0	1	1	1

BIT NUMBER	PURPOSE	BIT VALUE	MEANING
7:5	Not Used	000	Not used
4:2	Sets the default to either operate any time power is present or for the on/off to be controlled by ENABLE pin or OPERATION command	000	Not used
		101	Device starts from ENABLE pin only.
		110	Device starts from OPERATION command only.
1	Not Used	0	Not used
0	ENABLE pin action when commanding the unit to turn off	0	Use the configured ramp down settings.
		1	Turn off the output immediately.

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit will reassert immediately. This command will not restart a device if it has shut down, it will only clear the faults.
Data Length in Bytes: 0 Byte
Data Format: N/A
Type: Write Only
Protectable: Yes
Default Value: N/A
Units: N/A

STORE_DEFAULT_ALL (11h)

Definition: Stores all current PMBus™ values from the operating memory into the nonvolatile (NVRAM) DEFAULT store memory. To clear the DEFAULT store, perform a RESTORE_FACTORY then STORE_DEFAULT_ALL. To add to the DEFAULT store, perform a RESTORE_DEFAULT_ALL, write commands to be added, then STORE_DEFAULT_ALL. This command should not be used during device operation, the device will be unresponsive for 20ms while storing values.
Data Length in Bytes: 0
Data Format: N/A
Type: Write Only
Default Value: N/A
Units: N/A

RESTORE_DEFAULT_ALL (12h)

Definition: Restores PMBus™ settings from the nonvolatile (NVRAM) DEFAULT Store memory into the operating memory. These settings are loaded during at power-up if not superseded by settings in USER store. Security level is changed to level 1 following this command. This command should not be used during device operation, the device will be unresponsive for 20ms while restoring values.
Data Length in Bytes: 0
Data Format: N/A
Type: Write Only
Default Value: N/A
Units: N/A

STORE_USER_ALL (15h)

Definition: Stores all PMBus™ settings from the operating memory to the nonvolatile (NVRAM) USER store memory. To clear the USER store, perform a RESTORE_FACTORY then STORE_USER_ALL. To add to the USER store, perform a RESTORE_USER_ALL, write commands to be added, then STORE_USER_ALL. This command should not be used during device operation, the device will be unresponsive for 20ms while storing values.
Data Length in Bytes: 0
Data Format: N/A
Type: Write Only
Default Value: N/A
Units: N/A

RESTORE_USER_ALL (16h)

Definition: Restores all PMBus™ settings from the USER store memory to the operating memory. Security level is changed to Level 1 following this command. This command should not be used during device operation, the device will be unresponsive for 20ms while restoring values.
Data Length in Bytes: 0
Data Format: N/A
Type: Write Only
Default Value: N/A
Units: N/A

VOUT_MODE (20h)

Definition: Reports the V_{OUT} mode and provides the exponent used in calculating several V_{OUT} settings.
Data Length in Bytes: 1
Data Format: BIT Field
Type: Read ONLY
Protectable: N/A
Default Value: 13h (Linear Mode, Exponent is -13d)
Units: N/A

COMMAND	VOUT_MODE (20h)							
Format	BIT FIELD							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	See Following Table							
Default Value	0	0	0	1	0	0	1	1

BIT	FIELD NAME	VALUE	DESCRIPTION
7:0	Mode	13h	Five bit two's complement exponent for the mantissa delivered as the data bytes for an output voltage related command.

VOUT_COMMAND (21h)

Definition: This command sets or reports the target output voltage. The integer value is multiplied by 2 raised to the power of -13h. This command cannot be set to be higher than VOUT_MAX.
Data Length in Bytes: 2
Data Format: Linear -16 Unsigned
Type: R/W
Protectable: Yes
Default Value: Pin-strap Setting
Units: Volts
Equation: VOUT = VOUT_COMMAND × 2^{-13}
Range: 0 to VOUT_MAX
Example: VOUT_COMMAND = 699Ah = 27,034
Target voltage equals 27034 × 2^{-13} = 3.3V

COMMAND	VOUT_COMMAND (21h)															
Format	Linear, unsigned binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default Value	Pin-strap setting															

VOUT_CAL_OFFSET (23h)

Definition: The VOUT_CAL_OFFSET command is used to apply a fixed offset voltage to the output voltage command value. This command is typically used by the user to calibrate a device in the application circuit. The two bytes are formatted as a two's complement binary mantissa, used in conjunction with the exponent of -13h.
Data Length in Bytes: 2
Data Format: Linear -16 Signed
Type: R/W
Protectable: Yes
Default Value: 0000h
Units: V
Equation: V_{OUT} cal offset = VOUT_CAL_OFFSET × 2^{-13}
Range: ±3.99V

COMMAND	VOUT_CAL_OFFSET (23h)															
Format	Linear-16 Signed															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

VOUT_MAX (24h)

Definition: The VOUT_ MAX command sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. If a VOUT_COMMAND is sent with a value higher than VOUT_MAX, the device will set the output voltage to VOUT_MAX.
Data Length in Bytes: 2
Data Format: Linear -16 Unsigned
Type: R/W
Protectable: Yes
Default Value: 1.10 × VOUT_COMMAND pin-strap setting
Units: V
Equation: VOUT max = VOUT_MAX × 2^{-13}
Range: 0V to 5.5V

COMMAND	VOUT_MAX (24h)															
Format	Linear, unsigned binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default Value	1.10 x VOUT_COMMAND Pin-strap Setting															

VOUT_MARGIN_HIGH (25h)

Definition: Sets the value of the V_{OUT} during a margin high. This VOUT_MARGIN_HIGH command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin High”.
Data Length in Bytes: 2
Data Format: Linear -16 Unsigned.
Type: R/W Word
Protectable: Yes
Default Value: 1.05 x VOUT_COMMAND pin-strap setting
Units: V
Equation: VOUT margin high = VOUT_MARGIN_HIGH x 2^{-13}
Range: 0V to VOUT_MAX

COMMAND	VOUT_MARGIN_HIGH (25h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default Value	1.05 x VOUT_COMMAND pin-strap setting															

VOUT_MARGIN_LOW (26h)

Definition: Sets the value of the V_{OUT} during a margin low. This VOUT_MARGIN_LOW command loads the unit with the voltage to which the output is to be changed when the OPERATION command is set to “Margin Low”.
Data Length in Bytes: 2
Data Format: Linear -16 Unsigned
Type: R/W
Protectable: Yes
Default Value: 0.95 x VOUT_COMMAND pin-strap setting
Units: V
Equation: VOUT margin low = VOUT_MARGIN_LOW
Range: 0V to VOUT_MAX

COMMAND	VOUT_MARGIN_LOW (26h)															
Format	Linear, two’s complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default Value	0.95 x VOUT_COMMAND pin-strap setting															

VOUT_TRANSITION_RATE (27h)

Definition: This command sets the rate at which the output should change voltage when the device receives an OPERATION command (Margin High, Margin Low) that causes the output voltage to change. The maximum possible positive value of the two data bytes indicates that the device should make the transition as quickly as possible. This commanded rate does not apply when the device is commanded to turn on or to turn off.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: BA00h (1.0V/ms)

Units: V/ms

Equation: VOUT_TRANSITION_RATE = Y x 2N

Range: 0.1 to 4V/ms

COMMAND	VOUT_TRANSITION_RATE (27h)															
Format	Linear Data Format															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

VOUT_DROOP (28h)

Definition: The VOUT_DROOP sets the effective load line (V/I slope) for the rail in which the device is used. It is the rate, in mV/A at which the output voltage decreases with increasing output current for use with Adaptive Voltage Positioning requirements and passive current sharing schemes. For devices that are set to sink output current (negative output current), the output voltage continues to increase as the output current is negative. VOUT_DROOP is not needed with a single (2-phase) ZL8801. VOUT_DROOP is needed when multiple ZL8801s are operated in current sharing mode, i.e. 4-, 6- and 8-phase configurations. In this case, VOUT_DROOP is calculated based on the combined output current of all 4, 6 or 8 phases as applicable.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: 0000h (0mV/A)

Units: mV/A

Equation: VOUT_DROOP = Y x 2N

Range: 0 to 40mV/A

COMMAND	VOUT_DROOP (28h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. Initial default value is defined by a pin-strap and this value can be overridden by writing this command. If an external SYNC is utilized, this value should be set as close as possible to the external clock value. The output must be disabled when writing this command. Available frequencies are defined by equation f_{SW} = 16MHz/n where 12 ≤ n ≤ 80.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: Pin-strap Setting
Units: kHz
Equation: FREQUENCY_SWITCH = Y x 2N
Range: 200kHz to 1.33MHz

COMMAND	FREQUENCY_SWITCH (33h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	Pin-strap setting															

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. A desired phase position is specified. Interleave is used for setting the phase offset between individual devices, current sharing groups and/or combinations of devices and current sharing groups. For devices within a single current sharing group the phase offset is set automatically. The ZL8801 uses dual edge modulation. Phase offset should measured with respect to the center of PWM4 pulses.
Data Length in Bytes: 2
Data Format: Bit Field
Type: R/W
Protectable: Yes
Default Value: Set by pin-strapped PMBus address
Units: N/A

COMMAND	INTERLEAVE (37h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	Four LSB's of PMBus Address			

BITS	PURPOSE	VALUE	DESCRIPTION
15:4	Not Used	0	Not used
3:0	Position in Group	0 to 15	Sets position of the device's rail within the group. A value of 0 is interpreted as 16. Position 1 will have a 22.5° offset.

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.
Data Length in Bytes: 2
Data Format: Linear-16 Unsigned
Type: R/W
Protectable: Yes
Default Value: 1.15 x VOUT_COMMAND pin-strap setting
Units: V
Equation: VOUT OV fault limit = VOUT_OV_FAULT_LIMIT x 2^{-13}
Range: 0V to 7.99V

COMMAND	VOUT_OV_FAULT_LIMIT (40h)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default Value	1.15 x VOUT_COMMAND pin-strap setting															

VOUT_OV_FAULT_RESPONSE (41h)

Definition: Configures the V_{OUT} overvoltage fault response.
Data Length in Bytes: 1
Data Format: Bit Field
Type: R/W
Protectable: Yes
Default Value: 80h (Shut down immediately, no retries)
Units: Retry time unit = 70ms

COMMAND	VOUT_OV_FAULT_RESPONSE (41h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not Used
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not Used
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not Used
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	111	Not used. Retry time is fixed at 70ms.

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp, before power-good is asserted or when the device is disabled.
Data Length in Bytes: 2
Data Format: Linear-16 Unsigned
Type: R/W
Protectable: Yes
Default Value: 0.85 x VOUT_COMMAND pin-strap setting
Units: V
Equation: VOUT UV fault limit = VOUT_UV_FAULT_LIMIT x 2^{-13}
Range: 0V to 7.99V

COMMAND	VOUT_UV_FAULT_LIMIT (44h)															
Format	Linear-16 unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default Value	0.85 x VOUT_COMMAND															

VOUT_UV_FAULT_RESPONSE (45h)

Definition: Configures the V_{OUT} undervoltage fault response. Note that VOUT UV faults can only occur after power-good (PG) has been asserted. Under some circumstances this will cause the output to stay fixed below the power-good threshold indefinitely.
Data Length in Bytes: 1
Data Format: BIT Field
Type: R/W
Protectable: Yes
Default Value: 80h (Shut down immediately, no retry)
Units: Retry time = 70ms

COMMAND	VOUT_UV_FAULT_RESPONSE (45h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not Used
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not Used
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not Used
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	111	Not used. Retry time is fixed at 70ms.

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the I_{OUT} peak overcurrent fault threshold for each inductor (Phase 0 and Phase 1). Either phase can trigger an overcurrent fault. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. A fault occurs after this limit is exceeded for the number of consecutive switching periods as defined in ISENSE_CONFIG. This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_AVG_OC_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: DBC0h (30A)

Units: A

Equation: IOUT_OC_FAULT_LIMIT = Y x 2^N

Range: -100 to 100A

COMMAND	IOUT_OC_FAULT_LIMIT (46h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	1	0	1	1	1	1	0	0	0	0	0	0

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the I_{OUT} valley undercurrent fault threshold for each inductor (Phase 0 and Phase 1). Either phase can trigger an undercurrent fault. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. A fault occurs after this limit is exceeded for the number of consecutive switching periods as defined in ISENSE_CONFIG. This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_AVG_UC_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D440h (-15A)

Units: A

Equation: IOUT_UC_FAULT_LIMIT = Y x 2^N

Range: -100 to 100A

COMMAND	IOUT_UC_FAULT_LIMIT (4Bh)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	0	1	0	0	0	1	0	0	0	0	0	0

OT_FAULT_LIMIT (4Fh)

Definition: The OT_FAULT_LIMIT command sets the temperature at which the device should indicate an over-temperature fault. When using XTEMP (0, 1), either temperature sensor can trigger a fault. In response to the OT_FAULT_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, Sets the OT_WARNING bit in STATUS_TEMPERATURE and the FAULT_INT, FAULT_XTEMP0 or FAULT_XTEMP1 as applicable and notifies the host.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: EBE8h (+125˚C)
Units: Celsius
Equation: OT_FAULT_LIMIT = Y x 2^N
Range: 0°C to +175°C

COMMAND	OT_FAULT_LIMIT (4Fh)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	1	1	1	0	1	0	0	0

OT_FAULT_RESPONSE (50h)

Definition: The OT_FAULT_RESPONSE command instructs the device on what action to take in response to an over-temperature fault. The setting "10" in Bits 7:6 should not be used with setting "111" in Bits 5:3 since this could result in a thermal runaway condition.
Data Length in Bytes: 1
Data Format: Bit Field
Type: R/W
Protectable: Yes
Default Value: 80h (Shut down immediately, no retry)
Units: Retry time = 210ms

COMMAND	OT_FAULT_RESPONSE (50h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: The Device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not Used
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not Used
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not Used
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	111	Not used. Retry delay is 210ms.

OT_WARN_LIMIT (51h)

Definition: The OT_WARN_LIMIT command sets the temperature at which the device should indicate an over-temperature warning alarm. When using XTEMP (0,1), either temperature sensor can trigger a warning. In response to the OT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, Sets the OT_WARNING bit in STATUS_TEMPERATURE and the FAULT_INT, FAULT_XTEMP0 or FAULT_XTEMP1 as applicable and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: EB70h (+110°C)

Units: Celsius

Equation: OT_WARN_LIMIT = Y x 2^N

Range: 0°C to +175°C

COMMAND	OT_WARN_LIMIT (51h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	1	0	1	1	0	1	1	1	0	0	0	0

UT_WARN_LIMIT (52h)

Definition: The UT_WARN_LIMIT command set the temperature at which the device should indicate an under-temperature warning alarm. When using XTEMP (0,1), either temperature sensor can trigger a warning. In response to the UT_WARN_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, Sets the UT_WARNING bit in STATUS_TEMPERATURE and the FAULT_INT, FAULT_XTEMP0 or FAULT_XTEMP1 as applicable and notifies the host.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: DC40h (-30°C)

Units: Celsius

Equation: UT_WARN_LIMIT = Y x 2^N

Range: -55°C to +25°C

COMMAND	UT_WARN_LIMIT (52h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	1	1	0	0	0	1	0	0	0	0	0	0

UT_FAULT_LIMIT (53h)

Definition: The UT_FAULT_LIMIT command sets the temperature, in degrees Celsius, of the unit at which it should indicate an under-temperature fault. When using XTEMP (0,1), either temperature sensor can trigger a fault. In response to the UT_FAULT_LIMIT being exceeded, the device: Sets the TEMPERATURE bit in STATUS_WORD, Sets the UT_FAULT bit in STATUS_TEMPERATURE and the FAULT_INT, FAULT_XTEMP0 or FAULT_XTEMP1 as applicable and notifies the host.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: E530h (-45°C)
Units: Celsius
Equation: UT_FAULT_LIMIT = Y x 2^N
Range: -55°C to +25°C

COMMAND	UT_FAULT_LIMIT (53h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	0	0	1	0	1	0	0	1	1	0	0	0	0

UT_FAULT_RESPONSE (54h)

Definition: Configures the under-temperature fault response as defined by the following table. The delay time is the time between restart attempts.
Data Length in Bytes: 1
Data Format: Bit Field
Type: R/W
Protectable: Yes
Default Value: 80h (Shut down immediately, no retry)
Units: Retry time unit = 210ms

COMMAND	UT_FAULT_RESPONSE (54h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: The Device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not Used
		10	Disable and retry according to the setting in bits [5:3].
		11	Not Used
5:3	Retry Setting	000	No retry. The output remains disabled until the device is restarted.
		001-110	Not Used
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	111	Not used. Retry time is fixed at 210ms.

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: D380h (14V)
Units: V
Equation: VIN_OV_FAULT_LIMIT = Y x 2^N
Range: 0 to 19V

COMMAND	VIN_OV_FAULT_LIMIT (55h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N								Signed Mantissa, Y							
Default Value	1	1	0	1	0	0	1	1	1	0	0	0	0	0	0	0

VIN_OV_FAULT_RESPONSE (56h)

Definition: Configures the V_{IN} overvoltage fault response as defined by the following table. The delay time is the time between restart attempts.
Data Length in Bytes: 1
Data Format: BIT Field.
Type: R/W
Protectable: Yes
Default Value: 80h (Immediate shutdown, no retry)
Units: Retry time unit = 70ms

COMMAND	VIN_OV_FAULT_RESPONSE (56h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: The Device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00-01	Not Used
		10	Disable and retry according to the setting in Bits[5:3].
		11	Not Used
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not Used
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	111	Not used. Retry time is fixed at 70ms.

VIN_OV_WARN_LIMIT (57h)

Definition: Sets the V_{IN} overvoltage warning threshold as defined by the following table. In response to the OV_WARN_LIMIT being exceeded, the device: Sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, Sets the VIN_OV_WARNING bit in STATUS_INPUT and notifies the host.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: D360h (13.5V)
Units: V
Equation: VIN_OV_FAULT_LIMIT = Y x 2^N
Range: 0 to 19V

COMMAND	VIN_OV_WARN_LIMIT (57h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	0	0	1	1	0	1	1	0	0	0	0	0

VIN_UV_WARN_LIMIT (58h)

Definition: Sets the V_{IN} undervoltage warning threshold. In response to the UV_WARN_LIMIT being exceeded, the device: Sets the NONE OF THE ABOVE and INPUT bits in STATUS_WORD, Sets the VIN_UV_WARNING bit in STATUS_INPUT and notifies the host.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: 1.10 x VIN_UV_FAULT_LIMIT pin-strap setting
Units: V
Equation: VIN_UV_WARN_LIMIT = Y x 2^N
Range: 0 to 19V

COMMAND	VIN_UV_WARN_LIMIT (58h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1.10 x VIN_UV_FAULT_LIMIT pin-strap setting															

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: Pin-strap setting
Units: V
Equation: VIN_UV_FAULT_LIMIT = Y x 2^N
Range: 0 to 19V

COMMAND	VIN_UV_FAULT_LIMIT (59h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	Pin-strapped Value															

VIN_UV_FAULT_RESPONSE (5Ah)

Definition: Configures the V_{IN} undervoltage fault response as defined by the following table. The delay time is the time between restart attempts.
Data Length in Bytes: 1
Data Format: Bit Field
Type: R/W
Protectable: Yes
Default Value: 80h (Immediate shut down, no retry)
Units: Retry time unit = 70ms

COMMAND	VIN_UV_FAULT_RESPONSE (5Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: The Device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault Bits are only cleared by the CLEAR_FAULTS command.	00-01	Not Used
		10	Disable and retry according to the setting in Bits [5:3].
		11	Not Used
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not Used
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	111	Not used. Retry time is fixed at 70ms.

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for power-good indication. Power-good asserts when the output voltage exceeds POWER_GOOD_ON and deasserts when the output voltage is less than VOUT_UV_FAULT_LIMIT.
Data Length in Bytes: 2
Data Format: Linear-16 Unsigned
Type: R/W
Protectable: Yes
Default Value: 0.9 x VOUT_COMMAND pin-strap setting
Units: V

COMMAND	POWER_GOOD_ON (5Eh)															
Format	Linear, unsigned binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default Value	0.9 x VOUT_COMMAND pin-strap setting															

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: CA80h, 5ms
Units: ms
Equation: TON_DELAY = Y x 2^N
Range: 0 to 5 seconds

COMMAND	TON_DELAY (60h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} after ENABLE and TON_DELAY for 2-phase (single device) operation. To adjust the rise time in 4-, 6- or 8-phase operation, use MULTI_PHASE_RAMP_GAIN (70h).
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: CA80h, 5ms
Units: ms
Equation: TON_RISE = Y x 2^N
Range: 5 to 100ms. Short rise times may cause excessive input and output currents to flow, thus triggering overcurrent faults at start-up.

COMMAND	TON_RISE (61h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of V_{OUT} fall.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: CA80h, 5ms
Units: ms
Equation: TON_DELAY = Y x 2^N
Range: 0 to 5 seconds

COMMAND	TOFF_DELAY (64h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

TOFF_FALL (65h)

Definition: Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY. This setting is only valid in 2-phase operation. Setting the TOFF_FALL to values less than 5ms will cause the ZL8801 to turn off both the high and low-side FETs (or disable the DrMOS device) immediately after the expiration of the TOFF_DELAY time. In 4-, 6- or 8-phase operation, the ZL8801 will always turn off both the high and low-side FETs (or disable the DrMOS device) immediately after the expiration of the TOFF_DELAY time.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: CA80h, 5ms
Units: ms
Equation: TOFF_FALL = Y x 2^N
Range: 5 to 100ms. Short fall times may cause excessive negative output current to flow, thus triggering undercurrent faults at shutdown.

COMMAND	TOFF_FALL (65h)															
Format	Linear, two's complement binary															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

STATUS_BYTE (78h)

Definition: The STATUS_BYTE command returns the low byte of information from the STATUS_WORD. Based on the information in this byte, the host can get more information by reading the appropriate status registers.

Data Length in Bytes: 1

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Value: 0000h

Units: N/A

COMMAND	STATUS_BYTE (78h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	Not Used	Not used

STATUS_WORD (79h)

Definition: The STATUS_WORD command returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: Bit Field

Type: Read Only

Protectable: No

Default Value: 0000h

Units: N/A

COMMAND	STATUS_WORD (79h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
15	VOUT	An output voltage fault or warning has occurred.
14	IOUT	An output current or output power fault or warning has occurred.
13	INPUT	An input voltage, input current, or input power fault or warning has occurred.
12	MFG_SPECIFIC	A manufacturer specific fault or warning has occurred.
11	POWER_GOOD #	The POWER_GOOD signal, if present, is negated. (Note 15).
10	Not Used	Not used
9	OTHER	A bit in STATUS_VOUT, STATUS_IOUT, STATUS_INPUT, STATUS_TEMPERATURE, STATUS_CML or STATUS_MFR_SPECIFIC is set.
8	Not Used	Not used
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault or warning has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	Not Used	Not used

NOTE:

15. If the POWER_GOOD# bit is set, this indicates that the POWER_GOOD signal, if present, is signaling that the output power is not good.

STATUS_VOUT (7Ah)

Definition: The STATUS_VOUT command returns one data byte with the status of the output voltage.
Data Length in Bytes: 1
Data Format: Bit Field
Type: Read Only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_VOUT (7Ah)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6	VOUT_OV_WARNING	These bits are not used.
5	VOUT_UV_WARNING	Indicates an output undervoltage.
4	VOUT_UV_FAULT	Indicates an output undervoltage fault.
3:0	N/A	These bits are not used.

STATUS_IOUT (7Bh)

Definition: The STATUS_IOUT command returns one data byte with the status of the output current.
Data Length in Bytes: 1
Data Format: BIT Field
Type: Read Only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_IOUT (7Bh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	IOUT_OC_FAULT	An output overcurrent fault has occurred.
6	IOUT_OC_LV_FAULT	An output overcurrent and low voltage fault has occurred.
5	IOUT_OC_WARNING	An output overcurrent warning has occurred.
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.
3	Phase 0 FAULT	A fault occurred on Phase 0.
2	Phase 1 FAULT	A fault occurred on Phase 1.
0:1	Not Used	These bits are not used.

STATUS_INPUT (7Ch)

Definition: The STATUS_INPUT command returns input voltage and input current status information.
Data Length in Bytes: 1
Data Format: BIT Field
Type: Read Only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_INPUT (7Ch)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	VIN_OV_FAULT	An input overvoltage fault has occurred.
6	VIN_OV_WARNING	An input overvoltage warning has occurred.
5	VIN_UV_WARNING	An input undervoltage warning has occurred.
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3:0	Not Used	Not used

STATUS_TEMPERATURE (7Dh)

Definition: The STATUS_TEMPERATURE command returns one byte of information with a summary of any temperature related faults or warnings.
Data Length in Bytes: 1
Data Format: BIT Field
Type: Read Only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_TEMPERATURE (7Dh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	STATUS BIT NAME	MEANING
7	OT_FAULT	An over-temperature fault has occurred.
6	OT_WARNING	An over-temperature warning has occurred.
5	UT_WARNING	An under-temperature warning has occurred.
4	UT_FAULT	An under-temperature fault has occurred.
3	FAULT_INT	A warning or fault occurred from the internal temperature sensor.
2	FAULT_XTEMP0	A warning or fault occurred from the external temperature sensor 0.
1	FAULT_XTEMP1	A warning or fault occurred from the external temperature sensor 1.
0	Not Used	Not used

STATUS_CML (7Eh)

Definition: The STATUS_WORD command returns one byte of information with a summary of any Communications, Logic and/or Memory errors.
Data Length in Bytes: 1
Data Format: Bit Field
Type: Read Only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_CML (7Eh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT NUMBER	MEANING
7	Invalid or unsupported PMBus™ Command was received.
6	The PMBus™ command was sent with Invalid or Unsupported data.
5	A packet error was detected in the PMBus™ command.
4:2	Not used
1	A PMBus™ command tried to write to a read only or protected command, or a communication fault other than the ones listed in this table has occurred.
0	Not used

STATUS_MFR_SPECIFIC (80h)

Definition: The STATUS_MFR_SPECIFIC command returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults. Note: The VMON OV/UV warnings are set at ±10% of the VMON_XX_FAULT commands.
Data Length in Bytes: 1
Data Format: BIT Field
Type: Read Only
Protectable: No
Default Value: 00h
Units: N/A

COMMAND	STATUS_MFR_SPECIFIC (80h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT	FIELD NAME	MEANING
7	Not Used	Not used
6	Phase	A phase or phases of a multi-phase current sharing group did not initialize.
5	VMON UV Warning	The voltage on the VMON pin has dropped 10% below the level set by MFR_VMON_UV_FAULT.
4	VMON OV Warning	The voltage on the VMON pin has risen 10% above the level set by MFR_VMON_OV_FAULT.
3	External Switching Period Fault	Loss of external clock synchronization has occurred.
2	Not Used	Not used
1	VMON UV Fault	The voltage on the VMON pin has dropped below the level set by MFR_VMON_UV_FAULT.
0	VMON OV Fault	The voltage on the VMON pin has risen above the level set by MFR_VMON_OV_FAULT.

READ_VIN (88h)

Definition: Returns the input voltage reading.
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: V
Equation: READ_VIN = Y x 2^N
Range: N/A

COMMAND	READ_VIN (88h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_IIN (89h)

Definition: Returns the input current reading.
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: A
Equation: READ_IIN = Y x 2^N
Range: N/A

COMMAND	READ_IIN (89h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.
Data Length in Bytes: 2
Data Format: Linear-16 Unsigned.
Type: Read Only
Protectable: No
Default Value: N/A
Equation: READ_VOUT = READ_VOUT x 2^{-13}
Units: V

COMMAND	READ_VOUT (8Bh)															
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_IOUT (8Ch)

Definition: Returns the combined output current of Phase 0 and Phase 1, i.e., the total output current.
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: A
Equation: READ_IOUT = Y x 2^N
Range: N/A

COMMAND	READ_IOUT (8Ch)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_TEMPERATURE_1 (8Dh)

Definition: Returns the temperature reading internal to the device.
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: °C
Equation: READ_TEMPERATURE_1 = Y x 2^N
Range: N/A

COMMAND	READ_INTERNAL_TEMP_1 (8Dh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_TEMPERATURE_2 (8Eh)

Definition: Returns the temperature reading from the external temperature device connected to XTEMP0.
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: °C
Equation: READ_TEMPERATURE_2 = Y x 2^N
Range: N/A

COMMAND	READ_EXTERNAL_TEMP_2 (8Eh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_TEMPERATURE_3 (8Fh)

Definition: Returns the temperature reading from the external temperature device connected to XTEMP1.
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: °C
Equation: READ_TEMPERATURE_2 = Y x 2^N
Range: N/A

COMMAND	READ_EXTERNAL_TEMP_3 (8Fh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_DUTY_CYCLE (94h)

Definition: Reports the duty cycle of the converter during the enable state. The duty cycle read is essentially an average of the duty cycles of Phase 0 and Phase 1.
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: %
Equation: READ_DUTY_CYCLE = Y x 2^N
Range: 0 to 100%

COMMAND	READ_DUTY_CYCLE (94h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Default Value: N/A
Units: kHz
Equation: READ_FREQUENCY = Y x 2^N
Range: N/A
Units: N/A

COMMAND	READ_FREQUENCY (95h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

PMBUS_REVISION (98h)

Definition: The PMBUS_REVISION command returns the revision of the PMBus Specification to which the device is compliant.
Data Length in Bytes: 1
Data Format: BIT Field
Type: Read Only
Protectable: N/A
Default Value: 11h (Part 1 Revision 1.2, Part 2 Revision 1.2)
Units: N/A

COMMAND	PMBUS_REVISION (98h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	See Following Table							
Default Value	0	0	1	0	0	0	1	0

BITS 7:4	PART 1 REVISION	BITS 3:0	PART 2 REVISION
0000	1.0	0000	1.0
0001	1.1	0001	1.1
0010	1.2	0010	1.2

MFR_ID (99h)

Definition: MFR_ID sets a user defined identification string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.
Data Length in Bytes: User Defined
Data Format: ASCII. ISO/IEC 8859-1
Type: Block R/W
Protectable: Yes
Default Value: null
Units: N/A

MFR_MODEL (9Ah)

Definition: MFR_MODEL sets a user defined model string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.
Data Length in Bytes: User Defined
Data Format: ASCII. ISO/IEC 8859-1
Type: Block R/W
Protectable: Yes
Default Value: null
Units: N/A

MFR_REVISION (9Bh)

Definition: MFR_REVISION sets a user defined revision string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User Defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: null

Units: N/A

MFR_LOCATION (9Ch)

Definition: MFR_LOCATION sets a user defined location identifier string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User Defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: null

Units: N/A

MFR_DATE (9Dh)

Definition: MFR_DATE sets a user defined date string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User Defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: null

Units: N/A

MFR_SERIAL (9Eh)

Definition: MFR_SERIAL sets a user defined serialized identifier string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 bytes. This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.

Data Length in Bytes: User Defined

Data Format: ASCII. ISO/IEC 8859-1

Type: Block R/W

Protectable: Yes

Default Value: null

Units: N/A

READ_IOUT0 (A1h)

Definition: Returns the output current of phase 0.
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: A
Equation: READ_IOUT = Y x 2^N
Range: N/A

COMMAND	READ_IOUT0 (A1h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

READ_IOUT1 (A2h)

Definition: Returns the output current of Phase 1.
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: A
Equation: READ_IOUT = Y x 2^N
Range: N/A

COMMAND	READ_IOUT1 (A2h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

LEGACY_FAULT_GROUP (A8h)

Definition: This command allows the ZL8801 to sequence and fault spread with devices other than the ZL8800 and ZL8801. This command sets which rail DDC IDs should be listened to for fault spreading information. The data sent is a 4-byte, 32-bit vector where every bit represents a rail's DDC ID. A bit set to 1 indicates a device DDC ID to which the configured device will respond upon receiving a fault spreading event. In this vector, Bit 0 of byte 0 corresponds to the rail with DDC ID 0. Following through, Bit 7 of byte 3 corresponds to the rail with DDC ID 31.

NOTE: The device/rail's own DDC ID should not be set within the LEGACY_FAULT_GROUP command for that device/rail.

All devices in a current share rail (devices other than the ZL8800/1) must shut down for the rail to report a shut down.

If fault spread mode is enabled in USER_CONFIG, the device will immediately shut down if one of its DDC_GROUP members fail. The device/rail will attempt its configured restart only after all devices/rails within the DDC_GROUP have cleared their faults.

If fault spread mode is disabled in USER_CONFIG, the device will perform a sequenced shutdown as defined by the SEQUENCE command setting. The rails/devices in a sequencing set only attempt their configured restart after all faults have cleared within the DDC_GROUP. If fault spread mode is disabled and sequencing is also disabled, the device will ignore faults from other devices and stay enabled.

Data Length in Bytes: 4
Data Format: BIT Field
Type: Block R/W
Protectable: Yes
Default Value: 00000000h
Units: N/A

COMMAND	LEGACY_FAULT_GROUP (A8h)															
Format	Bit Field															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
31:0	Fault Group	NA	00000000h	Identifies the devices in the fault spreading group.

IC_DEVICE_ID (ADh)

Definition: Reports device identification information.
Data Length in Bytes: 4
Data Format: CUS
Type: Block Read
Protectable: No
Default Value: 49A02300h
Units: N/A

COMMAND	IC_DEVICE_ID (ADh)			
Format	Block Read			
Byte Position	3	2	1	0
Function	MFR code	ID High Byte	ID Low Byte	Reserved
Default Value	49h	A0h	23h	00h

IC_DEVICE_REV (AEh)

Definition: Reports device revision information.
Data Length in Bytes: 4
Data Format: CUS
Type: Block Read
Protectable: No
Default Value: 01000000h
Units: N/A

COMMAND	IC_DEVICE_REV (AEh)			
Format	Block Read			
Byte Position	3	2	1	0
Function	Firmware Major	Firmware Minor	Factory Config	Reserved
Default Value	01h	00h	00h	00h

USER_DATA_00 (B0h)

Definition: USER_DATA_00 sets a user defined data string not to exceed 32 bytes. The sum total of characters in MFR_ID, MFR_MODEL, MFR_REVISION, MFR_LOCATION, MFR_DATE, MFR_SERIAL and USER_DATA_00 plus one byte per command cannot exceed 128 bytes This limitation includes multiple writes of this command before a STORE command. To clear multiple writes, perform a RESTORE, write this command then perform a STORE/RESTORE.
Data Length in Bytes: user defined
Data Format: ASCII. ISO/IEC 8859-1
Type: Block R/W
Protectable: Yes
Default Value: null
Units: N/A

DEADTIME_MAX (BFh)

Definition: Sets the maximum dead time value for the adaptive dead time algorithm. Settings are applied to both phases.
Data Length in Bytes: 2
Data Format: BIT Field
Type: R/W
Protectable: Yes
Default Value: 3838h (56ns/56ns)
Units: ns
Range: 0 to 60ns
Reference: N/A

COMMAND	DEADTIME_MAX (BFh)															
Format	Bit Field/Linear-7 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	0	0	1	1	1	0	0	0	0	0	1	1	1	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
15	Not Used	0	Not used
14:8	Sets the maximum H-to-L dead time	H	Limits the maximum allowed H-to-L dead time when using the adaptive dead time algorithm. Dead time = Hns (signed).
7	Not Used	0	Not used
6:0	Sets the maximum L-to-H dead time	L	Limits the maximum allowed L-to-H dead time when using the adaptive dead time algorithm. Dead time = Lns (signed).

IOUT0_CAL_GAIN (CAh)

Definition: Sets the effective impedance across the Phase 0 current sense circuit for use in calculating output current at +25°C.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: AA66h (0.3mΩ)
Units: mΩ
Equation: IOUT_CAL_GAIN = Y x 2^N

COMMAND	IOUT0_CAL_GAIN (CAh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0

IOUT1_CAL_GAIN (CBh)

Definition: Sets the effective impedance across the Phase 1 current sense circuit for use in calculating output current at +25°C.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: AA66h (0.3mΩ)
Units: mΩ
Equation: IOUT_CAL_GAIN = Y x 2N

COMMAND	IOUT1_CAL_GAIN (CBh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	0	1	0	1	0	0	1	1	0	0	1	1	0

IOUT0_CAL_OFFSET (CCh)

Definition: Used to null out any offsets in the output current sensing circuit and to compensate for delayed measurements of current ramp due to ISENSE blanking time for Phase 0.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: 0000h (0A)
Units: A
Equation: IOUT_CAL_OFFSET = Y x 2^N

COMMAND	IOUT0_CAL_OFFSET (CCh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

IOUT1_CAL_OFFSET (CDh)

Definition: Used to null out any offsets in the output current sensing circuit and to compensate for delayed measurements of current ramp due to ISENSE blanking time for Phase 1.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: 0000h (0A)
Units: A
Equation: IOUT_CAL_OFFSET = Y x 2^N

COMMAND	IOUT1_CAL_OFFSET (CDh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

MIN_VOUT_REG (CEh)

Definition: Sets the minimum output voltage in millivolts (mV) that the device will attempt to regulate to during start-up and shutdown ramps.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: F258h (150mV)
Units: A
Equation: MIN_VOUT_REG = Y x 2^N

COMMAND	MIN_VOUT_REG (CEh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	1	1	0	0	1	0	0	1	0	1	1	0	0	0

ISENSE_CONFIG (D0h)

Definition: Configures current sense circuitry. Settings are applied to both phases.
Data Length in Bytes: 2
Data Format: BIT Field
Type: R/W Word
Protectable: Yes
Default Value: 4204h (256ns, 5 counts, downslope, low range)
Units: N/A
Range: N/A

COMMAND	ISENSE_CONFIG (D0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	0	1	0	0	0	0	1	0	0	0	0	0	0	1	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:11	Current Sense Blanking Time	00000	0	Sets the blanking time current sense blanking time in increments of 32ns
		00001	32	
		00010	64	
		00011	96	
		00100	128	
		00101	160	
		00110	192	
		00111	224	
		01000	256	
		01001	288	
		01010	320	
		01011	352	
		01100	384	
		01101	416	
		01110	448	
		01111	480	
		10000	512	
		10001	544	
		10010	576	
		10011	608	
		10100	640	
		10101	672	
		10110	704	
		10111	736	
		11000	768	
		11001	800	
		11010	832	
10:8	Current Sense Fault Count	000	1	Sets the number of consecutive overcurrent (OC) or undercurrent (UC) events required for a fault. An event can occur once during each switching cycle. For example, if 5 is selected, an OC or UC event must occur for 5 consecutive switching cycles, resulting in a delay of at least 5 switching periods.
		001	3	
		010	5	
		011	7	
		100	9	
		101	11	
		110	13	
		111	15	
7:4	Not Used	000	Not Used	Not used
3:2	Current Sense Control	00	Not Used	Selection of current sensing method (DCR based: V_{OUT} referenced).
		01	DCR (Down Slope)	
		10	DCR (Up Slope)	
		11	Not Used	
1:0	Current Sense Range	00	Low Range	Low Range ±25mV, Medium Range ±35mV, High Range ±50mV
		01	Medium Range	
		10	High Range	
		11	Not Used	

USER_CONFIG (D1h)

Definition: Configures several user-level features.
Data Length in Bytes: 2
Data Format: BIT Field
Type: R/W
Protectable: Yes
Default Value: 0402h
Units: N/A

COMMAND	USER_CONFIG (D1h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:11	Minimum Duty Cycle	00000	0-31d	Sets the minimum duty-cycle to 2x(VALUE+1)/512. Must be enabled with Bit 7.
10	Enable DR MOS	0	Disable	0 = PWML and PWMH are direct drive to MOSFET driver.
		1	Enable	1 = PWML is DrMOS Enable, PWMH is DrMOS PWM input.
9:8	Not Used	00	Not Used	Not Used
7	Minimum Duty Cycle Control	0	Disable	1 = Minimum Duty Cycle Control is Enabled, 0 = Minimum Duty Cycle Control is Disabled.
		1	Enable	
6:5	Not Used	00	Not Used	Not Used
4	Margin Ratio Enable	0	Disable	Use VOUT_MARGIN_RATIO to configure margin values when enabled.
		1	Enable	
3	Not Used	0	Not Used	Not Used
2	Power-good Configuration	0	Open Drain	0 = PG is open-drain output.
		1	Push-pull	1 = PG is push-pull output.
1	XTEMP Enable	0	Disable	Enable external temperature sensor.
		1	Enable	
0	XTEMP Fault Select	0	Disable	Selects external temperature sensor to determine temperature faults.
		1	Enable	

IIN_CAL_GAIN (D2h)

Definition: Sets the effective impedance across the current sense circuit for use in calculating input current at +25°C.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: C200h (2mΩ)
Units: mΩ
Equation: IIN_CAL_GAIN = Y x 2^N

COMMAND	IIN_CAL_GAIN (D2h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0

DDC_CONFIG (D3h)

Definition: Configures DDC addressing and current sharing for up to 8 phases. To operate as a 4-phase controller, set both devices to the same Rail ID, set Phases in Rail to 4, then set each phase ID sequentially, for example, 0 and 1. The ZL8801 will automatically equally offset all phases in the rail. Note that phase spreading is done automatically as part of the DDC_CONFIG command, the INTERLEAVE command only applies to non-current sharing rails. Following is a table illustrating how DDC_CONFIG automatically sets phases for multi-phase configurations. In 2-phase single device operation, the phases are set to position 0 and 4 automatically.

	4 PHASES				6 PHASES				8 PHASES			
	ID	# PHASE	PHASE 0	PHASE 1	ID	# PHASE	PHASE 0	PHASE 1	ID	# PHASE	PHASE 0	PHASE 1
Device 1	0	4	0	4	0	6	0	4	0	8	0	4
Device 2	1	4	2	6	1	6	1	5	1	8	1	5
Device 3					2	6	2	6	2	8	2	6
Device 4									3	8	3	7

Data Length in Bytes: 2
Data Format: Bit FIELD
Type: R/W
Protectable: Yes
Default Value: PMBus™ address pin-strap dependent
Units: N/A

COMMAND	DDC_CONFIG (D3h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	0	0	0	Lower 5 bits of device address					0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15:13	Phase ID	0 to 3	0	Sets the device's phase position within the rail (see chart above)
12:8	Rail ID	0 to 31d	0	Identifies the device as part of a current sharing rail (Shared output).
7:3	Not Used	00	00	Not used
2:0	Phases In Rail	1, 3, 5, 7d	0	Identifies the number of phases on the same rail (+1).

POWER_GOOD_DELAY (D4h)

Definition: Sets the delay applied between the output exceeding the PG threshold (POWER_GOOD_ON) and asserting the PG pin. The delay time can range from 0ms up to 500s, in steps of 125ns. A 1ms minimum configured value is recommended to apply proper debounce to this signal.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: CA00h, 4ms
Units: ms
Equation: POWER_GOOD_DELAY = Y x 2^N
Range: 0 to 5 seconds

COMMAND	POWER_GOOD_DELAY (D4h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0

MULTI_PHASE_RAMP_GAIN (D5h)

Definition: MULTI_PHASE_RAMP_GAIN command value indirectly determines the output voltage rise time during the turn-on ramp. Typical gain values range from 1 to 5. Lower gain values produce longer ramp times.
MULTI_PHASE_RAMP_GAIN mode is automatically selected when the ZL8801 is configured to operate in a 4-, 6- or 8-phase current sharing group. When in MULTI_PHASE_RAMP_GAIN mode the turn-on ramp-up is done with the high bandwidth ASCR control circuitry disabled, resulting in a lower loop bandwidth during start-up ramps. Once POWER_GOOD has been asserted, ASCR circuitry is enabled and the ZL8801 operates normally. When MULTI_PHASE_RAMP_GAIN mode is enabled, Soft-off ramps are not allowed (TOFF_FALL is ignored). When the ZL8801 is commanded to shut down, both the high-side and low-side MOSFETs are turned off, or in the case of DrMOS, the enable pin is pulled low (DrMOS disabled). Large load current transitions during multi-phase ramp ups will cause output voltage discontinuities.
When the phase count is 2; i.e., when the ZL8801 is operating standalone, ASCR is enabled at all times and all commands associated with turn-on and turn-off (TON_RISE, TOFF_FALL, Soft-Off) operate normally.
Data Length in Bytes: 1
Data Format: 1 byte binary
Type: R/W
Protectable: Yes
Default Value: 03h
Units: N/A

COMMAND	MULTI_PHASE_RAMP_GAIN (D5h)							
Format	1 Byte Binary							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Default Value	0	0	0	0	0	0	1	1

BIT	FIELD NAME	VALUE	DESCRIPTION
7:0	• Gain	00-FF	Start-up ramp gain

INDUCTOR (D6h)

Definition: Informs the device of the circuit's inductor value. This is used in adaptive algorithm calculations relating to the inductor ripple current.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: B23Dh (0.56µH)
Units: µH
Equation: INDUCTOR = Y x 2^N
Range: 0 to 100µH

COMMAND	INDUCTOR (D6h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	0	0	1	0	0	0	1	1	1	1	0	1

VOUT_MARGIN RATIO (D7h)

Definition: Percentage to set MARGIN_HIGH and MARGIN_LOW above and below VOUT_COMMAND when feature is enabled by USER_CONFIG.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: 5 (CA80h)
Units: %
Equation: VOUT_MARGIN_RATIO = Y x 2^N
Range: 0 to 50%

COMMAND	VOUT_MARGIN_RATIO (D7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	1	0	0	0	0	0	0	0

OVUV_CONFIG (D8h)

Definition: Configures the output voltage OV and UV fault detection feature
Data Length in Bytes: 1
Data Format: BIT Field
Type: R/W
Protectable: Yes
Default Value: 00h
Units: N/A

COMMAND	OVUV_CONFIG (D8h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
7	Controls how an OV fault response shutdown sets the output driver state	0	An OV fault does not enable low-side power device.
		1	An OV fault enables the low-side power device.
6:4	Not Used	0	Not used
3:0	Defines the number of consecutive limit violations required to declare an OV or UV fault	N	N+1 consecutive OV or UV violations initiate a fault response.

XTEMP_SCALE (D9h)

Definition: Sets a scalar value that is used for calibrating both of the external temperature sensors (Phase 0 and Phase 1). The constant is applied in Equation 27 to produce the read value of XTEMP via the PMBus™ command READ_TEMPERATURE_2 and READ_TEMPERATURE_3.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: BA00h (1.0)
Units: 1/°C
Equation:

$$\text{READ\_TEMPERATURE\_2} = \left(\text{ExternalTemperature} \cdot \frac{1}{\text{XTEMP\_SCALE}}\right) + \text{XTEMP\_OFFSET} \quad \text{(EQ. 27)}$$

Range: 0.1 to 10

COMMAND	XTEMP_SCALE (D9h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	0	1	1	1	0	1	0	0	0	0	0	0	0	0	0

XTEMP_OFFSET (DAh)

Definition: Sets an offset value that is used for calibrating both of the external temperature sensors (Phase 0 and Phase 1). The constant is applied in Equation 28 to produce the read value of XTEMP via the PMBus™ command READ_TEMPERATURE_2 and READ_TEMPERATURE_3.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: 0000h (0)
Units: °C
Equation:

$$\text{READ\_TEMPERATURE\_2} = \left(\text{ExternalTemperature} \cdot \frac{1}{\text{XTEMP\_SCALE}}\right) + \text{XTEMP\_OFFSET} \quad \text{(EQ. 28)}$$

Range: -100°C to +100°C

COMMAND	XTEMP_OFFSET (DAh)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TEMPCO_CONFIG (DCh)

Definition: Configures the correction factor and temperature measurement source when performing temperature coefficient correction for current sense. TEMPCO_CONFIG values are applied as negative correction to a positive temperature coefficient. When using external temperature sensors, the coefficient applies to both temperature sensors.
Data Length in Bytes: 1
Data Format: Bit Field
Type: R/W
Protectable: Yes
Default Value: 27h (3900ppm/°C)
Equation: To determine the hex value of the Tempco Correction factor (TC) for current scale of a power stage current sensing, first determine the temperature coefficient of resistance for the sensing element, α. This is found with Equation 29:

$$\alpha = \frac{R_{REF} - R}{R_{REF}(T_{REF} - T)} \quad \text{(EQ. 29)}$$

Where:
R = Sensing element resistance at temperature "T"
R_{REF} = Sensing element resistance at reference temperature T_{REF}
α = Temperature coefficient of resistance for the sensing element material
T = Temperature measured by temperature sensor, in Degrees Celsius
T_{REF} = Reference temperature that α is specified at for the sensing element material
After α is determined, convert the value in units of 100ppm/°C. This value is then converted to a hex value by using Equation 30:

$$TC = \frac{\alpha \times 10^6}{100} \quad \text{(EQ. 30)}$$

Typical Values: Copper = 3900ppm/°C (27h), silicon = 4800ppm/°C (30h)
Range: 0 to 6300ppm/°C

COMMAND	TEMPCO_CONFIG (DCh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	0	0	1	0	0	1	1	1

BITS	PURPOSE	VALUE	DESCRIPTION
7	Selects the temp sensor source for tempco correction	0	Selects the internal temperature sensor.
		1	Selects the XTEMP0 and XTEMP1 pins for temperature measurements (2N3904 Junction) Note that XTEMP must be enabled in USER_CONFIG, Bit1.
6:0	Sets the tempco correction in units of 100ppm/°C for IOUT_CAL_GAIN	TC	RSEN (DCR) = IOUT_CAL_GAIN x (1+TC x (T-25)). where RSEN = resistance of sense element.

DEADTIME (DDh)

Definition: Sets the nonoverlap between PWM transitions using a 2 byte data field. The most significant byte controls the high-side to low-side deadtime value as a single 2's-complement signed value in units of ns. The least-significant byte controls the low-side to high-side deadtime value. Positive values imply a nonoverlap of the FET drive on-times. Negative values imply an overlap of the FET drive on-times. Writing a value to this command immediately before writing the DEADTIME_CONFIG command will set a new maximum for the adaptive deadtime algorithm. The device will operate at the deadtime values written to this command when adaptive deadtime is disabled.

Data Length in Bytes: 2

Data Format: CUS

Type: R/W

Protectable: Yes

Default Value: 1010h (16ns/16ns)

Units: ns

Range: -15ns to 60ns

COMMAND	DEADTIME (DDh)															
Format	Linear-8 Signed															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	High to low-side deadtime 8 bit two's complement signed								Low to high-side deadtime 8 bit two's complement signed							
Default Value	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

DEADTIME_CONFIG (DEh)

Definition: Configures the adaptive deadtime optimization mode. Also sets the minimum deadtime value for the adaptive deadtime mode range.

Data Length in Bytes: 2

Data Format: BIT Field

Type: R/W

Protectable: Yes

Default Value: 8888h (Frozen deadtime control, 8ns/8ns minimum deadtime)

Units: N/A

COMMAND	DEADTIME_CONFIG (DEh)															
Format	Bit Field/Linear-7 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
15	Sets the high-to-low transition deadtime mode	0	Adaptive H-to-L deadtime control.
		1	Freeze the H-to-L deadtime.
14:8	Sets the minimum H-to-L deadtime	0-126d	Limits the minimum allowed H-to-L deadtime when using the adaptive deadtime algorithm (2ns resolution).
7	Sets the low-to-high transition deadtime mode	0	Adaptive L-to-H deadtime control.
		1	Freeze the L-to-H deadtime.
6:0	Sets the minimum L-to-H deadtime	0-126d	Limits the minimum allowed L-to-H deadtime when using the adaptive deadtime algorithm (2ns resolution).

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings. ChargeMode control achieves a fast acting, low deviation transient response by detecting and reacting to very small variations in the output voltage. ChargeMode control performance is optimized when ΔV due to capacitor ripple is 1% or less of the output voltage.

Data Length in Bytes: 4

Data Format: BIT Field and non-signed binary

Type: R/W

Protectable: Yes

Default Value: 015A0190h (ASCR enabled, Gain 400, Residual 90)

Units: N/A

COMMAND	ASCR_CONFIG (DFh)															
Format	Bit Field/Linear-8 Unsigned															
Bit Position	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	1	0	1	0	1	1	0	1	0
Format	Linear-16 Unsigned															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	1	1	0	1	1	0	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
31:25	Not Used	0000000h	Not Used
24	ASCR Enable	1	Enable
		0	Disable
23:16	ASCR Residual Setting	90	ASCR residual
15:0	ASCR Gain Setting	400	ASCR gain

SEQUENCE (E0h)

Definition: Identifies the Rail DDC ID of the prequel and sequel rails when performing multirail sequencing. The device will enable its output when its EN or OPERATION enable state, as defined by ON_OFF_CONFIG, is set and the prequel device has issued a power-good event on the DDC bus. The device will disable its output (using the configured delay values) when the sequel device has issued a power-down event on the DDC bus.

The data field is a two-byte value. The most-significant byte contains the 5-bit Rail DDC ID of the prequel device. The least-significant byte contains the 5-bit Rail DDC ID of the sequel device. The most significant bit of each byte contains the enable of the prequel or sequel mode.

Data Length in Bytes: 2

Data Format: BIT Field

Type: R/W

Protectable: Yes

Default Value: 00h (Prequel and Sequel disabled)

Units: N/A

COMMAND	SEQUENCE (E0h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
15	Prequel Enable	0	Disable	Disable, no prequel preceding this rail.
		1	Enable	Enable, prequel to this rail is defined by Bits 12:8.
14:13	Not Used	0	Not Used	Not used
12:8	Prequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the prequel rail.
7	Sequel Enable	0	Disable	Disable, no sequel following this rail.
		1	Enable	Enable, sequel to this rail is defined by Bits 4:0.
6:5	Not Used	0	Not Used	Not used
4:0	Sequel Rail DDC ID	0-31d	DDC ID	Set to the DDC ID of the sequel rail.

TRACK_CONFIG (E1h)

Definition: Configures the voltage tracking modes of the device. Single device (2-phase) tracking is supported. Tracking as part of a 4-, 6- or 8-phase current sharing group is not supported.

Data Length in Bytes: 1

Data Format: BIT Field

Type: R/W

Protectable: Yes

Default Value: 00h

Units: N/A

COMMAND	TRACK_CONFIG (E1h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	SETTING	DESCRIPTION
7	Voltage Tracking Control	0	Disable	Tracking is disabled.
		1	Enable	Tracking is enabled.
6:3	Not Used	0000	Not Used	Not used
2	Tracking Ratio Control	0	100%	Output tracks at 100% ratio of VTRK input.
		1	50%	Output tracks at 50% ratio of VTRK input.
1	Tracking Upper Limit	0	Target Voltage	Output voltage is limited by target voltage.
		1	VTRK Voltage	Output voltage is limited by VTRK voltage.
0	Not Used	0	Not Used	Not used

DDC_GROUP (E2h)

Definition: Rails (output voltages) are assigned group numbers in order to share specified behaviors. The DDC_GROUP command configures fault spreading group ID and enable, broadcast OPERATION group ID and enable and broadcast VOUT_COMMAND group ID and enable. Note that DDC Groups are separate and unique from DDC Phases. Current sharing rails need to be in the same DDC Group in order to respond to broadcast VOUT_COMMAND and OPERATION commands. Power fail event responses are automatically spread in current sharing rails when they are configured using DDC_CONFIG, regardless of their setting in DDC_GROUP.
Data Length in Bytes: 3
Data Format: BIT Field
Type: R/W
Protectable: Yes
Default Value: 000000h (Ignore broadcast VOUT_COMMAND and operation, sequence shutdown on power fail event)
Units: N/A

COMMAND	DDC_GROUP (E2h)																							
Format	Bit Field																							
Bit Position	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table																							
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
23	Broadcast Margin Command Response	1	Responds to broadcast margin command with same Group ID.
		0	Ignores broadcast margin command.
22:18	Broadcast VOUT_COMMAND Group ID	0-31d	Group ID sent as data for broadcast VOUT_COMMAND events.
17	Broadcast VOUT_COMMAND Response	1	Responds to broadcast VOUT_COMMAND with same Group ID.
		0	Ignores broadcast VOUT_COMMAND.
16:12	Broadcast VOUT_COMMAND Group ID	0-31d	Group ID sent as data for broadcast VOUT_COMMAND events.
11	Broadcast Operation Response	1	Responds to broadcast operation with same Group ID.
		0	Ignores broadcast operation.
10:6	Broadcast Operation Group ID	0-31d	Group ID sent as data for broadcast Broadcast operation events.
5	Power Fail Response	1	Responds to power fail events with same group ID by shutting down immediately.
		0	Responds to power fail events with same group ID with sequenced shutdown.
4:0	Power Fail Group ID	0-31d	Group ID sent as data for broadcast power fail events.

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string.
Data Length in Bytes: 16
Data Format: ASCII. ISO/IEC 8859-1
Type: Block Read
Protectable: No
Default Value: <part number/die revision/firmware revision>
Units: N/A

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the table below. The command format is the same as the PMBus™ standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT.
Data Length in Bytes: 1
Data Format: BIT Field
Type: R/W
Protectable: Yes
Default Value: 80h (Immediate shut down, no retries)
Units: Retry time = 70ms

COMMAND	MFR_IOUT_OC_FAULT_RESPONSE (E5h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: For all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Not used
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	111	Not used. Retry time is 70ms.

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the table below. The command format is the same as the PMBus™ standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT.
Data Length in Bytes: 1
Data Format: BIT Field
Type: R/W
Protectable: Yes
Default Value: 80h (Immediate shutdown, no retries)
Units: Retry time = 70ms

COMMAND	MFR_IOUT_UC_FAULT_RESPONSE (E6h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: For all modes, the device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Not used
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	111	Not used. Retry time is 70ms.

IOUT_AVG_OC_FAULT_LIMIT (E7h)

Definition: Sets the I_{OUT} average overcurrent fault threshold for each phase (Phase 0 and Phase 1). For downslope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For upslope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_ OC_FAULT_LIMIT.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: DA80h (20A)
Units: Amperes
Equation: IOUT_AVG_OC_FAULT_LIMIT = Y x 2N
Range: -100 to 100A

COMMAND	IOUT_AVG_OC_FAULT_LIMIT (E7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	1	0	1	0	1	0	0	0	0	0	0	0

IOUT_AVG_UC_FAULT_LIMIT (E8h)

Definition: Sets the I_{OUT} average undercurrent fault threshold for each phase (Phase 0 and Phase 1). For downslope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For upslope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_ UC_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D580h (-10A)

Units: Amperes

Equation: IOUT_AVG_UC_FAULT_LIMIT = Y x 2N

Range: -100 to 100A

COMMAND	IOUT_AVG_UC_FAULT_LIMIT (E8h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	0	1	0	1	1	0	0	0	0	0	0	0

MFR_USER_CONFIG (E9h)

Definition: This command is used to set options for output voltage sensing, maximum output voltage override, SMBus time out and DDC and SYNC output configurations.

Data Length in Bytes: 2

Data Format: BIT Field

Type: R/W

Protectable: Yes

Default Value: 0000h

Units: N/A

COMMAND	MFR_USER_CONFIG (E9h)															
Format	Bit Field															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table															
Default Value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BITS	PURPOSE	VALUE	DESCRIPTION
15:7	Not Used	000000000	Not used
6	DDC output Configuration	0	DDC output open drain.
		1	DDC output push-pull.
5	Not Used	0	Not used
4	Disable SMBus Time-outs	0	SMBus time outs enabled.
		1	SMBus time outs disabled.
3	Not Used	0	Not used
2:1	Sync I/O Control	00	Use internal clock.
		01	Use internal clock and output internal clock.
		10	Use external clock.
		11	Not used
0	Not Used	0	Not used

SNAPSHOT (EAh)

Definition: The SNAPSHOT command is a 32 Byte read-back of parametric and status values. It allows monitoring and status data to be stored to NVRAM either during a fault condition or via a system-defined time using the SNAPSHOT_CONTROL command. Snapshot is continuously updated in RAM and can be read using the SNAPSHOT command after a SNAPSHOT_CONTROL 03h (erase snapshot data) has been written when the device is disabled. When a fault occurs, the latest snapshot in RAM is stored to NVRAM. Snapshot data can read back by writing a 01h to the SNAPSHOT_CONTROL command, then reading SNAPSHOT. SNAPSHOT data will not update automatically and SNAPSHOT data in NVRAM will not be written after a fault until a SNAPSHOT_CONTROL 03h has been written again. Note: It is advised that this step be performed while the device's operation is disabled.

Data Length in Bytes: 32
Data Format: BIT Field
Type: Block Read
Protectable: No
Default Value: N/A
Units: N/AI

BYTE NUMBER	VALUE	PMBus™ COMMAND	FORMAT
31:29	Not Used	Not Used	0000h
28:27	I_{OUT} 1	READ_IOUT1 (A1h)	2 Byte Linear-11
26:25	I_{OUT} 0	READ_IOUT0 (A2h)	2 Byte Linear-11
24:23	External Temperature 1	READ_TEMPERATURE_3 (8Fh)	2 Byte Linear-11
22	NVRAM Memory Status Byte	N/A	Bit Field
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	1 Byte Bit Field
20	CML Status Byte	STATUS_CML (7Eh)	1 Byte Bit Field
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	1 Byte Bit Field
18	Input Status Byte	STATUS_INPUT (7Ch)	1 Byte Bit Field
17	I_{OUT} Status Byte	STATUS_IOUT (7Bh)	1 Byte Bit Field
16	V_{OUT} Status Byte	STATUS_VOUT (7Ah)	1 Byte Bit Field
15:14	Switching Frequency	READ_FREQUENCY (95h)	2 Byte Linear-11
13:12	External Temperature 0	READ_TEMPERATURE_2 (8Eh)	2 Byte Linear-11
11:10	Internal Temperature	READ_TEMPERATURE_1 (8Dh)	2 Byte Linear-11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	2 Byte Linear-11
7:6	Highest Measured Output Current	N/A	2 Byte Linear-11
5:4	Output Current	READ_IOUT (8Ch)	2 Byte Linear-11
3:2	Output Voltage	READ_VOUT (8Bh)	2 Byte Linear-16 Unsigned
1:0	Input Voltage	READ_VIN (88h)	2 Byte Linear-11

BLANK_PARAMS (EBh)

Definition: Returns a 16 Byte string which indicates which parameter values were either retrieved by the last RESTORE operation or have been written since that time. Reading BLANK_PARAMS immediately after a restore operation allows the user to determine which parameters are stored in that store. A one indicates the parameter is not present in the store and has not been written since the RESTORE operation.

Data Length in Bytes: 16
Data Format: BIT Field
Type: Block Read
Protectable: No
Default Value: FF...FFh

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01h will cause the device to copy the current SNAPSHOT values from NVRAM to the 32 Byte SNAPSHOT command parameter. Writing a 02h will cause the device to write the current SNAPSHOT values to NVRAM, 03 will erase all SNAPSHOT values from NVRAM. All other values will be ignored. SNAPSHOT 03h must be written to the device when the device is DISABLED. Data will not be updated, or written to NVRAM after a fault occurs until the SNAPSHOT 03h command has been written.

Data Length in Bytes: 1

Data Format: BIT Field

Type: R/W Byte

Protectable: Yes

Default Value: 00h

Units: N/A

COMMAND	SNAPSHOT_CONTROL (F3h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	0	0	0	0	0	0	0	0

VALUE	DESCRIPTION
01	Read SNAPSHOT values from NVRAM
02	Write SNAPSHOT values to NVRAM
03	Erase SNAPSHOT values from NV RAM

RESTORE_FACTORY (F4h)

Definition: Restores the device to the hard-coded factory default values and pin-strap definitions. The device retains the DEFAULT and USER stores for restoring. Security level is changed to Level 1 following this command.

Data Length in Bytes: 0

Data Format: N/A

Type: Write Only

Protectable: Yes

Default Value: N/A

Units: N/A

MFR_VMON_OV_FAULT_LIMIT (F5h)

Definition: Sets the VMON overvoltage fault threshold. A VMON parameter equals 16 times the voltage applied to the VMON pin. The VMON overvoltage warn limit is automatically set to 90% of this fault value.

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: D300h (12V)

Units: V

Equation: MFR_VMON_OV_FAULT_LIMIT = Y x 2^N

Range: 0 to 19V

COMMAND	MFR_VMON_OV_FAULT_LIMIT (F5h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	1	0	0	1	1	0	0	0	0	0	0	0	0

MFR_VMON_UV_FAULT_LIMIT (F6h)

Definition: Sets the VMON undervoltage fault threshold. A VMON parameter equals 16 times the voltage applied to the VMON pin. The VMON undervoltage warn limit is automatically set to 110% of this fault value.
Data Length in Bytes: 2
Data Format: Linear-11
Type: R/W
Protectable: Yes
Default Value: CA00h (4.0V)
Units: V
Equation: MFR_VMON_UV_FAULT_LIMIT = Y x 2^N
Range: 0 to 19V

COMMAND	MFR_VMON_UV_FAULT_LIMIT (F6h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	1	1	0	0	1	0	1	0	0	0	0	0	0	0	0	0

MFR_READ_VMON (F7h)

Definition: Reads the VMON voltage.
Data Length in Bytes: 2
Data Format: Linear-11
Type: Read Only
Protectable: No
Default Value: N/A
Units: V
Equation: MFR_READ_VMON = Y x 2^N
Range: 0 to 19V

COMMAND	MFR_READ_VMON (F7h)															
Format	Linear-11															
Bit Position	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	Signed Exponent, N					Signed Mantissa, Y										
Default Value	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

MFR_VMON_OV_FAULT_RESPONSE (F8h)

Definition: Configures the VMON overvoltage fault response as defined by the following table.
Note: The delay time is the time between restart attempts
Data Length in Bytes: 1
Data Format: BIT Field
Type: R/W
Protectable: Yes
Default Value: 80h (Immediate shut down, no retries)
Units: Retry time = 70ms

COMMAND	MFR_VMON_OV_FAULT_RESPONSE (F8h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: The Device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Not used
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	111	Not used. Retry time is 70ms.

MFR_VMON_UV_FAULT_RESPONSE (F9h)

Definition: Configures the VMON undervoltage fault response as defined by the following table. Note: The delay time is the time between restart attempts.
Data Length in Bytes: 1
Data Format: BIT Field.
Type: R/W
Protectable: Yes
Default Value: 80h (Immediate shut down, no retries)
Units: Retry time = 70ms

COMMAND	MFR_VMON_UV_FAULT_RESPONSE (F9h)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w
Function	See Following Table							
Default Value	1	0	0	0	0	0	0	0

BIT	FIELD NAME	VALUE	DESCRIPTION
7:6	Response Behavior: The Device: • Pulls SALRT low • Sets the related fault bit in the status registers. Fault bits are only cleared by the CLEAR_FAULTS command.	00	Not used
		01	Not used
		10	Disable without delay and retry according to the setting in Bits 5:3.
		11	Not used
5:3	Retry Setting	000	No retry. The output remains disabled until the fault is cleared.
		001-110	Not used
		111	Attempts to restart continuously, without limitation, until it is commanded OFF (by the CONTROL pin or OPERATION command or both), bias power is removed, or another fault condition causes the unit to shut down.
2:0	Not Used	111	Not used. Retry time is 70ms.

SECURITY_LEVEL (FAh)

Definition: The device provides write protection for individual commands. Each bit in the UNPROTECT parameter controls whether its corresponding command is writable (commands are always readable). If a command is not writable, a password must be entered in order to change its parameter (i.e., to enable writes to that command). There are two types of passwords, public and private. The public password provides a simple lock-and-key protection against accidental changes to the device. It would typically be sent to the device in the application prior to making changes. Private passwords allow commands marked as nonwritable in the UNPROTECT parameter to be changed. Private passwords are intended for protecting Default-installed configurations and would not typically be used in the application. Each store (USER and DEFAULT) can have its own UNPROTECT string and private password. If a command is marked as nonwritable in the DEFAULT UNPROTECT parameter (its corresponding bit is cleared), the private password in the DEFAULT store must be sent in order to change that command. If a command is writable according to the Default UNPROTECT parameter, it may still be marked as nonwritable in the User Store UNPROTECT parameter. In this case, the User private password can be sent to make the command writable.

The device supports four levels of security. Each level is designed to be used by a particular class of users, ranging from module manufacturers to end users, as discussed in the following. Levels 0 and 1 correspond to the public password. All other levels require a private password. Writing a private password can only raise the security level. Writing a public password will reset the level down to 0 or 1.

Figure 13 shows the algorithm used by the device to determine if a particular command write is allowed.

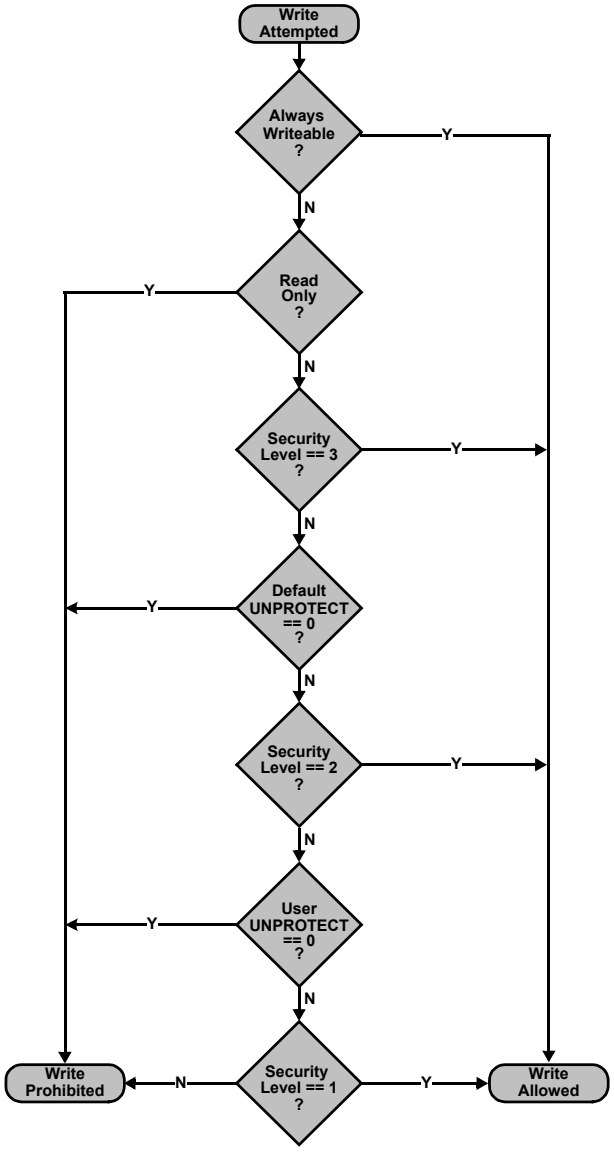


FIGURE 13. ALGORITHM USED TO DETERMINE WHEN A COMMAND IS WRITABLE

Security Level 3 – Module Vendor

Level 3 is intended primarily for use by Module vendors to protect device configurations in the Default Store. Clearing a UNPROTECT bit in the Default Store implies that a command is writable only at Level 3 and above. The device's security level is raised to Level 3 by writing the private password value previously stored in the Default Store. To be effective, the module vendor must clear the UNPROTECT bit corresponding to the STORE_DEFAULT_ALL and RESTORE_DEFAULT commands. Otherwise, Level 3 protection is ineffective since the entire store could be replaced by the user, including the enclosed private password.

Security Level 2 – User

Level 2 is intended for use by the end user of the device. Clearing a UNPROTECT bit in the User Store implies that a command is writable only at Level 2 and above. The device's security level is raised to Level 2 by writing the private password value previously stored in the User Store. To be effective, the user must clear the UNPROTECT bit corresponding to the STORE_USER_ALL, RESTORE_DEFAULT_ALL, STORE_DEFAULT_ALL and RESTORE_DEFAULT commands. Otherwise, Level 2 protection is ineffective since the entire store could be replaced, including the enclosed private password.

Security Level 1 – Public

Level 1 is intended to protect against accidental changes to ordinary commands by providing a global write-enable. It can be used to protect the device from erroneous bus operations. It provides access to commands whose UNPROTECT bit is set in both the Default and User Store. Security is raised to Level 1 by writing the public password stored in the User Store using the PUBLIC_PASSWORD command. The public password stored in the Default Store has no effect.

Security Level 0 - Unprotected

Level 0 implies that only commands which are always writable (e.g., PUBLIC_PASSWORD) are available. This represents the lowest authority level and hence the most protected state of the device. The level can be reduced to 0 by using PUBLIC_PASSWORD to write any value, which does not match the stored public password.

Data Length in Bytes: 1
Data Format: Hex
Type: Read Byte
Protectable: No
Default Value: 01h
Units: N/A
Reference: AN2031 - Writing Configuration Files for Intersil Digital Power Devices

COMMAND	SECURITY_LEVEL (FAh)							
Format	Bit Field							
Bit Position	7	6	5	4	3	2	1	0
Access	r	r	r	r	r	r	r	r
Function	See Following Table							
Default Value	0	0	0	0	0	0	1	1

BIT	FIELD NAME	VALUE	DESCRIPTION
7:2	Not Used	00000	Not used
1:0	Security Level	00	Security level 0
		01	Security level 1
		10	Security level 2
		11	Security level 3

PRIVATE_PASSWORD (FBh)

Definition: Sets the private password string.
Data Length in Bytes: 9
Data Format: ASCII. ISO/IEC 8859-1
Type: R/W Block
Protectable: No
Default Value: 00000000000000000h
Units: N/A
Reference: AN2031 - Writing Configuration Files for Intersil Digital Power Devices

PUBLIC_PASSWORD (FCh)

Definition: Sets the public password string.
Data Length in Bytes: 4
Data Format: ASCII. ISO/IEC 8859-1
Type: R/W
Protectable: No
Default Value: 00000000h
Units: N/A
Reference: AN2031 - Writing Configuration Files for Intersil Digital Power Devices

UNPROTECT (FDh)

Definition: Sets a 256-bit (32-byte) parameter which identifies which commands are to be protected against write-access at lower security levels. Each bit in this parameter corresponds to a command according to the command's code. The command with a code of 01h (OPERATION), for example, is protected by the 2nd least-significant bit of the least-significant byte, followed by the command with a code of 02h (ON_OFF_CONFIG) and so forth. Note that all possible commands have a corresponding bit regardless of whether they are protectable or supported by the device. Clearing a command's UNPROTECT bit indicates that write-access to that command is only allowed if the device's security level has been raised to an appropriate level. The UNPROTECT bits in the DEFAULT store require a security level 3 to be writable. The UNPROTECT bits in the USER store require a security level of 2 or higher to be writable.
Data Length in Bytes: 32
Data Format: Custom
Type: R/W Block
Protectable: No
Default Value: FF...FFh
Units: N/A
Reference: AN2031 - Writing Configuration Files for Intersil Digital Power Devices

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the Intersil website to make sure you have the latest revision.

DATE	REVISION	CHANGE
March 27, 2015	FN8614.3	"Simplified Application" on page 3 removed wire connecting ISENA0, ISENB0, and VDRV.
January 8, 2015	FN8614.2	• Pin Configuration, page 6, pin names swapped for Pins 40 and 41: Pin 40 - XTEMP1P changed to: XTEMP1N Pin 41 - XTEMP1N changed to: XTEMP1P • Pin Description table, page 6, pin names swapped for Pins 40 and 41: Pin 40 - XTEMP1P changed to: XTEMP1N Pin 41 - XTEMP1N changed to: XTEMP1P
September 25, 2014	FN8614.1	Added table "KEY DIFFERENCES BETWEEN FAMILY OF PARTS" on page 1. On page 1: Added related literature. Added part number ZL8801ALAFT7A and Demonstration boards to ordering information table. Added Demo boards to ordering information table
June 18, 2014	FN8614.0	Initial Release

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

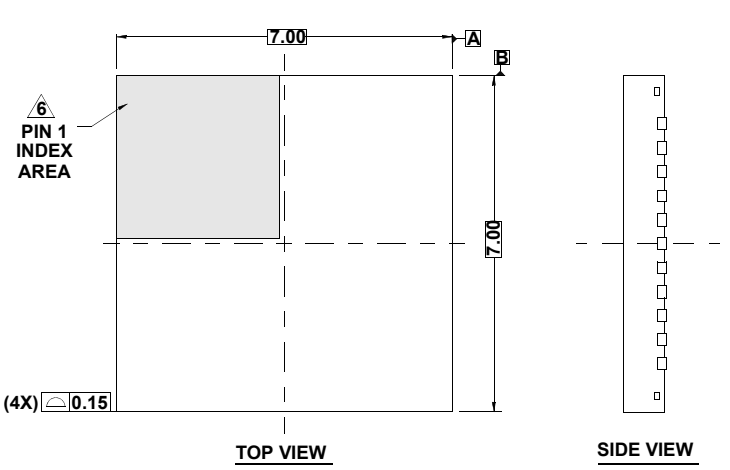
Reliability reports are also available from our website at www.intersil.com/support

Package Outline Drawing

L44.7x7B

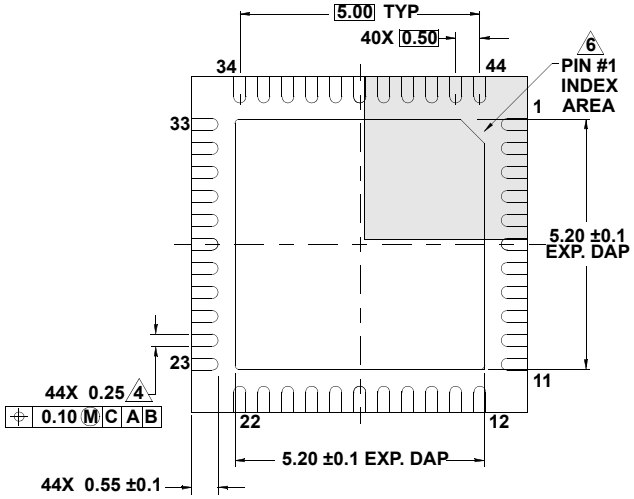
44 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 10/09

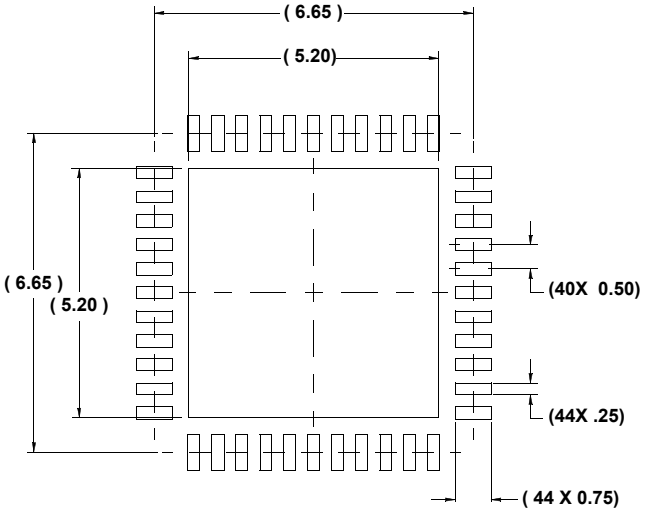


TOP VIEW

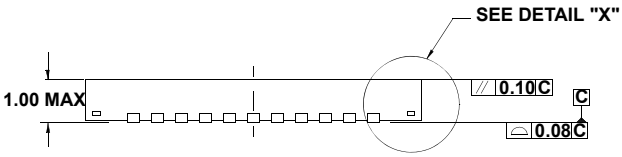
SIDE VIEW



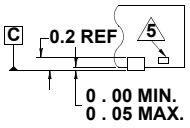
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.
7. Complies to JEDEC MO220 VKKD-1.