RC32508A

FemtoClock 2 Jitter Attenuator and Clock Generator

The RC32508A is a fully integrated, low-power, ultra high-performance jitter attenuator and clock generator. The device supports SyncE for network-based synchronization.

The RC32508A is ideal for providing reference clocks for high-speed serial links up to 112Gbps Ethernet in modular switch line cards and fabric cards in data center equipment. The device is a member of Renesas' high-performance FemtoClock 2 family.

Applications

- Switches / routers
- Jitter attenuation for 10 / 25 / 40 / 100 / 200 / 400 Gbps Ethernet PHYs in switch line cards
- Clock generation for 10 /25 / 40 / 100 / 200 / 400 Gbps Ethernet PHYs in switch fabric cards
- Medical imaging
- Professional audio and video

Product Options

- 7 × 7 × 0.9 mm 48-QFN package
- 8 differential or 16 single-ended outputs

Features

- Can be configured as clock generator or jitter attenuator/synchronizer
- Low power, less than 0.8W typical
- Low jitter, less than 50fs-RMS
- Compliant with ITU-T G.8262 and G.8262.1 option 1 and 2 for synchronous Ethernet Equipment Clock (EEC/eEEC) without degrading output jitter
- PCIe Gen 1-6 CC, SRIS, and SRNS support
- Jitter attenuation with programmable loop bandwidth from 0.1Hz to 12kHz
- Up to two independent frequency domains and eight integer output dividers
- Each frequency domain can be slaved with DPLL or free-run
- DPLL can be configured as DCO
- LVCMOS, AC-LVPECL, AC-LVDS, HCSL, AC-CML output modes supported with programmable output swing
- Up to two single ended or one differential clock inputs, one crystal/XO/TCXO/OCXO input
- Supports 1MHz I^2C, 400kHz SMBus, or 50MHz SPI serial port
- Internal non-volatile memory (up to eight different configurations) provides default device settings on power-up
- 1.8V core and output operation
- -40° to +85°C industrial temperature operation

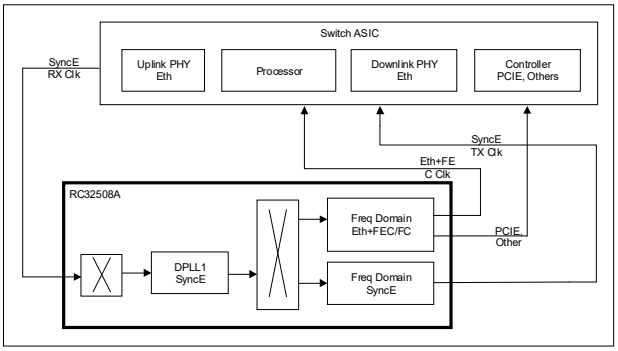

Figure 1. Switch Line Card

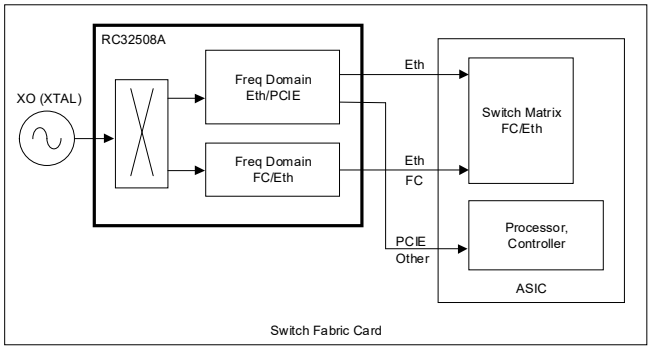

Figure 2. Switch Fabric Card

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1. Overview

The RC32508A is a fully integrated, low-power, ultra-high performance frequency synthesizer with jitter attenuation and network synchronization capabilities. The device can be set up either as a clock generator that is locked to the external crystal or oscillator and providing free-run clock outputs, or as a jitter attenuator that is locked to an external reference and providing low-jitter clock outputs when used with an external crystal or oscillator. The device can provide up to two frequency domains using the two analog PLLs, and each analog PLL is fed into four outputs.

The RC32508A is optimized to deliver excellent phase noise as required for driving up to 112Gbps Ethernet PHYs, ASICs or FPGAs in 10G, 25G, 40G, 100G, 200G, or 400G switch line cards and switch fabric cards. The device supports SyncE for network-based synchronization.

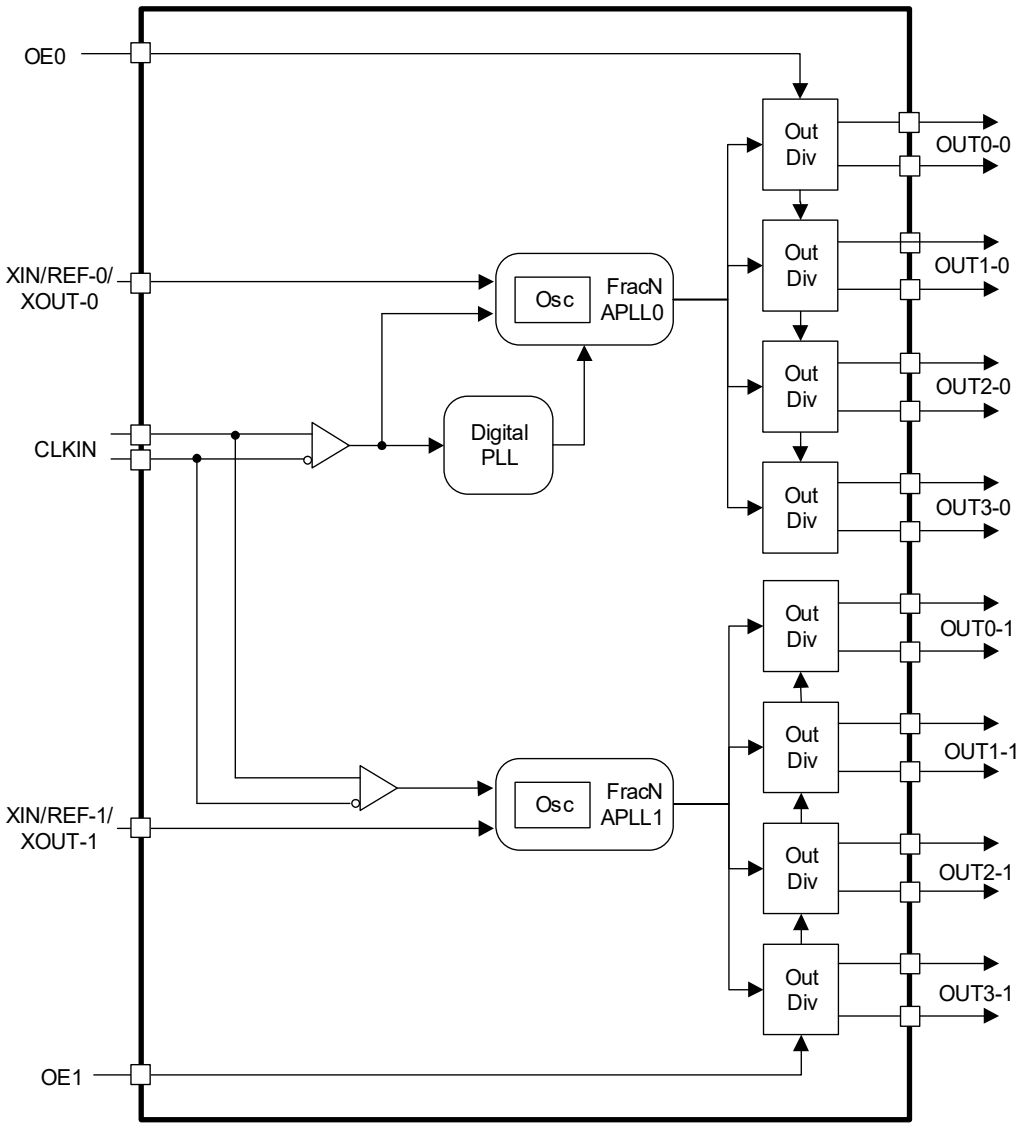


Figure 3. Block Diagram

1.1 Clock Generator Mode

The RC32508A can be set in Clock Generator mode and locked to an external reference to CLKIN, nCLKIN pins by following the steps:

- DPLL/DCO is powered down.
- When locking to an external clock or oscillator applied to CLKIN, nCLKIN, both APLL0 and APLL1 are locked to the clock input.
- APLL0 provides high frequency clock to each of four output dividers that is in turn fed to four clock outputs, namely OUT0-0, OUT1-0, OUT2-0, and OUT3-0.
- APLL1 provides a high frequency clock that is either the same frequency as from APLL0 or a different frequency, to each of four output dividers that is in term fed to four clock outputs, OUT0-1, OUT1-1, OUT2-1, and OUT3-1.
- As shown in Figure 4, up to two frequency domains can be obtained in this configuration and up to eight differential or 16 LVCMOS outputs can be obtained.

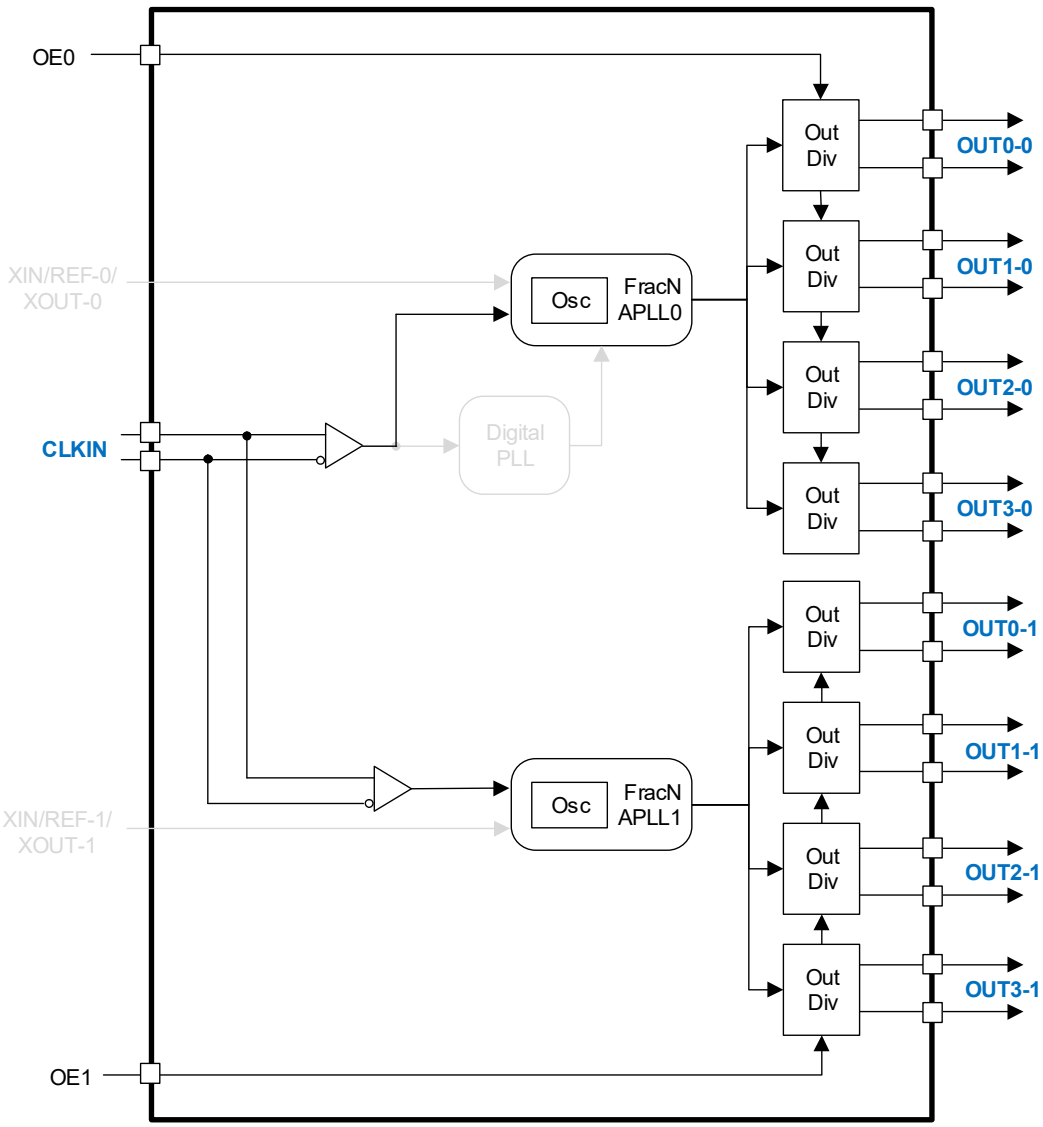


Figure 4. Clock Generator Mode with RC32508A when External Reference is Fed into CLKIN

The RC32508A can be set in Clock Generator mode and locked to an external crystal applied to XIN/REF-0/XOUT-0 pins by following the steps:

- DPLL/DCO is powered down.
- When locking to an external crystal applied to XIN/REF-0/XOUT-0, APLL0 is locked to the crystal.
- APLL0 provides high frequency clock to each of four output dividers that is in turn fed to four clock outputs, OUT0-0, OUT1-0, OUT2-0, and OUT3-0.
- One of the four outputs from APLL0 is programmed as complementary LVCMOS outputs, and for example, OUT3-0-N is fed back into XIN/REF-1 pin and used as a reference to APLL1. APLL1 then provides a high-frequency clock that is either the same frequency as from APLL0 or a different frequency to each of the four output dividers that is in term fed to four clock outputs, OUT0-1, OUT1-1, OUT2-1, and OUT3-1.
- As shown in Figure 5, up to two frequency domains can be obtained in this configuration and up to seven differential outputs and 1 LVCMOS output or 15 LVCMOS outputs can be obtained.

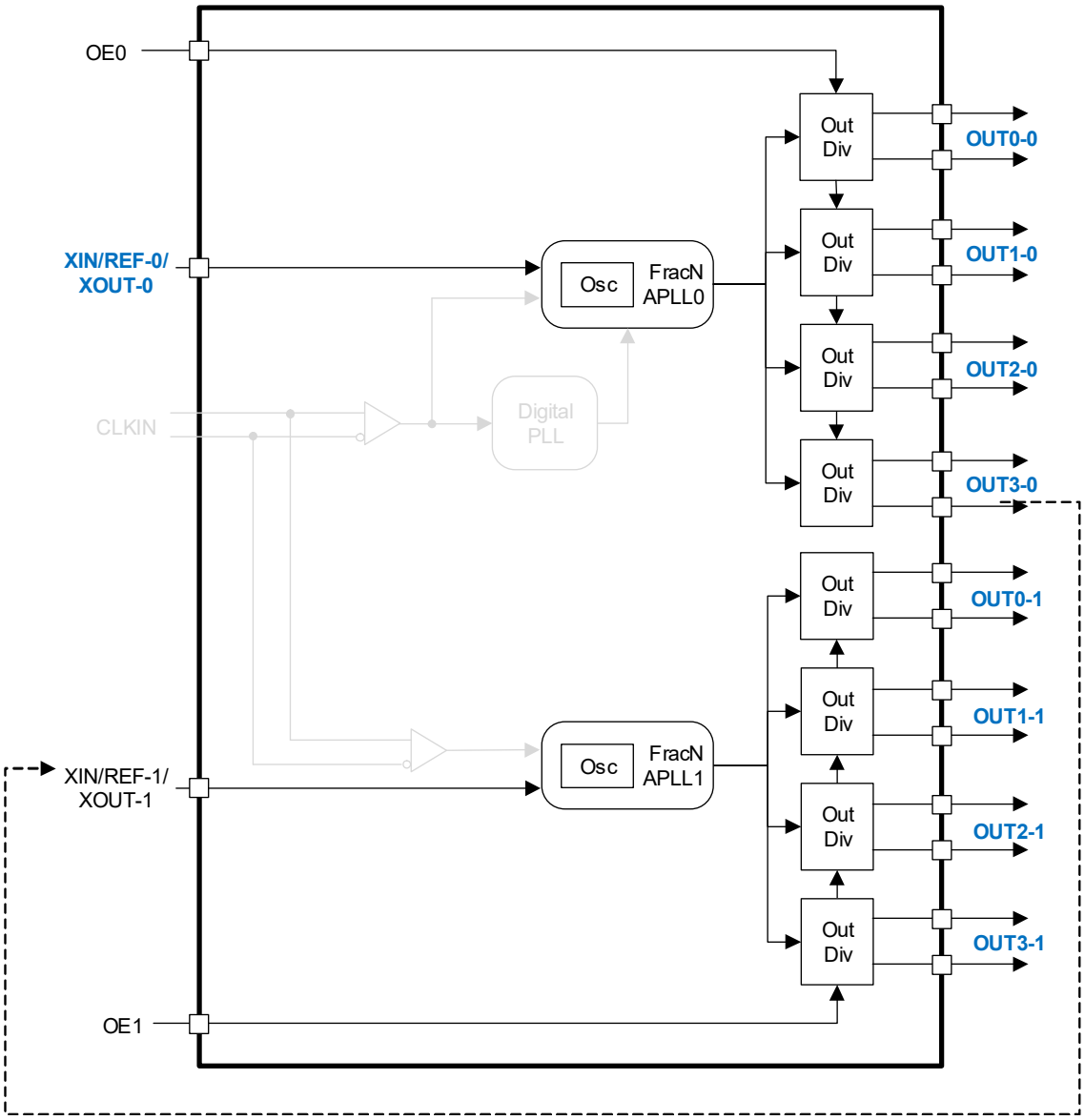


Figure 5. Clock Generator Mode with RC32508A when External Crystal fed into XIN/REF-0/XOUT-0

1.2 Jitter Attenuator or Synchronizer Mode

The RC32508A can be set in Jitter Attenuator or Synchronizer mode and locked to an external reference applied to CLKIN, nCLKIN pins by following the steps:

- APLL0 is locked to external crystal or oscillator that is applied to XIN/REF-0/XOUT-0.
- DPLL/DCO uses APLL0 to be synchronized and locked to external reference applied to CLKIN, nCLKIN
- APLL0 provides high frequency clock to each of four output dividers that is in turn fed to four clock outputs, OUT0-0, OUT1-0, OUT2-0, and OUT3-0.
- One of the four outputs from APLL0 is programmed as complementary LVCMOS outputs, and for example, OUT3-0-N is fed back into XIN/REF-1 pin and used as a reference to APLL1. APLL1 then provides a high-frequency clock that is either the same frequency as from APLL0 or a different frequency to each of four output dividers that is in term fed to four clock outputs, OUT0-1, OUT1-1, OUT2-1, and OUT3-1.
- As shown in Figure 6, up to two frequency domains can be obtained in this configuration and up to seven differential outputs and one LVCMOS output or 15 LVCMOS outputs can be obtained.

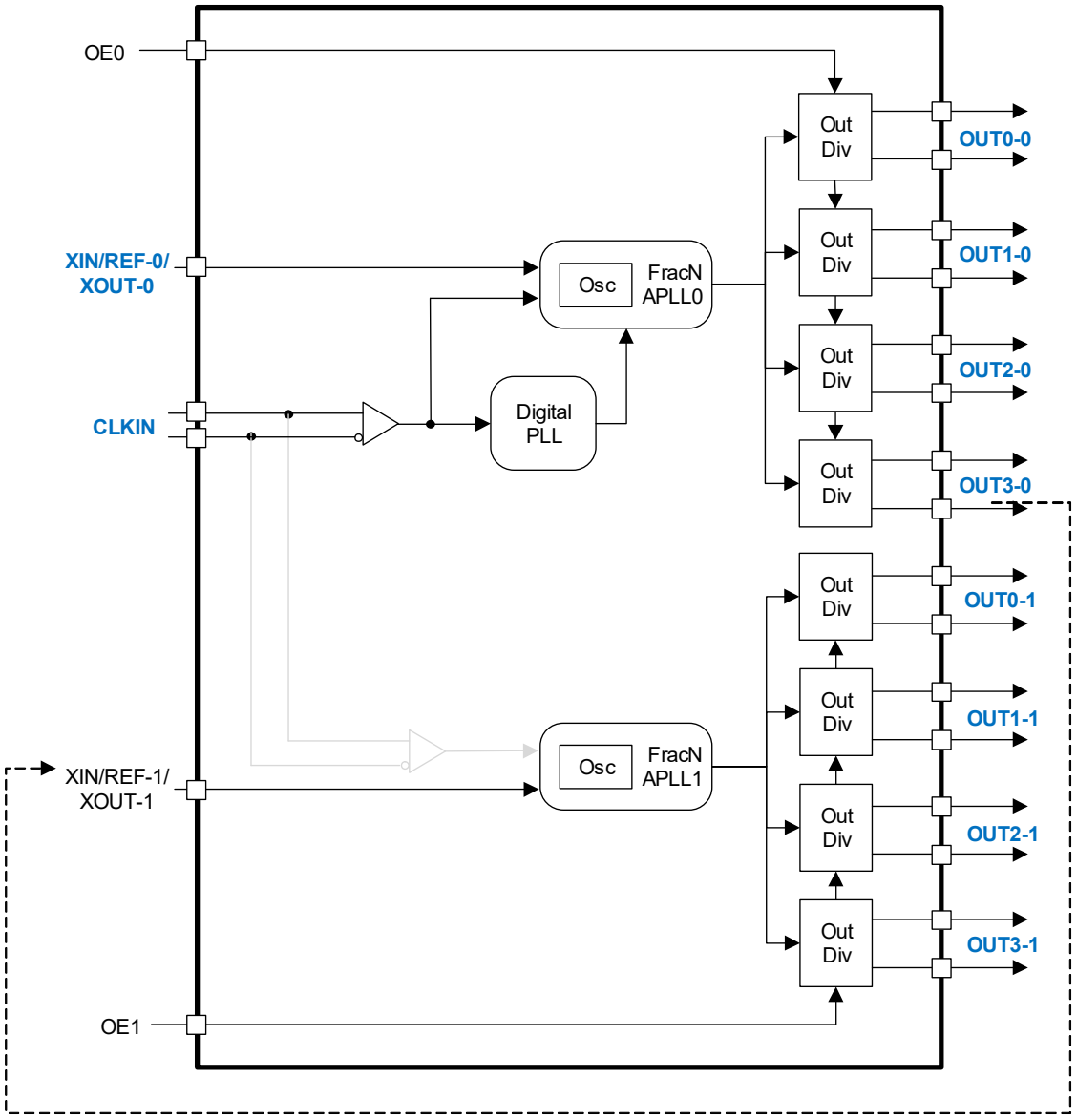


Figure 6. Jitter Attenuator or Synchronizer Mode with RC32508A when External Reference is Fed into CLKIN

1.3 Power-Up, Configuration, and Serial Interfaces

The RC32508A can be powered up and configured in two ways:

- From internal non-volatile memory using OTP user configurations (UserCfgs)
- From its slave serial interface – The RC32508A supports two slave serial interfaces: I2C and SPI. These interfaces share the same pins, so only one is available at a time. Additionally, all of the device logic pins are sampled at the rising edge of the internal master reset signal and some of them may be used in setting the initial configuration.

1.4 Input Clocks

The RC32508A supports one crystal/reference input that is used as a reference to each of the two analog PLLs (APLLs). One differential or two single-ended clock inputs that are used as a reference to the digital PLL (DPLL) and support hitless reference switching.

1.4.1 Crystal/Oscillator Input

The crystal input supports crystal frequencies of 25MHz to 80MHz with a recommended load capacitance of 8-12pF. The crystal input can being overdriven with differential or single-ended inputs with proper external terminations. The supported frequency range is 25MHz to 80MHz when doubler logic for APLL is enabled, and 50Mz to 160MHz when doubler logic for APLL is disabled. An available LOS monitor detects the loss of signal on crystal input.

1.4.2 Reference Clock Input

There is differential reference clock input that supports one differential or two single-ended CMOS logic levels without external terminations. If set to single-ended type, each of the differential inputs turn into two single-ended inputs. Internal biasing is available for AC-coupled applications. The two clock inputs can be left floating when unused. An available LOS monitor detects the loss of signal on reference clock inputs.

1.5 Input Monitors

1.5.1 DPLL Input Monitors

There are two types of reference clock monitors. The APLL input is monitored for Loss of Signal (LOS). While the DPLL clock inputs (CLKIN, nCLKIN) each have LOS, activity, and frequency monitoring.

- The LOS monitor detects missing edges over a window of several reference clock periods. For the best accuracy, it is recommended to program the window to be equal to at least eight times that of the measuring clock period.
- The frequency monitor can be configured to measure the reference over a nominal 5ms time window in order to achieve ~1ppm granularity.
- The frequency monitor can be configured to measure the reference over a nominal 0.4s time window in order to achieve ~12ppb granularity.

1.5.2 APLL Input Monitors

The APLL input is monitored for Loss of Signal (LOS). The LOS monitor detects missing edges over a window of several reference clock periods. For the best accuracy, it is recommended to program the window to be equal to at least eight times that of the measuring clock period.

1.6 APLL

Each of the two APLLs, APLL0 and APLL1, is a fractional LC-VCO based PLL with an operating range from 9.7GHz to 10.7GHz. The crystal or oscillator input clock is used to drive each of the APLLs, and can be frequency doubled for increased performance. The APLLs are temperature compensated for the utmost

frequency stability. The high-frequency clock output from each of the APLL is provided to each of the four output dividers that feed into two pairs of four outputs each (OUT0-0/1, OUT1-0/1, OUT2-0/1, OUT3-0/1).

1.6.1 APLL Feedback Divider

Each of the APLL Feedback dividers consists of two parts. The Multi-Modulus Divider (MMD) performs the actual division of the VCO frequency down to the nominal frequency needed to match the PFD input reference frequency (from frequency doubler). The MMD contains a number of integer divide ratios that are switched between under control of the Sigma-Delta Modulator (SDM) block. This allows a fractional divide ratio to be achieved while also providing noise shaping to minimize the spurs that switching would otherwise cause. The fractional portion of the divide ratio is a 27-bit integer representing the numerator of an M/N fraction. The denominator is fixed at 2^{27}. It is recommended that fractions close to 0, 1, or 1/2 be avoided for best phase noise performance.

1.6.2 APLL Lock Detector

The APLL lock detector is available for each APLL and each indicates whether the APLL is locked to a functioning crystal or reference input by monitoring the phase errors. Lock status is available on the LOCK-x or in the register map.

1.6.3 Direct DCO Control

When each of the APLLs is in Synthesizer mode, a frequency offset can be programmed. The frequency adjustment's LSB resolution is 2^{-40}, which translates to approximately 0.91ppt.

1.7 DPLL

To operate in Jitter Attenuator or Synchronizer mode, the APLL0 is used as a DCO and forms a fractional-N DPLL architecture that is locked to the chosen reference clock input. The fractional portion of the divide ratio is a 27-bit integer representing the numerator of an M/N fraction. The denominator is fixed at 2^{27}. It is recommended that fractions close to 0, 1, or 1/2 be avoided for best phase noise performance.

1.8 DPLL Reference Selection

The DPLL can lock to either the differential or one of the two single-ended input clocks. The reference selection can be either automatic or manual and when enabled, hitless switching results in negligible (< 100ps) output clock initial phase hit during reference switching or the DPLL exiting from holdover.

1.8.1 Manual Reference Selection

In manual mode, the selection is set in the register map.

1.8.2 Automatic Reference Selection

In automatic mode, the selection is based on clock quality statuses and priorities. The quality statuses are from clock monitors. If two clock inputs are programmed to the same priority, the one with lower index number takes precedence.

The automatic reference selection can either be revertive or non-revertive. In revertive mode, the reference clock that is qualified and of the highest priority is always selected. If a reference clock of higher priority than the currently selected one becomes qualified, the DPLL will switch to that reference clock. If a reference clock of equal or lower priority than the currently selected one becomes qualified, the DPLL will keep the current reference clock. In non-revertive mode, if there is a higher priority reference clock is coming back (from disqualified to qualified), the current selected reference clock remains selected unless it gets disqualified.

1.8.3 Hitless Reference Switching

If hitless switching is enabled, the output clock initial phase hit will be minimized (< 200ps) during reference switching or the DPLL exiting from holdover, while the input clock and output clock may no longer be aligned. If

hitless switching is disabled, the output clock phase change slope is determined by DPLL loop characteristics and phase slope limit.

Minimal initial phase hit of < 200ps can only be met during reference switching when the reference clocks are of same fractional frequency offset. If they are of different fractional frequency offset (up to 244ppm), the output clock phase will track to the new reference clock.

1.9 DPLL Operating Modes

The DPLL can operate in six different states: Free-run, Acquire, Normal, Holdover, Hitless-switch, and Write-frequency. The state transitions can be either manual or automatic.

1.9.1 Free-run

During power-on reset or VCO calibration or in synthesizer mode, the DPLL is in the free-run state. In this state, no reference clock is used and the output clocks track the APLL reference clock.

1.9.2 Acquire

When there is at least one qualified reference, the DPLL tracks the selected qualified reference at the acquisition bandwidth and damping factor settings. If the reference clock is disqualified and no other qualified reference clock is available, the DPLL transitions to either the free-run state or the holdover state. When lock-detector detects a lock, DPLL transitions to the normal state.

1.9.3 Normal

In the normal state, the DPLL tracks the selected reference clock with the normal locking bandwidth and damping factor settings.

If the selected reference clock is disqualified, state machine goes to either the holdover or the free-run state. At a reference switch, the state machine goes via the Holdover state to the Hitless Switch state or the Acquire state.

1.9.4 Holdover

In the holdover state, the DPLL output frequency is held at the instantaneous value or a value that is low-pass filtered and/or restored from the holdover history registers.

1.9.5 Hitless Switch

At a hitless reference switch or a hitless transition from the holdover state, the DPLL's TDC measures the phase offset between the (newly) selected reference clock and the feedback clock, both of which are averaged. This offset is stored in an internal phase offset register. As a result, the output clocks experience a minimal phase transient due to the reference switch or coming out of holdover. After the hitless switch procedure finishes, the state machine transitions to the Acquire state unless the reference clock fails.

1.9.6 Write Frequency

In the write-frequency mode the DPLL tracks an external stable oscillator like TCXO or OCXO. The DPLL feedback divider is controlled via I2C or SPI to operate the DPLL in DCO mode.

1.9.7 Manual Mode

The DPLL operation can be forced to the free-run, holdover, and write-frequency states.

1.10 DPLL Lock Detector

The DPLL lock detector declares lock when the phase from the phase detector remains within a programmable range for a programmable time interval both of which are set in the register map. This indicates that the DPLL is locked to the reference clock input. When the phase output from the phase detector is below the lock threshold for half of the programmed lock interval, the internal lock signal is asserted and the normal loop filter bandwidth and damping applied to the DPLL's loop filter instead of the acquire filter settings.

1.11 Output Dividers

The RC32508A provides eight integer output dividers (IOD), and each of the two APLLs feeds into four output dividers.

1.11.1 Integer Output Dividers

All eight IODs are identical and first four IODs derive the input clock from APLL0, and second four IODs derive the input clock from APLL1. Each IOD provides output frequencies from 1MHz to 1GHz. Changing IOD values results in an immediate change to the new frequency. Glitchless squelch and release of the IOD clock is supported.

1.12 Clock Outputs

The RC32508A supports up to 8 differential or 16 single-ended clock outputs or any combination of differential and single-ended clock outputs. Each differential clock output can be programmed as two single-ended clock outputs.

1.12.1 Output Buffer in Single-Ended Mode

When used as a single-ended output buffer, two copies of the same output clock are created with LVCMOS output levels. Each clock will have the same frequency, phase, voltage, and current characteristics.

1.12.2 Output Buffer in Differential Mode

When used as a differential output buffer, the user can control the output voltage swing (V_{OVS}) and common mode voltage (V_{CMR}) of the buffer that can be DC-coupled to HCSL input interface and AC-coupled to LVDS, LVPECL, or CML input interfaces.

1.12.3 Output Enable Control

During the power-up sequence, the clock output drivers are powered down (OUTx-0/1 and nOUTx-0/1 are tri-stated) until the power supplies have stabilized. Then the output drivers are powered up in the default disabled state (OUTx-0/1 and nOUTx-0/1 are both held low).

After the OTP configuration load completes, the clock output drivers can be held disabled until the APLL and/or DPLL locks:

- Clock output drivers are disabled until APLL lock asserts
- Clock output drivers are disabled until DPLL lock asserts
- Clock output drivers are enabled immediately

After startup, the clock output drivers are then user-controllable using output enable control.

1.13 OTP

The RC32508A supports four user-definable, non-volatile start-up configurations stored in an internal OTP (one-time programmable) memory that covers the blocks related to DPLL, APLL0, four output dividers feeding OUT0-0, OUT1-0, OUT2-0, OUT3-0. An additional four user-definable non-volatile start-up configurations stored in an internal OTP memory that covers the blocks related to APLL1, four output dividers feeding OUT0-1, OUT1-1, OUT2-1, OUT3-1. Each configuration can store values for all write-able configuration registers. The configuration for DPLL, APLL0 and the four outputs fed by APLL0 is selected by the values of LOCK-0, OE_nCS-0, and latched at power-up. The configuration for APLL1 and the four outputs fed by APLL1 is selected by the values of LOCK-1, OE_nCS-1 and latched at power-up. The serial interfaces are inactive until all register values specified in the selected configuration are written. The OTP contents can be locked to prevent further programming. The RC32508A supports OTP read with a $V_{DDD0/1}$ supply voltage of 1.8V.

2. Pin Assignments

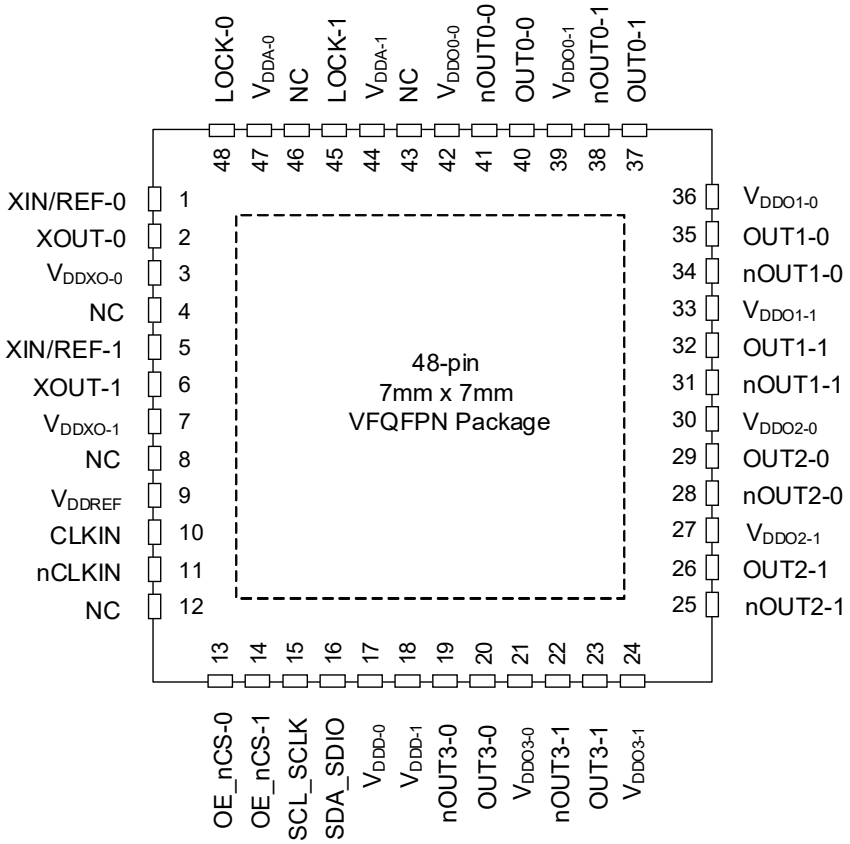


Figure 7. Pin Assignments

3. Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type		Description
1	XIN/REF-0	I		Crystal Input for APLL0. The interface can be overdriven with an oscillator input. If CLKIN and nCLKIN are used as the reference input to APLL0 then this pin should be left unconnected.
2	XOUT-0	O		Crystal Output for APLL0. This pin should be connected to a crystal. If an oscillator is connected to XIN/REF-0 then this pin must be left unconnected.
3	V_{DDXO-0}	Power		Oscillator supply for APLL0. This pin should be connected to 1.8V supply rail. XIN/REF-0 and XOUT-0 are referenced to this voltage supply.
4	NC	NA		No connect.
5	XIN/REF-1	I		Crystal Input for APLL1. The interface can be overdriven with an oscillator input. If CLKIN and nCLKIN are used as the reference input to APLL1 then this pin should be left unconnected.
6	XOUT-1	O		Crystal Output for APLL1. This pin should be connected to a crystal. If an oscillator is connected to XIN/REF-1 then this pin must be left unconnected.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type		Description
7	V_{DDXO-1}	Power		Oscillator supply for APLL1. This pin should be connected to 1.8V supply rail. XIN/REF-1 and XOUT-1 are referenced to this voltage supply.
8	NC	NA		No connect.
9	V_{DDREF}	Power		Reference input supply. This pin should be connected to 1.8V supply rail. CLKIN and nCLKIN are referenced to this voltage supply.
10	CLKIN	I		Non-inverting differential reference clock input/CMOS single-ended reference clock input. Input buffer should be disabled if unused. When in single-ended operation, the input supports the termination of a single leg of an LVDS clock (no additional external termination).
11	nCLKIN	I		Inverting differential reference clock input/CMOS single-ended reference clock input.
12	NC	NA		No connect.
13	OE_nCS-0	I	Optional Pull-up/ Pull-down	I^2C Mode: Output Enable signal for clock outputs from APLL0. Polarity, pull-up enable, and pull-down enable can be programmed. SPI Mode: Chip Select, active low for programming APLL0 and DPLL blocks.
14	OE_nCS-1	I	Optional Pull-up/ Pull-down	I^2C Mode: Output Enable signal for clock outputs from APLL1. Polarity, pull-up enable, and pull-down enable can be programmed. SPI Mode: Chip Select, active low for programming APLL1 blocks.
15	SCL_SCLK	I	Optional Pull-up	I^2C Mode: I^2C interface bi-directional clock. SPI Mode: Serial Clock.
16	SDA_SDIO	I/O	Optional Pull-up	I^2C Mode: I^2C interface bi-directional data in open-drain mode. SPI Mode: Serial Data In and Out (3-wire)
17	V_{DDD-0}	Power		Core digital function supply for APLL0 and DPLL blocks. This pin should be connected to 1.8V supply rail. OE_nCS-0, SCL_SCLK, and SDA_SDIO are referenced to this voltage.
18	V_{DDD-1}	Power		Core digital function supply for APLL1 blocks. This pin should be connected to 1.8V supply rail. OE_nCS-1, SCL_SCLK, and SDA_SDIO are referenced to this voltage.
19	nOUT3-0	O		Output Clock 3 negative from APLL0.
20	OUT3-0	O		Output Clock 3 positive from APLL0.
21	V_{DDO3-0}	Power		Supply voltage for output pair OUT3-0 and nOUT3-0. This pin should be connected to 1.8V supply rail. This pin can be left unconnected if clock output 3 from APLL0 is unused and outputs are programmed to be powered down.
22	nOUT3-1	O		Output Clock 3 negative from APLL1.
23	OUT3-1	O		Output Clock 3 positive from APLL1.
24	V_{DDO3-1}	Power		Supply voltage for output pair OUT3-1 and nOUT3-1. This pin should be connected to 1.8V supply rail. This pin can be left unconnected if clock output 3 from APLL1 is unused and outputs are programmed to be powered down.
25	nOUT2-1	O		Output Clock 2 negative from APLL1.
26	OUT2-1	O		Output Clock 2 positive from APLL1.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type		Description
27	V_{DDO2-1}	Power		Supply voltage for output pair OUT2-1 and nOUT2-1. This pin should be connected to 1.8V supply rail. This pin can be left unconnected if clock output 2 from APLL1 is unused and outputs are programmed to be powered down.
28	nOUT2-0	O		Output Clock 2 negative from APLL0.
29	OUT2-0	O		Output Clock 2 positive from APLL0.
30	V_{DDO2-0}	Power		Supply voltage for output pair OUT2-0 and nOUT2-0. This pin should be connected to 1.8V supply rail. This pin can be left unconnected if clock output 2 from APLL0 is unused and outputs are programmed to be powered down.
31	nOUT1-1	O		Output Clock 1 negative from APLL1.
32	OUT1-1	O		Output Clock 1 positive from APLL1.
33	V_{DDO1-1}	Power		Supply voltage for output pair OUT1-1 and nOUT1-1. This pin should be connected to 1.8V supply rail. This pin can be left unconnected if clock output 1 from APLL1 is unused and outputs are programmed to be powered down.
34	nOUT1-0	O		Output Clock 1 negative from APLL0.
35	OUT1-0	O		Output Clock 1 positive from APLL0.
36	V_{DDO1-0}	Power		Supply voltage for output pair OUT1-0 and nOUT1-0. This pin should be connected to 1.8V supply rail. This pin can be left unconnected if clock output 1 from APLL0 is unused and outputs are programmed to be powered down.
37	OUT0-1	O		Output Clock 0 positive from APLL1.
38	nOUT0-1	O		Output Clock 0 negative from APLL1.
39	V_{DDO0-1}	Power		Supply voltage for output pair OUT0-1 and nOUT0-1. This pin should be connected to 1.8V supply rail. This pin can be left unconnected if clock output 0 from APLL1 is unused and outputs are programmed to be powered down.
40	OUT0-0	O		Output Clock 0 positive from APLL0.
41	nOUT0-0	O		Output Clock 0 negative from APLL0.
42	V_{DDO0-0}	Power		Supply voltage for output pair OUT0-0 and nOUT0-0. This pin should be connected to 1.8V supply rail. This pin can be left unconnected if clock output 0 from APLL0 is unused and outputs are programmed to be powered down.
43	NC	NA		No connect.
44	V_{DDA-1}	Power		Analog function supply for core analog functions of APLL1. This pin should be connected to 1.8V supply rail. LOCK-1 is referenced to this voltage.
45	LOCK-1	O	See description	APLL1 lock status or other status, including polarity, pull-up enable and pull-down enable, can be programmed.
46	NC	NA		No connect.
47	V_{DDA-0}	Power		Analog function supply for core analog functions of DPLL and APLL0. This pin should be connected to 1.8V supply rail. LOCK-0 is referenced to this voltage.

Table 1. Pin Descriptions (Cont.)

Number	Name	Type		Description
48	LOCK-0	O	See description	DPLL/APLL0 lock status or other status, including polarity, pull-up enable and pull-down enable, can be programmed.
EPAD	V_{SS}	Power		Negative supply voltage. EPAD must be connected before any positive supply voltage is applied.

Table 2. Pin Characteristics

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Unit
C_{IN}	Input Capacitance	CLKIN		-	4	-	pF
		nCLKIN		-	4	-	pF
		XIN/REF-0, XIN/REF-1		-	4	-	pF
		OE_nCS-0, OE_nCS-1		-	4	-	pF
		SCL_SCLK		-	8	-	pF
		SDA_SDIO		-	8	-	pF
R_{PULLUP}	Input Pull-Up Resistor	OE_nCS-0, OE_nCS-1		51	54	57	kΩ
		SCL_SCLK		51	54	57	kΩ
		SDA_SDIO		51	54	57	kΩ
	Output Pull-Up Resistor	LOCK-0, LOCK-1		51	54	57	kΩ
$R_{PULLDOWN}$	Input Pull-Down Resistor	CLKIN	en_HCSL = 1	44	50	57	kΩ
		nCLKIN		44	50	57	kΩ
		OE_nCS0, OE_nCS1		51	54	57	kΩ
	Output Pull-Down Resistor	LOCK-0, LOCK-1		51	54	57	kΩ
R_{OUT}	Output Impedance	LOCK-0, LOCK-1	V_{DDA-0}, V_{DDA-1} = 1.89V	30	43	70	Ω
		SDA_SDOIO	V_{DDD-0}, V_{DDD-1} = 1.89V	48	49	50	Ω

4. Specifications

4.1 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RC32508A at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions can affect device reliability.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Test Condition	Minimum	Maximum	Unit
V_{DD33}	3.3V power supplies	V_{DDD-0}, V_{DDD-1}	-0.5	3.63	V
V_{DD18}	1.8V power supplies	V_{DDREF}, V_{DDXO-0}, V_{DDXO-1}, V_{DDA-0}, V_{DDA-1}, V_{DDO3-0}, V_{DDO3-1}, V_{DDO2-0}, V_{DDO2-1}, V_{DDO1-0}, V_{DDO1-1}, V_{DDO0-0}, V_{DDO0-1}	-0.5	1.98	V
V_{IN}	Voltage on any input	CLKIN, nCLKIN	0	1.98	V
		XIN/REF-0, XIN/REF-1 [1]	0	2.75	V
		All other inputs	-0.5	3.63	V
I_{IN}	Differential Input Current	CLKIN, nCLKIN	-	±50	mA
I_O	Output Current - Continuous	OUT0-0/1-0/2-0/3-0, OUT0-1/1-1/2-1/3-1	-	30	mA
		LOCK-0, LOCK-1, SDA_SDIO	-	25	mA
	Output Current - Surge	OUT0-0/1-0/2-0/3-0, OUT0-1/1-1/2-1/3-1	-	60	mA
		LOCK-0, LOCK-1, SDA_SDIO	-	50	mA
T_{JMAX}	Maximum Junction Temperature		-	150	°C
T_S	Storage temperature		-65	150	°C
-	ESD - Human Body Model		-	2000	V
-	ESD - Charged Device Model		-	500	V

1. This limit only applies to the XIN/REF-0 and XIN/REF-1 inputs when being overdriven by an external signal. No limit is implied when this is connected directly to a crystal.

4.2 Recommended Operating Conditions

Table 4. Recommended Operating Conditions [1][2]

Symbol	Parameter	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction temperature	-	-	125	°C
T_A	Ambient air temperature	-40	-	85	°C
V_{DDREF}	Supply Voltage for Input Clock Buffers and Dividers	1.71	1.8	1.89	V
V_{DDXO-0}, V_{DDXO-1}	Supply Voltage for Crystal Oscillators to APLL0 (V_{DDXO-0}) and APLL1 (V_{DDXO-1})	1.71	1.8	1.89	V
V_{DDA-0}, V_{DDA-1}	Supply Voltage for Analog blocks of DPLL/APLL0 (V_{DDA-0}) and APLL1(V_{DDA-1})	1.71	1.8	1.89	V
V_{DDD-0}, V_{DDD-1}	Supply Voltage for Digital Core of DPLL/APLL0 (V_{DDD-0}) and APLL1 (V_{DDD-1}) [3]	1.71	1.8/3.3	3.465	V

Table 4. Recommended Operating Conditions [1][2] (Cont.)

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{DDOx-0}, V_{DDOx-1}[4]	Supply Voltage for Output Clock Driver and Divider of APLL0 and APLL1 [5]	1.71	1.8	1.89	V
t_{PU}	Power Up Time for V_{DDx} - for all supply voltages to reach minimum specified voltage (power ramps must be monotonic) [6]	0.05	-	5	ms

1. It is the user's responsibility to ensure that device junction temperature remains below the maximum allowed.
2. All conditions in this table must be met to ensure device functionality.
3. Supports 1.8V ±5% or 3.3V ±5% operation, not a continuous range.
4. V_{DDOx} represents any of V_{DDO3-0}, V_{DDO3-1}, V_{DDO2-0}, V_{DDO2-1}, V_{DDO1-0}, V_{DDO1-1}, V_{DDO0-0}, V_{DDO0-1}.
5. Currents for the outputs are shown in Table 11 as appropriate for the mode the individual output is operating in.
6. This implies all supply rails must reach their minimum voltage within maximum T_{PU}.

4.3 Reference Clock Phase Jitter and Phase Noise

Table 5. Output Phase Jitter Characteristics [1][2]

Symbol	Parameter		Test Condition		Typical	Maximum	Unit
tjit(Φ)	Phase Jitter, RMS (Random)		10kHz to 20MHz 78.125MHz XTAL on XIN/REF-0 [3]; Synthesizer Mode, APLL0	125MHz	70	100	fs
				156.25MHz	67	100	fs
				312.5MHz	61	100	fs
tjit(Φ)	Phase Jitter, RMS (Random) [4]		10kHz to 20MHz 60MHz XTAL; JA Mode Locked to 156.25MHz CLKIN, DPLL/APLL0	156.25MHz	119	150	fs
				312.5MHz	107	150	fs
tjit(Φ)	Phase Jitter, RMS (Random) [5]		10kHz to 20MHz 78.125MHz Input [6]; Clock Generator Mode, APLL0/1	125MHz	72	100	fs
				156.25MHz	69	100	fs
				312.5MHz	63	100	fs
Φ_{SSB}(100k)	Single Sideband Phase Noise	100kHz	156.25MHz input, ck Generator Mode; APLL0/1 All outputs enabled at 156.25MHz		-146	-	dBc/Hz
Φ_{SSB}(1M)		1MHz			-154	-	dBc/Hz
Φ_{SSB}(10M)		10MHz			-165	-	dBc/Hz
Φ_{SSB}(30M)		≥30MHz			-165	-	dBc/Hz
$F_{isolation}$	Isolation between output channels		Measured between OUT3-1 at 156.25MHz and OUT3-0 at 125MHz		-67		dB

1. V_{DDXO-0}, V_{DDXO-1} = V_{DDA-0}, V_{DDA-1} = V_{DDOx-0},V_{DDOx-0} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.
2. Electrical parameters are ensured over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.
3. APLL0 at 10.625GHz to allow for outputting common ETH/FC frequencies.

4. Characterized using a Rohde and Schwarz SMA100A driving the CLKIN.
5. Characterized using a Rohde and Schwarz SMA100A overdriving the XTAL Interface.
6. Characterized using a Rohde and Schwarz SMA100A driving the CLKIN.

4.4 AC Electrical Characteristics

Table 6. Input Frequency Characteristics [1]

Symbol	Parameter		Test Condition	Minimum	Maximum	Unit
f_{XTAL}	Input Frequency for XIN/REF-0, XIN/REF-1		Using a Crystal [2] (see Table 7)	25	80	MHz
			Over-driving Crystal Input Doubler Logic Enabled	25	80	MHz
			Over-driving Crystal Input Doubler Logic Disabled	50	160	MHz
f_{CLKIN}	Input Frequency for CLKIN [3]		Clock Synthesizer Mode (Doubler Logic Disabled)	50	312.5	MHz
			Jitter Attenuator Mode - Differential Mode	1	800	MHz
			Jitter Attenuator Mode - Single-ended Mode	1	250	MHz
f_{SCLK}	Serial Port Clock SCL_CLK	I^2C Operation	Slave Mode	100	1200	kHz
		SPI Operation	Slave Mode	0.1	20	MHz

1. V_{DDXO-0}, V_{DDXO-1} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C
2. For crystal characteristics, see Table 7.
3. For proper device operation, the input frequency must be divided down to f_{TDC} or less (see Table 8).

Table 7. Crystal Characteristics [1]

Parameter	Test Condition	Minimum	Maximum	Unit
Mode of Oscillation		Fundamental		
Frequency		25	80	MHz
Equivalent Series Resistance (ESR) [2]	Crystal frequency ≤ 80MHz	-	80	Ω
Load Capacitance (C_L)		8	12	pF

1. V_{DDXO-0}, V_{DDXO-1} = 1.8V±5%, V_{SS} = 0V, T_A = -40°C to 85°C.
2. Measured ESR is always more than 2 × 80Ω.

Table 8. PLL Characteristics [1][2]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
f_{VCO-0}, f_{VCO-1}	Analog PLL0/1 VCO Operating Frequency		9.7	-	10.7	GHz
Δf_{OUT}	Output frequency tuning resolution	DCO Mode	$[2^{-40} \times 1e12] = 0.91$			ppt
$f_{PFD0/1}$	Analog PLL0/1 Phase/Frequency Detector (PFD) Operating Frequency	Integer VCO feedback	50	-	312.5	MHz
f_{TDC}	Digital Phase Detector (TDC) Operating Frequency		1	-	33	MHz

Table 8. PLL Characteristics [1][2] (Cont.)

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
f_{MON}	Reference Monitor Operating Frequency	CLKMON0/1		-	-	33	MHz
		CLKMON2		-	-	312.5	MHz
$t_{startup}$	Start-up Time [3]	Internal OTP Start-up	Synthesizer mode	-	7	10	ms

1. V_{DDXO-0}, V_{DDXO-1} = V_{DDD-0}, V_{DDD-1} = V_{DDA-0}, V_{DDA-1} = V_{DDOx-0}, V_{DDOx-1} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.
2. Electrical parameters are ensured over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.
3. Measured from when all power supplies have reached > 80% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked analog or digital PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected.

Table 9. Output Frequency Characteristics [1][2]

Symbol	Parameter		Test Condition		Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency	Differential Output			10	-	1000	MHz
		LVCMOS Output			10	-	180	MHz
t_{SK}	Output to Output Skew [3][4]	Differential [5]	Any two outputs between OUTx-0		-	9	38	ps
			Any two outputs between OUTx-0 and OUTx-1			41	128	ps
		LVCMOS [6]	Any two outputs between OUTx-0		-	30	50	ps
			Any two outputs between OUTx-0 and OUTx-1		-	50	96	ps
Δt_{SK}	Temperature Variation [7] Output-Output		On OUTx-0, OUTx-1		-	-	1	ps/°C
t_{PD}	Input to Output Skew [8] Differential [5] WRT CLKIN [9]		Delay for SYNTH mode on OUTx-0, OUTx-1		0.73	1.14	1.55	ns
t_{PD}	Input to Output Skew [10] Differential [5] WRT CLKIN [11]		Delay for JA mode, integer DPLL feedback on OUTx-0		0.65	1.08	1.52	ns
			Delay for JA mode, fractional DPLL feedback on OUTx-0		0.72	1.09	1.47	ns
			Delay for SYNTH mode on OUTx-1		0.74	1.14	1.55	ns
Δt_{PD}	Input to Output Delay Variation Differential [5]		Any mode on OUTx-0, OUTx-1		-	-	255	ps
t_R / t_F	Output Rise and Fall Times 20% to 80%	Differential Output [12]	HCSL Mode		-	-	160	ps
			LVDS Mode		-	-	180	ps
		LVCMOS Output [13]	V_{DDOx} = 1.8V ±5%		-	-	800	ps

Table 9. Output Frequency Characteristics [1][2] (Cont.)

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
odc	Output Duty Cycle	Differential Output	$f_{OUT} \le f_{VCO}$ / N; N = 10, 12, …	48	50	52	%
			$f_{OUT} \le f_{VCO}$ / N; N = 39, 41, …	48	50	52	%
			$f_{OUT} \le f_{VCO}$ / N; N = 11, 13, …37	45	50	55	%
		LVCMOS	Any frequency	45	50	55	%
ΔF/F	Frequency Stability (Free-run)		Inclusive of initial tolerance	-100		100	PPM

1. V_{DDXO-0}, V_{DDXO-1} = V_{DDD-0}, V_{DDD-1} = V_{DDA-0}, V_{DDA-1} = V_{DDOx-0}, V_{DDOx-1} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.
2. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.
3. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
4. This parameter is defined in accordance with JEDEC Standard 65.
5. Measured at the differential cross points.
6. Measured at $V_{DDOx-0/1}$ / 2.
7. This parameter is measured across the full operating temperature range and the difference between the slowest and fastest numbers is the variation.
8. Defined as the time between the output rising edge and the input rising edge that caused it.
9. ClkIn was from Rhode and Schwarz SMA 100B Signal Generator.
10. Defined as the time between the output rising edge and the input rising edge that caused it.
11. ClkIn was from Rhode and Schwarz SMA 100B Signal Generator.
12. Measured with outputs terminated with 50Ω to GND.
13. Measured with outputs terminated with 50Ω to V_{DDOx} / 2.

Table 10. Power Supply Noise Rejection [1][2]

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit
PSNR	Power Supply Noise Rejection [3][4]	f_{NOISE} ≤ 1MHz	V_{DDOx-0}, V_{DDOx-1} = 1.8V [5]	-105	-94	-	dBc
			V_{DDXO-0}, V_{DDXO-1} = 1.8V	-95	-87	-	dBc
		f_{NOISE} ≤ 100kHz	V_{DDREF} = 1.8V	-95	-86	-	dBc
			V_{DDD-0}, V_{DDD-1} = 1.8V	-140	-114	-	dBc
		100kHz < f_{NOISE} ≤ 600kHz	V_{DDREF} = 1.8V	-140	-109	-	dBc
			V_{DDD-0}, V_{DDD-1} = 1.8V	-100	-96	-	dBc
		600kHz < f_{NOISE} ≤ 1MHz	V_{DDREF} = 1.8V	-155	-143	-	dBc
			V_{DDD-0}, V_{DDD-1} = 1.8V	-105	-99	-	dBc

1. V_{DDXO-0}, V_{DDXO-1} = V_{DDD-0}, V_{DDD-1} = V_{DDA-0}, V_{DDA-1} = V_{DDOx-0}, V_{DDOx-1} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.
2. Electrical parameters are ensured over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device meets specifications after thermal equilibrium has been reached under these conditions.
3. 50mV peak-to-peak sine-wave noise signal injected on indicated power supply pin(s).
4. Noise spur amplitude measured relative to 156.25MHz carrier.
5. Excluding V_{DDOx} of the output being measured.

4.5 DC Electrical Characteristics

Table 11. Power Supply DC Characteristics – Supply Current [1][2][3]

Symbol	Parameter	Test Condition		Current Consumption		Unit
				Typ	Max	
I_{DDREF}	Supply Current for V_{DDREF} [4]	1.8V LVCMOS input		16	30	mA
		HCSL input		20		mA
		LVDS input		22		mA
		AC-coupled differential input		11		mA
I_{DDXO-0}, I_{DDXO-1}	Supply Current for each supply: V_{DDXO-0}, V_{DDXO-1}	V_{DDXO-0}, V_{DDXO-1} = 1.89V		5.5	10	mA
I_{DDA-0}, I_{DDA-1}	Supply Current for each supply: V_{DDA-0}, V_{DDA-1}	V_{DDA-0}, V_{DDA-1} = 1.89V		129	150	mA
I_{DDDD-0}, I_{DDD-1}	Supply Current for each supply: V_{DDD-0}, V_{DDD-1}	V_{DDD-0}, V_{DDD-1} = 1.89V		25	30	mA
		V_{DDD-0}, V_{DDD-1} = 3.465V		26		mA
I_{DDOx-0}, I_{DDOx-1} [5]	Supply Current for each supply: V_{DDOx-0}, V_{DDOx-1} [6][7]	HCSL Mode	SWING = 200mV	31	50	mA
			SWING = 250mV	32		mA
			SWING = 300mV	33		mA
			SWING = 350mV	34		mA
			SWING = 400mV	35		mA
			SWING = 450mV	36		mA
			SWING = 500mV	37		mA
			SWING = 550mV	39		mA
			SWING = 600mV	40		mA
			SWING = 650mV	41		mA
			SWING = 700mV	42		mA
			SWING = 750mV	43		mA
			SWING = 800mV	44		mA
			SWING = 850mV	45		mA
			SWING = 875mV	45		mA
			SWING = 900mV	46		mA
		LVDS Mode	AMP = 350mV	30	40	mA
			AMP = 400mV	31		mA
		Output Disabled		28	50	mA
		Output Hi-Z		26	30	mA
		LVCMOS Mode	In phase	34	45	mA
			Opposite phase	34		mA
			nOUTx Disabled	31	40	mA
			OUTx Disabled	31		mA

1. Output current consumption is not affected by any of the core device power supply voltage levels.
2. Internal dynamic switching current at maximum f_{OUT} is included.

3. V_{SS} = 0V, T_A = -40°C to 85°C.
4. Voltage of the input signal must be appropriate for the V_{DDREF} voltage supply level when using a DC-coupled connection.
5. $I_{DDOx-0/1}$ denotes the current consumed by each $V_{DDOx-0/1}$ supply.
6. $V_{DDOx-0/1}$ = 1.89V.
7. Measured with outputs unloaded.

Table 12. LVCMOS Status and Control Signal DC Characteristics [1][2]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage	V_{DDD-x} = 3.3V ±5%	2	-	V_{DDD-x} + 0.3	V
		V_{DDD-x} = 1.8V ±5%	0.65 × V_{DDD-x}	-	V_{DDD-x} + 0.3	
V_{IL}	Input Low Voltage	V_{DDD-x} = 3.3V ±5%	-0.3	-	0.8	V
		V_{DDD-x} = 1.8V ±5%	-0.3	-	0.35 × V_{DDD-x}	
I_{IH}	Input High Current	V_{IN} = V_{DDD-x} = V_{DDD-x} (max)	-	-	5	µA
I_{IL}	Input Low Current	V_{IN} = 0V, V_{DDD-x} = V_{DDD-x} (max)	-75	-	-	µA
V_{OH}	Output High Voltage	V_{DDD-x} = 3.3V ±5% or 1.8V ±5% I_{OH} = -100µA	V_{DDD-x} - 0.2	-	-	V
		(LOCK-x Signal Only) V_{DDA-x} = 1.8V ±5% I_{OH} = -100µA	V_{DDA-x} - 0.2	-	-	V
V_{OL}	Output Low Voltage	V_{DDD-x} = 3.3V ±5% or 1.8V ±5% V_{DDA-x} = 1.8V ±5% I_{OL} = 100µA	-	-	0.2	V

1. 3.3V characteristics in accordance with JESD8C-01, 1.8V characteristics in accordance with JESD8-7A.
2. V_{SS} = 0V, T_A = -40°C to 85°C.

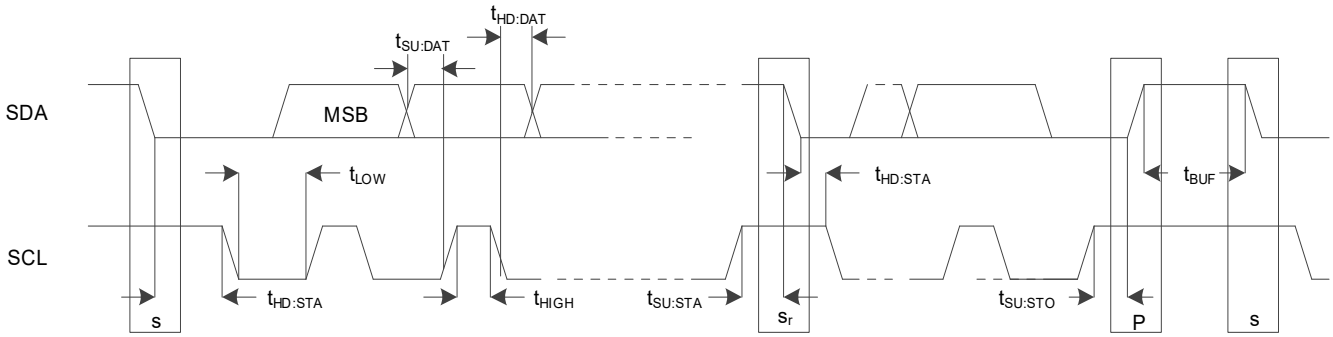


Figure 8. I²C Slave Timing Diagram

Table 13. I²C Slave Timing [1]

Parameter	Description	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
f_{SCL}	SCL clock frequency	0	100	0	400	0	1000	kHz
$t_{HD:STA}$	Hold time (repeated) START condition	4000	-	600	-	260	-	ns
t_{LOW}	LOW period of the SCL clock	4700	-	1300	-	500	-	ns
t_{HIGH}	HIGH period of the SCL clock	4000	-	600	-	260	-	ns
$t_{SU:STA}$	Set-up time for a repeated START condition	4700	-	600	-	260	-	ns
$t_{HD:DAT}$	Data hold time[2]	0[3]	[4]	0[3]	[4]	0	-	ns
$t_{SU:DAT}$	Data set-up time	250	-	100[5]	-	50	-	ns
$t_{SU:STO}$	Set-up time for STOP condition	4000	-	600	-	260	-	ns
t_{BUF}	Bus free time between a STOP and START condition	4700	-	1300	-	500	-	ns

1. All values referred to V_{IH} (minimum) and V_{IL} (maximum) levels (see Table 12).
2. $t_{HD:DAT}$ is the data hold time that is measured from the falling edge of SCL, and applies to data in transmission and the acknowledge.
3. A device must internally provide a hold time of at least 300ns for the SDA signal (with respect to the V_{IH} (min) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
4. The maximum $t_{HD:DAT}$ could be 3.45µs and 0.9µs for Standard mode and Fast mode, but must be less than the maximum of $t_{VD:DAT}$ or $t_{VD:ACK}$ by a transition time. This maximum must only be met if the device does not stretch the LOW period (t_{LOW}) of the SCL signal. If the clock stretches the SCL, the data must be valid by the set-up time before it releases the clock.
5. A Fast mode I²C-bus device can be used in a Standard mode I²C-bus system, but the requirement $t_{SU:DAT}$ 250ns must then be met. This is automatically the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_r(max) + $t_{SU:DAT}$ = 1000 + 250 = 1250ns (according to the Standard mode I²C-bus specification) before the SCL line is released. Also the acknowledge timing must meet this set-up time.

Table 14. I²C Bus Characteristics

Parameter	Description	Standard Mode		Fast Mode		Fast Mode Plus		Unit
		Minimum	Maximum	Minimum	Maximum	Minimum	Maximum	
t_r	Rise time of both SDA and SCL signals	-	1000	20	300	-	120	ns
t_f	Fall time of both SDA and SCL signals [1][2][3][4]	-	300	20 × (V_{DDD-x} / 5.5 V)	300	20 × (V_{DDD-x} / 5.5 V)[5]	120 [4]	ns
C_D	Capacitive load for device on bus	-	5	-	5	-	5	pF

1. A device must internally provide a hold time of at least 300ns for the SDA signal (with respect to the V_{IH} (minimum) of the SCL signal) to bridge the undefined region of the falling edge of SCL.
2. If mixed with Hs-mode devices, faster fall times are allowed.
3. The maximum t_f for the SDA and SCL bus lines is specified at 300ns. The maximum fall time for the SDA output stage t_f is specified at 250ns, allowing series protection resistors to be connected in between the SDA and the SCL pins and the SDA/SCL bus lines without exceeding the maximum specified t_f.
4. In Fast Mode Plus, fall time is specified the same for both output stage and bus timing. If series resistors are used, designers should allow for this when considering bus timing.
5. Necessary to be backwards compatible to Fast mode.

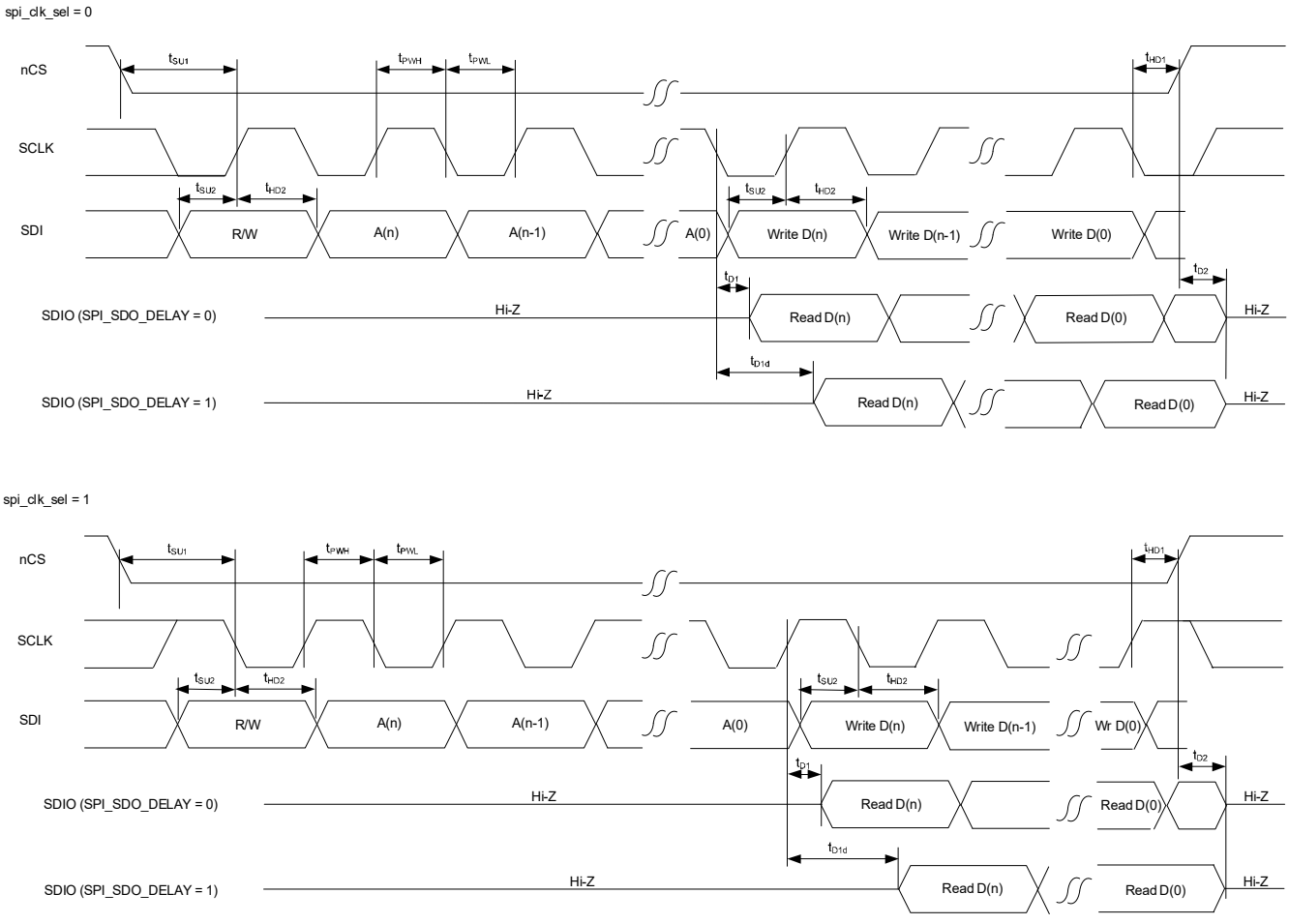


Figure 9. SPI Timing Diagram

Table 15. SPI Slave Timing

Parameter	Description	Minimum	Typical	Maximum	Unit
f_{MAX}	Maximum operating frequency	-	-	20	MHz
t_{PWH}	SCLK Pulse Width High	25	-	-	ns
t_{PWL}	SCLK Pulse Width Low	25	-	-	ns
t_{SU1}	nCS Setup Time to SCLK rising or falling edge	10	-	-	ns
t_{HD1}	nCS Hold Time from SCLK rising or falling edge	10	-	-	ns
t_{SU2}	SDIO Setup Time to SCLK rising or falling edge	10	-	-	ns
t_{HD2}	SDIO Hold Time from SCLK rising or falling edge	10	-	-	ns
t_{D1}	Read Data Valid Time from SCLK rising or falling edge with no data delay added	4	5.6	-	ns
t_{D1d}	Read Data Valid Time from SCLK rising or falling edge including half period of SCLK delay added to data timing [1]	t_{D1} + half SCLK period	-	-	ns
t_{D2}	SDIO Read Data Hi-Z Time from CS High [2]	-	10	-	ns

1. Adding the extra half period of delay is a register programming option to emulate read data being clocked out on the opposite edge of the SCLK to the write data.
2. This is the time until the RC32508A releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

Table 16. Differential Clock Input DC Characteristics [1]

Symbol	Parameter		Test Condition	Minimum	Typical	Maximum	Unit
I_{IH}	Input High Current	CLKIN	V_{IN} = V_{DDREF} =V_{DDREF} (max)	-	-	100	µA
		nCLKIN		-	-	100	µA
I_{IL}	Input Low Current	CLKIN	V_{IN} = 0V	-50	-	-	µA
		nCLKIN		-50	-	-	µA
$V_{I(PP)}$	Peak-to-Peak Voltage [2][3][4]			0.15	-	1.2	V
V_{CMR}	Common Mode Input Voltage [2][4][5][6]		PMOS input buffer (HCSL)	VI(PP) / 2	0.35	V_{DDREF} - 1.2	V
			NMOS input buffer (LVDS)	0.7	1.2	V_{DDREF} - (VI(PP) / 2)	V

1. V_{DDREF} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.
2. V^{IL} should not be less than -0.3V.
3. V_{PP} is the single-ended amplitude of the input signal. The differential specification is 2*V_{PP}.
4. V_{DDREF} = 1.8V ±5%. Voltage of the input signal must be appropriate for the V_{DDREF} voltage supply level when using a DC-coupled connection.
5. Common-mode voltage is defined as the cross-point.
6. Voltage of the input signal must be appropriate for the V_{DDREF} voltage supply level when using a DC-coupled connection. For example, when supplying an LVDS input signal that is referenced to a 2.5V supply at its source, the V_{DDREF} supply must also be 2.5V nominal voltage.

Table 17. LVCMOS Clock Input DC Characteristics [1][2][3]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage	V_{DDREF} = 1.8V ±5%	0.65 × V_{DDREF}	-	V_{DDREF} + 0.3	V
V_{IL}	Input Low Voltage	V_{DDREF} = 1.8V ±5%	-0.3	-	0.35 × V_{DDREF}	V
I_{IH}	Input High Current	VIN = V_{DDREF} = V_{DDREF} (max)	-	-	150	µA
I_{IL}	Input Low Current	V_{IN} = 0V	-150	-	-	µA

1. 1.8V characteristics in accordance with JESD8-7A.
2. V_{SS} = 0V, T_A = -40°C to 85°C.
3. Input specifications see both CLKIN and nCLKIN.

Table 18. Differential Clock Output DC Characteristics [1][2][3]

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit
$V_{OUTx-0/1}$	Absolute Voltage on HCSL output	[4]		-125 [5]	-	1150 [6]	mV
V_{CROSS}	Absolute Voltage Output Crossing	HCSL Mode [7]		350	-	500	mV
ΔV_{CROSS}	Total Variation on HCSL output crossing over all edges [8]	[9]		-	30	100	mV
V_{OVS} [10]	Output Voltage Swing	HCSL Mode	SWING = 200mV	195	-	250	mV
			SWING = 250mV	245	-	315	mV
			SWING = 300mV	295	-	380	mV
			SWING = 350mV	345	-	450	mV
			SWING = 400mV	395	-	520	mV
			SWING = 450mV	445	-	585	mV
			SWING = 500mV	495	-	645	mV
			SWING = 550mV	545	-	725	mV
			SWING = 600mV	595	-	780	mV
			SWING = 650mV	645	-	820	mV
			SWING = 700mV	685	-	855	mV
			SWING = 750mV	725	-	880	mV
			SWING = 800mV	755	-	915	mV
			SWING = 850mV	785	-	960	mV
			SWING = 875mV	810	-	1005	mV
			SWING = 900mV	825	-	1045	mV
		LVDS Mode	AMP = 350mV	350	-	460	mV
			AMP = 400mV	365	-	500	mV

Table 18. Differential Clock Output DC Characteristics [1][2][3] (Cont.)

Symbol	Parameter	Test Condition		Minimum	Typical	Maximum	Unit
V_{CMR}	Output Common Mode Voltage	LVDS Mode [11]	CENTER = 700mV	650	-	750	mV
			CENTER = 800mV	750	-	850	mV
			CENTER = 900mV	800	-	950	mV
			CENTER = 1000mV	900	-	1050	mV

1. V_{DDOx-0}, V_{DDOx-1} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.
2. Terminated with 100Ω across OUTx-0/1 and nOUTx-0/1.
3. OUTx-0/1 refers to any of the output pairs OUT3-0, OUT3-1, OUT2-0, OUT2-1, OUT1-0, OUT1-1, OUT0-0, OUT0-1.
4. Measurement taken from single-ended waveform.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Defined as the maximum instantaneous voltage including overshoot.
7. Terminated with 50Ω to GND on each of OUTx-0/1 and nOUTx-0/1.
8. Defined as the total variation of all crossing voltages of rising OUTx-0/1 and falling nOUTx-0/1, This is the maximum allowed variance for any particular system.
9. Measured at crossing point where the instantaneous voltage value of the rising edge of Qx equals the falling edge of nQx.
10. V_{OVS} is the single-ended amplitude of the output signal. The differential specs is 2*V_{OVS}.
11. Terminated with 100Ω across OUTx-0/1 and nOUTx-0/1.

Table 19. LVCMOS Clock Output DC Characteristics [1][2][3]

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage	I_{DDOx} = ±100µA	V_{DDOx} - 0.2	-	-	V
V_{OL}	Output Low Voltage		-	-	0.2	V
Z_{OUT}	Output Impedance		41	51	67	Ω

1. V_{DDOx} = 1.8V ±5%, V_{SS} = 0V, T_A = -40°C to 85°C.
2. Applies to any of OUT3-0, OUT3-1, OUT2-0, OUT2-1, OUT1-0, OUT1-1, OUT0-0, OUT0-1.
3. Output voltages compliant with JESD8-7A, Normal Range.

5. Applications Information

5.1 Recommendations for Unused Input and Output Pins

5.1.1 Inputs

5.1.1.1 CLKx / nCLKx Input

For applications that do not require the use of the reference clock input, both CLK and nCLK should be left floating. If the CLK/nCLK input is connected but not used by the device, it is recommended that CLK and nCLK not be driven with active signals.

5.1.1.2 LVCMOS Control Pins

LVCMOS control pins have internal pull-ups; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

5.1.2 Outputs

5.1.2.1 LVCMOS Outputs

Any LVCMOS output can be left floating if unused. There should be no trace attached. The mode of the output buffer should be set to tri-stated to avoid any noise being generated.

5.1.2.2 Differential Outputs

All unused differential outputs can be left floating. Renesas recommends that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

5.1.3 Power Connections

The power connections of the RC32508A can be grouped as shown if all members of the groups are using the same voltage level:

- $V_{DDD-0/1}$
- $V_{DDA-0/1}$
- $V_{DDOx-0/1}$ (can share supplies if output frequencies are the same, otherwise keep separated to avoid spur coupling)
  - If all outputs OUTx-0/1/nOUTx-0/1 associated with any particular $V_{DDOx-0/1}$ pin are not used, the power pin can be left floating

5.2 Clock Input Interface

The RC32508A accepts both single-ended and differential inputs. For information on input terminations, see *Quick Guide - Output Terminations (AN-953)* located on the RC32508A product page.

If you have additional questions on input types not covered in the application discussion, or if you require information about register programming sequences for changing the differential inputs to accept LVCMOS inputs levels, see *Termination - AC Coupling Clock Receivers (AN-844)* or contact Renesas technical support.

5.3 Overdriving the XTAL Interface

The XIN/REF-0/1 input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XIN/REF-0/1 input is internally biased at 1V. The XOUT-0/1 pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/ns. For 1.8V LVCMOS, inputs can be DC-coupled into the device as shown in Figure 10. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise.

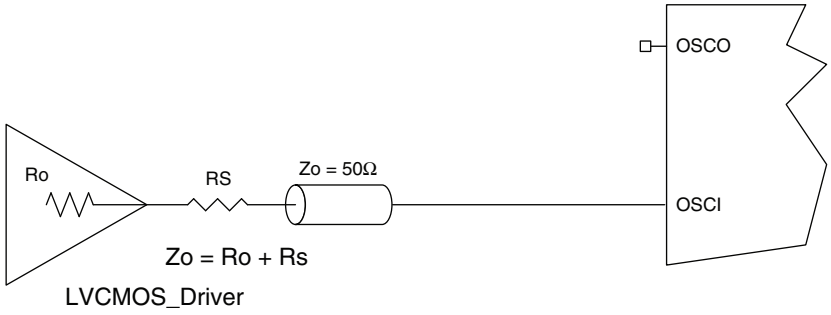


Figure 10. 1.8V LVCMOS Driver to XTAL Input Interface

Figure 11 shows an example of the interface diagram for a high-speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver.

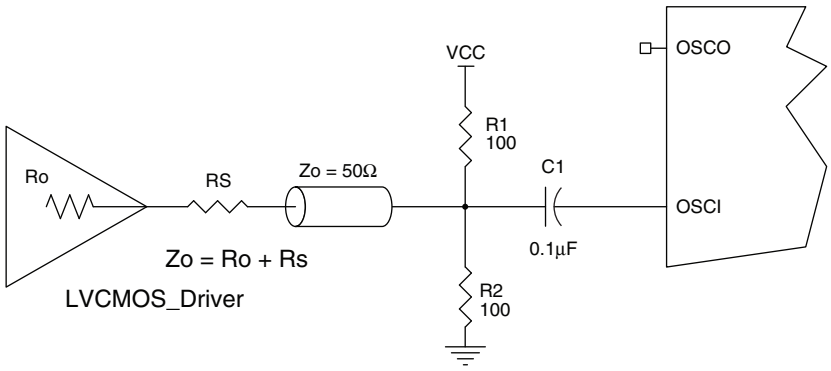


Figure 11. LVCMOS Driver to XTAL Input Interface

Figure 12 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components may not be used, they can be used for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

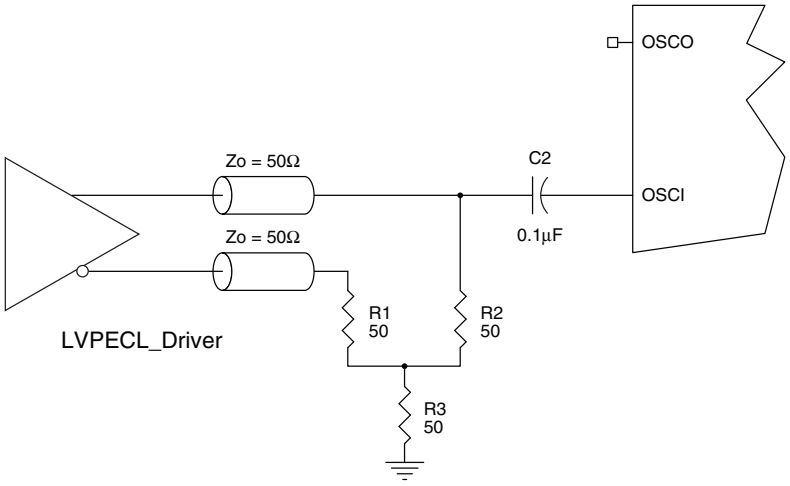


Figure 12. LVPECL Driver to XTAL Input Interface

5.4 Wiring the Differential Input to Accept Single-Ended Levels

For information, see the *Differential Input to Accept Single-ended Levels Application Note (AN-836)*.

5.5 Differential Output Termination

For all types of differential protocols, the same termination schemes are recommended (see Figure 13). These schemes are the same as normally used for an LVDS output type.

The recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_{Diff}) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. To avoid any transmission-line reflection issues, the components should be surface-mounted and must be placed as close to the receiver as possible.

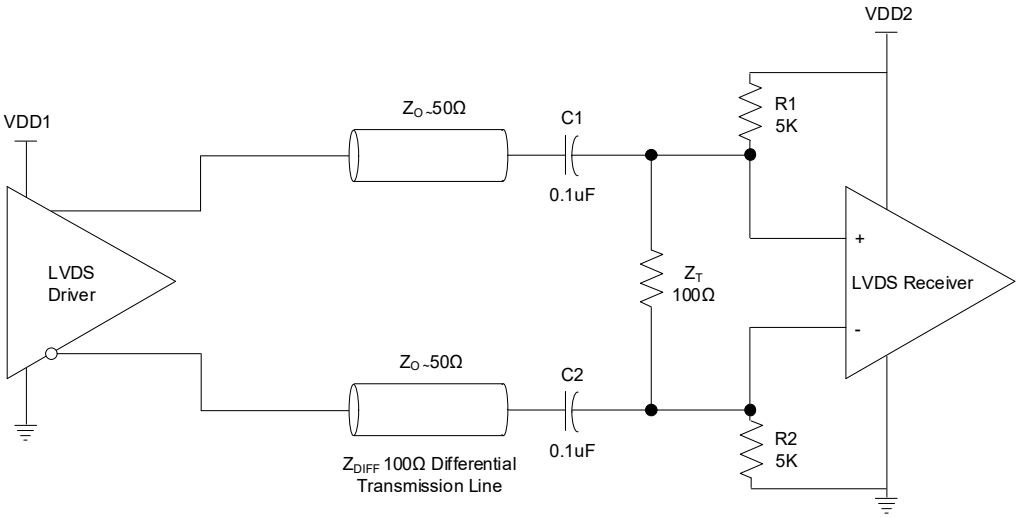


Figure 13. AC Coupled LVDS Termination

For alternate termination schemes, see “LVDS Termination” in *Quick Guide - Output Terminations (AN-953)* located on the device product page, or contact Renesas for support.

5.6 Power Considerations

For power and current consumption calculations, refer to Renesas’ Timing Commander tool.

6. Thermal Information

6.1 VFQFPN ePad Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 14. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

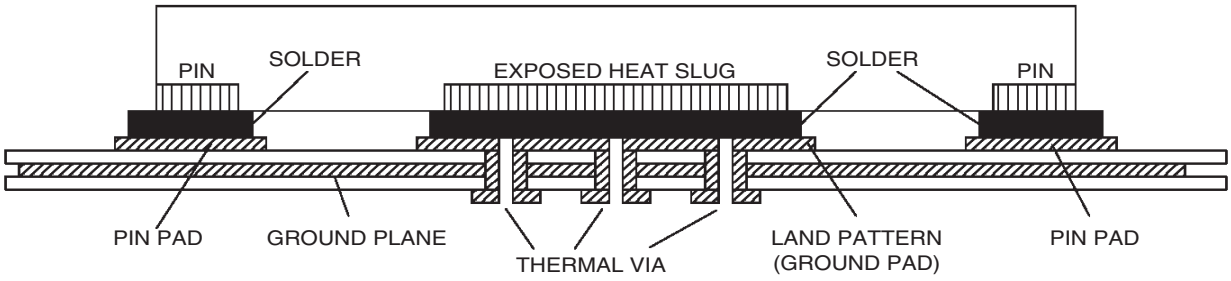


Figure 14. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to Scale)

6.2 Thermal Characteristics

Table 20. Thermal Characteristics

Symbol	Parameter	Value		Unit
		Top Die	Bottom Die	
θ_{JA}	Theta J_A. Junction to Ambient Air Thermal Coefficient; 0 m/s air flow [1][2]	49.6	33.5	°C/W
θ_{JB}	Theta J_B. Junction to ePad [1]	27.9	11.5	°C/W
θ_{JC}	Theta J_C. Junction to Device Case Thermal Coefficient [1]	17.6	17.1	°C/W
-	Moisture Sensitivity Rating (Per J-STD-020)	3	3	-

1. Multi-Layer PCB with two ground and two voltage planes.
2. Assumes ePad is connected to a ground plane using a grid of 9x9 thermal vias.

7. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

8. Marking Diagram

- Lines 2 and 3 are the part number
- Line 4:
  - “#” denotes the stepping number.
  - “YYWW” denotes the last two digits of the year and the work week the part was assembled.
  - “$” indicates the mark code.

9. Ordering Information

Part Number	Package	MSL Rating	Carrier Type	Temperature Range
RC32508AdddGNE#BB0[1]	7 × 7× 0.9 mm, 48-VFQFPN	3	Tray	-40° to +85°C
RC32508AdddGNE#KB0			Tape and Reel, Pin 1 Orientation: EIA-481-D	

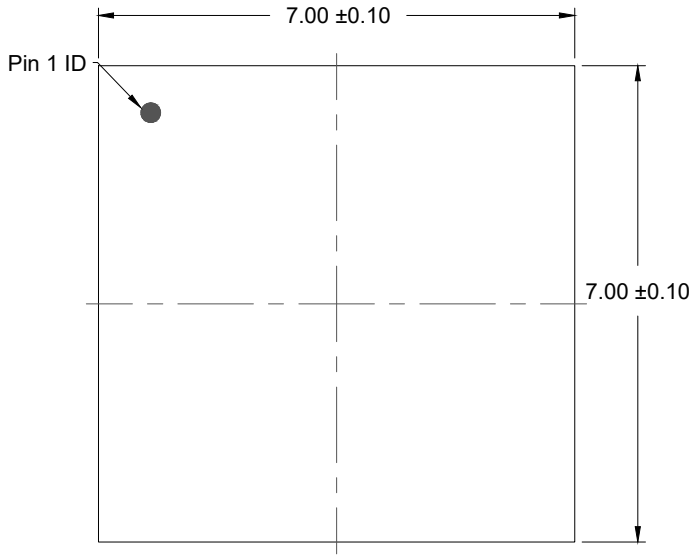
1. Replace “ddd” with the desired pre-programmed configuration code provided by Renesas in response to a custom configuration request or use “000” for unprogrammed parts.

10. Revision History

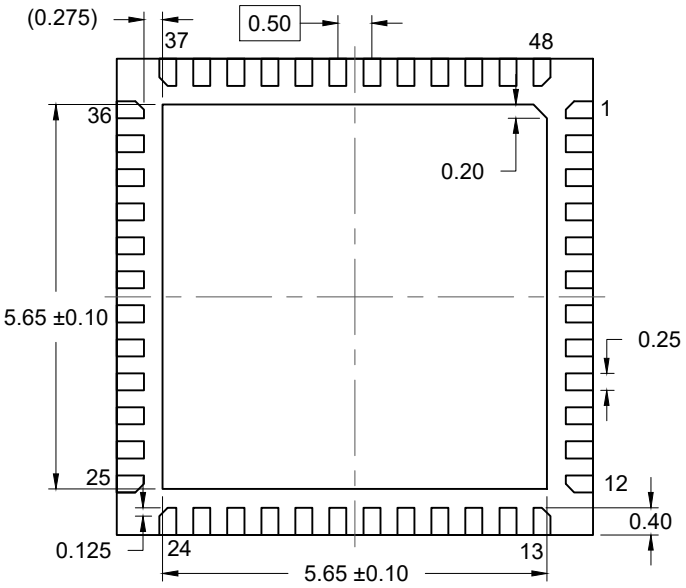
Revision	Date	Description
1.01	Jan 8, 2024	Updated the typical values for C_{IN} in Table 2.
1.00	Sep 23, 2022	Initial release.

Package Outline Drawing

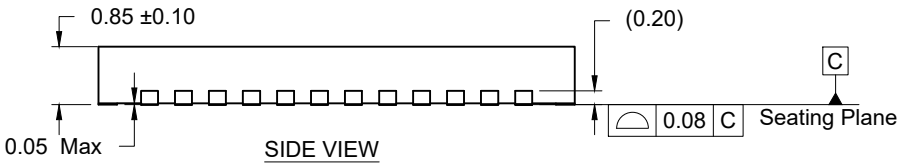
Package Code: NLG48P1
48-VFQFPN 7.0 x 7.0 x 0.85 mm Body, 0.5mm Pitch
PSC-4203-01, Revision: 03, Date Created: Apr 3, 2024



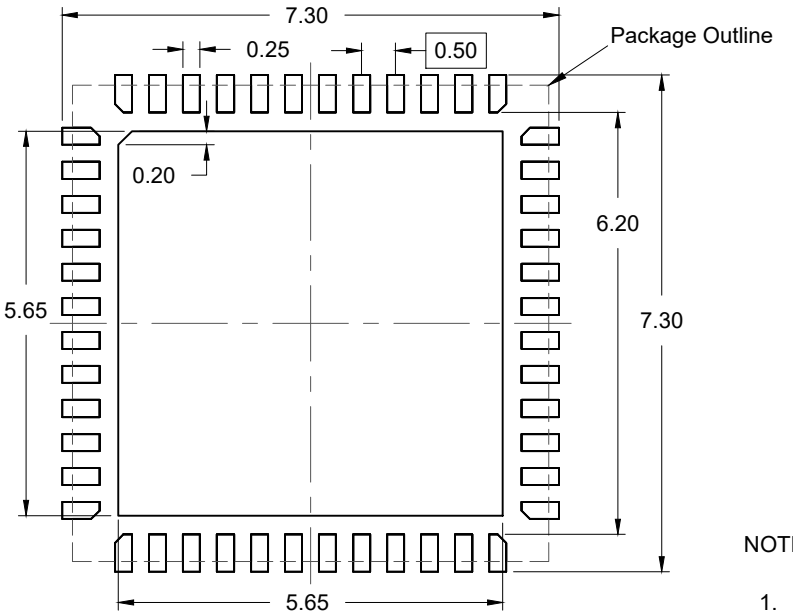
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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