RAA270000KFT

(RAA270000KFT#BA2)

General purpose Power Management IC

R02DS0021EJ0100
Rev1.00
2020.1

Description

The RAA270000KFT is a general purpose Power Management IC (PMIC), and suitable for RENESAS' microcontroller RH850 series. The features and detail information of the PMIC are described in this document.
The PMIC contains two current mode DCDC converters, four low dropout linear regulators (LDO) and two linear trackers. The switching frequency of DCDC is typical 2.1MHz.
In order to monitor internal status, monitor function is implemented. The input voltage, output of all regulators, and internal analog voltage corresponding to temperature are monitored through ADC in microcontroller. For testing ADC in microcontroller, reference voltage can be monitored as well.
Since this PMIC includes a power-up/down sequence controller, it allows user not to build external sequence circuit.

Features

- Input range: 6.0V to 18.5V to perform specified characteristics.
  5.4V~: Power rails, 5V/3.3V/1.25V and trackers functional (Not detect low voltage)
  3.9V~: Not issues reset.
- 2 switching regulators,
  For point of load: 5.7V/1000mA
  For MCU core: 1.25V/700mA
- 4 linear regulators,
  For MCU : 3.3V/10mA, 5.0V/300mA, 3.3V/160mA, 5.0V/60mA
- 2 linear trackers,
  150mA ability with short protection to battery
- Automatic power sequence
- Watchdog timer
- Analog multiplexer
- Interrupt request
- Thermal shut down
- Reset generator
- Exposed die pad, QFP package, 64pin 12mm x 12mm

Applications

- Automotive applications
- Industrial applications
- Ideal power supply for RENESAS' microcontroller, RH850 E1x and C1x series.

Table of Contents

1 Absolute Maximum Rating

1.1 Absolute maximum rating *

Items	Comment	MIN	MAX	Unit
VINR, VINPDC1A/B		-0.3	26 ***	V
VDDIO	Supply power for internal circuits	-0.3	6.0	V
VIN3V	Supply power for internal circuits	-0.3	4.0	V
VINP1/2, VINPTRQ1/2, VINPDC2A/B		-0.3	19	V
PGND1/2, AGND1/2	All ground pins	-0.3	0.3	V
FBDC1, FBDC2A/B	Feedback pins for DCDC	-0.3	19	V
LX1A/B		-1.0 **	VINPDC1A/B +0.3	V
LX2A/B		-1.0 **	VINPDC2A/B +0.3	V
TREF1/2	Input pins for trackers	-0.3	6.0	V
EN0/1, LDO0EN		-0.3	VINR+0.3	V
VOUT0		-0.3	VINR+0.3	V
VOUT1, VADC		-0.3	VINP1+0.3	V
VOUT2		-0.3	VINP2+0.3	V
VOUT0SW, BUFAD		-0.3	VIN3V+0.3	V
VTRQ1		-0.3	VINPTRQ1 +0.3	V
VTRQ2		-0.3	VINPTRQ2 +0.3	V
MUXOUT	Analog output pin	-0.3	VADC+0.3	V
ERROR1/2, WDI, WDENB, SPISDI, SPICLK, SPICSB	Digital input pins	-0.3	VDDIO+0.3	V
SPISDO, RSTB, INTOUT, SUSP FSOUT, EXCNT	Digital output pins	-0.3	VDDIO+0.3	V
Thermal resistance (Typical)	Junction to ambient	19.4 ****		°C/W
	Junction to case (Top)	17.3 ****		
	Junction to case (Bottom)	0.98 ****		
Junction Temperature *****		-40	150	°C
Storage Temperature Range		-55	150	°C

*: Stress beyond those listed under Absolute Maximum Rating may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**: Not allowed to apply continuous voltage.

***: Maximum voltage is 40V under load dump condition. (Duration time is 400ms.)

****: Simulation value based on JEDEC-2S2P condition.

*****: The PMIC includes over temperature protection that is intended to protect the device during momentary over load condition. Junction temperature will exceed the maximum operating junction temperature when over temperature is achieved. Continuous operating above specified maximum operating junction temperature may impair device reliability.

2 Pin Configuration

2.1 Pin configuration

Pin configuration is shown in below figure. The package is 64pin exposed die pad QFP.

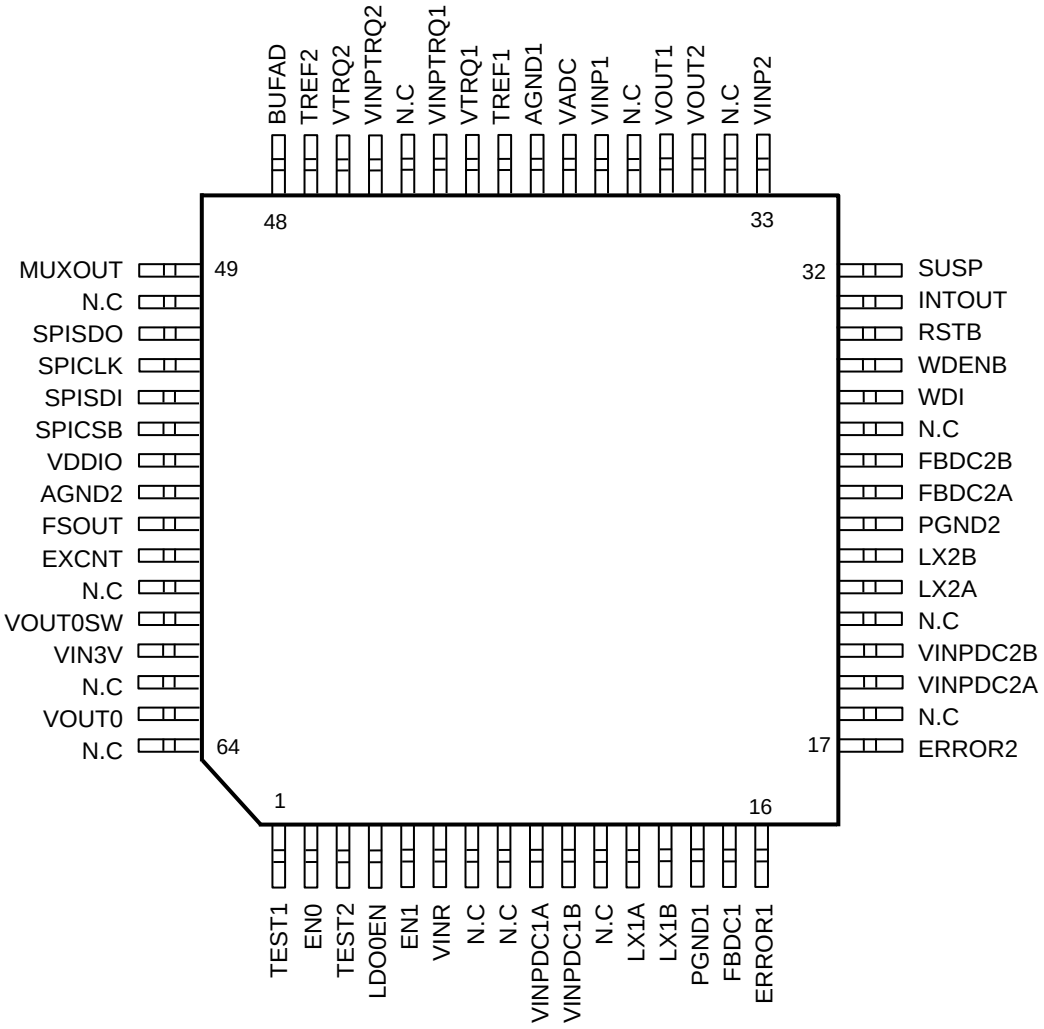


Fig. 2 Pin configuration (Top view)

2.2 Pin list

The pin list table is shown below.

PIN #	PIN name	Pin function	Analog or Digital	I/O/P/G	Interface level	Protect circuit to		Remarks
						VDD name	GND name	
1	TEST1	For test. It should be connected to ground.	-	-	-	VIN3V	AGND1/2	Should be connected to GND.
2	EN0	Power enable of the PMIC. (High : Enable the PMIC, Low : Disable the PMIC)	Digital	Input	NMOS	VINR	AGND1/2	Included pull-down resister.
3	TEST2	For test. It should be connected to ground.	-	-	-	VIN3V	AGND1/2	Should be connected to GND.
4	LDO0EN	Power enable of LDO0 without EN0 or EN1. (High : Enable LDO0, Low : Disable LDO0)	Digital	Input	NMOS	VINR	AGND1/2	Included pull-down resister.
5	EN1	Power enable of the PMIC. (High : Enable the PMIC, Low : Disable the PMIC)	Digital	Input	NMOS	VINR	AGND1/2	Included pull-down resister.
6	VINR	Power supply for LDO0.	-	Power	-	-	PGND1/2	
7	N.C	Not connected.	-	-	-	-	-	Should be open.
8	N.C	Not connected.	-	-	-	-	-	Should be open.
9	VINPDC1A	Power supply for DCDC1.	-	Power	-	-	PGND1/2	
10	VINPDC1B	Power supply for DCDC1.	-	Power	-	-	PGND1/2	
11	N.C	Not connected.	-	-	-	-	-	Should be open.
12	LX1A	DCDC1 Inductor driver output.	Analog	Output	-	-	PGND1/2	
13	LX1B	DCDC1 Inductor driver output.	Analog	Output	-	-	PGND1/2	
14	PGND1	Ground.	-	Ground	-	-	-	
15	FBDC1	DCDC1 Feedback from VD1.	Analog	Input	-	-	AGND1/2	
16	ERROR1	Input for monitor signal of microcontroller.	Digital	Input	CMOS	VDDIO	AGND1/2	Included pull-down resister.
17	ERROR2	Input for monitor signal of microcontroller.	Digital	Input	CMOS	VDDIO	AGND1/2	Included pull-down resister.
18	N.C	Not connected.	-	-	-	-	-	Should be open.
19	VINPDC2A	Power supply for DCDC2.	-	Power	-	-	PGND1/2	
20	VINPDC2B	Power supply for DCDC2.	-	Power	-	-	PGND1/2	

Note: AGND1/2 and PGND1/2 are connected in the PMIC.

Pin list (Continued)

PIN #	PIN name	Pin function	Analog or Digital	I/O/P/G	Interface level	Protect circuit to		Remarks
						VDD name	GND name	
21	N.C	Not connected.	-	-	-	-	-	Should be open.
22	LX2A	DCDC2 Inductor driver output.	Analog	Output	-	-	PGND1/2	
23	LX2B	DCDC2 Inductor driver output.	Analog	Output	-	-	PGND1/2	
24	PGND2	Ground.	-	Ground	-	-	-	
25	FBDC2A	DCDC2 Feedback from VD2.	Analog	Input	-	-	AGND1/2	
26	FBDC2B	DCDC2 Feedback from VD2.	Analog	Input	-	-	AGND1/2	
27	N.C	Not connected.	-	-	-	-	-	Should be open.
28	WDI	Clear watch dog timer.	Digital	Input	CMOS	VDDIO	AGND1/2	Included pull-down resister.
29	WDENB	Watch dog enable.	Digital	Input	CMOS	VDDIO	AGND1/2	Included pull-down resister.
30	RSTB	Reset output.	Digital	Output	Open drain	VDDIO	AGND1/2	
31	INTOUT	Interrupt signal output.	Digital	Output	CMOS	VDDIO	AGND1/2	
32	SUSP	Low voltage indicator of LDO1.	Digital	Output	CMOS	VDDIO	AGND1/2	
33	VINP2	Power supply for LDO2.	-	Power	-	-	AGND1/2	
34	N.C	Not connected.	-	-	-	-	-	Should be open.
35	VOUT2	LDO2 output.	Analog	Output	-	VINP2	AGND1/2	
36	VOUT1	LDO1 output.	Analog	Output	-	VINP1	AGND1/2	
37	N.C	Not connected.	-	-	-	-	-	Should be open.
38	VINP1	Power supply for LDO1.	-	Power	-	-	AGND1/2	
39	VADC	LDOAD output.	Analog	Output	-	VINP1	AGND1/2	
40	AGND1	Ground.	-	Ground	-	-	-	
41	TREF1	Input reference for TRACK1.	Analog	Input	-	-	AGND1/2	
42	VTRQ1	TRACK1 output.	Analog	Output	-	-	AGND1/2	

Note: AGND1/2 and PGND1/2 are connected in the PMIC.

Pin list (Continued)

PIN #	PIN name	Pin function	Analog or Digital	I/O/P/G	Interface level	Protect circuit to		Remarks
						VDD name	GND name	
43	VINPTRQ1	Power supply for TRACK1.	-	Power	-	-	AGND1/2	
44	N.C	Not connected.	-	-	-	-	-	Should be open.
45	VINPTRQ2	Power supply for TRACK2.	-	Power	-	-	AGND1/2	
46	VTRQ2	TRACK2 output.	Analog	Output	-	-	AGND1/2	
47	TREF2	Input reference for TRACK2.	Analog	Input	-	-	AGND1/2	
48	BUFAD	Voltage reference output.	Analog	Output	-	-	AGND1/2	
49	MUXOUT	Analog multiplexer output.	Analog	Output	-	VADC	AGND1/2	
50	N.C	Not connected.	-	-	-	-	-	Should be open.
51	SPISDO	Serial interface data output.	Digital	Output	CMOS	VDDIO	AGND1/2	
52	SPICLK	Serial interface clock input.	Digital	Input	CMOS	VDDIO	AGND1/2	Included pull-down resister.
53	SPISDI	Serial interface data input.	Digital	Input	CMOS	VDDIO	AGND1/2	Included pull-down resister.
54	SPICSB	Serial interface chip select input.	Digital	Input	CMOS	VDDIO	AGND1/2	Included pull-up resister.
55	VDDIO	Power supply for I/O of the PMIC.	-	Power	-	-	AGND1/2	
56	AGND2	Ground.	-	Ground	-	-	-	
57	FSOUT	Specified digital output.	Digital	Output	CMOS	VDDIO	AGND1/2	
58	EXCNT	Specified digital output.	Digital	Output	CMOS	VDDIO	AGND1/2	
59	N.C	Not connected.	-	-	-	-	-	Should be open.
60	VOUT0SW	LDO0 output through internal switch.	Analog	Output	-	-	AGND1/2	
61	VIN3V	Power supply for internal circuit.	-	Power	-	-	AGND1/2	
62	N.C	Not connected.	-	-	-	-	-	Should be open.
63	VOUT0	LDO0 output.	Analog	Output	-	VINR	AGND1/2	
64	N.C	Not connected.	-	-	-	-	AGND1/2	Should be open.

Note: AGND1/2 and PGND1/2 are connected in the PMIC.

3 Internal Block Diagram

The PMIC block diagram is shown in below figure.

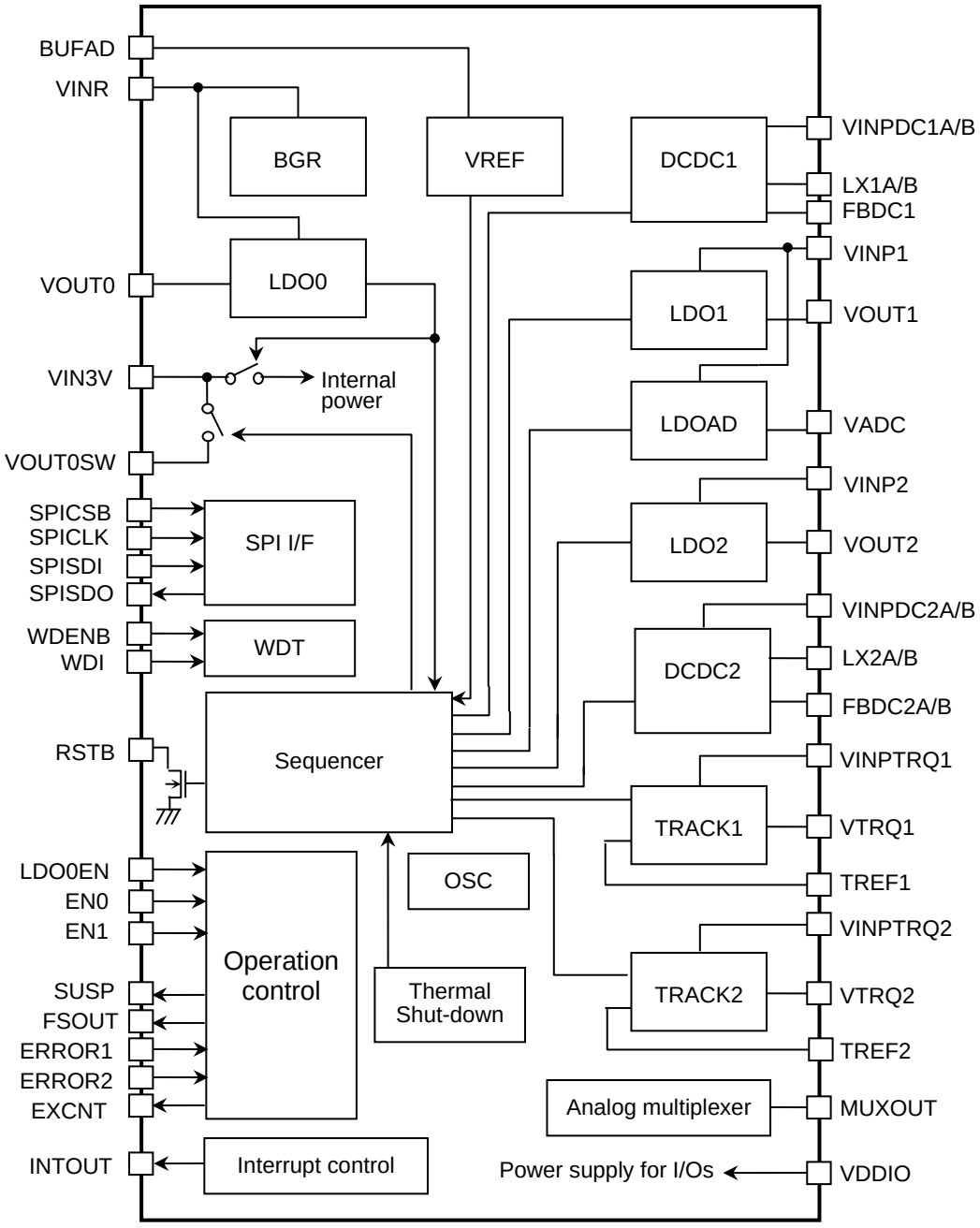


Fig. 3 The PMIC block diagram

The abstractive descriptions are here. Please refer to each section for more detail.

◆ **LDO0**
LDO0 is a low drop output regulator. It generates 3.3V power. The output current ability is 10mA.

◆ **LDO1**
LDO1 is a low drop output regulator. It generates 5.0V power. The output current ability is 300mA.

◆ **LDO2**
LDO2 is a low drop output regulator. It generates 3.3V power. The output current ability is 160mA.

- **LDOAD**
  LDOAD is a low drop output regulator. It generates 5.0V power. The output current ability is 60mA.
- **TRACK1**
  TRACK1 is a voltage tracker. The output tracks input voltage applied on TREF1. The current ability is 150mA.
- **TRACK2**
  TRACK2 is a voltage tracker. The output tracks input voltage applied on TREF2. The current ability is 150mA
- **DCDC1**
  DCDC1 is a switching regulator. It generates 5.7V power. The output current ability is 1000mA.
- **DCDC2**
  DCDC2 is a switching regulator. It generates 1.25V power. The output current ability is 700mA.
- **Band gap reference (BGR)**
  BGRs generate reference voltage for the regulators.
- **VREF**
  VREF generates necessary voltage for regulators. To reduce noise of LDO1 and LDOAD, an external capacitor can be added.
- **Analog multiplexer**
  An analog multiplexer outputs internal analog voltage of the PMIC.
- **SPI interface**
  SPI receives requests from microcontroller. Or it also sends register setting.
- **Watch dog timer (WDT)**
  WDT monitors system operating. WDT can be controlled by WDI pin or via SPI.
- **Sequencer**
  It controls power up/down of the regulators.
- **Operation control**
  It controls operation of the PMIC and external pins.
- **Interrupt control**
  It controls interrupt operations.
- **OSC**
  2.1MHz oscillator for sequencer and DCDC. No external part needed.
- **Thermal shut-down**
  It monitors temperature on the die. If the temperature rises higher than designated value, it informs to the sequencer.

4 PMIC Function

4.1 Abstract of the PMIC

In order to supply power to microcontroller or ASIC, the PMIC contains two current mode DCDC converters (DCDC) and four LDOs. The DCDC1's output is supposed to be used for all LDOs' and DCDC2's power sources. When battery voltage is applied to the PMIC, the regulators rise up automatically in accordance with designated sequence. And after all outputs of the regulators power up successfully, the "INTOUT" signal is released.

The PMIC also has a watchdog timer (WDT). When timer in the WDT expires, a reset signal occurs. The WDT is refreshed by a request via WDI pin or SPI.

When the junction temperature reaches over Tsd, a reset occurs and all regulators would be forced to power down immediately.

4.1.1 PMIC operation

The principal operate transitions and conditions are illustrated in below state diagram.

EN0 or EN1 is enables operation of the PMIC. If EN0 and EN1 are set low, the PMIC enters "Stand-by" state.

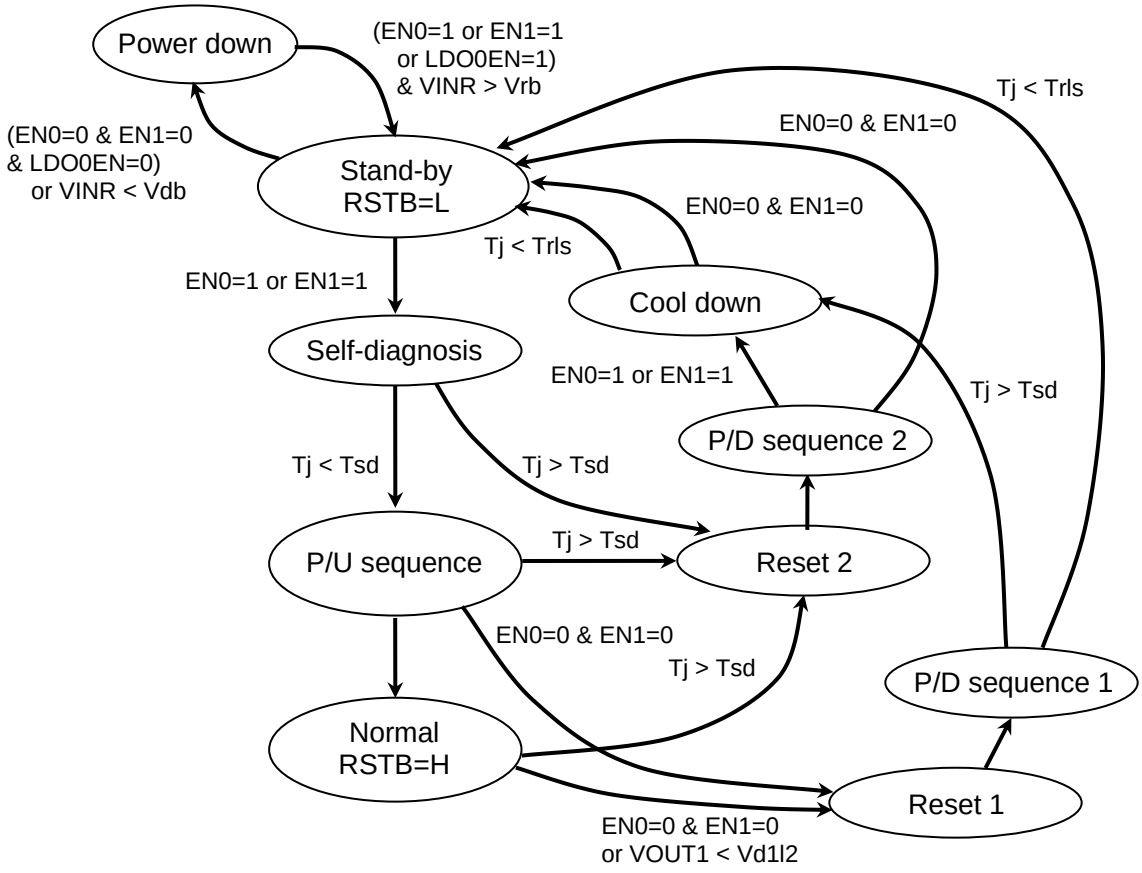


Fig.4 State diagram

◆ **Power down**

In this state, no block in the PMIC operates.

◆ **Stand-by**

In this state, the PMIC executes initial reset of internal registers and RSTB pin is asserted low. Only LDO0 operates in this state.

◆ **Self-diagnosis**

If EN0 or EN1 is set 1, self-diagnostic starts. In this state, over/under voltage detector in the regulators and the internal logic circuit are checked. If junction temperature is higher than Tsd, then it enters "Reset2" state.

◆ **P/U sequence**
After executing self-diagnostic, this state is automatically entered. Even if one of regulators doesn't rise up, it stays in this state. After all regulators rise up and it passed 12ms, reset is released. WDENB is detected in this state.

◆ **Normal**
After reset is released, this state is automatically entered. If WDENB is detected as low in this state, system monitor is started with using the WD function. If WDENB is detected as high, the WDT doesn't run. And also the PMIC monitors junction temperature.

◆ **Reset 1**
RSTB asserts low by setting low both EN0 and EN1, or low voltage detection of VOUT1 immediately.

◆ **P/D sequence 1**
This state is automatically entered from "Reset 1" state. All regulators except LDO0 start to fall down in designated order. Junction temperature is checked. If junction temperature is higher than Tsd, then it enters "Cool down" state. If lower than Trls, it enters back "Stand-by" state.

◆ **Reset 2**
When Tj comes over Tsd, RSTB pin asserts low.

◆ **P/D sequence 2**
This state is automatically entered from "Reset 2" state. All regulators except LDO0 start to fall down in designated order.

◆ **Cool down**
The PMIC checks if junction temperature is lower than Trls. If junction temperature is higher than Tsd, the PMIC wait until junction temperature cools down. After junction temperature comes below Trls, it enters "Stand-by" state.

4.1.2 Pin setting

The PMIC has several pins to define PMIC operation. For proper operation, these pins should be set to appropriate level. Appropriate setting voltages are described in "6. Electrical Characteristics"

◆ **The PMIC enabling**
User can control the PMIC by EN0 or EN1 pin. And it also makes only LDO0 power on by LDO0EN. These pins can be connected to battery.

Table 4-1 Setting PMIC operation

EN0	EN1	LDO0EN	PMIC operation
0	0	0	Disenable
0	0	1	Only LDO0 operates
0	1	*	The PMIC operates
1	0	*	The PMIC operates
1	1	*	The PMIC operates

*: Don't care

Note: If EN0 or EN1 is asserted high after LDO0EN=1, please keep VINR > Vrb.
In the condition of VINR < Vrb, the state is shifted to power down.

◆ **WDT enabling**
User can stop WDT operation by setting WDENB pin. When WDENB is set to disenable, the WDT stops operation. Below setting is defined at before start of P/U sequence.

Table 4-2 Setting WDT operation

WDENB	WDT operation
0	Enable
1	Disenable

4.1.3 Operating input voltage

The PMIC operates different mode in accordance with its input voltage. The PMIC operation in input voltage range is shown in below table.

Table 4-3 The PMIC operation mode

Operation mode	Function	Input range
Full operation	All regulators operate normaly.	6.0V ~
Partial operation	DCDC1 stops switching, but all LDOs, DCDC2 and trackers operate normaly. (Not issue low voltage detection.)	5.4V ~
Lingering mode	Not issue reset.	3.9V ~

4.1.4 Configuration register

In order to configure functional operation of the PMIC, it needs to set in this register. For more setting information, please refer to each described section.

- Configuration register

  This register is a secured register. It is necessary to enter “key” code, before entering this request. (See “4.2.3 Secured request”.) Brief explanations of register contents are described in below of the table following;

  - Address (CONF) : 10H

A5	A4	A3	A2	A1	A0
0	1	0	0	0	0

  - Register

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	RSTBER	WDTCNT	DL2RSTB	ADVWD	CWRSTB

  - Setting contents

Register name		Control contents	Setting	
			1	0
RSTBER	D4	Reset assertion by ERROR1/2 input	On	Off *
WDTCNT	D3	Select WDT clear input channel	SPI	WDI *
DL2RSTB	D2	Reset by DETDC2L or DET2L	On	Off *
ADVWD	D1	Advanced mode for WD operating	Enable	Disable *
CWRSTB	D0	Reset by WD trigger in close window.	On	Off *

* Default setting

Note1: This register is not initialized by RSTB.
Note2: Advanced mode for WD is effective when SPI is selected to refresh WDT.

RSTBER: The register can set to relate with ERROR1/2. After setting “On”, RSTB asserts low when ERROR indicates error.
WDTCNT: Select WDT clear input. To clear WDT through SPI, it needs to set this bit.
DL2RSTB: The register can set to make reset when low voltage of DCDC2 or LDO2 is detected. After setting “On”, reset is generated by low voltage of DCDC2 or LDO2.
ADVWD: The register can set to operate WDT in advanced mode. After setting “Enable”, WD operates in advanced mode. Please refer to “4.8 Watchdog timer”.
CWRSTB: The register can set to make reset when a trigger occurs in close window.

4.1.5 Product code

In order to identify the PMIC, product code can be read from the PMIC.

- Product code

  In order to identify the PMIC, each product has ID code. It can be read via SPI.

  - Address (CHIPID) : 00H

A5	A4	A3	A2	A1	A0
0	0	0	0	0	0

  - Register (Below bits are read only.)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	1	1	1	1

4.1.6 Pin monitor

WDENB and ERROR1/2 are significant pins related to PMIC behavior. These pins are monitored in this register.

- Pin monitor register

  This register is monitoring WDENB and ERROR1/2 pins.

  - Address (PINMON) : 02H

A5	A4	A3	A2	A1	A0
0	0	0	0	1	0

  - Register (Below bits are read only.)

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	-	PWDENB	PERR2	PERR1

  - Setting contents

Register name		Monitor pin
PWDENB	D2	WDENB pin's level
PERR2	D1	ERROR2 pin's level
PERR1	D0	ERROR1 pin's level

Bit	Contents
0	Low level
1	High level

Note1: Above WDENB is identified at "P/U sequence" state.

Note2: The PMIC starts to monitor ERROR1/2 after reset is released and sampled every 100µs.

4.2 Serial Interface

In order to request to the PMIC, the PMIC includes serial to peripheral interface. (SPI)
User can set or request following things. For more detail contents, please refer to each section.

- WDT operation (If SPI control is selected.)
- Control the monitor function
- Interrupt control, read factor, write interrupt clear
- TRACK1/2 power control
- Change shutdown or warning temperature

4.2.1 Signal format

The bit length of the communication is 16bits, and signal format is illustrated in below figures.
The data should be transmitted as MSB first. For this SPI, one SPICSB active is for one request. Therefore, it is necessary to make SPICSB rise up after transmitted data.

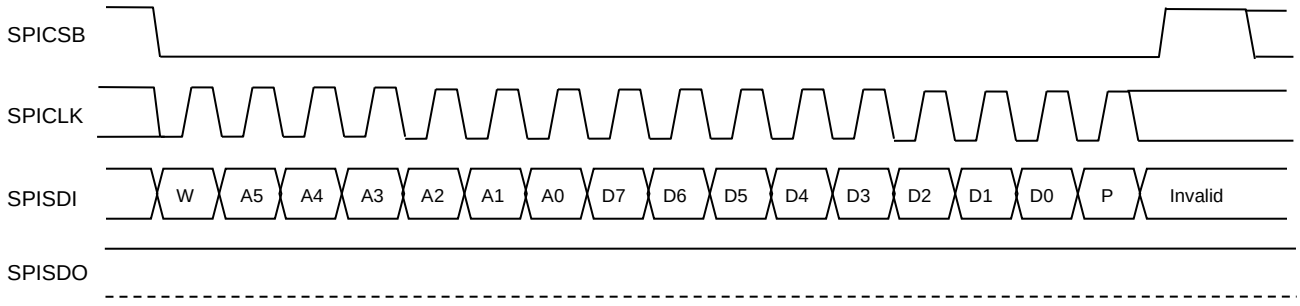


Fig. 4-2-1 SPI format (Write)

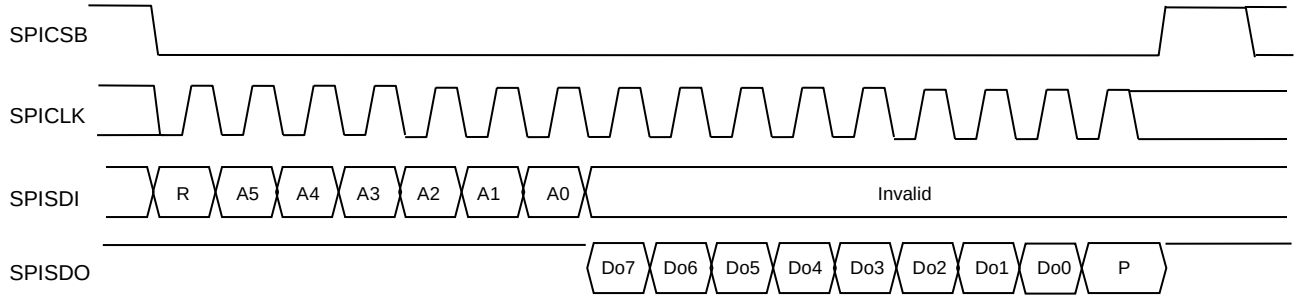


Fig. 4-2-2 SPI format (Read)

Caution: In the PMIC, entered data is latched by rising edge of SPICSB.
Caution: SPISDO pin should be terminated with pull-up resister to VOUT1.

◆ **W/R**
This bit indicates write or read registers. To write register, bit W/R should be set 0. To read register, bit W/R should be set 1. When user wants to read register, Do7-Do0 bits indicate contents. (D7-D0 bits are ignored in the PMIC.)

◆ **A5-A0**
The PMIC contains several registers. The addresses are described in these bits. Every registers can be read to confirm its content.

◆ **D7-D0**
These bits describe control bits of the PMIC to write into the PMIC.

◆ **Do7-Do0**
These bits describe content bits or flag bits to read from the PMIC.

◆ **P**

This bit indicates parity bit. It is calculated based on the number of logic contained in bits except parity bit itself.

SPISDO terminal stays Hi-Z during transmitting “W/R” bit and address bits, A5-A0. But parity bit of read data is calculated with considering “W/R” bit and all address bits as 1. Therefore, pull-up resister should be placed between SPISDO and VOUT1.

Bit P must be set 0 if the number of 1 is odd.
Bit P must be set 1 if the number of 1 is even.

4.2.2 Ensuring communication

To ensure the communication between the PMIC and microcontroller, the PMIC checks the SPI signal of following accesses. The PMIC counts how many times below access happen.

- Number of SPICLK
  The PMIC counts SPICLK clocks while SPICSB is low. If the number of clock is not 16, it is considered as a communication error. The PMIC ignores this command or request.
- Not related address
  When unrelated address is transmitted, the PMIC ignores this address’ contents.
- Parity bit
  The SPI format includes a parity bit. The PMIC checks the parity bit and if transmitted bits are not based on the parity bit, it is considered as a communication error. The PMIC ignores this command or request.

4.2.3 Secured request

There are some registers which need to be careful when register’s content is changed. When it needs to change following contents, microcontroller needs to request code as a “key” to the PMIC. And write below address with a “key” code at once before changing contents. Without a “key” code, the request would be ignored. To execute software reset, obtained “key” should be combined instead of sending protect code address.

- Configuration register (Address : 10H)
- DCDC protect operation setting (Address : 1BH)
- Power control for TRACK1/2 (Address : 1AH)
- Window time setting for WD timer (Address : 17H)
- Interrupt mask register (Address : 0CH-0FH)
- Reset mask register (Address : 14H)
- Temperature setting for thermal shut down (Address: 1EH)
- Software reset (Address: 1DH)

4.2.4 Register

The contents of SPI setting are described in this section.

- Protect remove code
  - Address (PRTCT) : 11H

A5	A4	A3	A2	A1	A0
0	1	0	0	0	1

  - Register

Before access secured register, need to obtain below random code by read mode.

Do7	Do6	Do5	Do4	Do3	Do2	Do1	Do0
RDMKEY(Do7:Do0)							

It needs to enter the obtained data before microcontroller enters request.

D7	D6	D5	D4	D3	D2	D1	D0
RDMKEY(D7:D0)							

  - Setting contents
    - RDMKEY(Do7:Do0) : Random code from the PMIC
    - RDMKEY(D7:D0) : Copy RDMO(Do7:Do0)

Note : Read PRTCT register to get key and write it back to PRTCT register before modify those function protect registers, instead of write the key to those function protect registers.

4.2.5 Register table

The registers which can be set in the PMIC are summarized in below table with its address and data. Detail contents are described in each section.

Address	Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Secured	Reset by	Function
0x00	CHIPID	R	CHIPID<7:0>								0xBF			Chip ID
0x02	PINMON	R	---	---	---	---	---	PWDENB	PERR2	PERR1	0x0*		DET00	Monitor digital output pins
0x03	INTFAC	R	---	---	INTRSFG	INTSD	INTR4	INTR3	INTR2	INTR1	0x00		DET00	Interrupt factor
0x04	INTREQ1	R	---	DETTRQ2U	DETTRQ1U	DETADU	DET2U	DET1U	DETDC2U	DETDC1U	0x00		DET00	Interrupt request 1
0x05	INTREQ2	R	DET0SWL	DETTRQ2L	DETTRQ1L	DETADL	DET2L	DET1L	DETDC2L	DETDC1L	0x00		DET00	Interrupt request 2
0x06	INTREQ3	R	---	WRTMP2	WRTMP1	WRWDT	DETREF	DETBAT1	DETDC2OC	DETDC1OC	0x00		DET00	Interrupt request 3
0x07	INTREQ4	R	DUMMY	SDOSC	SDSTA	SD0SW	PFSOUT	PEXCNT	PSUSP	PRSTB	0x00		DET00	Interrupt request 4
0x08	INTCL1	W	---	CLTRQ2U	CLTRQ1U	CLADU	CL2U	CL1U	CLDC2U	CLDC1U	-		RSTB	Interrupt clear 1
0x09	INTCL2	W	CL0SWL	CLTRQ2L	CLTRQ1L	CLADL	CL2L	CL1L	CLDC2L	CLDC1L	-		RSTB	Interrupt clear 2
0x0a	INTCL3	W	---	CLTMP2	CLTMP1	CLWDT	CLREF	CLBAT1	CLDC2OC	CLDC1OC	-		RSTB	Interrupt clear 3
0x0b	INTCL4	W	CLDUMMY	---	CLSTA	CL0SW	CLPFSOUT	CLPEXCNT	CLPSUSP	CLPRSTB	-		RSTB	Interrupt clear 4
0x0c	INTMSK1	R/W	---	MSKTRQ2U	MSKTRQ1U	MSKADU	MSK2U	MSK1U	MSKDC2U	MSKDC1U	0x00	○	RSTB	Interrupt mask1
0x0d	INTMSK2	R/W	MSK0SWL	MSKTRQ2L	MSKTRQ1L	MSKADL	MSK2L	MSK1L	MSKDC2L	MSKDC1L	0x00	○	RSTB	Interrupt mask2
0x0e	INTMSK3	R/W	---	MSKTMP2	MSKTMP1	MSKWDT	---	MSKBAT1	MSKDC2OC	MSKDC1OC	0x00	○	RSTB	Interrupt mask3
0x0f	INTMSK4	R/W	MSKDUMMY	MSKOSC	MSKSTA	---	MSKPFSOUT	MSKPEXCNT	MSKPSUSP	MSKPRSTB	0x00	○	RSTB	Interrupt mask4
0x10	CONF	R/W	---	---	---	RSTBER	WDTCNT	DL2RSTB	ADVWD	CWRSTB	0x00	○	DET00	Configuration register
0x11	PRTCT	R/W	RDMKEY<7:0>								0x**		RSTB	Protect remove code
0x12	RSTFAC	R	---	---	---	LVLDO2	TSDTMP	WDEXP	LVDC2	LVLDO1	0x00		DET00	Reset factor
0x13	RSTFCL	W	---	---	---	CLLVLDO2	CLTSDTMP	CLWDEXP	CLLVDC2	CLLVLDO1	-		RSTB	Reset factor clear
0x14	RSTFMSK	R/W	---	---	---	MSKLVLDO2	MSKTSDTMP	MSKWDEXP	MSKLVDC2	---	0x00	○	RSTB	Reset factor mask
0x15	PINSET	R/W	---	---	SETSUSP	SETEXCNT	---	---	SELDT	EMODE	0x30		RSTB	EXCNT and SUSP pin, error monitor setting
0x16	WDTRG	R/W	OPE<1:0>			SUBU<5:0>					0xFF		RSTB	WD advanced mode
0x17	WDTIME	R/W	---	---	---	---	CWSET<1:0>		WDTIME<1:0>		0x03	○	RSTB	Window time setting
0x18	MUXCNT	R/W	---	MUXCNT	---	---	MUXSEL<3:0>				0x00		RSTB	Muxamp control
0x19	QAEVA	R	ACCVA<7:0>								0x00		RSTB	Accumulated value for WD advanced mode
0x1A	TRQCNT	R/W	---	---	---	---	---	---	VTRQ2CNT	VTRQ1CNT	0x00	○	RSTB	TRACK1/2 on/off control
0x1B	DCLIM	R/W	INTIME2<1:0>		DTIME2<1:0>		INTIME1<1:0>		DTIME1<1:0>		0x44	○	DET00	Limit control for DCDC
0x1C	RSTVA	R/W	SETVA<7:0>								0xff		RSTB	Numer of reset for WD advanced mode
0x1D	SFTRST	W	RDMKEY<7:0>								-	○	RSTB	Software reset
0x1E	SENTMP	R/W	WARREL<1:0>		THREL<1:0>		WARDET<1:0>		THDET	---	0x94	○	DET00	Thermal shutdown temperature

Note: The initial value of PINMON is set with according to level of the pins.
The initial value of “PRTCT” register is unknown.

4.2.6 Electrical characteristics

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
SPICLK delay	tdck	From SPICSB fall	400	-	-	ns
SPICLK period	tcyc		800	-	-	ns
High period of SPICLK	thigh		320	-	-	ns
Low period of SPICLK	tlow		320	-	-	ns
Rise time of SPICLK/SDI	tr		-	-	10	ns
Fall time of SPICLK/SDI	tf		-	-	10	ns
Command set-up	tcmsu	From last SPICLK rise	400	-	-	ns
Data set-up	tsu	Before SPICLK rise	100	-	-	ns
Data hold	thd	After SPCLK rise	100	-	-	ns
Data access time	tacc	From last address clock fall	-	-	50	ns
Read data Hi-Z time	thiz		-	-	50	ns
High width of SPICSB	twidth		2800	-	-	ns

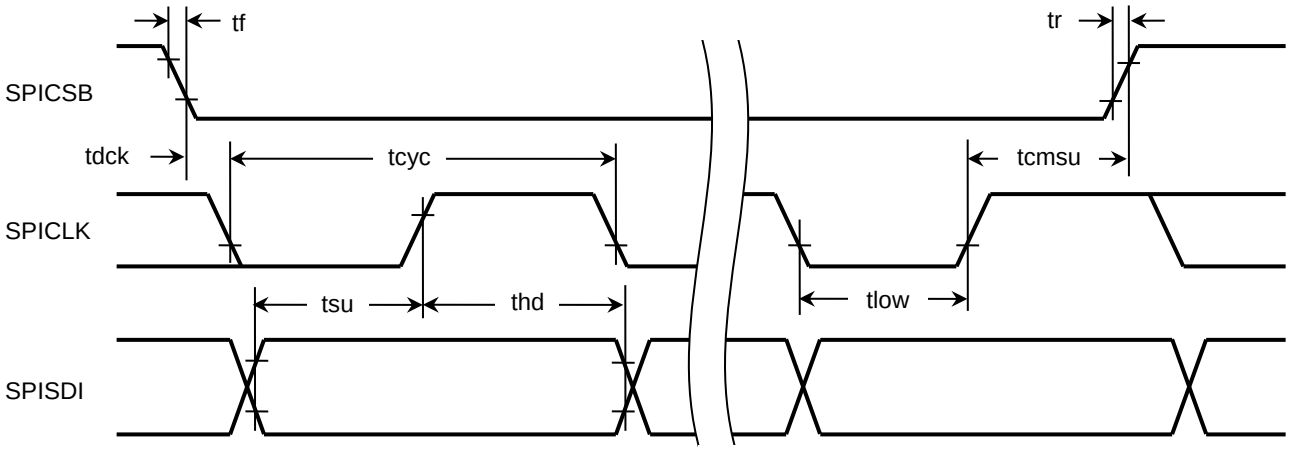


Fig. 4-2-3 SPI write timing

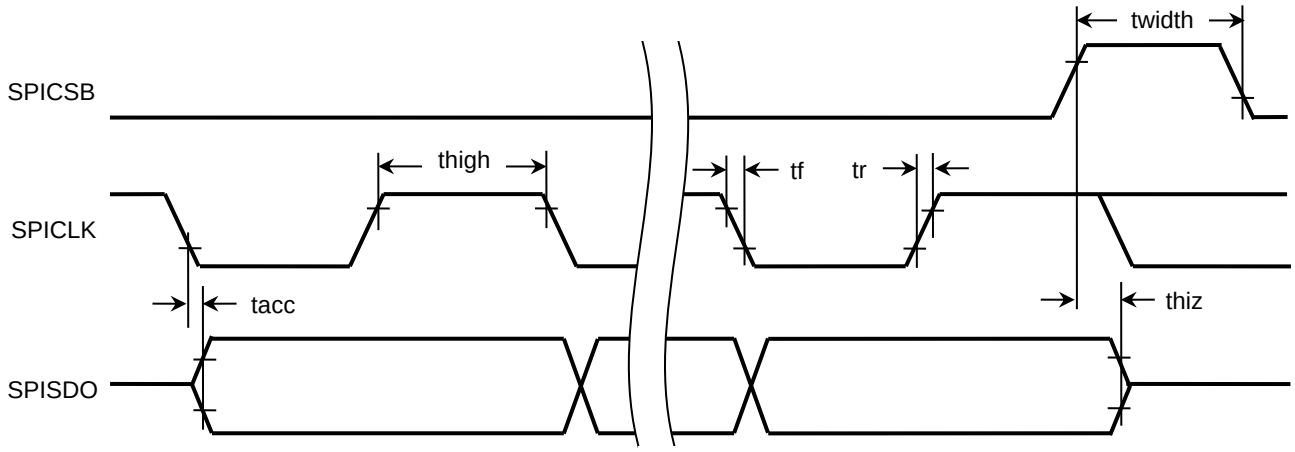


Fig. 4-2-4 SPI read timing

4.3 Reference Voltage

Below figure shows simplified reference voltage generator block.

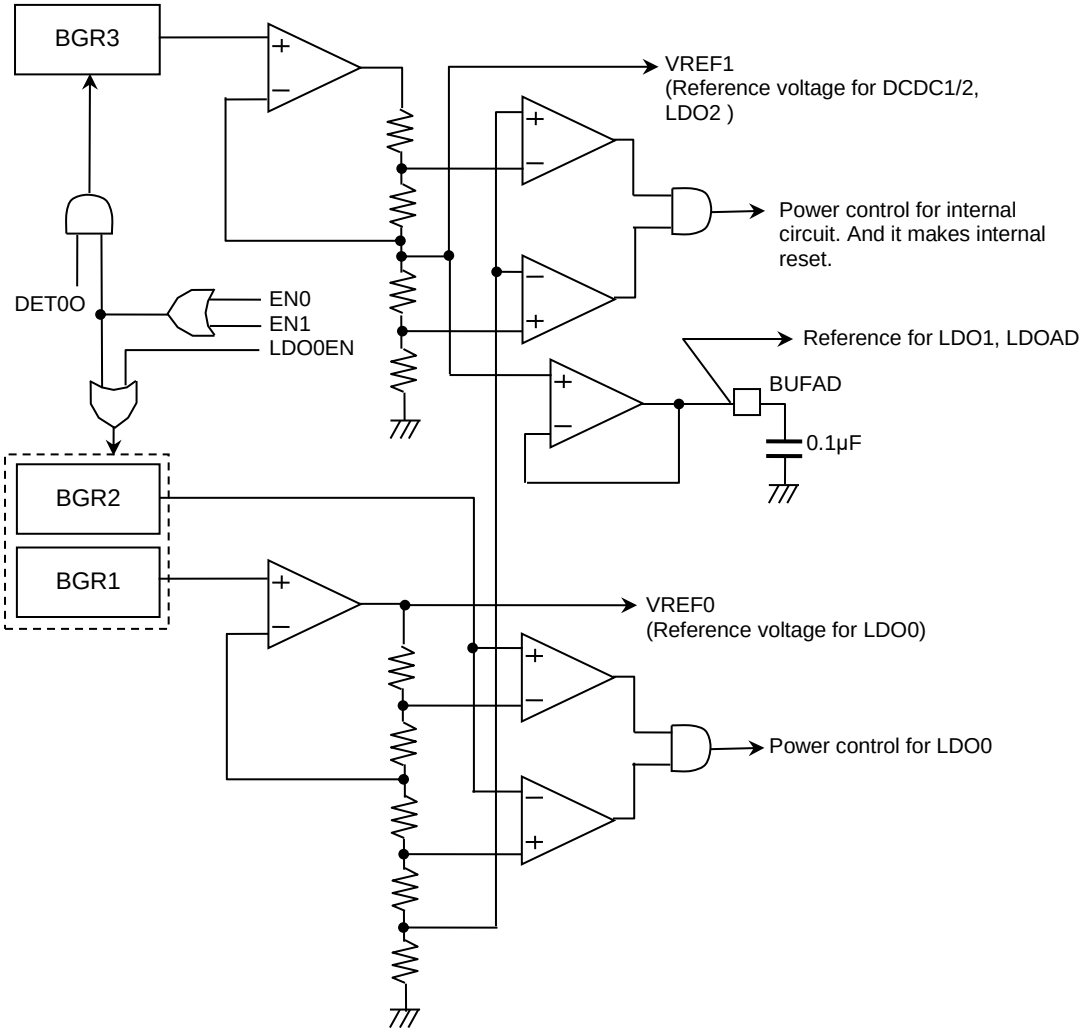


Fig 4-3 REF block diagram

There are three Band Gap Reference (BGR) circuits in the PMIC. In the upper figure, if BGR1 or BGR2 has damage, the PMIC would not power up. And if BGR3 suffers damage, all regulators except LDO0 would not power up.

BUFAD is reference voltage for LDO1 and LDOAD. In order to apply “clear” supply for ADC in microcontroller, 0.1µF capacitor is recommended to connect to ground.

4.3.1 Electrical characteristics

Below table shows characteristic of reference output.

C0=0.1µF (ESR=0~0.1Ω)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output voltage	VBUF		1.176	1.200	1.224	V

4.4 LDO

The PMIC includes four LDOs. Each LDO needs a ceramic capacitor on its output. This allows improvement of output transient response. The gain stage of LDOs except LDO0 is operated with 3.3V generated by LDO0. And each input of power stage is supposed to be connected to DCDC1's output .All LDOs have protection circuit with fold back characteristics.

◆ LDO0

Typically, the LDO0 output should be used as power supply for internal circuit of the PMIC. The typical output voltage is 3.3V.

It contains output voltage detector.

Especially, when over voltage is detected, the power line switch for internal circuit of the PMIC will be cut off supply power. Or when low voltage is detected, it makes reset and initializes internal register. The detect voltages are described in section 4.12.4

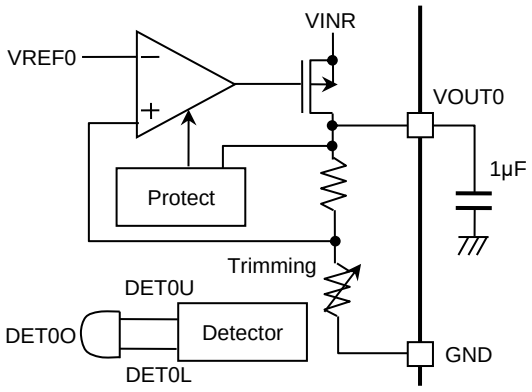


Fig. 4-4-1 LDO0 block diagram

◆ LDO1

Typically, the LDO1 output should be used as power supply for I/O of microcontroller. The typical output voltage is 5.0V.

It includes output voltage detector. If output voltage comes across unexpected voltage, a flag is set into register and INTOUT asserts low. Especially, when DET1L1 is detected, SUSP is asserted as warning. And when DET1L2 is detected, RSTB is asserted. The detect voltages are described in section 4.12.4.

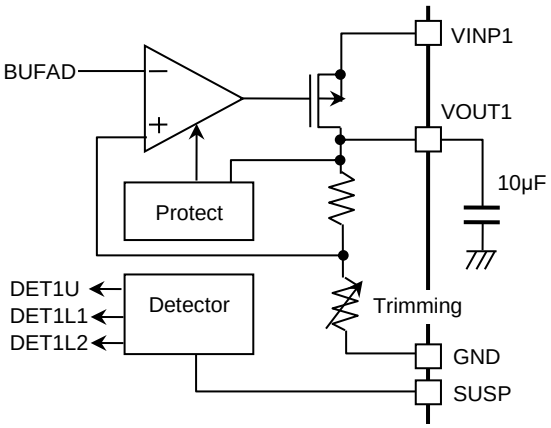


Fig. 4-4-2 LDO1 block diagram

◆ LDO2

The LDO2 output is used as power supply for analog part of microcontroller. The typical output voltage is 3.3V.

It includes output voltage detectors. If output voltage comes across unexpected voltage, a flag is set into register and INTOUT asserts low. The detect voltages are described in section 4.12.4.

If over voltage is detected, it forces DCDC1 to enter protect mode. For more detail DCDC1's behavior, please refer to section 4.6.1.

Low voltage detection can be added to reset condition by setting configuration register. When low voltage is detected, reset occurs immediately. Reset asserts low while VOUT2 is below low voltage detection level. After VOUT2 comes up usual output and 12ms passes, the reset is released.

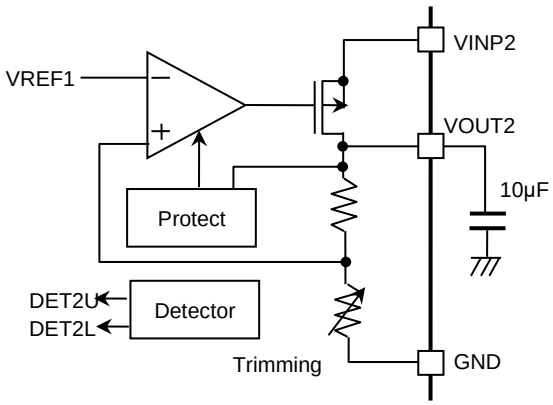


Fig. 4-4-3 LDO2 block diagram

◆ **LDOAD**

Typically, the LDOAD output is used as power supply for ADC of microcontroller. The typical output voltage is 5.0V.

It includes output voltage detectors. If output voltage comes across unexpected voltage, a flag is set into register and INTOUT asserts low. Actual detect voltage is described in section 4.12.4.

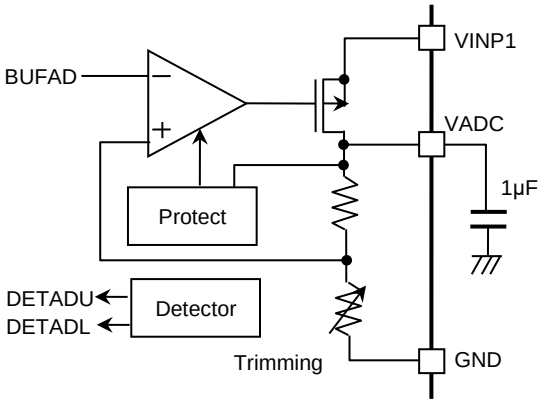


Fig. 4-4-4 LDOAD block diagram

◆ **VOUT0SW**

VOUT0SW is a pin which applies voltage for retention area of microcontroller. The output voltage comes through internal switch. In order to prevent to apply unusual high voltage of LDO0, the switch is controlled by over voltage detect of LDO0.

If output voltage comes down unexpected low voltage, a flag is set into register and INTOUT asserts low. Actual detect voltage is described in section 4.12.4.

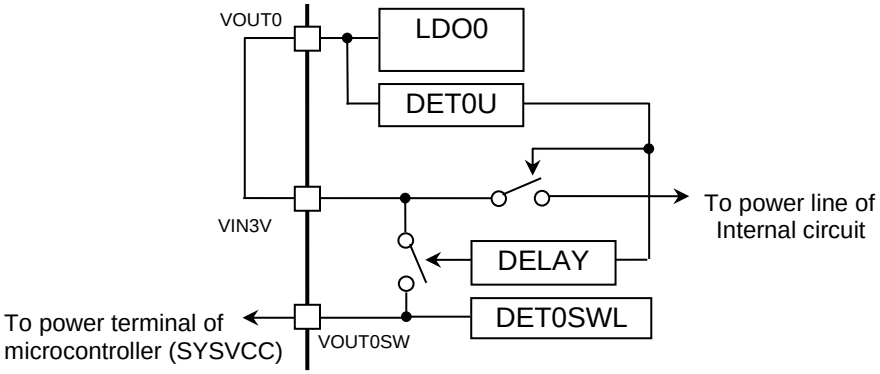


Fig. 4-4-5 Internal switch of VOUT0SW

4.4.1 Output protect function

When something wrong like solder bridge happens, huge current flows to ground. This may cause heat issue. To prevent flowing over current from the output, all LDOs have a current limit function. Fold-back characteristic is illustrated in below figure.

In this figure, “Io” is a guaranteed current which maintains specified output voltage. For more than “Io” current, the more output current flows, the lower output voltage goes down with decreasing output current.

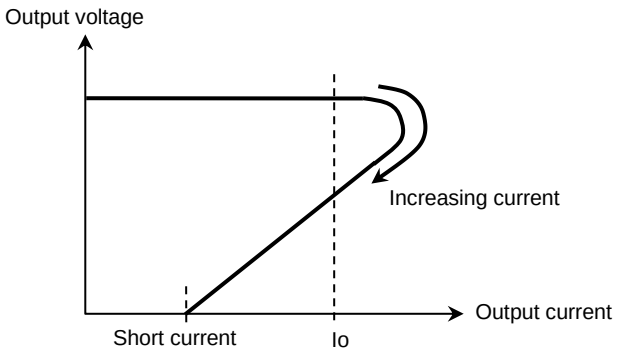


Fig. 4-4-6 Fold-back characteristic

4.4.2 Electrical characteristics

Characteristics noted under conditions GND=0V, unless otherwise noted. The condition is Tj=-40 to 150°C, unless otherwise specified.

◆ **LDO0**

C0=1µF (ESR=0~0.1Ω)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output voltage	Vo0	Io=0~10mA (DC)	3.250	3.300	3.399	V
Short current	Is0	Vo=0V	-	-	20	mA

◆ **LDO1**

C1=10µF (ESR=0~0.1Ω)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output voltage	Vo11	Io=0~150mA (DC)	4.90	5.00	5.10	V
		Io=150~300mA (DC)	4.85 *	-	5.10	
	Vo12	VINP1=4.95V, Io=150mA (DC)	4.75	-	4.95	V
	Vo13	VINP1=3.5V, Io=150mA (DC)	3.18	-	3.50	V
Short current	Is1	Vo=0V	-	-	80	mA

* Guaranteed by design.

◆ **LDO2**

C2=10µF (ESR=0~0.1Ω)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output voltage	Vo2	Io=0~160mA (DC)	3.234	3.300	3.366	V
Short current	Is2	Vo=0V	-	-	80	mA

◆ **LDOAD**

CAD=1µF (ESR=0~0.1Ω)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output voltage	VoA1	5.0V setting, Io=0~60mA (DC)	4.95	5.00	5.05	V
Short current	IsA	Vo=0V	-	-	30	mA

Note: “(DC)” means it doesn’t include AC factor like transient response.

4.5 Tracker

The PMIC includes two trackers. Each tracker needs a ceramic capacitor on its output. And each input of power stage is supposed to be connected to DCDC1's output.

◆ **TRACK1/2**

TRACK1 and TRACK2 are auxiliary power rails. The output voltage is set by input voltage. Power up control is set via SPI. These trackers have high voltage protect function to prevent reverse current from the output. When outputs touch high voltage like battery, this circuit stops reverse current toward the PMIC.

The trackers have protect function as same as LDO's fold-back characteristic.

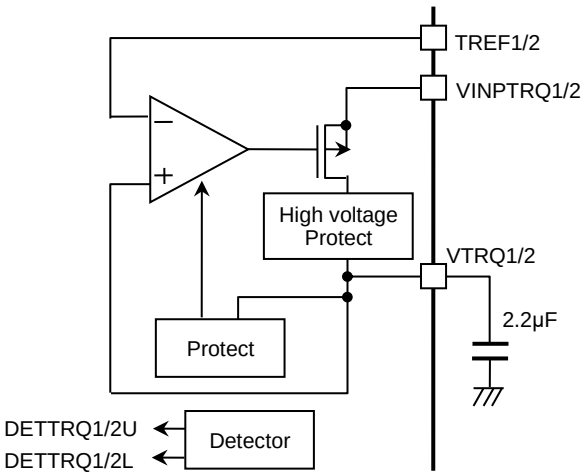


Fig. 4-5 Voltage tracker diagram

4.5.1 Register

The content of TRACK1/2 setting is only for power control.

➢ TRACK1/2 power control

■ Address (TRQCNT) : 1AH

A5	A4	A3	A2	A1	A0
0	1	1	0	1	0

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	--	-	-	VTRQ2CNT	VTRQ1CNT

■ Setting contents

Register name		Control contents	Setting	
			1	0
VTRQ2CNT	D1	TRACK2 on/off	On	Off *
VTRQ1CNT	D0	TRACK1 on/off	On	Off *

* Default setting

4.5.2 Electrical characteristics

Characteristics noted under conditions GND=0V, unless otherwise noted. The condition is Tj=-40 to 150°C, unless otherwise specified.

◆ **TRACK1**

CTRQ1=2.2µF (ESR=0~0.1Ω)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Matching output error	dVTR1	5V input, Io=150mA (DC)	-10	-	10	mV
Short current	IsTR1	Vo=0V	-	-	80	mA
Power on time *	Trtrq1	5V input voltage, 90% output	-	1.78	2.34	ms

* Guaranteed by design.

Note: "(DC)" means it doesn't include AC factor like transient response.

◆ **TRACK2**

CTRQ2=2.2µF (ESR=0~0.1Ω)

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Matching output error	dVTR2	5V input, Io=150mA (DC)	-10	-	10	mV
Short current	IsTR2	Vo=0V	-	-	80	mA
Power on time *	Trtrq2	5V input voltage, 90% output	-	1.78	2.34	ms

* Guaranteed by design.

Note: “(DC)” means it doesn’t include AC factor like transient response.

4.6 DCDC

The PMIC includes two DCDCs. Internal high-side PMOS power stages are implemented in each DCDC to reduce the PCB space. Each DCDC needs schottky diode, inductor and ceramic capacitor on its output like the diagram. Analog processing circuit except power PMOS is operated with the 3.3V generated by LDO0. Two DCDCs include output voltage detectors. The detectors monitor over voltage and lower voltage, and have output protect function and over current protection.

◆ DCDC1

The DCDC1 operates with current mode control. And it is supposed to supply power as intermediate power supply. This means all regulators' power input should be connected to DCDC1's output. (Except LDO0) The DCDC1 includes output voltage detector. If output voltage comes across unexpected voltage, the flag is set into register and INTOUT signal occurs. Actual detect voltage is described in section 4.12.4.

Hereafter, VD1 refers to as the output of DCDC1.

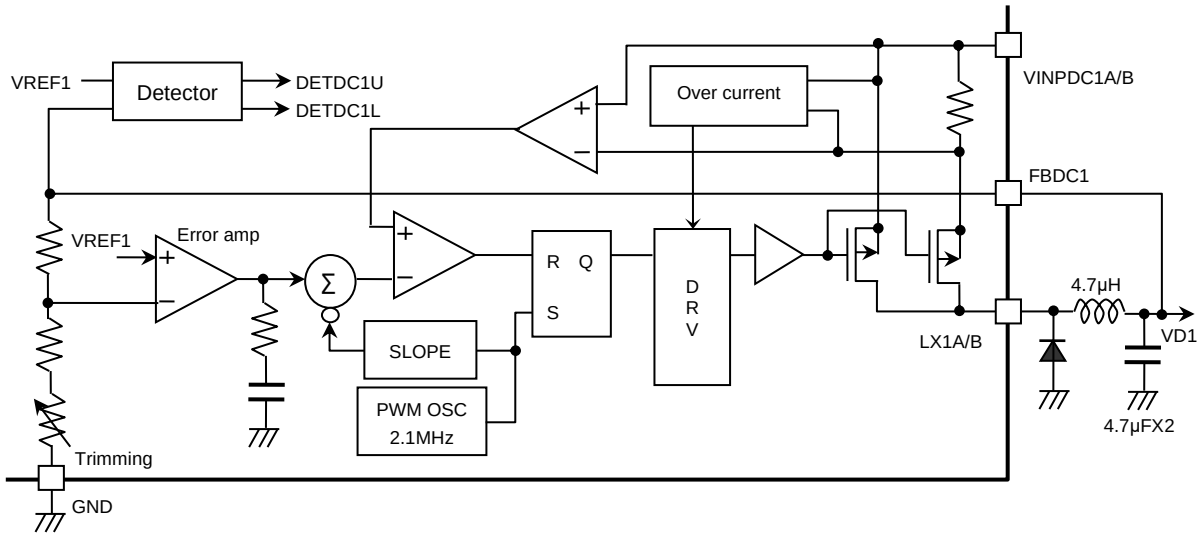


Fig.4-6-1 DCDC1 block diagram

◆ DCDC2

The DCDC2 also operates with current mode. The DCDC2 is supposed to supply power to microcontroller's core circuit. The DCDC2 includes output voltage detector. If output voltage comes across unexpected voltage, the flag is set into register and INTOUT signal occurs as well. Actual detect voltage is described in section 4.12.4.

Hereafter, VD2 refers to as the output of DCDC2.

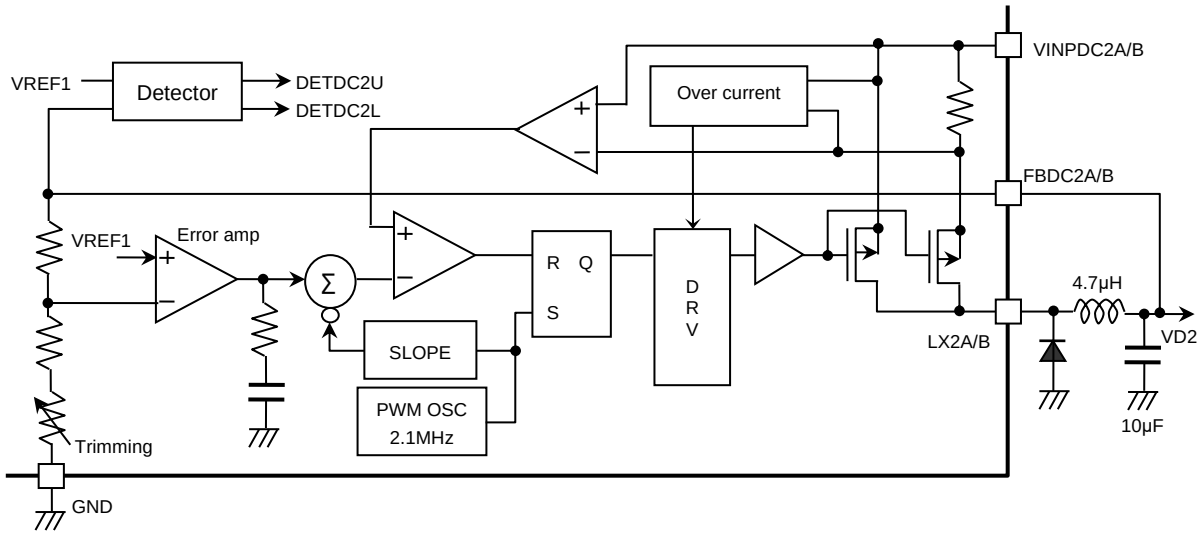


Fig.4-6-2 DCDC2 block diagram

4.6.1 Output protect function

To operate the PMIC safety, interval operation would start in the case of output abnormal conditions. Each DCDC operation is as follows.

◆ **DCDC1**

When DCDC1 fall into unusual condition, DCDC1 enters to protect mode.

The protection circuit monitors output current and output voltage. In the case that over voltage is detected on DCDC1, it would force to stop the DCDC1's and DCDC2's switching. When over current or low voltage are detected with taking over detect mask time, then DCDC1 would enter interval operation. The mask time of over current detection can be set via SPI. During protect mode, the DCDC1 tries to resume its operation regularly. The interval time of resuming can be set via SPI as well. When root cause of unusual condition is taken away, the DCDC1 comes to operate normally.

And when over voltage is detected in either DCDC2 or LDO2, DCDC1 would operate in protect mode as well. Before DCDC1's operation comes into protect mode, INTOUT asserts low.

The operation timing is shown in below figure. And detect mask times are described in next table.

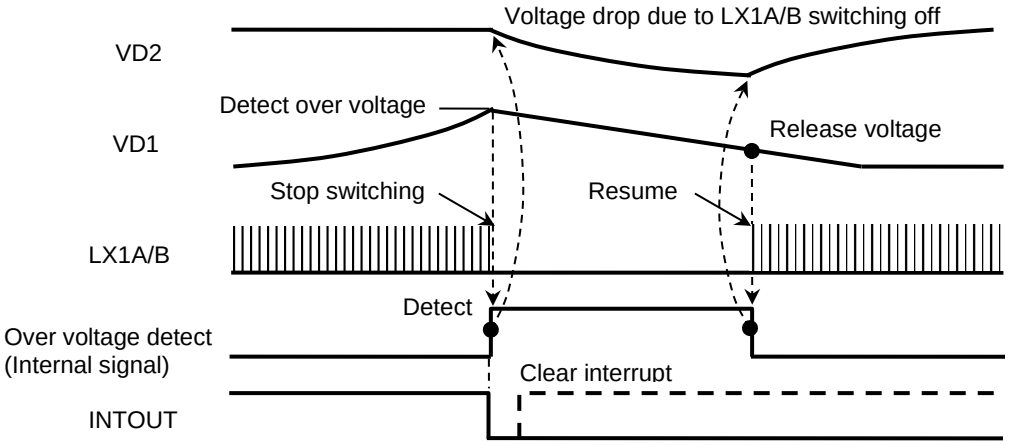


Fig.4-6-3 DCDC1 protect function behavior 1

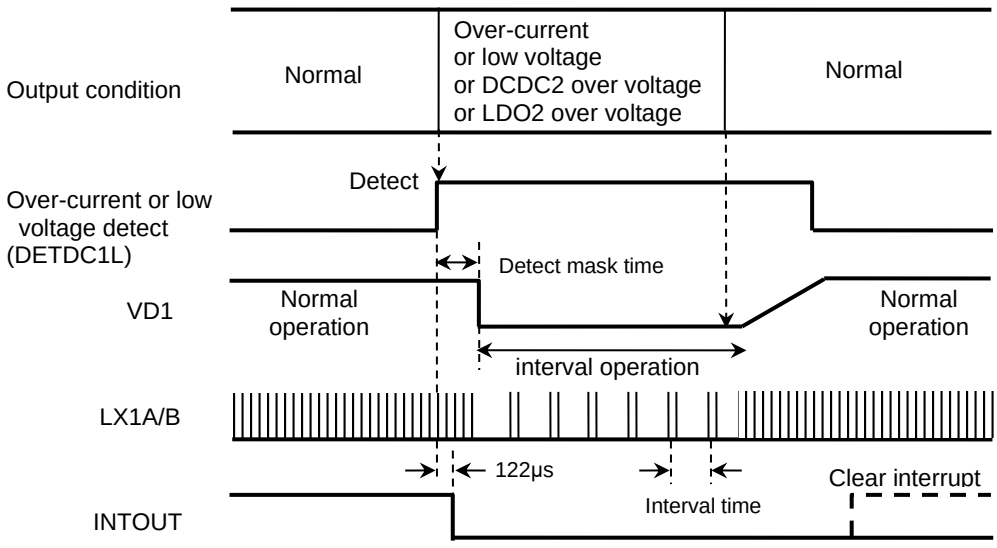


Fig.4-6-4 DCDC1 protect function behavior 2

Table 4-6-1 Detect mask time

Over current detect	Low voltage detect	DCDC2 detect
Variable	92µs	92µs

◆ **DCDC2**

DCDC2's protect operation is almost same as DCDC1's.

The protection circuit monitors load current and output voltage. When over current or low voltage is detected with taking over detect mask time, then DCDC2 would enter interval operation. The mask time of over current detection can be set via SPI. During protect mode, the DCDC2 tries to resume its operation regularly. The interval time of resuming can be also set via SPI. In the case of over voltage is detected, it would force to stop switching of both DCDC1 and DCDC2. Before DCDC2's operation comes into protect mode, INTOUT asserts low.

The operation timing is shown in below figure. And detect mask times are described in below table.

Low voltage detection can be added to reset condition by setting configuration register.

When low voltage is detected, reset occurs immediately. Reset asserts low while VD2 is below low voltage detection level. After VD2 comes up usual output and 12ms passes, the reset is released.

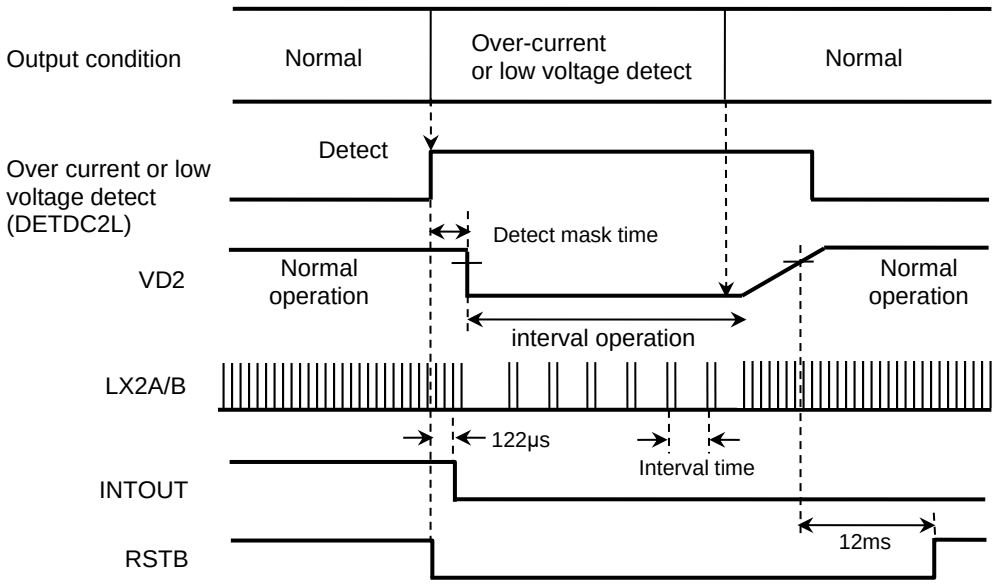


Fig.4-6-5 DCDC2 protect function behavior 1
(In case of DL2RSTB bit in CONF register is set "1".)

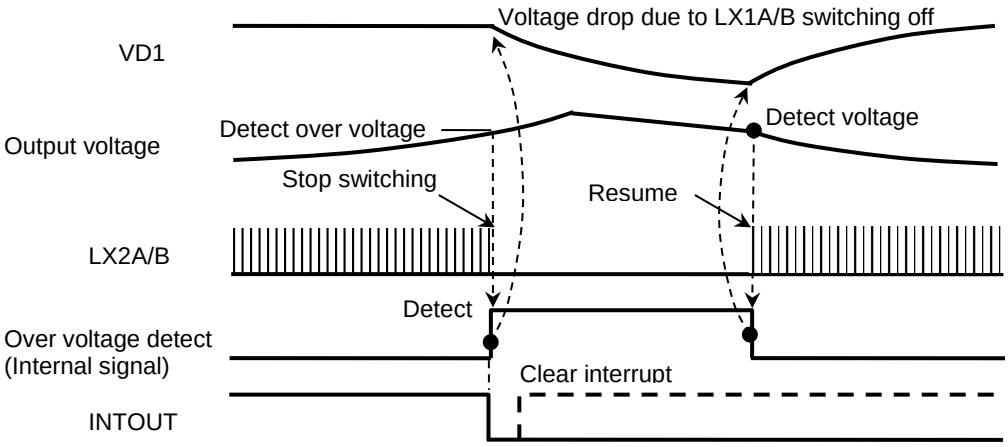


Fig.4-6-6 DCDC2 protection behavior 2

Table 4-6-2 Protect detect mask time

Over current detect	Low voltage detect
Variable	92µs

4.6.2 Register

The contents of protect function setting are described here.

➢ DCDC protection mode setting

■ Address (DCLIM) : 1BH

A5	A4	A3	A2	A1	A0
0	1	1	0	1	1

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
INTIME2(1:0)		DTIME2(1:0)		INTIME1(1:0)		DTIME1(1:0)	

■ Setting contents

Interval time and over current detect mask time for DCDC2.

INTIME2(1:0)		Interval time
D7	D6	
0	0	15.6ms
0	1	31.2ms *
1	0	124.9ms
1	1	249.9ms

DTIME2(1:0)		Detect mask time
D5	D4	
0	0	122µs *
0	1	122µs
1	0	610µs
1	1	1098µs

* Default setting

Interval time and over current detect mask time for DCDC1.

INTIME1(1:0)		Interval time
D3	D2	
0	0	15.6ms
0	1	31.2ms *
1	0	124.9ms
1	1	249.9ms

DTIME1(1:0)		Detect mask time
D1	D0	
0	0	122µs *
0	1	122µs
1	0	610µs
1	1	1098µs

* Default setting

Note1: This register is not initialized by RSTB.

4.6.3 Electrical characteristics

Characteristics noted under conditions, GND=0V, unless otherwise noted. The condition is Tj=-40 to 150°C, unless otherwise specified.

◆ **DCDC1**

Co=4.7µFx2 (ESR=0.0~0.1Ω), L=3.3/4.7µH

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output voltage	VoDC1	Io=0~1000mA (DC)	5.40	5.70	6.00	V
OSC frequency	Fosc1		1890	2100	2310	kHz

◆ **DCDC2**

Co=10µF (ESR=0.0~0.1Ω), L=3.3/4.7µH

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output voltage	VoDC2	Io=0~700mA (DC)	1.225	1.25	1.275	V
OSC frequency	Fosc2		1890	2100	2310	kHz

Note: “(DC)” means it doesn’t include AC factor like transient response.

4.7 Power Rail Sequence

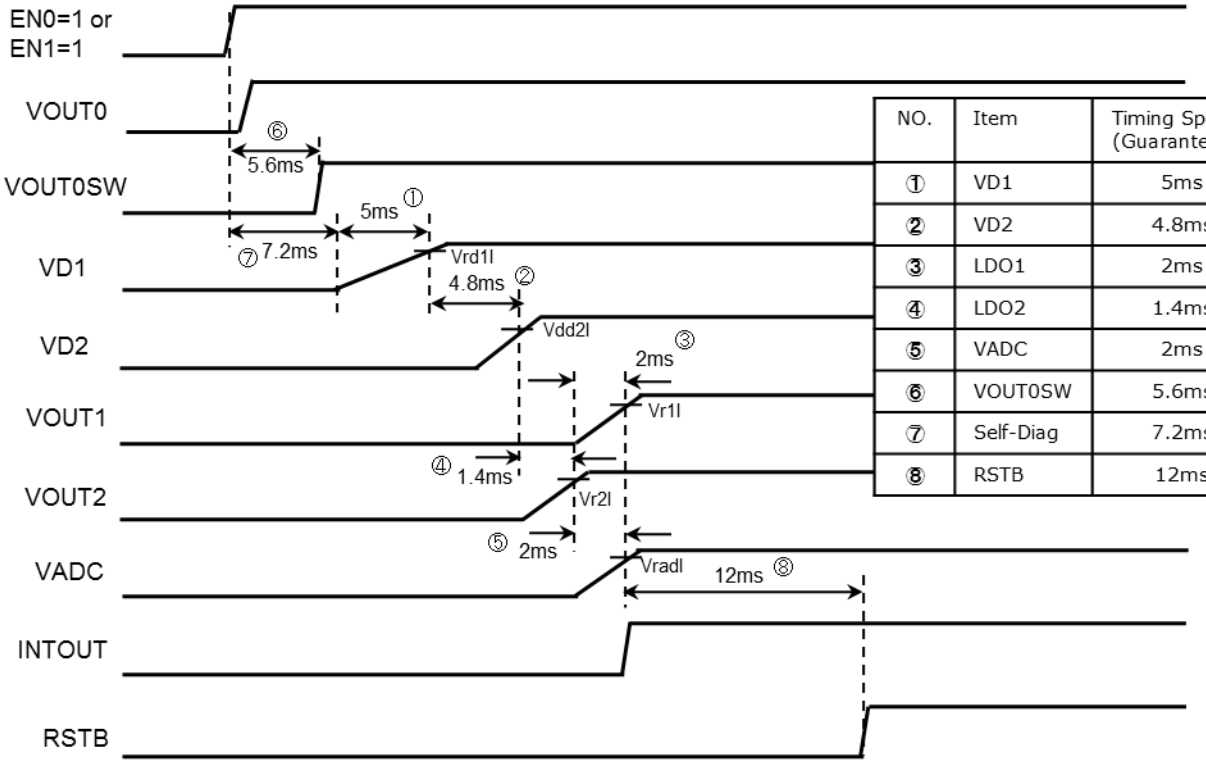
When battery voltage is applied to the PMIC, the LDO0 rises up first. After the LDO0 rises up, the other regulators are powered up in the sequence automatically. Therefore, user doesn't need to consider power rail sequence at all. After all regulators rise up, reset signal is released.

4.7.1 Power up sequence

After the PMIC is applied supply voltage, all regulators rise up automatically. Difference of rise up time between regulators is suitable for RENESAS MCUs.

◆ **Power up with using EN0 or EN1**

While supply voltage is applied, the PMIC can be controlled by EN0 or EN1 pin. After EN0 or EN1 is entered, self-diagnosis execution starts first. The order of each regulator's rising is controlled by internal sequencer. After all regulators rise up, interrupt signal is released. Further 12ms passes, reset signal is released as well. Each timing specification is specified in the below table and guaranteed by design.

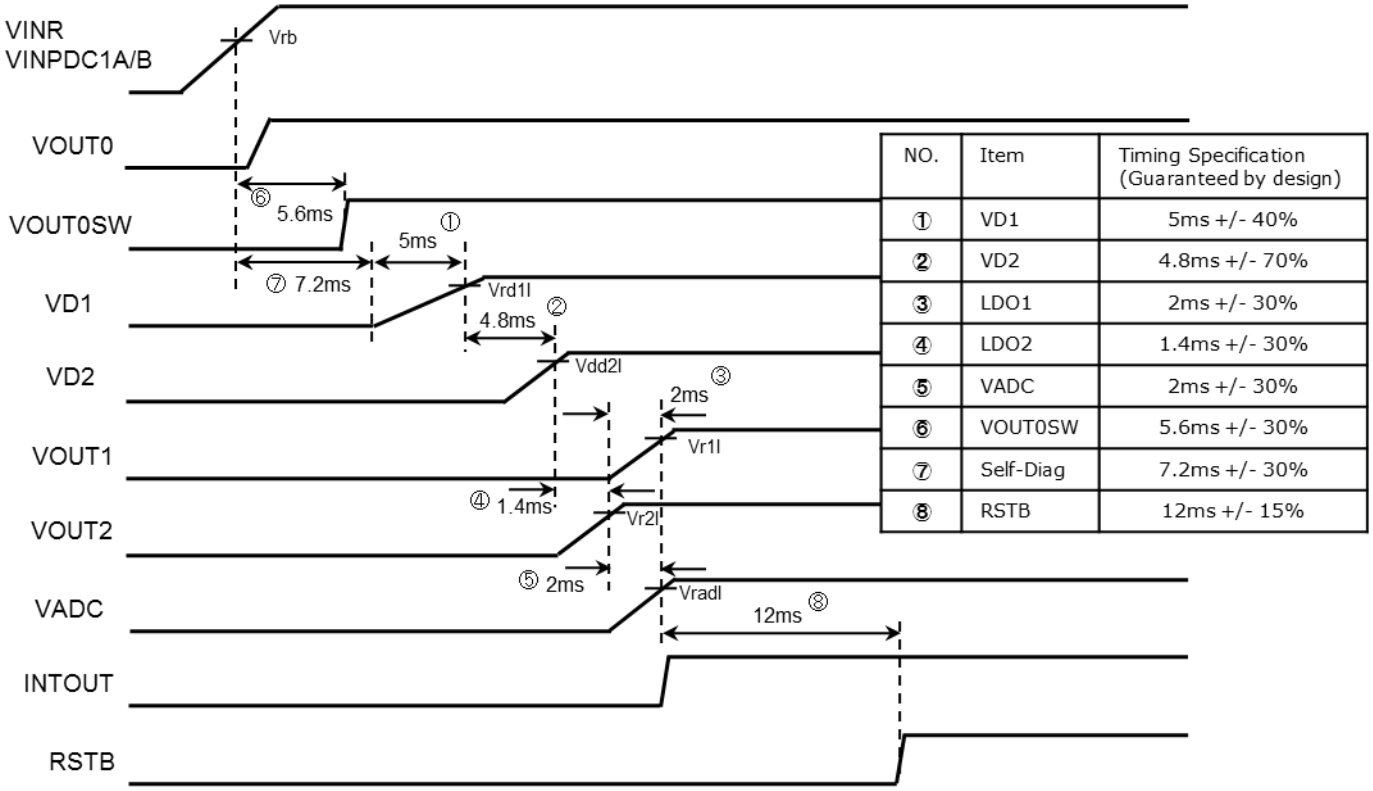


NO.	Item	Timing Specification (Guaranteed by design)
①	VD1	5ms +/- 40%
②	VD2	4.8ms +/- 70%
③	LDO1	2ms +/- 30%
④	LDO2	1.4ms +/- 30%
⑤	VADC	2ms +/- 30%
⑥	VOUT0SW	5.6ms +/- 30%
⑦	Self-Diag	7.2ms +/- 30%
⑧	RSTB	12ms +/- 15%

Fig. 4-7-1 Power up timing (with EN0/1 setting)

◆ **Power up without using EN0 or EN1**

When EN0 and/or EN1 are connected to supply voltage and supply voltage comes up, power up sequence starts automatically. Power up sequence behavior is same as using EN0 or EN1. Each timing specification is specified in the below table and guaranteed by design.

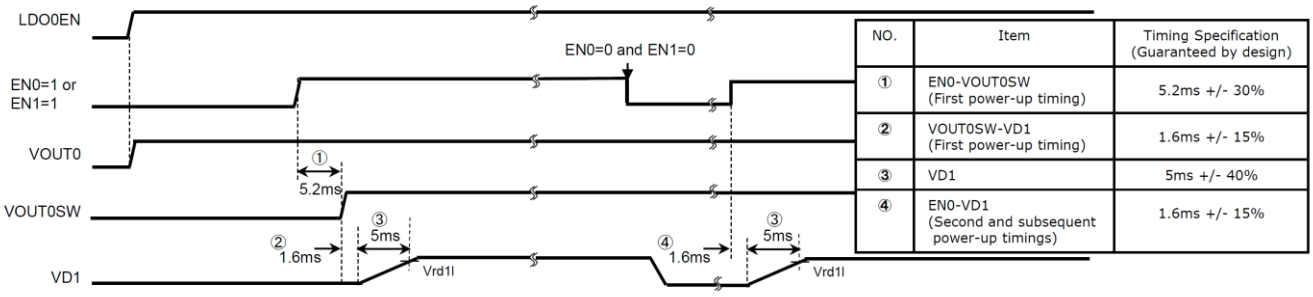


NO.	Item	Timing Specification (Guaranteed by design)
①	VD1	5ms +/- 40%
②	VD2	4.8ms +/- 70%
③	LDO1	2ms +/- 30%
④	LDO2	1.4ms +/- 30%
⑤	VADC	2ms +/- 30%
⑥	VOUT0SW	5.6ms +/- 30%
⑦	Self-Diag	7.2ms +/- 30%
⑧	RSTB	12ms +/- 15%

Fig. 4-7-2 Power up timing (Supply power coming up)

◆ **Power up after LDO0EN**

While supply voltage is applied to the PMIC, only LDO0 can rise up with using LDO0EN control. The PMIC executes self-diagnosis after either EN0 or EN1 rises. After either EN0 or EN1 set up, self-diagnosis of detectors are executed and power-up sequence starts. Each timing specification is specified in the below table and guaranteed by design.



NO.	Item	Timing Specification (Guaranteed by design)
①	EN0-VOUT0SW (First power-up timing)	5.2ms +/- 30%
②	VOUT0SW-VD1 (First power-up timing)	1.6ms +/- 15%
③	VD1	5ms +/- 40%
④	EN0-VD1 (Second and subsequent power-up timings)	1.6ms +/- 15%

Fig. 4-7-3 Power up timing (Supply power coming up)

Note: Please make EN0 or EN1 high in the condition of VINR > Vrb.
Otherwise, the state is shifted to power down.

4.7.2 Power down sequence

When the PMIC powers down, all regulators fall down automatically. Difference of fall down time between regulators is suitable for RENESAS MCUs.

◆ **Power down with using EN0 or EN1**

When the PMIC is stopped operating by EN0 or EN1, interrupt and reset signal would be asserted.

After the PMIC sets RSTB to low, power down sequence starts automatically. If the system needs to maintain VOUT0 output, LDO0EN should be set high before LDO0 power down. The time deviation in below figure is +/-10%. That value is guaranteed by design.

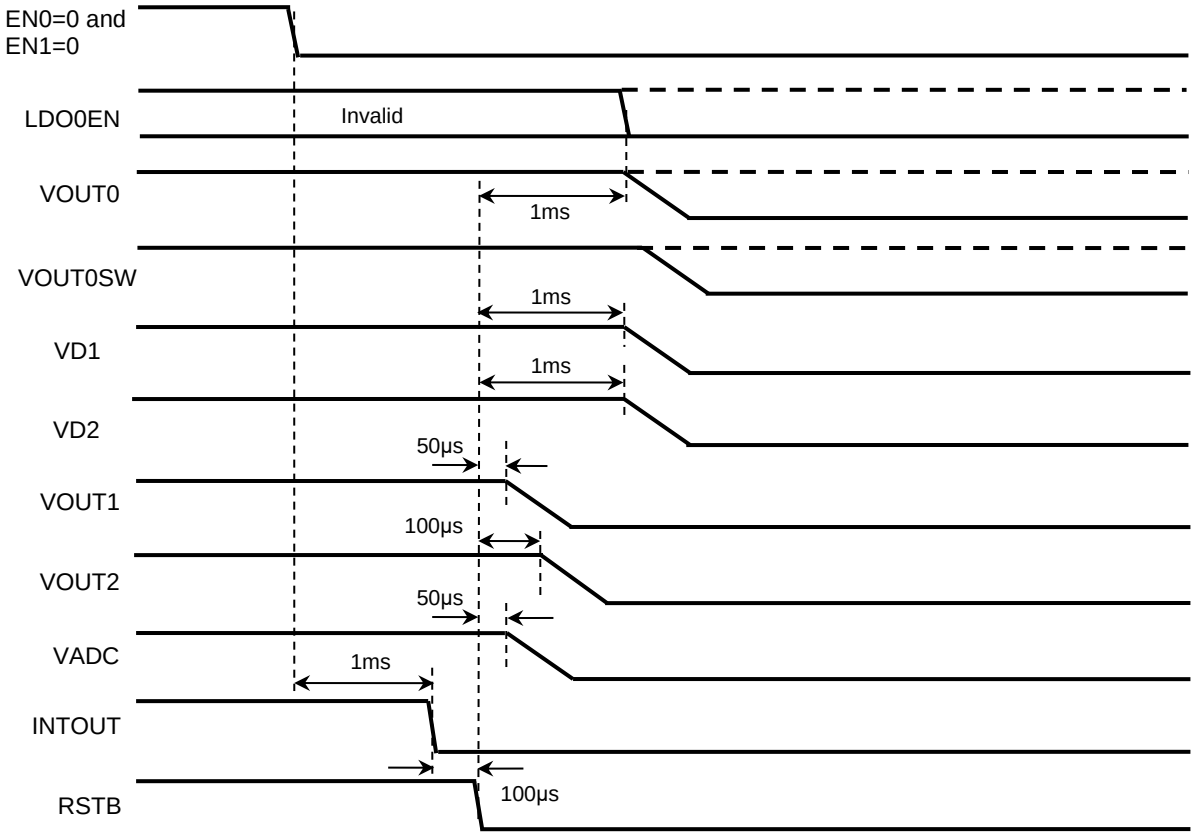


Fig. 4-7-4 Power down timing (with EN0/1 setting)

◆ **Power down without using EN0 or EN1**

Output behavior in low supply voltage is shown in below figure. Even though the supply voltage of the PMIC goes down lower than the output voltage, regulators can generate output voltage. But output voltage becomes to be almost same as supply voltage.

When supply voltage falls down and LDO1 goes across Vd1l1, the PMIC asserts SUSP signal as a warning. Further the supply voltage falls down across Vdb, the PMIC asserts RSTB and all regulators except LDO0 fall down.

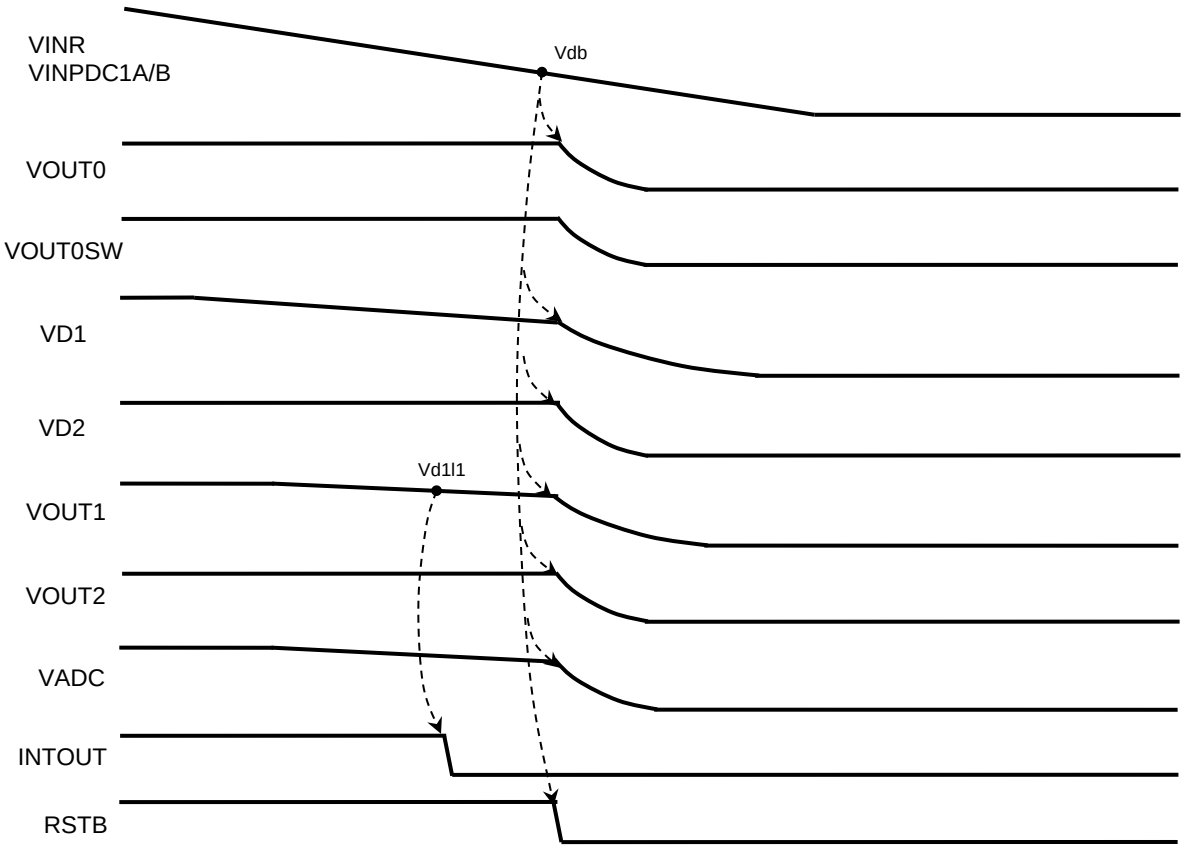


Fig. 4-7-5 Power down timing (Supply voltage falling down)

◆ **Power down except LDO0**

LDO0 and output part of DCDC1 have terminal for supply voltage respectively. Below figure shows the behavior of cutting off supply voltage for DCDC1. Since supply voltage maintains for the LDO0, the output of LDO0 generates its output. On the other hand, supply voltage of DCDC1 is cut off, the outputs of regulators which powered by DCDC1 fall down. Turn-off time of regulators is controlled by the sequencer. The time deviation in below figure is +/-10%.That value is guaranteed by design.

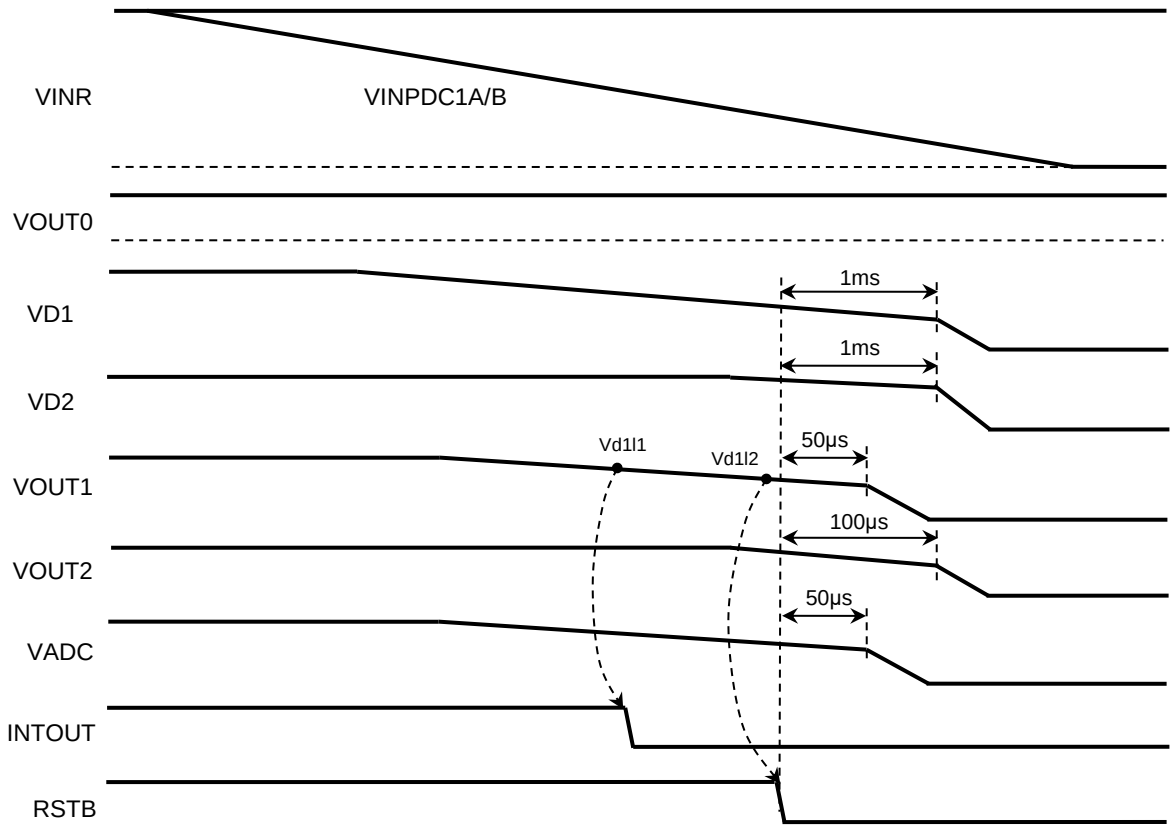


Fig. 4-7-6 Power down timing (VINPDC1A/B falling down)

4.8 Watchdog (WD) Timer

The watchdog (WD) timer can be used for monitoring the system health to prevent a runaway operation. In order to refresh WD timer (WDT), a trigger via SPI or on WDI pin is needed.

Further, to improve functional safety, it can be done with logical operation to monitor microcontroller's operation. And also watchdog time can be set via SPI.

In order to operate WD, WDENB should be set low at "P/U sequence" state. Once WD starts its operation, WDENB setting can't stop WD function. WDENB setting in the PMIC can be set in any state except "Normal" state.

◆ **WDI pin or SPI control**

There are two ways to start WD operating or refresh the timer. One way is to use WDI pin, and the other one is to use SPI. It can select WDI pin or SPI by setting configuration register. To use WDI pin is default setting.

4.8.1 Window WDT

Window WDT is implemented in the PMIC. It needs a trigger to start WD operation during first window (FW) in "Normal" state. If the trigger is not executed, a reset pulse occurs and the PMIC wait for a FW trigger again. After WD starts operating in "System monitor" state, a trigger should not be executed during Close Window (CW). If a trigger is executed, INTOUT would be asserted and enter Open Window (OW). A trigger should be executed to refresh the timer during OW. If the refreshing is not executed within designated time, a reset pulse occurs. While WDT is operating and when SUSP is asserted, WDT would stop its operating. And when SUSP is released, then WDT resumes from "Normal" state.

CW time and OW time are programmed via SPI.

4.8.2 WDT operation

Detail WD operation is described in this section. In order to clear the timer, toggling on WDI or SPI is needed.

◆ **Operation in normal**

Below figure shows normal operation of WDT when the trigger from WDI pin or SPI is entered within designated time. Certified point as a trigger is the changing point of WDI or rising edge of SPICSB.

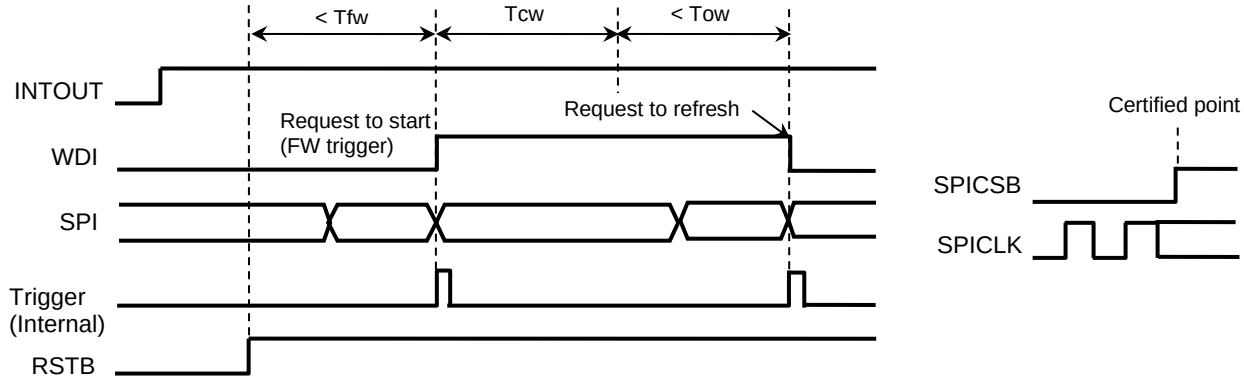


Fig.4-8-1 WDT normal operation

◆ **Behaviors in unusual operation**

When the trigger is not executed and the timer expires, then a reset occurs.

(1) No trigger in FW

When the trigger is not entered in FW, reset would occur. After that, if the triggers aren't entered, reset occurs regularly.

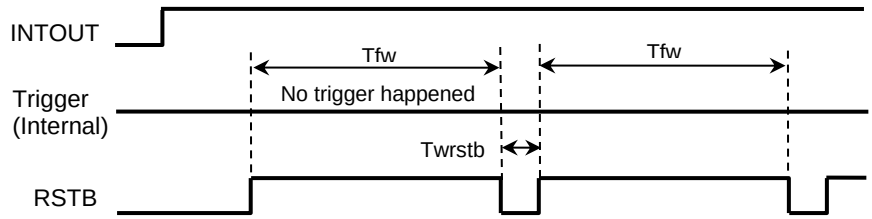


Fig.4-8-2 No trigger in FW

(2) A Trigger in CW

When the trigger is entered in CW, INTOUT would assert low.

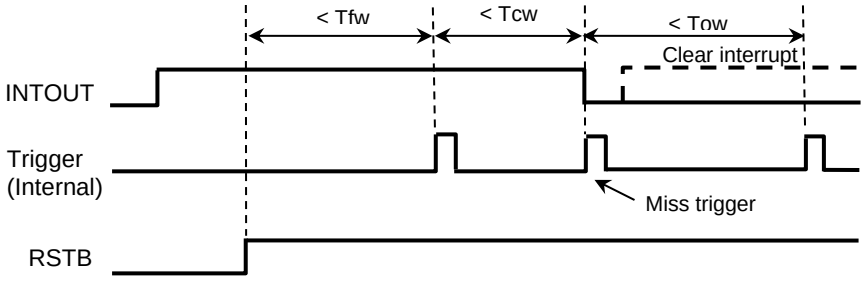


Fig.4-8-3 Trigger in CW 1

And when the configuration register is set to make reset, WD behavior is show in below figure.

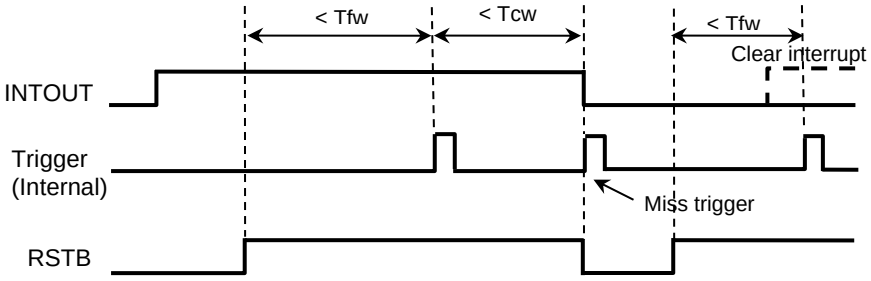


Fig.4-8-4 Trigger in CW 2

(3) No trigger in OW

When the trigger is not entered in OW, the timer expires and reset would be asserted. After reset is released, WD starts from FW again and the PMIC maintains asserting low so that microcontroller is able to know that the reset is caused by timer expire.

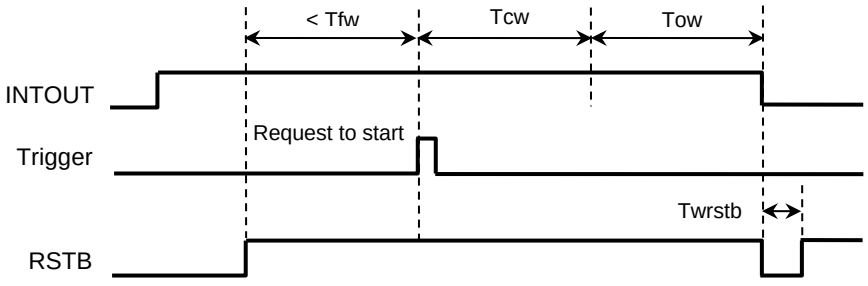


Fig.4-8-5 No trigger in OW

◆ **Suspend WD operating**

When the output voltage on VOUT1 comes down and SUSP asserts low, then WD stops its operation. And SUSP changed to high, WD resumes operation form FW.

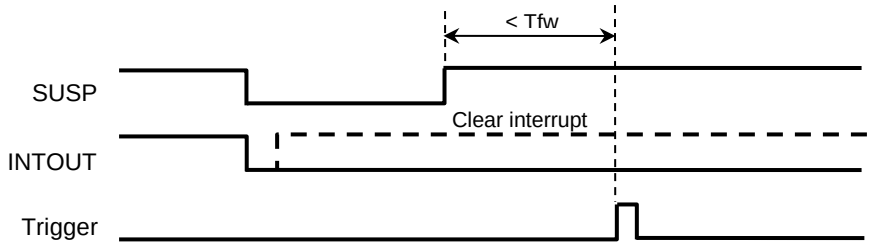


Fig.4-8-6 Suspend WD operating

4.8.3 Advanced mode

To use advanced mode, it needs to set configuration register, “SPI mode” and “Advanced mode”. This functionality is for using SPI. In this mode, it can monitor microcontroller’s and PMIC’s operation each other. After WD operation starts, microcontroller needs to obtain a “question” to send an “answer” to the PMIC. (QA monitoring) The “question” contains operand and objective data. The microcontroller should send a request to refresh WD timer with data of the “answer”. The “answer” is in accordance with the operand in the previous “question”. The PMIC refresh the WD timer and gives a point for the “answer”, and then it stores and accumulates the points to evaluation register. When accumulated point reaches designated value, a reset would happen.

If “Advanced mode” is not selected, only refreshing the WD timer is executed.

Note: In the advanced mode, CW rate to watchdog time is fixed 50%.

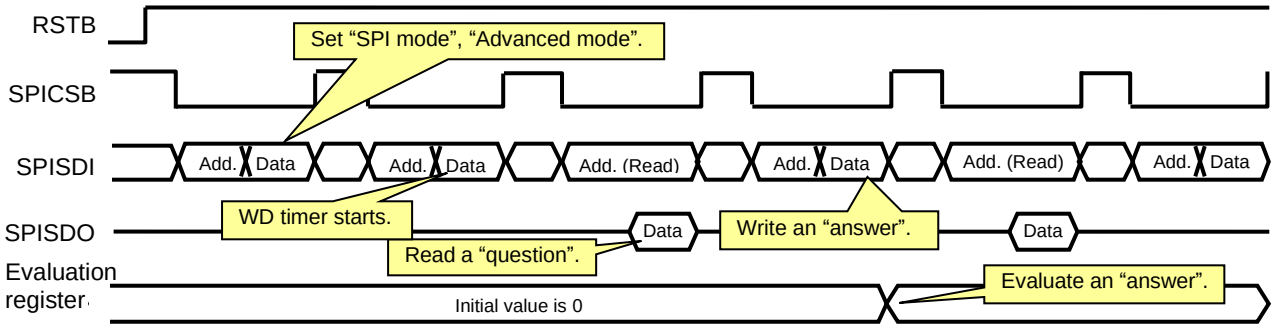


Fig.4-8-7 QA monitoring operation

◆ **Procedure**

Below figure illustrates procedure in accordance with Fig.4-8-5 and behavior scenario is described in below.

- Select “SPI mode” and “Advanced mode”
  In order to control WD via SPI and use advanced mode, it needs to set configuration register first. In above example, D3 bit and D1 bit are set 1.
- Request to start
  In order to start WD function, WD trigger address is needed to enter. The data accompanied with WD trigger address is not defined, but parity bit is checked.
- Read “question”
  The PMIC generates random data as a question containing 2bit operand and 6bit objective data. Microcontroller must read the question to respond with an answer.
- Write “answer”

  Microcontroller should enter an answer to the obtained data. The address data to enter an answer is same as a WD trigger address and refresh the WD timer simultaneously. The data contains 2bit operand and 6bit data operated along with the operand.

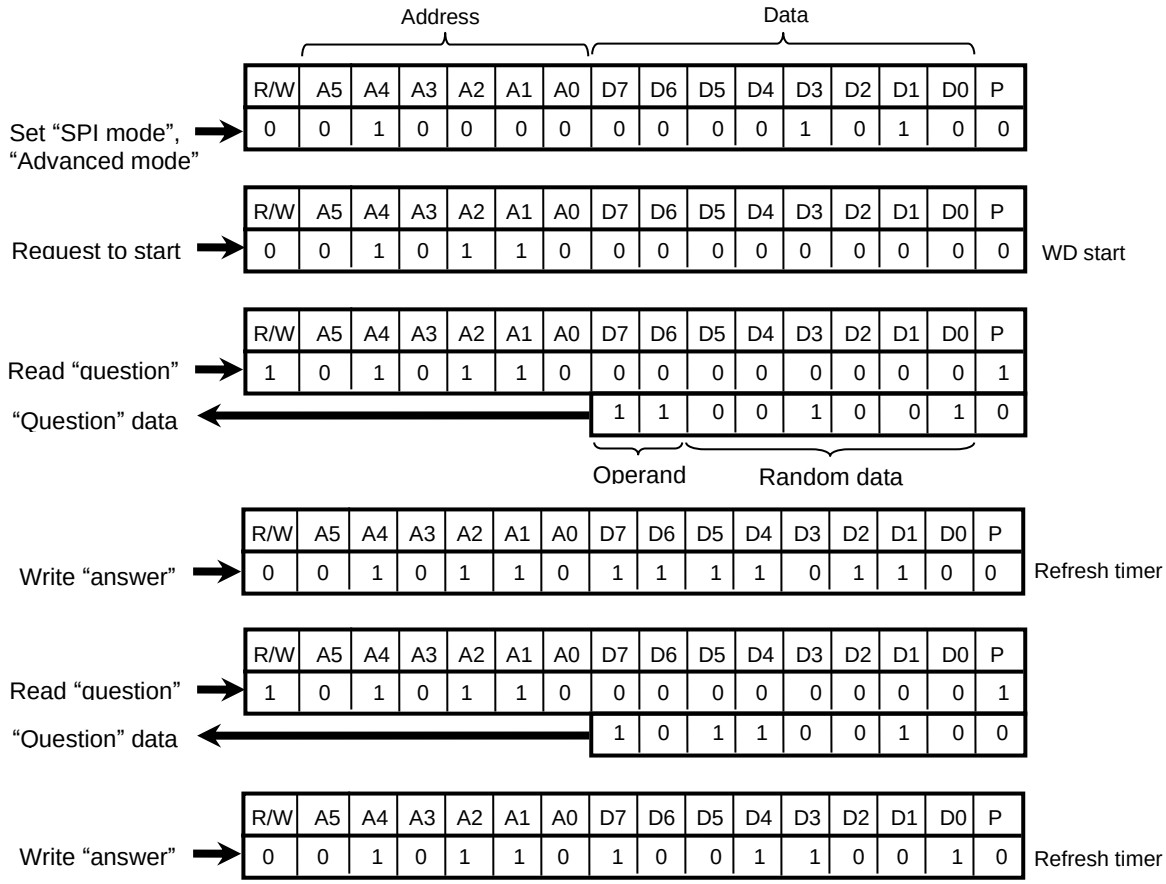


Fig.4-8-8 Refresh procedure of advanced mode

◆ **Evaluation register**

The PMIC gives a point to the entered answer and has a register to accumulate the points. The accumulated value is read via SPI. The value to occur reset can be set in a register. When the WD starts, accumulated point is 0. Or evaluation is executed in OW.

- Right answer

When an answer is entered to the PMIC and it is expected, it gives “-1” point to evaluation register. If accumulated value in evaluation register is 0, it maintains the value 0.

In below example, a right answer A1 is entered as a response of Q1. And then, “-1” is added to current value of evaluation register.

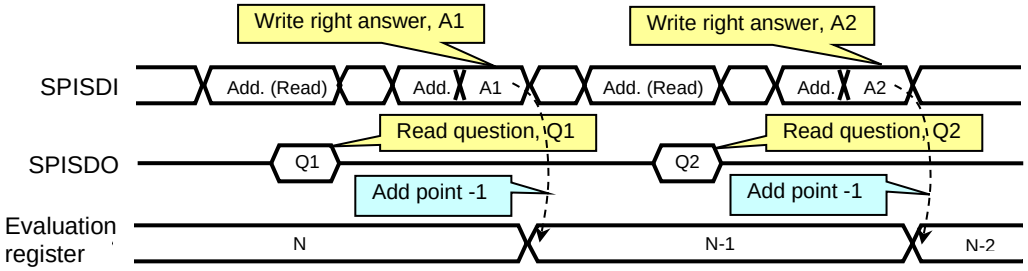


Fig.4-8-9 Evaluation for entered answer (Right answer)

- Wrong answer

When the answer is not expected answer, it gives “+2” point to evaluation register. And next question is same as previous one.

In below example, a wrong answer Ax is entered as a response of Q1. And then, “+2” is added to current value of evaluation register. In spite of wrong answer, the PMIC refreshes the WD timer.

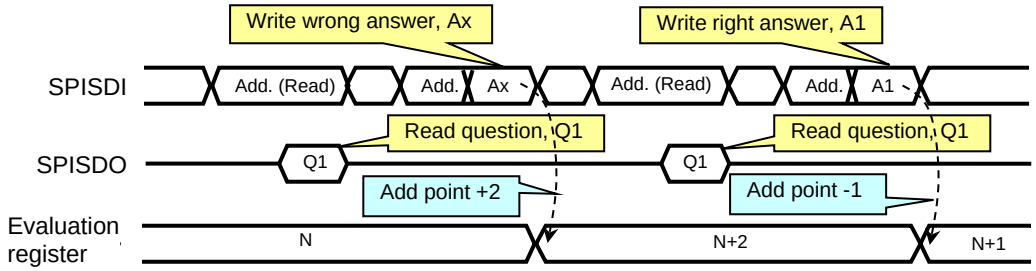


Fig.4-8-10 Evaluation for entered answer (Wrong answer)

- All answer bits are zero

When entered bits of the answer are all 0, the PMIC gives “+3” point to evaluation register. Of course, the PMIC never create a question which leads the answer’s bits are all 0.

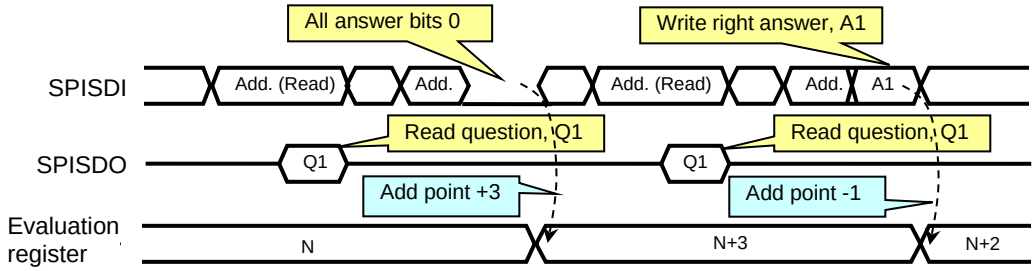


Fig.4-8-11 Evaluation for entered answer (All answer bits are zero)

- Evaluation term

The answer is evaluated in OW. The answer in CW is ignored whether the answer is right or wrong. And it makes INTOUT assert low.

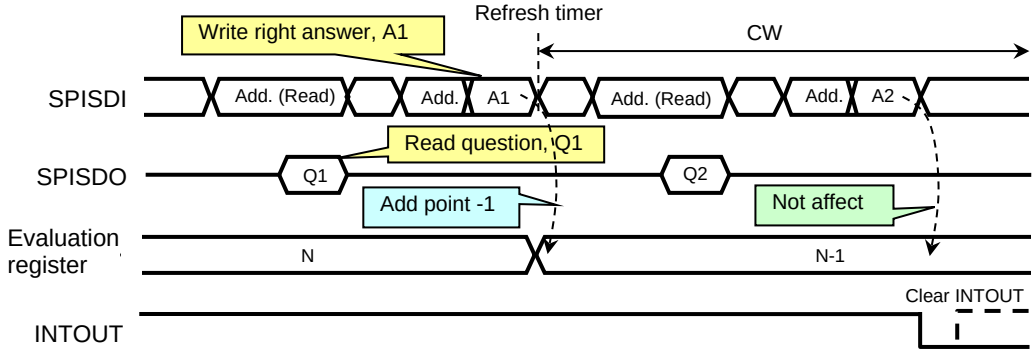


Fig.4-8-12 Evaluation for entered answer (In appropriate term)

- Reset by accumulated value

Through QA monitoring, when accumulated value is more than designated value, then reset occurs.

In below example, reset value of evaluation register is more than “N+1”. It assumes that the current value of the evaluation register is “N”. When a wrong answer is entered, the value comes up to “N+2”. Eventually, reset occurs after 4µs passes. Pulse width of the reset is 2ms.

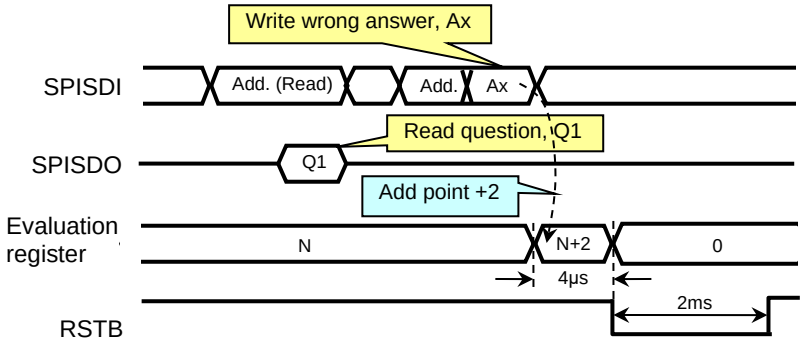


Fig.4-8-13 Evaluation for entered answer (In appropriate term)

4.8.4 Register

The contents of WDT setting are described in this section.

➢ WD trigger

If advanced mode is not selected in configuration register, only entering address allows refresh the timer. (The data (D7-D0) is ignored but parity bit is checked.)

■ Address (WDTRG) : 16H

A5	A4	A3	A2	A1	A0
0	1	0	1	1	0

■ Register

To evaluate “answer”, microcontroller should enter below data in accordance with the question.

D7	D6	D5	D4	D3	D2	D1	D0
OPE(1:0)		Data with requested operation					

Microcontroller should obtain below “question”.

Do7	Do6	Do5	Do4	Do3	Do2	Do1	Do0
OPE(1:0)		SUBJ(5:0)					

■ Contents

Microcontroller should operate with below received D5-D0 bits.

OPE(1:0)		Control contents
Do7	Do6	
0	0	Copy Do5-Do0 bits for D5-D0
0	1	Shift D05-Do0 bits to the 1bit left for D5-D0
1	0	Shift Do5-Do0 bits to the 1bit right for D5-D0
1	1	Invert Do5-Do0 bits for D5-D0 *

* Default setting

Subjected data bits are created by the PMIC.

SUBJ(5:0)	Control contents
Do5-Do0	Random data

Note: Default data is all “1” in SUBJ(5:0).

Note: When data is shifted to left or right, “0” is inserted into empty Do0 or Do5.

➢ Watch dog time

This register can set watch dog time and rate of close window to watchdog time.

This register is a secured register. It is necessary to enter “key” code before enter this request. (See “4.2.3 Secured request”.)

■ Address (WDTIME) : 17H

A5	A4	A3	A2	A1	A0
0	1	0	1	1	1

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	-	CWSET(1:0)		WDTIME(1:0)	

■ Setting contents

Below table shows OW and CW time setting.

CWSET(1:0)		Setting time
D3	D2	
0	0	CW rate : 0% *
0	1	CW rate : 25%
1	0	CW rate : 50%
1	1	CW rate : 75%

* Default setting

WDTIME(1:0)		Setting time
D1	D0	
0	0	WD time : 8ms
0	1	WD time : 16ms
1	0	WD time : 32ms
1	1	WD time : 64ms *

* Default setting

Caution: CWSET is not available in “Advanced mode”.

Warning: Please do not change setting during WD running.

➢ Evaluation value

The accumulated value of QA monitoring is read via this register.

■ Address (QAEVA) : 19H

A5	A4	A3	A2	A1	A0
0	1	1	0	0	1

■ Register (Below bits are read only.)

Do7	Do6	Do5	Do4	Do3	Do2	Do1	Do0
ACCVA(7:0)							

➢ Accumulated value for reset

This register can set a value to occur reset.

■ Address (RSTVA) : 1CH

A5	A4	A3	A2	A1	A0
0	1	1	1	0	0

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
SETVA(7:0)							

■ Setting contents

Any numbers is allowed to set this register. The default value of this register is “255”.

But setting number of “zero” is prohibited. Since reset always occurs when “Advanced mode” is selected in configuration register.

4.8.5 Electrical characteristics

◆ Watchdog time

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
First window time	Tfw		230.4	256.0	281.6	ms
Watch dog time1	Twd1	Setting: WDTIME(1:0)=(0,0)	7.2	8.0	8.8	ms
Watch dog time2	Twd2	Setting: WDTIME(1:0)=(0,1)	14.4	16.0	17.6	ms
Watch dog time3	Twd3	Setting: WDTIME(1:0)=(1,0)	28.8	32.0	35.2	ms
Watch dog time4	Twd4	Setting: WDTIME(1:0)=(1,1)	57.6	64.0	70.4	ms

◆ WDI pulse

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Rise time	trwdi		-	-	10	ns
Fall time	tfwdi		-	-	10	ns
Pulse width	twwdi		2.0	-	-	µs

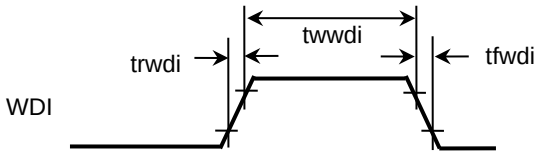


Fig.4-8-14

4.9 Reset

The PMIC generates reset signal. RSTB pin should be connected to an external pull-up resistor. The pull-up resister can be connected to 5V or 3.3V level.

4.9.1 Reset factor

There are several cases to force reset happen. Reset signal would happen by following case.

- LDO1 output
  The output voltage downs to Vd1l2 (3.09V typ) supply voltage down such as crank pulse situation or over current sinks from LDO1's output. These situations are regarded as unusual condition so that the PMIC generate reset signal. Please refer to "4.7 Power rail sequence".
- No first trigger to start WDT operation
  After initial reset is released, the WDT needs 1st trigger to start its operation. If the trigger is not entered, it generates 2ms reset pulse. Please refer to "4.8 Watchdog Timer".
- WD timer expires in Open Window and Close window
  After WDT starts to operate, the system should enter a request to refresh WD timer. If no trigger is entered and the timer expires, then it generates 2ms reset pulse. And when configuration register is set, it makes reset by trigger in close window. Please refer to "4.8 Watchdog Timer".
- Reach the designated number in QA monitoring
  In "Advanced mode" of WDT operation, evaluation register has accumulated evaluation value. If the value reaches designated number, it generates 2ms reset pulse. Please refer to "4.8.3 Advanced mode".
- Microcontroller's safety monitor
  The PMIC monitors ERROR1/2 pins indicating microcontroller's safety operation. If the system needs reset when ERROROUT1 or ERROROUT2 pin of microcontroller indicates something happens, it needs to set configuration register. Please refer to "4.10 Specified Output Pins".
- EN0, EN1
  Once either EN0 or EN1 are set 1, the PMIC starts its operation. When both EN0 and EN1 turn to 0, reset occurs. Please refer to "4 PMIC function".
- Thermal shut down
  Before the PMIC enters thermal shut down, reset occurs and set the register as a reset factor.
- Low voltage detection in DCDC2 and LDO2
  It needs to set "configuration register". Detail is described in "4.1.4 Configuration register".
- Low voltage of supply voltage
  In order to prevent malfunction of the PMIC, the PMIC asserts reset below Vdb (3.7V typ.) supply voltage.

4.9.2 Reset factor register

The PMIC provides reset factor which indicates what caused abnormal reset. These registers are initialized by DET0O which indicates LDO0 powered up. In other words, the registers are initialized only when the PMIC starts to operate.

Table 4-9 Reset factor

Reset factor	Symbol	Note
Low voltage detection on VOUT1	LVLDO1	
Low voltage detection on VD2	LVDC2	With setting configuration register
Expired watch dog time	WDEXP	
Thermal shut down	TSDTMP	
Low voltage detection on VOUT2	LVLDO2	With setting configuration register

➢ Reset factor

The factors which cause occurring reset are lined up in this register. Even after reset is released, it can recognize what factor causes reset.

■ Address (RSTFAC) : 12H

A5	A4	A3	A2	A1	A0
0	1	0	0	1	0

■ Register (Below bits are read only.)

Do7	Do6	Do5	Do4	Do3	Do2	Do1	Do0
-	-	-	LVLDO2	TSDTMP	WDEXP	LVDC2	LVLDO1

■ Contents

Bit	Contents
0	No interrupt request *
1	Interrupt request

* Default setting

Note1: This register is not initialized by RSTB.

Note2: If “CWRSTB” bit in CONF register is set “1”, “WDEXP” bit will be set “1” as well when WD trigger is executed during CW.

➢ Reset factor clear

Reset factor clear for “RSTFAC” register is placed in this address. If all contents of this address are cleared, “INTRSFG” bit of “INTFAC” register is cleared, too.

■ Address (RSTFCL) : 13H

A5	A4	A3	A2	A1	A0
0	1	0	0	1	1

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	CLLVLDO2	CLTSDTMP	CLWDEXP	CLLCDC2	CLLVLDO1

■ Contents

Bit	Contents
0	No change *
1	Clear interrupt

* Default setting

➢ Reset factor mask

Reset factor mask for “RSTFAC” register is placed in this address.

■ Address (RSTFMSK) : 14H

A5	A4	A3	A2	A1	A0
0	1	0	1	0	0

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
-	-	-	MSKLVLDO2	MSKTSDTMP	MSKWDEXP	MSKLVDC2	-

■ Contents

Bit	Contents
0	No mask *
1	Execute mask

* Default setting

4.9.3 Software reset

Even though no reset factors exist, the PMIC can make reset pulse via SPI. To prevent unexpected reset, it needs one request to execute reset.

➢ Software reset

This register is a secured register. It is necessary to enter with “key” code. (See “4.2.3 Secured request”.)

■ Address (SFTRST) : 1DH

A5	A4	A3	A2	A1	A0
0	1	1	1	0	1

■ Register

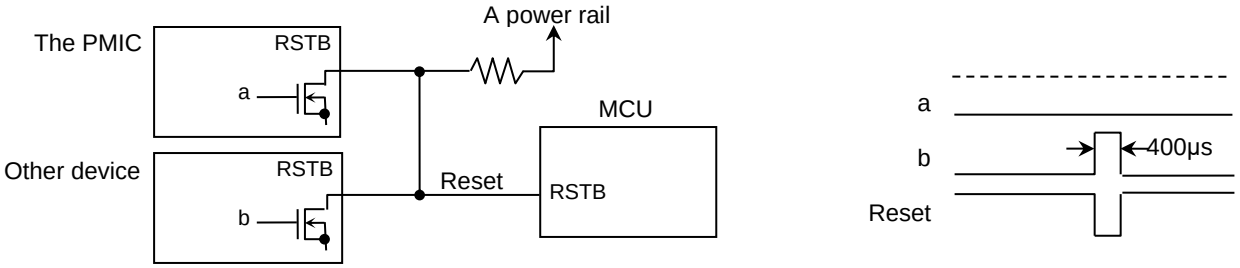
Do7	Do6	Do5	Do4	Do3	Do2	Do1	Do0
RDMKEY(7:0)							

■ Setting content

- Should enter RDMKEY data which is obtained by reading PRTCT register.

4.9.4 External reset

RSTB should be pulled up to a power rail with resister. Since RSTB is O/D, RSTB is able to be wired to reset pin of other device. (See below figure. The other reset should be also O/D.) To avoid accidental reset of other device, more than 400µs of forced reset is needed.



(a) Wired reset (b) Narrow reset pulse

Fig. 4-9-1 Wired reset

4.9.5 Electrical characteristics

◆ **Reset timing 1**

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Reset release time	Tdrstb	From initial INTOUT rise	0	-	-	ms
Reset pulse width	Twrstb		1.8	2.0	2.2	ms
Forced reset period	Tintrstb	External forced reset	360	400	440	µs

◆ **Reset timing 2**

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Detect to reset	Tuv		-	60	-	µs
Reset	Tuvrst		-	12	-	ms

Caution: The reset caused by VD2 and VOUT2 low voltage needs to set “Configuration Register”.

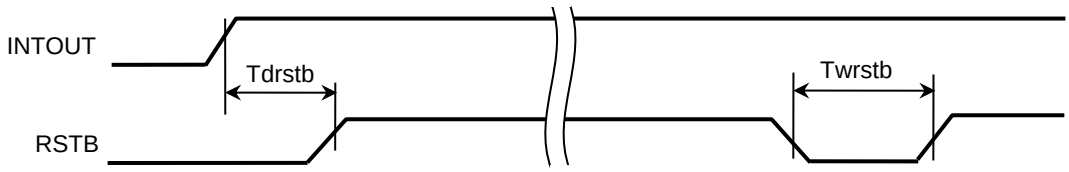


Fig. 4-9-2 RSTB timing 1

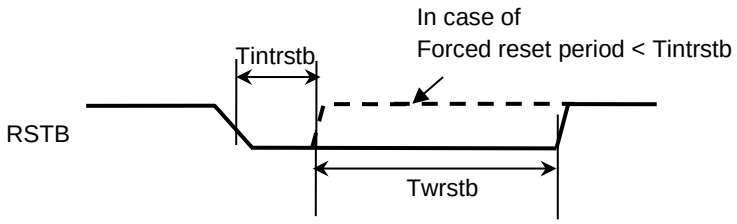


Fig. 4-9-3 Forced reset duration for internal reset

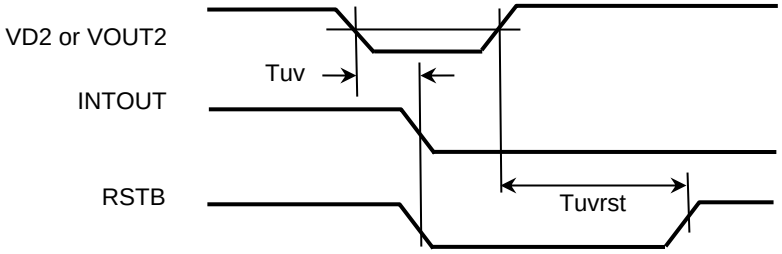


Fig. 4-9-4 RSTB timing 2

4.10 Specified Output Pins

The PMIC has some specified digital output pins. These pins serve safety operation in entire system. Operation of each pin is described in below.

◆ **Low voltage indicator (SUSP)**

When VOUT1 which applies for MCU's I/O goes down low voltage Vd1l1 level, it asserts SUSP low. Detail detect level is shown in 4.12.4.

Additionally, it can set High/Low level via a register. This setting can be done after SUSP pin asserts high.

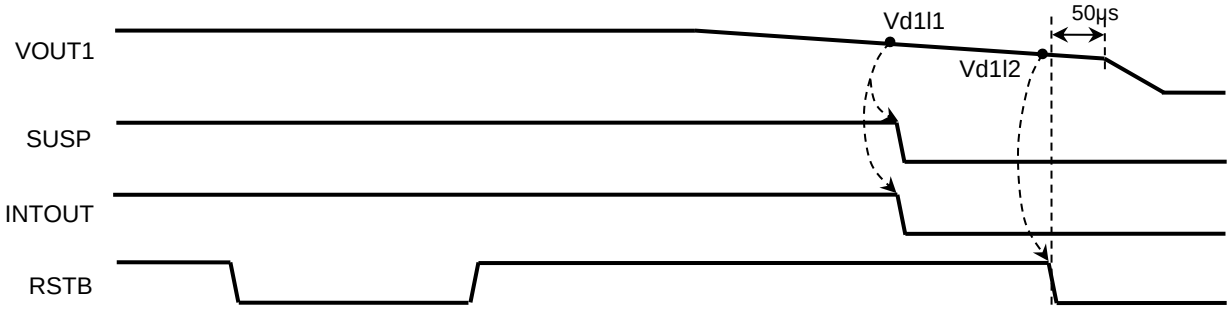


Fig. 4-10-1 SUSP timing

◆ **Safety management (FSOUT)**

Safety management is a function realized with microcontroller. RENESAS' microcontroller has output pins which indicate that unusual situation happens in the microcontroller. For more detail, please refer to user's manual of RENESAS' microcontroller.

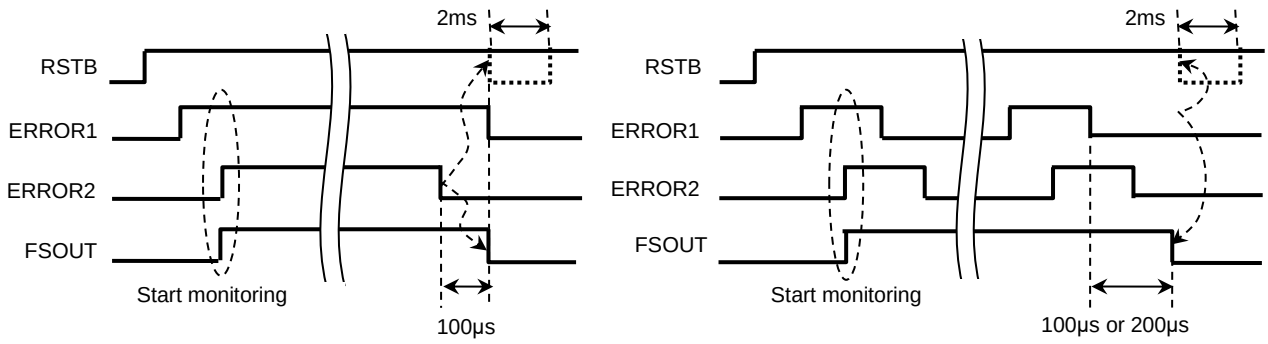
The PMIC has ERROR1/2 pin to receive the error indication signals of microcontroller. When ERROR1 or ERROR2 signal indicates error, the PMIC makes FSOUT assert low. If system needs reset when the PMIC detects unusual situation in microcontroller, it needs to set configuration register. (The behavior is illustrated as dot line in the next figure)

There are two kinds of format in unusual signal. One is static operation and the other one is dynamic operation. To determine unusual situation in microcontroller, it needs to select signal format. If static level is selected, low level on ERROR1 or ERROR2 indicates error occurs in microcontroller. And the PMIC detects low, it makes RSTB assert low. If dynamic mode, no toggling indicates error occurs in microcontroller. And the PMIC detects no toggling during 100µs or 200µs, it makes RSTB assert low as well. In initial operation, after ERROR1/2 signal rises, the PMIC starts monitoring ERROR1/2 pins.

There is a case that microcontroller assigns one monitor pin. If then, remaining pin should be connect to both ERROR1/2 pins on PWB.

When RSTB= Low, FSOUT will be also low level.

Note1: Toggling time needs to be 100µs+/-10µs or 200µs+/-20µs.



(a) Static mode (b) Dynamic mode

Fig. 4-10-2 Safety guardian operation

◆ **External control (EXCNT)**

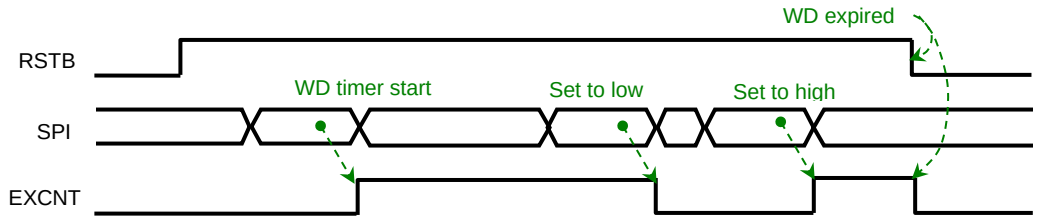
In order to control another device through the PMIC, the PMIC has a specified output pin, EXCNT.

After WDT is requested to start, EXCNT is set to high. When reset occurs by expired WD or other reasons, EXCNT asserts low. And it can control the pin via SPI. And occurring reset makes EXCNT assert low. In “Advanced mode” for WD, EXCNT asserts high after QA monitoring starts. Pin control can be done via SPI as well.

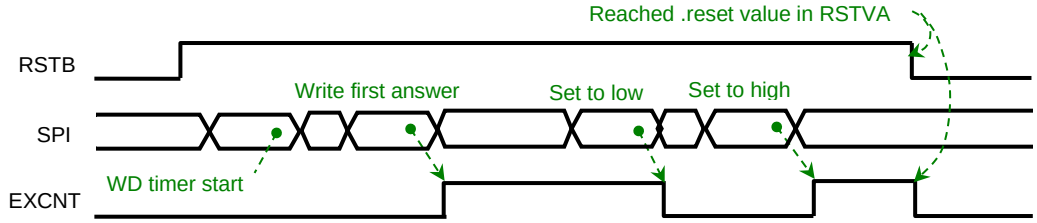
In the case not to occur reset by setting reset mask register MSKWDEXP, when WDT expires then only EXCNT pin asserts low until the trigger is applied to start WDT. (Fig.4-10-3 (c))

Additionally, in the case to make reset by a trigger during CW, EXCNT pin asserts low by unexpected trigger in CW as well.

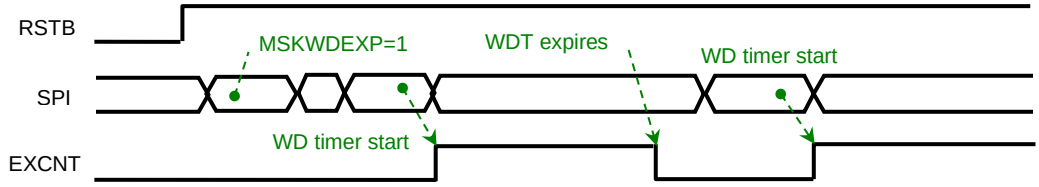
When WDT suspends by SUSP=Low (DET1L detection), EXCNT will be also low level.



(a) In WD normal mode



(b) In WD “Advanced mode”



(c) Set reset mask register not to occur reset

Fig. 4-10-3 EXCNT operation

4.10.1 Register

➢ Select pin level and microcontroller’s error indication signal mode

■ Address (PINSET) : 15H

A5	A4	A3	A2	A1	A0
0	1	0	1	0	1

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
-	-	SETSUSP	SETEXCNT	-	-	SELDT	EMODE

■ Setting contents

Register name		Control contents	Setting	
			1	0
SETSUSP	D5	SUSP pin control	Set high *	Set low
SETEXCNT	D4	EXCNT pin control	Set high *	Set low
SELDT	D1	ERROR toggle expire time	100µs	200µs *
EMODE	D0	Error indication mode	Dynamic	Static *

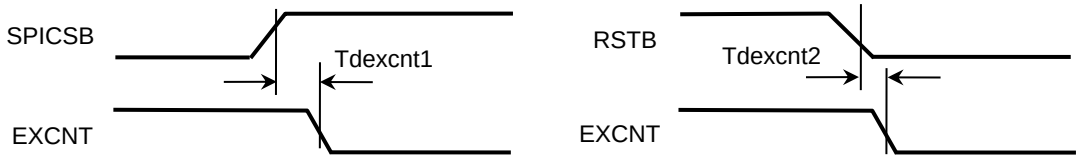
* Default setting

Note1: SETEXCNT setting is available after WD timer starts.
Note2: Setting of the SELDT bit is effective at EMODE=1 (dynamic mode).
Note3: When EMODE=0(static mode), expire time is 100µs fixing.

4.10.2 Electrical characteristics

◆ **External control (EXCNT)**

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Delay time 1	Tdexcnt1	From SPICSB rise	-	-	3.0	µs
Delay time 2	Tdexcnt2	From RSTB fall	-	-	1.0	µs



(a) Low setting via SPI (b) Asserting low by reset

Fig. 4-10-4 EXCNT delay

4.11 Interrupt Signal

The purpose of interrupt signal is to inform what happened inside the PMIC to microcontroller. The INTOUT pin indicates that interrupt factor occurs and microcontroller can identify what interrupt factor is via SPI.

4.11.1 Interrupt control

When interrupt factor happens, interrupt signal is asserted. The information of interrupt factor is stored into interrupt register and microcontroller can read what the interrupt factor is. User can clear the interrupt register by writing clear register. If several interrupt factors are stored, it needs to clear all clear registers which cause interrupt assertion.

Interrupt informing can be suspended by setting interrupt mask registers. After setting these registers, interrupt is not asserted even though interrupt factor occurs.

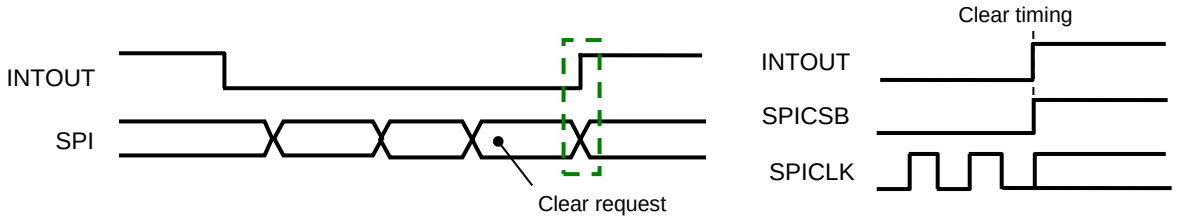


Fig. 4-11-1 Interrupt clear timing

4.11.2 Interrupt factor

The interrupt factors are listed below. Interrupt bit names are indicated as symbol.

After 500µs passed from the point where interrupt clear was executed, if interrupt factor remains such situation, INTOUT asserts low again.

Table 4-11 List of interrupt factor

Interrupt factor		Symbol	Note
Interrupt factor 1	Over voltage detection on VTRQ2	DETTRQ2U	
	Over voltage detection on VTRQ1	DETTRQ1U	
	Over voltage detection on VADC	DETADU	
	Over voltage detection on VOUT2	DET2U	
	Over voltage detection on VOUT1	DET1U	
	Over voltage detection on VD2	DETDC2U	Enters protect function
	Over voltage detection on VD1	DETDC1U	Stops its switching
Interrupt factor 2	Low voltage detection on VOUT0SW	DET0SWL	
	Low voltage detection on VTRQ2	DETTRQ2L	
	Low voltage detection on VTRQ1	DETTRQ1L	
	Low voltage detection on VADC	DETADL	
	Low voltage detection on VOUT2	DET2L	
	Low voltage detection on VOUT1	DET1L	
	Low voltage detection on VD2	DETDC2L	Enters protect function
	Low voltage detection on VD1	DETDC1L	Enters protect function
Interrupt factor 3	High temperature warning at TRACK1/2	WRTMP2	
	High temperature warning at DCDC1 or LDO1	WRTMP1	
	WD trigger in CW	WRWDT	
	Self-diagnosis of detectors of LDO0 and BGR	DETREF	
	Detection of VINR low voltage	DETBAT1	
	Detection of DCDC2 over current	DETDC2OC	Enters protect function
	Detection of DCDC1 over current	DETDC1OC	Enters protect function

Interrupt factor (Continued)

Interrupt factor		Symbol	Note
Interrupt factor 4	Intentional interrupt	DUMMY	Checks connection to MCU
	Self-diagnosis of oscillator	SDOSC	
	Self-diagnosis of state machine	SDSTA	
	Self-diagnosis of VOUT0SW	SD0SW	Checks connection to VIN3V
	Monitoring of digital output, FSOUT pin	PFSOUT	
	Monitoring of digital output, EXCNT pin	PEXCNT	
	Monitoring of digital output, SUSP pin	PSUSP	
	Monitoring of digital output, RSTB pin	PRSTB	

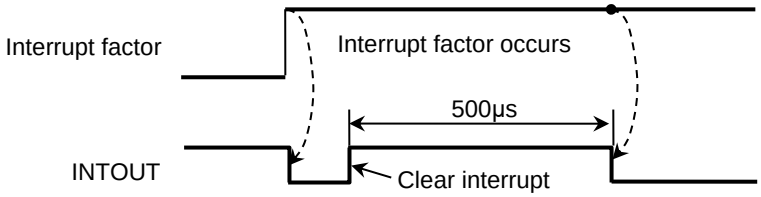


Fig. 4-11-2 INTOUT behavior when interrupt factor continues

Note: Once INTOUT is cleared, occurring interrupt factor doesn't make INTOUT assert low during 500µs.

4.11.3 Register

Interrupt register indicates the factor that causes INTOUT assertion. Even one or more interrupt factor occurs, INTOUT would assert low.

- Interrupt factor

  This register indicates what interrupt register occurs so that it can read interrupt factor directly.

  For INTSD register, it indicates fail occurred in self-diagnosis. And if the factor belonged in each interrupt request address failed in self-diagnosis, D3-D0 is set "1" simultaneously. For INTRSFG register, it indicates the factor which makes reset exists. The factors are collected in INTRSFG register.

  In order to clear this register, it needs to clear all interrupt factors.

■ Address (INTFAC) : 03H

A5	A4	A3	A2	A1	A0
0	0	0	0	1	1

■ Register (Below bits are read only.)

Do7	Do6	Do5	Do4	Do3	Do2	Do1	Do0
-	-	INTRSFG	INTSD	INTR4	INTR3	INTR2	INTR1

■ Contents

Register name		Control contents	Setting	
			1	0
INTRSFG	D5	Flags of reset factor	Occurs	None *
INTSD	D4	Interrupt factor in self diagnosis	Occurs	None *
INTR4	D3	Interrupt factor in INTREQ4	Occurs	None *
INTR3	D2	Interrupt factor in INTREQ3	Occurs	None *
INTR2	D1	Interrupt factor in INTREQ2	Occurs	None *
INTR1	D0	Interrupt factor in INTREQ1	Occurs	None *

* Default setting

Note1: This register is not initialized by RSTB.

➢ Interrupt request 1

Interrupts of over voltage detection are collected in this address.
When fail is detected in self-diagnosis, interrupt request occurs in corresponding block as well.

■ Address (INTREQ1) : 04H

A5	A4	A3	A2	A1	A0
0	0	0	1	0	0

■ Register (Below bits are read only.)

Do7	Do6	Do5	Do4	Do3	Do2	Do1	Do0
-	DETTRQ2U	DETTRQ1U	DETADU	DET2U	DET1U	DETDC2U	DETDC1U

■ Contents

Bit	Contents
0	No interrupt request *
1	Interrupt request

* Default setting

Note: This register is not initialized by RSTB.

➢ Interrupt request 2

Interrupts of low voltage detection are collected in this address.
When fail is detected in self-diagnosis, interrupt request occurs in corresponding block.

■ Address (INTREQ2) : 05H

A5	A4	A3	A2	A1	A0
0	0	0	1	0	1

■ Register (Below bits are read only.)

Do7	Do6	Do5	Do4	Do3	Do2	Do1	Do0
DET0SWL	DETTRQ2L	DETTRQ1L	DETADL	DET2L	DET1L	DETDC2L	DETDC1L

Note: In the case that DET2L is added to reset factor, if DET2L causes reset, DET2L bit remains even after reset is released.

■ Contents

Bit	Contents
0	No interrupt request *
1	Interrupt request

* Default setting

Note: This register is not initialized by RSTB.

➢ Interrupt request 3

Other interrupt factors are collected in this address.

■ Address (INTREQ3) : 06H

A5	A4	A3	A2	A1	A0
0	0	0	1	1	0

■ Register (Below bits are read only.)

Do7	Do6	Do5	Do4	Do3	Do2	Do1	Do0
-	WRTMP2	WRTMP1	WRWDT	DETREF	DETBAT1	DETDC2OC	DETDC1OC

■ Contents

Bit	Contents
0	No interrupt request *
1	Interrupt request

* Default setting

Note: This register is not initialized by RSTB.

➢ Interrupt request 4

Interrupts of diagnosis are collected in this address.

■ Address (INTREQ4) : 07H

A5	A4	A3	A2	A1	A0
0	0	0	1	1	1

■ Register

Below bits are read only except “DUMMY” bit. In order to make intentional assertion, only DUMMY bit is allowed to be written. (It also can be read.)

D7	Do6	Do5	Do4	Do3	Do2	Do1	Do0
DUMMY	SDOSC	SDSTA	SD0SW	PFSOUT	PEXCNT	PSUSP	PRSTB

■ Contents

Bit	Contents
0	No interrupt request *
1	Interrupt request

* Default setting

Note: This register is not initialized by RSTB.

After INTOUT occurs by the DUMMY bit, please set 0 as the DUMMY bit, directly. After that, set 1 as the CLDUMMY bit.

➢ Interrupt clear 1

Clear for “INTREQ1” register is placed in this address. If all contents of this address are cleared, “INTR1” bit in “INTFAC” register is clear, too.

■ Address (INTCL1) : 08H

A5	A4	A3	A2	A1	A0
0	0	1	0	0	0

■ Register (Below bits are written only.)

D7	D6	D5	D4	D3	D2	D1	D0
-	CLTRQ2U	CLTRQ1U	CLADU	CL2U	CL1U	CLDC2U	CLDC1U

■ Contents

Bit	Contents
0	No change *
1	Clear interrupt

* Default setting

➢ Interrupt clear 2

Clear for “INTREQ2” register is placed in this address. If all contents of this address are cleared, “INTR2” bit of “INTFAC” register is clear, too.

■ Address (INTCL2) : 09H

A5	A4	A3	A2	A1	A0
0	0	1	0	0	1

■ Register (Below bits are written only.)

D7	D6	D5	D4	D3	D2	D1	D0
CL0SWL	CLTRQ2L	CLTRQ1L	CLADL	CL2L	CL1L	CLDC2L	CLDC1L

■ Contents

Bit	Contents
0	No change *
1	Clear interrupt

* Default setting

➢ Interrupt clear 3

Clear for “INTREQ3” register is placed in this address. If all contents of this address are cleared, “INTR3” bit of “INTFAC” register is clear, too.

■ Address (INTCL3) : 0AH

A5	A4	A3	A2	A1	A0
0	0	1	0	1	0

■ Register (Below bits are written only.)

D7	D6	D5	D4	D3	D2	D1	D0
-	CLTMP2	CLTMP1	CLWDT	CLREF	CLBAT1	CLDC2OC	CLDC1OC

■ Contents

Bit	Contents
0	No change *
1	Clear interrupt

* Default setting

➢ Interrupt clear 4

Clear for “INTREQ4” register is placed in this address. If all contents of this address are cleared, “INTR4” bit of “INTFAC” register is clear, too.

■ Address (INTCL4) : 0BH

A5	A4	A3	A2	A1	A0
0	0	1	0	1	1

■ Register (Below bits are written only.)

D7	D6	D5	D4	D3	D2	D1	D0
CLDUMMY	-	CLSTA	CL0SW	CLPFSOUT	CLPEXCNT	CLPSUSP	CLPRSTB

Note: After INTOUT occurs by the DUMMY bit, please set 0 as the DUMMY bit, directly. After that, set 1 as the CLDUMMY bit.

■ Contents

Bit	Contents
0	No change *
1	Clear interrupt

* Default setting

➢ Interrupt mask 1

Interrupt mask for “INTR1” register is placed in this address.

■ Address (INTMSK1) : 0CH

A5	A4	A3	A2	A1	A0
0	0	1	1	0	0

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
-	MSKTRQ2U	MSKTRQ1U	MSKADU	MSK2U	MSK1U	MSKDC2U	MSKDC1U

■ Contents

Bit	Contents
0	No mask *
1	Execute mask

* Default setting

➢ Interrupt mask 2

Interrupt mask for “INTR2” register is placed in this address.

■ Address (INTMSK2) : 0DH

A5	A4	A3	A2	A1	A0
0	0	1	1	0	1

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
MSK0SWL	MSKTRQ2L	MSKTRQ1L	MSKADL	MSK2L	MSK1L	MSKDC2L	MSKDC1L

■ Contents

Bit	Contents
0	No mask *
1	Execute mask

* Default setting

➢ Interrupt mask 3

Interrupt mask for “INTR3” register is placed in this address.

■ Address (INTMSK3) : 0EH

A5	A4	A3	A2	A1	A0
0	0	1	1	1	0

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
-	MSKTMP2	MSKTMP1	MSKWDT	-	MSKBAT1	MSKDC2OC	MSKDC1OC

■ Contents

Bit	Contents
0	No mask *
1	Execute mask

* Default setting

➢ Interrupt mask 4

Interrupt mask for “INTR4” register is placed in this address.

■ Address (INTMSK4) : 0FH

A5	A4	A3	A2	A1	A0
0	0	1	1	1	1

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
MSKDUMMY	MSKOSC	MSKSTA	-	MSKPFSOUT	MSKPEXCNT	MSKPSUSP	MSKPRSTB

■ Contents

Bit	Contents
0	No mask *
1	Execute mask

* Default setting

4.12 Functional Safety

In order to protect microcontroller or the PMIC from extraordinary accident, the PMIC has a sort of protect function.

4.12.1 Voltage detection

All regulators in the PMIC have voltage detector to its output. And battery voltage detector has same function as well. The voltage-detect function operates after self-diagnosis completes.

◆ **High and low voltage detection 1**

High and low voltage detect behavior is shown in below figure. When high or low voltage is detected, it makes INTOUT assert low.

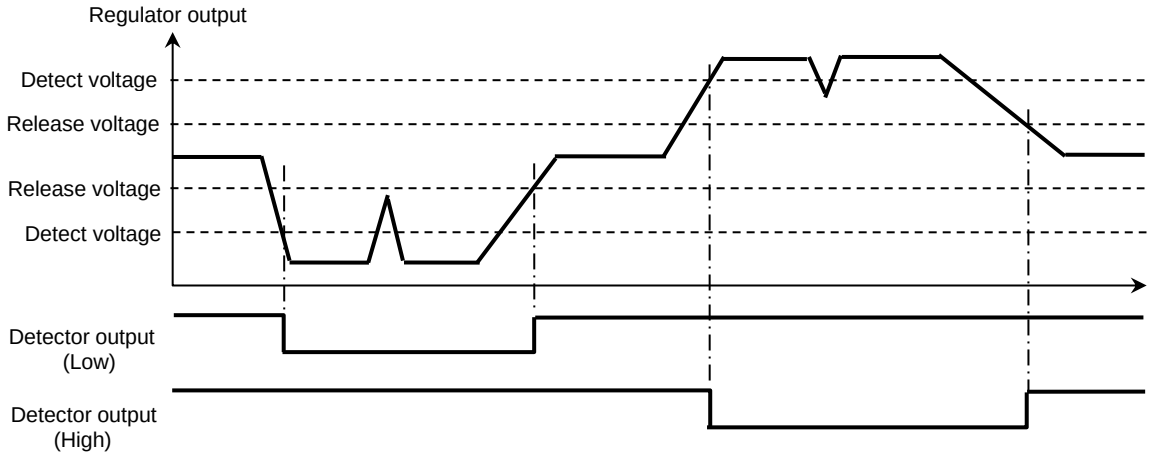


Fig. 4-12-1 High and low voltage detector's behavior

◆ **High and low voltage detection 2**

In DCDC2, high and low voltage detect policy are different from above behavior.

The detectors have no release level. Instead, they have anti glitch circuit to prevent nuisance reset. If any transient on the output with continuing more than designated duration is monitored, then it makes INTOUT assert low.

It can be set to generate reset when low voltage is detected. Please refer to "4.1.4 Configuration register".

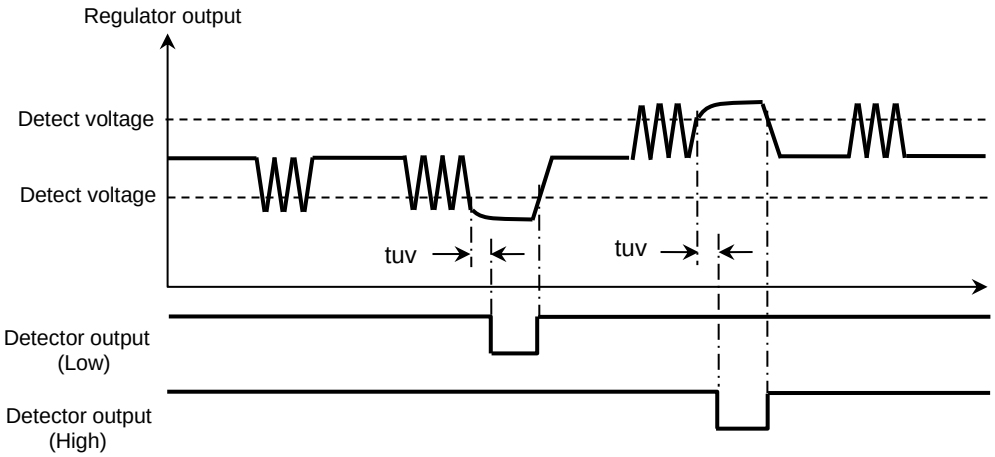


Fig. 4-12-2 High and low voltage detector's behavior in DCDC2

4.12.2 PMIC behavior after unusual detection

The all the regulators have high or low voltage detectors. Some of detection may lead serious situation, other of them does not affect whole system. The behaviors in case of unusual detections are summarized below table. The behavior to temperature detection is described as well.

Table 4-12 Listed PMIC behavior

Unusual detection	Description	Behavior of the PMIC
DETBAT1	Low voltage detection of battery	INTOUT would be asserted All regulator will stop operating
DETDC1U	Over voltage detection of DCDC1	DCDC1/2 stops switching behavior INTOUT would be asserted
DETDC1L	Low voltage detection of DCDC1	DCDC1 enters interval operating INTOUT would be asserted
DETDC1OC	Over current detection of DCDC1	DCDC1 enters interval operating INTOUT would be asserted
DET0SWL	Low voltage detection of VOUT0SW	INTOUT would be asserted
DET1U	Over voltage detection of LDO1	INTOUT would be asserted
DET1L1	Low voltage detection of LDO1	SUSP, INTOUT would be asserted
DET1L2	Low voltage detection of LDO1	Reset occurs
DET2U	Over voltage detection of LDO2	INTOUT would be asserted DCDC1 enters interval operating
DET2L	Low voltage detection of LDO2	INTOUT would be asserted
DETADU	Over voltage detection of LDOAD	INTOUT would be asserted
DETADL	Low voltage detection of LDOAD	INTOUT would be asserted
DETDC2U	Over voltage detection of DCDC2	DCDC2 stops switching DCDC1 enters interval operating INTOUT would be asserted
DETDC2L	Low voltage detection of DCDC2	DCDC2 enters interval operating INTOUT would be asserted
DETDC2OC	Over current detection of DCDC2	DCDC2 enters interval operating INTOUT would be asserted
DETTRQ1U	Over voltage detection of TRACK1	INTOUT would be asserted
DETTRQ1L	Low voltage detection of TRACK1	INTOUT would be asserted
DETTRQ2U	Over voltage detection of TRACK2	INTOUT would be asserted
DETTRQ2L	Low voltage detection of TRACK2	INTOUT would be asserted
WRTMP1/2	Warning temperature detection	INTOUT would be asserted
TSDTMP	Shut down temperature detection	Force to stop PMIC operation INTOUT would be asserted

In above table, when the PMIC detect low voltage of DCDC2, it leads to enter protect mode and asserted INTOUT.

4.12.3 Self-diagnosis

Built-in-self-test is implemented in the PMIC so that self-diagnostic of the PMIC's function is executed during initial reset. The self-diagnostic is done to prevent serious situation such as applying unexpected voltage to MCU or communication disability with microcontroller. The following blocks are checked as self-diagnostic.

- Detectors: Confirm detect function
- Logic circuit: Confirm timer function
- Oscillator: Confirm if oscillation frequency is expected
- Temperature sensor: Confirm the function of thermal shutdown

◆ **Detectors**

To make sure output voltage of each regulator, detect functionality is tested before regulators power up. A voltage for comparator test is applied to the detector part. During diagnosis execution, detect function is checked by changing comparator's input. If error is detected, INTOUT is asserted.

◆ **Logic circuit**

The logic circuit in the PMIC is checked before reset is released. Self-diagnosis is done by test circuit implemented in the PMIC. If error is detected in self-diagnosis, the PMIC does not start to operate.

◆ **Oscillator**

The oscillator is used for not only switching in DCDC but also state machine. Damage in the oscillator may affect PMIC function.

There are two oscillators which have quite same operation. They monitor oscillation each other, and if unusual oscillation is detected then switched to the oscillator which acts usual operation. And then the PMIC informs INTOUT assertion. If unusual oscillation is detected, INTOUT is asserted.

◆ **Temperature sensor**

The temperature sensor senses a voltage corresponding to the die temperature. During self-diagnosis period, thermal shutdown function is checked. If error is detected, INTOUT is asserted.

Note : When errors were detected by self-diagnostic before power supply start, INTOUT is kept low level.

4.12.4 Electrical characteristics

Detect level of each regulators are shown in below tables.
The condition is Tj=-40 to 150°C, unless otherwise specified.

◆ Battery voltage detector

Table 4-12-1 Detect level of battery

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
DETBAT1						
Detect voltage	Vdb		3.50	3.70	3.90	V
Release voltage	Vrb		5.70	6.00	6.30	V

◆ **Detector in DCDC1**

Table 4-12-2 Detect level of DCDC1

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
DETDC1U						
Detect voltage	Vdd1u		6.500	6.750	7.000	V
Release voltage	Vrd1u		6.200	6.450	6.700	V
DETDC1L						
Detect voltage	Vdd1l		2.700	2.850	3.000	V
Release voltage	Vrd1l		4.800	5.000	5.200	V

◆ **Detector in DCDC2**

Table 4-12-3 Detect level of DCDC2

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
DETDC2U						
Detect voltage	Vdd2u		1.350	1.380	1.410	V
DETDC2L						
Detect voltage	Vdd2l	More than 60µs duration time	1.150	1.174	1.197	V

◆ **Detector in LDO0**

Table 4-12-4 Detect level of LDO0

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
DET0U						
Detect voltage	Vd0u		3.432	3.531	3.630	V
Release voltage	Vr0u		3.366	3.465	3.564	V
DET0L						
Detect voltage	Vd0l		2.970	3.053	3.135	V
Release voltage	Vr0l		3.069	3.152	3.234	V

◆ **Detector in VOUT0SW**

Table 4-12-5 Detect level of VOUT0SW

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
DET0SWL						
Detect voltage	Vd0sw		3.000	3.075	3.150	V
Release voltage	Vr0sw		3.073	3.150	3.227	V

◆ **Detector in LDO1**

Table 4-12-6 Detect level of LDO1

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
DET1U						
Detect voltage	Vd1u		5.200	5.350	5.500	V
Release voltage	Vr1u		5.100	5.250	5.400	V
DET1L1						
Detect voltage	Vd1l1		4.500	4.625	4.750	V
Release voltage	Vr1l1		4.650	4.775	4.900	V
DET1L2						
Detect voltage	Vd1l2		3.000	3.090	3.180	V

◆ **Detector in LDO2**

Table 4-12-7 Detect level of LDO2

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
DET2U						
Detect voltage	Vd2u		3.402	3.500	3.598	V
Release voltage	Vr2u		3.366	3.465	3.564	V
DET2L						
Detect voltage	Vd2l		3.006	3.090	3.174	V
Release voltage	Vr2l		3.069	3.152	3.234	V

◆ **Detector in LDOAD**

Table 4-12-8 Detect level of LDOAD

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
DETADU						
Detect voltage	Vdadu		5.200	5.350	5.500	V
Release voltage	Vradu		5.100	5.250	5.400	V
DETADL						
Detect voltage	Vdadl		4.500	4.625	4.750	V
Release voltage	Vradl		4.650	4.775	4.900	V

◆ **Detector in TRACK1/2**

Table 4-12-9 Detect level of TRACK1/2

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
DETTRQ1/2U						
Detect voltage	Vdtrq1u	Based on input voltage	104.0	107.0	110.0	%
Release voltage	Vrtrq1u	Based on input voltage	102.1	105.0	108.0	%
DETTRQ1/2L						
Detect voltage	Vdtrq1l	Based on input voltage	90.0	92.5	95.0	%
Release voltage	Vrtrq1l	Based on input voltage	93.0	95.5	98.0	%

4.13 Temperature Sensor

Temperature sensors are implemented in the PMIC. In order to sense temperature at several points of PMIC, several sensors are placed.

4.13.1 Thermal shut down

For product safety, a thermal shutdown function is implemented. Temperature sensors detect a voltage corresponding to internal temperature. When warning temperature is detected, INTOUT asserts low. Further, when shutdown temperature is detected, it forces the PMIC execute power down sequence.

Four temperature sensors are placed near by DCDC1, TRACK1, TRACK2, and LDO1. If one of these sensors detects high temperature, detection behavior occurs.

After the temperature goes down across the release temperature, the PMIC restart in the power-up sequence. But TRACK1 and TRACK2 need request to resume operation.

Table 4-13 Thermal detect temperature

Items	Symbol	Conditions	MIN	TYP	MAX	Unit
Warning temperature	Twng		140	160	180	°C
Shutdown temperature	Tsd		160	180	200	
Release temperature	Trls		125	145	165	
Warning release temperature	Twrls		115	135	155	

Note: Above values are guaranteed by design.
Relationship of above temperature order maintains anytime.

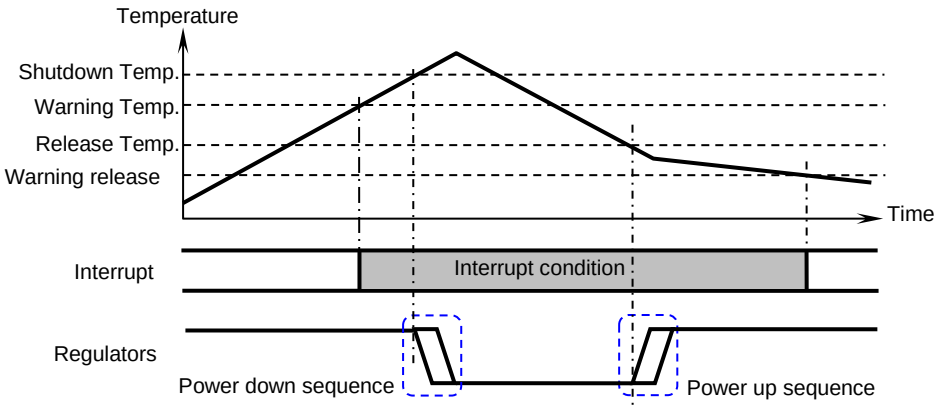


Fig. 4-13 Thermal shutdown function

4.13.2 Register

It can change temperature setting of both detect and release temperature.

- Temperature setting

  This register is a secured register. It is necessary to enter “key” code before enter this request. (See “4.2.3 Secured request”.)

■ Address (SENTMP) : 1EH

A5	A4	A3	A2	A1	A0
0	1	1	1	1	0

■ Register

D7	D6	D5	D4	D3	D2	D1	D0
WARREL(1:0)		THREL(1:0)		WARDET(1:0)		THDET	-

■ Setting contents

Register name		Control contents	Setting	
			1	0
THDET	D1	Thermal shutdown temperature	170°C	180°C *

* Default setting

WARDET(1:0)		Warning temp.
D3	D2	
0	0	170°C
0	1	160°C *
1	0	150°C
1	1	140°C

* Default setting

THREL(1:0)		Shutdown release
D5	D4	
0	0	155°C
0	1	145°C *
1	0	135°C
1	1	125°C

* Default setting

WARREL(1:0)		Warning release
D7	D6	
0	0	155°C
0	1	145°C
1	0	135°C *
1	1	125°C

* Default setting

Note: This register is not initialized by RSTB.

4.14 Monitoring Function

The PMIC has monitoring function.

Analog monitoring function is indicates internal analog voltage. Digital monitoring function is monitoring digital output pins.

4.14.1 Monitoring internal analog voltage

The PMIC has an analog monitoring function. It outputs the regulator level of the PMIC or internal analog voltage with using operational amplifier. The voltage to output is selected via SPI. Microcontroller can read these analog voltages through its ADC and can understand PMIC's situation. Power on and off, output select are done by setting register.

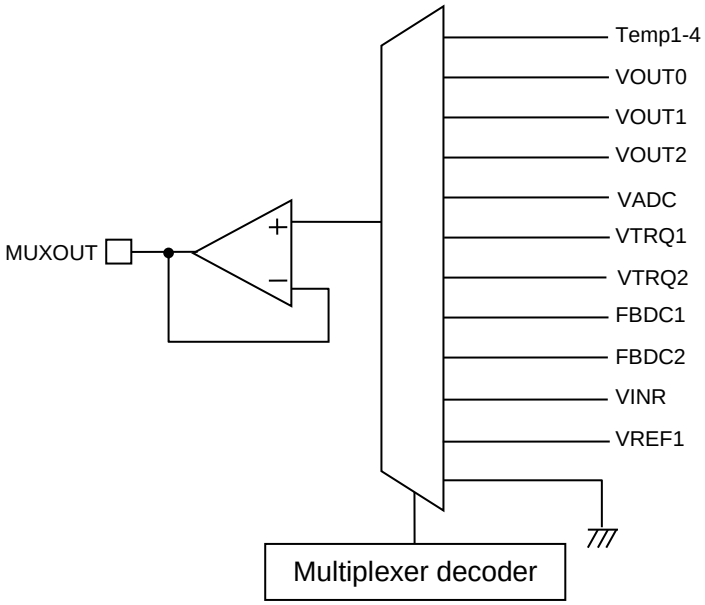


Fig.4-14-1 Diagram of analog monitoring

4.14.2 Monitoring digital output

The PMIC has a digital monitoring function. It compares with output and control signal of digital output buffer. If differentiation is detected, it makes INTOUT assert low.

The objective outputs are FSOUT, EXCNT, SUSP, and RSTB pins. But INTOUT pin can't be monitored. In order to check INTOUT pin, "DUMMY" bit in interrupt register, address 07H, is recommended to set. Microcontroller can asserts INTOUT pin low by setting "DUMMY" bit. If microcontroller can't recognize interruption, something happens on INTOUT.

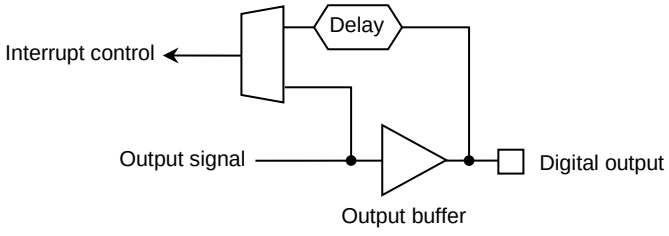


Fig.4-14-2 Diagram of digital monitoring

◆ **Monitoring delay time**

The output transition time depends on external environment. In order to make sure certain comparison, the monitoring function compares with delayed output signal. The delay time is 1µs except RSTB. In particular, dependency of external element on RSTB is large. Therefore, the delay time of RSTB is 100µs.

4.14.3 Register

Operation setting for monitoring function is described in this section.

- Signal select
  - Address (MUXCNT) : 18H

A5	A4	A3	A2	A1	A0
0	1	1	0	0	0

  - Register

D7	D6	D5	D4	D3	D2	D1	D0
-	MUXCNT	-	-	MUXSEL(3:0)			

  - Setting contents

This bit controls on and off control.

Register name		Control contents	Setting	
			1	0
MUXCNT	D6	On/Off control	On	Off *

* Default setting

These bits control output channel.

MUXSEL(3:0)				Monitoring name
D3	D2	D1	D0	
0	0	0	0	GND *
0	0	0	1	VINR
0	0	1	0	VOUT0
0	0	1	1	VOUT1
0	1	0	0	VOUT2
0	1	0	1	GND
0	1	1	0	VADC
0	1	1	1	VTRQ1
1	0	0	0	VTRQ2
1	0	0	1	FBDC1
1	0	1	0	FBDC2A/B
1	0	1	1	TEMP1 (Near DCDC1)
1	1	0	0	TEMP2 (Near LDO1)
1	1	0	1	TEMP3 (Near TRACK1)
1	1	1	0	TEMP4 (Near TRACK2)
1	1	1	1	VREF1

* Default setting

4.14.4 Electrical characteristics

Electrical characteristic on recommended operating condition.

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output voltage	Voinr	Selected VINR *1	1.16	1.2	1.24	V
	Voldo0	Selected VOUT0	1.57	1.65	1.73	
	Voldo1	Selected VOUT1	2.41	2.5	2.59	
	Voldo2	Selected VOUT2	1.59	1.65	1.71	
	Voldoad	Selected VADC	2.44	2.5	2.56	
	Votrack1	Selected VTRQ1	2.46	2.5	2.54	
	Votrack2	Selected VTRQ2	2.46	2.5	2.54	
	Vodc1	Selected FBDC1	2.64	2.85	3.06	
	Vodc2	Selected FBDC2A/B	1.207	1.25	1.293	
	Votmp1	At 25°C	0.62	0.67	0.72	
	Votmp2		0.62	0.67	0.72	
	Votmp3		0.62	0.67	0.72	
	Votmp4		0.62	0.67	0.72	
	Vref	Selected VREF1	1.159	1.2	1.241	
Output stable time*2	tstb	From SPICSB rising	-	-	40	µs

*1 Applied VINR voltage is 12V.
*2 Guaranteed by design.

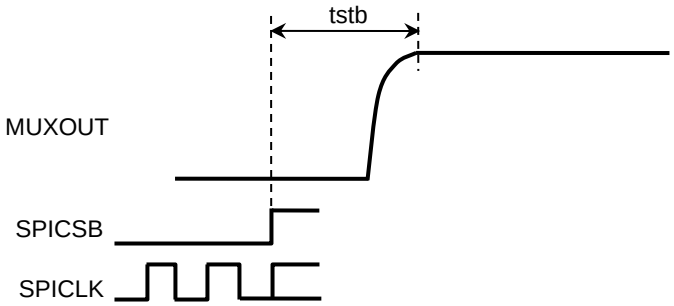


Fig. 4-14-3 Output timing

◆ **Output of temperature sensor**

The outputs of temperature depend on junction temperature. For reference, output temperature characteristic is shown in below figure.

The approximate equation of the output voltage is as follow. And output deviation is +/-50mV for every temperature.

Votmp1-4 = 718-1.9*T (mV) where “T” is Tj.

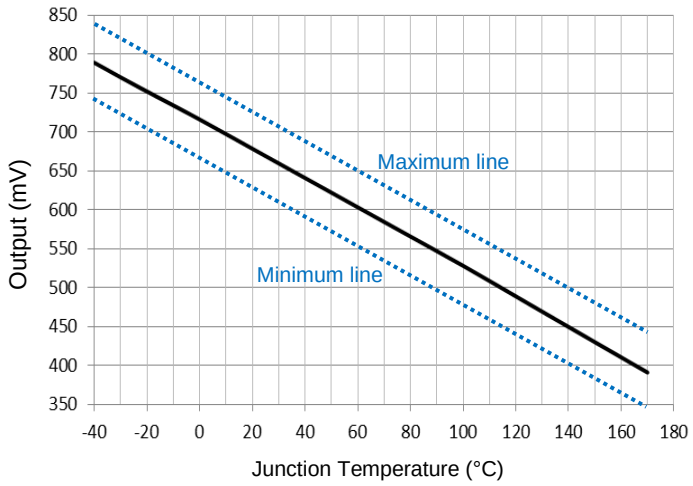
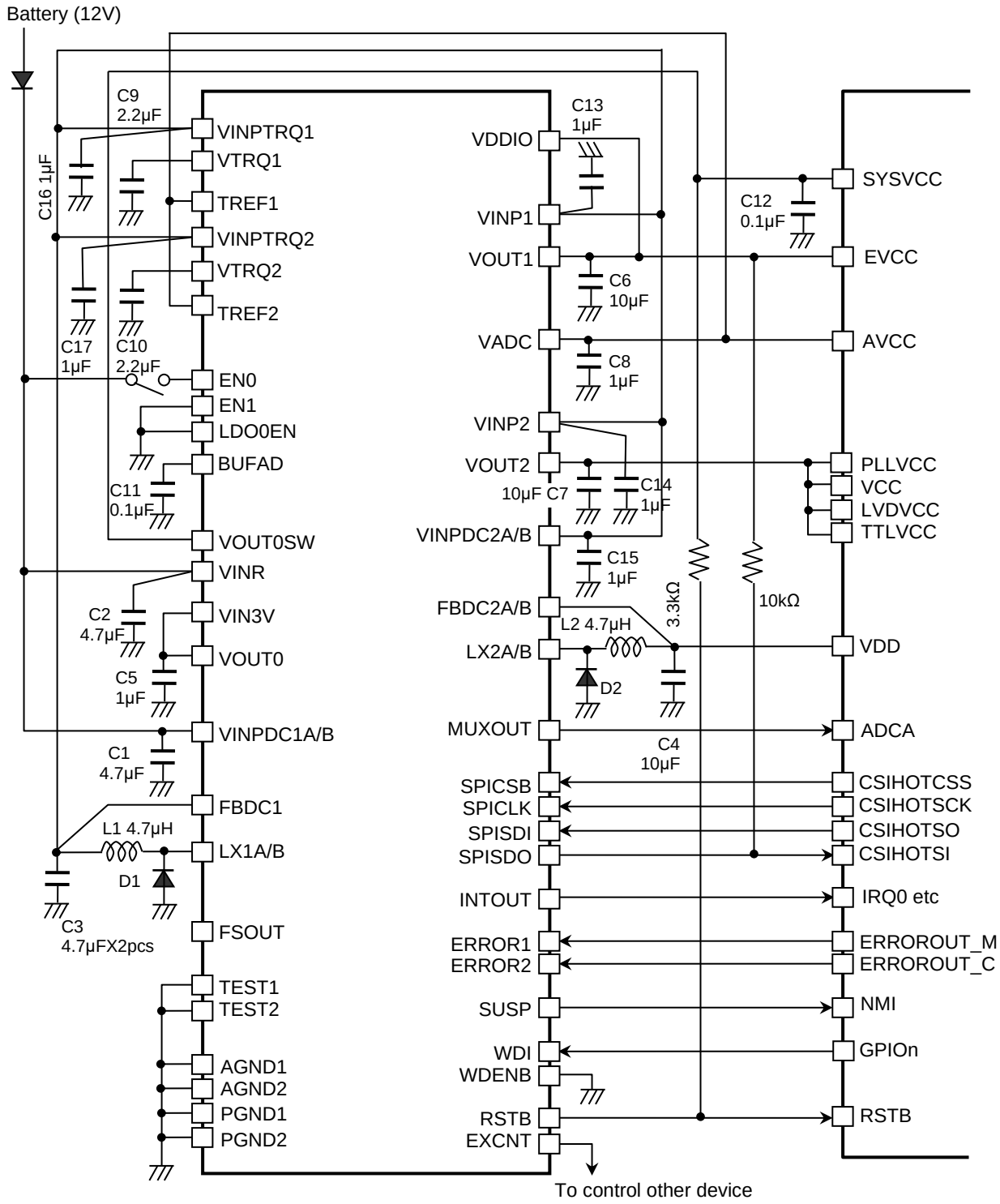


Fig. 4-14-4 Output of temperature sensor

5 Application Diagram

Below figure shows typical application diagram which contains elements around the PMIC.



D1,2 M1FS4 (SHINDENGEN) L1,2 CLF6045T-4R7-H (TDK) C1,C2 GCM32ER71H475K (MURATA)
C3 GCM31CR71C475K (MURATA) C4,C6,C7 GCM21BR70J106K (MURATA) C5 GCM219R71C105K(MURATA)
C8 GCM188C71A105K (MURATA) C9,C10 GCM21BR71C225K (MURATA) C11,C12 GCM188R71C104K (MURATA)
C13-17 GCM219R71C105K (MURATA)

Fig.5 Application circuit

Note: This is a very simplified example of an application. The function must be verified in the real application.

5.1 Layout guide lines

Important thing to consider the layout is component placement on the PCB. Please take into account following things for PCB trace design.

- ◆ For proper operation and to prevent EMI radiation, the freewheeling diode and inductor have to be placed as close as possible to the PMIC. Also output capacitors have to be placed near by the inductor.
- ◆ The feedback trace of DCDC converter never crosses the inductor, and recommended connection point is near output capacitor.
- ◆ For DCDC converter, GND connection of components is important. GNDs of input capacitor, output capacitor, and freewheeling diode are connected to the same point.
- ◆ For LDO, in order to avoid influence of stray resistance on the PCB, output capacitor has to be placed as close as possible to the PMIC.
- ◆ If application needs to apply power supply for multi devices, power distribution at output capacitor of each regulator is recommended.
- ◆ In order to maximum heat spread performance, the exposed pad on the backside of the package is recommended to make soldering to GND plane.
- ◆

6 Electrical Characteristics

6.1 Recommended operating condition

Parameter	Symbol	Pin name	MIN	TYP	MAX	Unit
Input voltage	VBAT	VINR,VINPDC1A/B	6.0 *	12.0	18.5	V
LDO power line	VPLDO	VINP1/2,VINPTRQ1/2,VINPDC2A/B	5.4	5.7	6.0	V
Digital I/O power	VDDIO	VDDIO	4.5	5.0	5.5	V
Circuit power line	VIN	VIN3V	3.0	3.3	3.6	V
Operational temp.	Ta		-40	25	125	°C
Pull up resistor	Rpur	RSTB	3.3	-	-	kΩ
	Rpus	SPISDO	10	-	-	kΩ

* After the PMIC starts to operate, the PMIC keeps operate down to this voltage.

6.2 Electrical characteristics

6.2.1 DC characteristics

◆ **Digital input**

DC characteristics of digital pins are shown in below table.

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
High level input voltage 1	VIH1	EN0/1, LDO0EN	2.5	-	VBAT+0.3	V
High level input voltage 2	VIH2	ERROR1/2	0.7*VIN3V	-	VDDIO+0.3	
High level input voltage 3	VIH3	Below pin group	0.7*VDDIO	-	VDDIO+0.3	
Low level input voltage 1	VIL1	EN0/1, LDO0EN	-0.3	-	1.0	V
Low level input voltage 2	VIL2	ERROR1/2	-0.3	-	0.3*VIN3V	
Low level input voltage 3	VIL3	Below pin group	-0.3	-	0.3*VDDIO	

Pin group: SPICSB, SPICLK, SPISDI, WDI, WDENB

◆ **Digital output**

DC characteristics of digital pins are shown in below table.

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
High level output voltage	VoH	IoH=2mA, below pin group	0.8*VDDIO	-	-	V
Low level output voltage	VoL1	IoL=-2mA, below pin group	-	-	0.2*VDDIO	V
Low level output voltage	VoL2	IoL=-2mA, SUSP only	-	-	0.13*VDDIO	V
Low level output voltage	VoLr	RSTB pin, IoL=-2mA	-	-	0.4	V
RSTB output leak	Ilkrstb	Hi-Z, RSTB pin	-	-	10	µA

Pin group: INTOUT, SPISDO, FSOUT, EXCNT,SUSP(VoH)

◆ **Switch resistance**

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
VOUT0SW	Ronsw	From VIN3V to VOUT0SW	-	-	8	Ω

◆ **Pull up/down resistor**

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Pull up resistor	Rpu	SPICSB	76	100	127	kΩ
Pull down resistor 1	Rpd1	EN0, EN1, LDO0EN	390	-	-	kΩ
Pull down resistor 2	Rpd2	Below pin group	76	100	127	kΩ

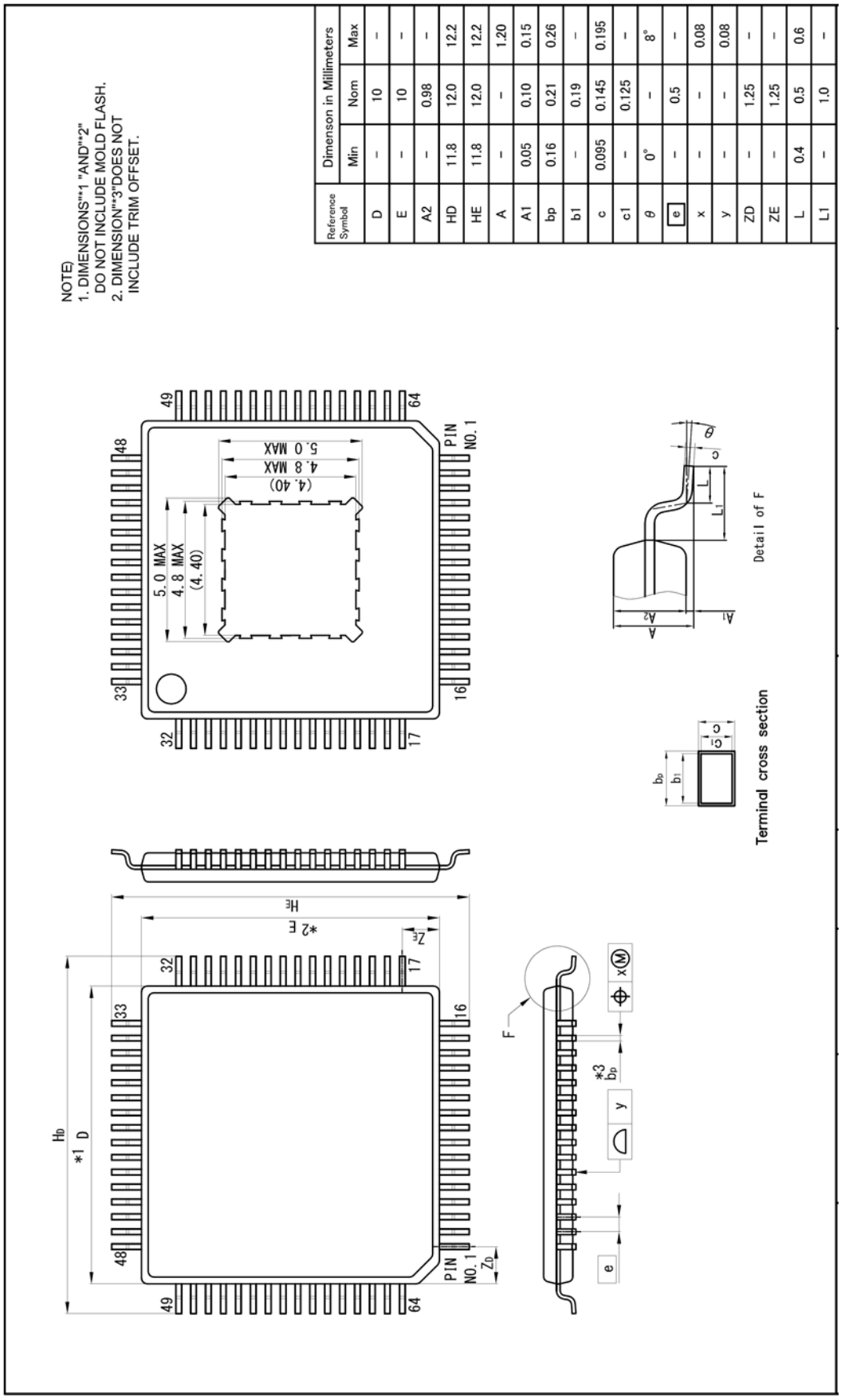
Pin group: SPICLK, SPISDI, ERROR1/2, WDI, WDENB

◆ **Operating current (VINR and VINPDC1A/B = 12V, No load current on each regulators)**

Parameter	Symbol	Condition	MIN	TYP	MAX	Unit
Stand by current	Iddoff	EN0/1=0 and LDO0EN=0	-	16	40	µA
Operating current 1	Idd1	EN0/1=0 and LDO0EN=1 Ta=+25°C and VIN3V=3.3V	-	210	300	µA
Operating current 2 *	Idd2	EN0=1 or EN1=1	-	2.7	4.5	mA
Operating current 3 *	Idd3	Including trackers' current	-	4.9	14.0	mA

* Except external diode leakage current

7 Package Information



Reference Symbol	Dimenson in Millimeters		
	Min	Nom	Max
D	–	10	–
E	–	10	–
A2	–	0.98	–
HD	11.8	12.0	12.2
HE	11.8	12.0	12.2
A	–	–	1.20
A1	0.05	0.10	0.15
bp	0.16	0.21	0.26
b1	–	0.19	–
c	0.095	0.145	0.195
c1	–	0.125	–
θ	0°	–	8°
e	–	0.5	–
x	–	–	0.08
y	–	–	0.08
ZD	–	1.25	–
ZE	–	1.25	–
L	0.4	0.5	0.6
L1	–	1.0	–

Fig.7 Package diagram

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