ISL8121

3V to 20V, Two-Phase Buck PWM Controller with Integrated 4A MOSFET Drivers

FN6352
Rev 2.00
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The ISL8121 is a two-phase buck PWM controller featuring an input voltage range of 3V to 20V and integrated MOSFET drivers. Precision voltage regulation is provided for point-of-load and other high-current applications that require efficient and compact implementation. Multiphase buck converter architecture uses interleaved timing to multiply channel ripple frequency allowing smaller filter inductors and reducing input and output ripple currents due to the ripple cancellation effect. Lower ripple results in fewer input and output capacitors. Smaller and low cost transistors can be used resulting from the higher efficiency and reduced power dissipation.

The ISL8121 offers an internal 0.6V reference with a system regulation accuracy of ±0.8% (Industrial Temperature range), an optional external reference input, and user-adjustable switching frequency. Unity gain differential amplifier targeted at remote voltage sensing capability enhances the regulation. A power good signal (PGD) is issued when the output voltage is within the regulated window. An internal shunt regulator with optional external connection capability extends the operational input voltage range. For applications requiring voltage tracking or sequencing, the ISL8121 offers a host of possibilities, including coincidental, ratiometric, or offset tracking, as well as sequential start-ups, user adjustable for a wide range of applications.

Additional features include overvoltage and overcurrent protection. Overcurrent protection can be tailored to various applications with no need for additional parts. The ISL8121 uses cost and space-saving $r_{DS(ON)}$ sensing for channel current balance, dynamic voltage positioning, and overcurrent protection. Channel current balancing is automatic and accurate with the integrated current-balance control system.

Features

- Integrated Two-Phase Power Conversion
- Precision Output Voltage Regulation
  - ±0.8% System Accuracy Over-Temperature (Industrial)
  - Differential Remote Voltage Sensing for Increased Voltage Sensing Accuracy
- Shunt Regulator for Wide Input Power Conversion
  - 5V and Higher Bias
  - Up to 20V Power Down-Conversion
- Precision Channel Current Sharing
  - Loss-Less $r_{DS(ON)}$ Current Sampling
- Integrated High Capable 4A Drivers
- 0.6V Internal Reference
- Full Spectrum Voltage Tracking
  - Coincidental, Ratiometric, or Offset
- Sequential Start-up Control
- Selectable Switching Frequency up to 2MHz Per Phase
- Fast Transient Recovery Time
- Overcurrent Protection
- Overvoltage Protection
- Capable of Start-up in a Pre-Biased Load
- QFN Packages:
  - QFN - Compliant to JEDEC PUB95 MO-220
  - QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Pb-Free Available (RoHS Compliant)

Applications

- General Purpose High Current DC/DC Converters
- High Current, Low Voltage FPGA/ASIC DC/DC Converters
- Telecom System

Ordering Information

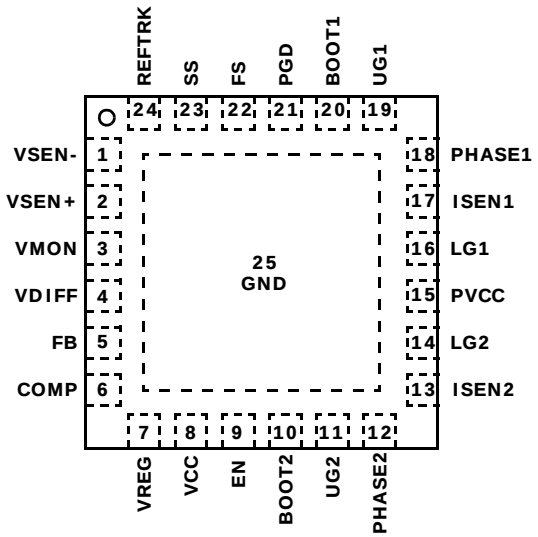
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL8121IRZ	81 21IRZ	-40 to +85	24 Ld 4x4 QFN	L24.4x4C

NOTES:

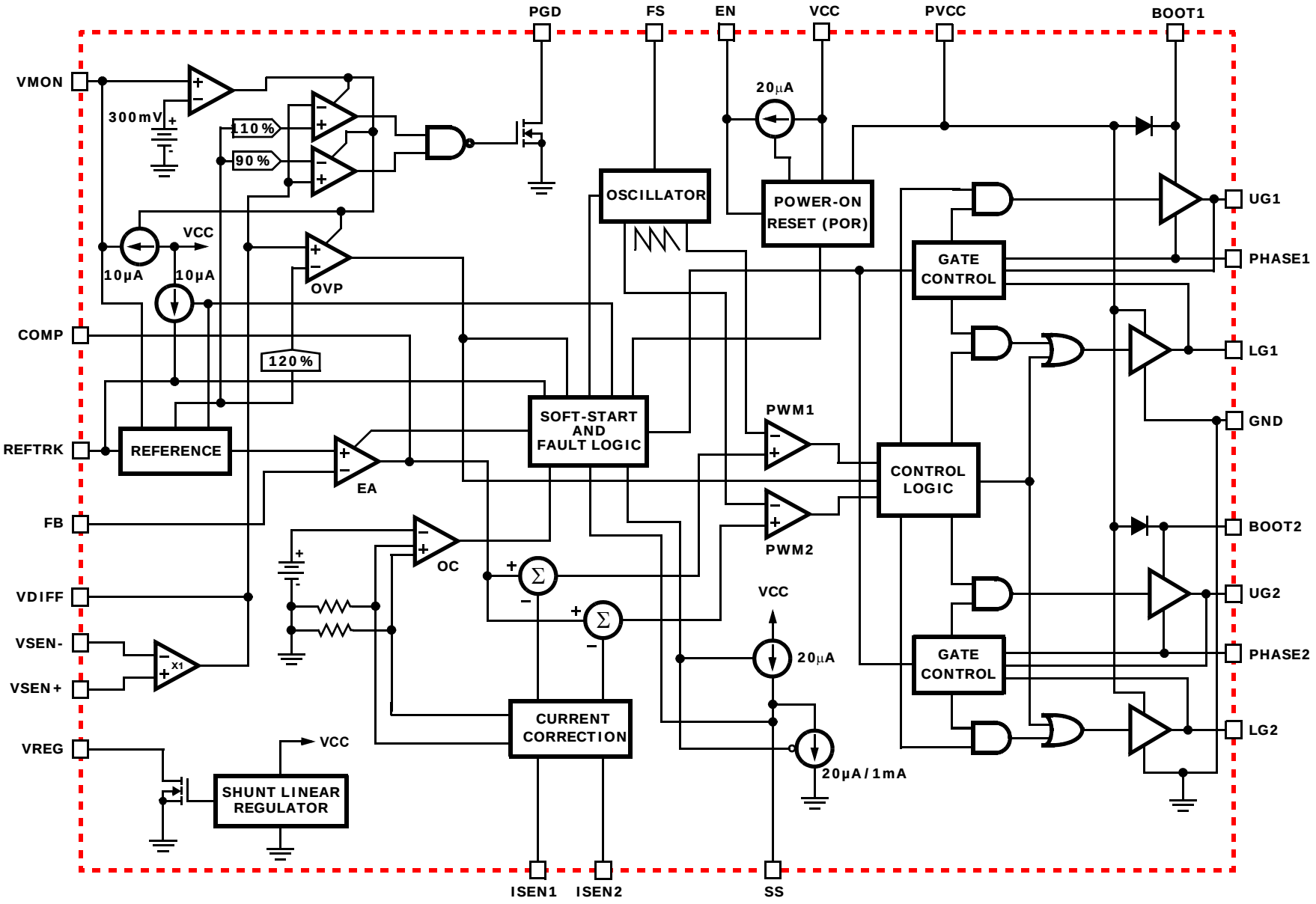
1. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8121. For more information on MSL please see techbrief TB363.

Pin Configuration

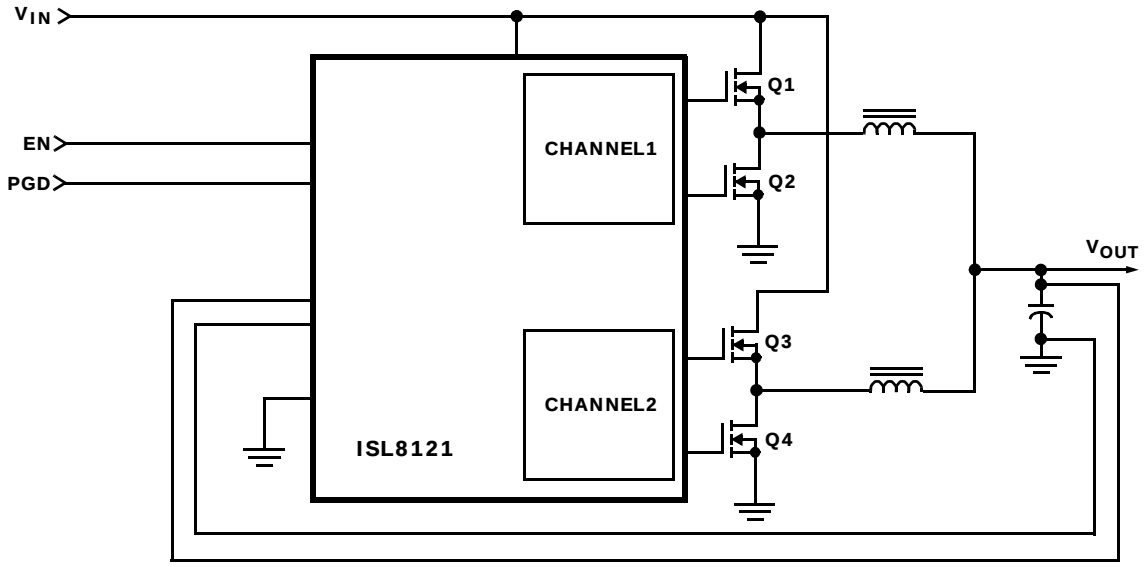
ISL8121
(24 LD QFN)
TOP VIEW



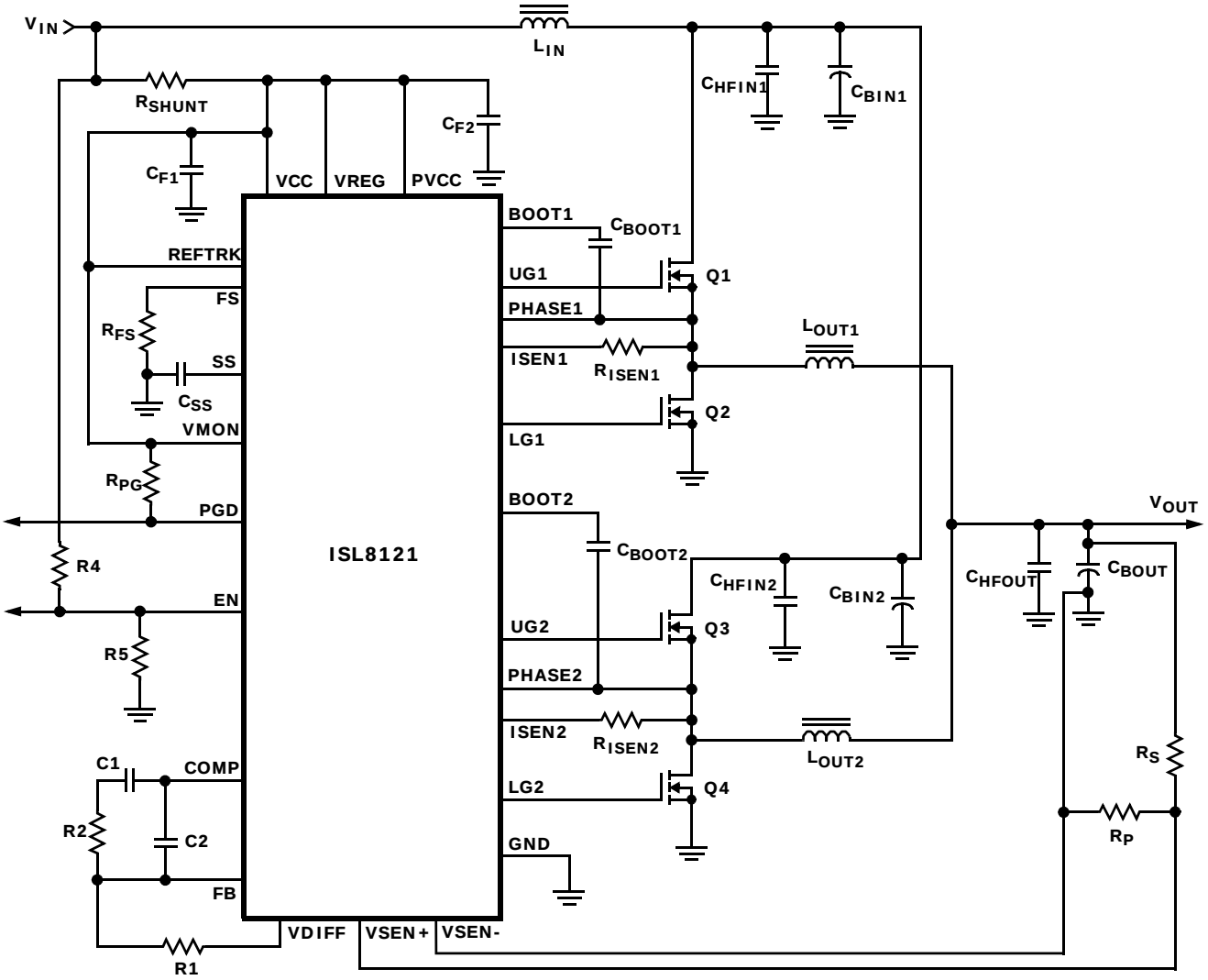
Block Diagram



Simplified Power System Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage, VCC, PVCC . . . . . -0.3V to +6.5V
Shunt Regulator Voltage, V_{VREG}. . . . . -0.3V to +6.5V
Boot Voltage, V_{BOOT}. . . . . .PGND - 0.3V to PGND + 27V
Phase Voltage, V_{PHASE} . . . . . .V_{BOOT} - 7V to V_{BOOT} + 0.3V
Upper Gate Voltage, V_{UG}. . . .V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
Lower Gate Voltage, V_{LG}. . . . . PGND - 0.3V to VCC + 0.3V
Input, Output, or I/O Voltage. . . . GND - 0.3V to VCC + 0.3V

Recommended Operating Conditions

Supply Voltage, VCC. . . . . .+4.9V to +5.5V
Ambient Temperature . . . . . .-40°C to +85°C
Junction Temperature Range . . . . . .-40°C to +125°C

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 4, 5)	43	7

Maximum Junction Temperature (Note 6). . . . . +150°C
Maximum Storage Temperature Range . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
6. Operation with die temperatures between +125°C and +150°C can be tolerated for short periods of time, however, in order to maximize the operating life of the IC, it is strongly recommended that the effective continuous operating junction temperature of the die should not exceed +125°C.

Electrical Specifications

Operating Conditions: V_{CC} = 5V, T_J = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
BIAS SUPPLY AND INTERNAL OSCILLATOR					
Input Bias Supply Current	I_{VCC}; EN > 0.7V; LG, UG open		7.6	**9**	mA
Rising VCC POR (Power-On Reset) Threshold		**4.30**	4.40	**4.50**	V
VCC POR Hysteresis		**0.46**	0.51	**0.58**	V
Rising PVCC POR Threshold		**3.60**	3.67	**3.75**	V
Shunt Regulation	V_{VCC}; I_{VREG} = 0mA to 120mA	**4.90**	5.10	**5.35**	V
Maximum Shunt Current	I_{VREG_MAX}	**120**			mA
Switching Frequency (per Channel; Note 8)	F_{SW}	**150**		**2000**	kHz
Frequency Tolerance	F_{SW}	**-10**		**10**	%
Oscillator Peak-to-Peak Ramp Amplitude	V_{OSC}		1.4		V
Maximum Duty Cycle	d_{MAX}		66		%
CONTROL THRESHOLDS					
EN Threshold			0.65		V
EN Hysteresis Current			20		µA
VMON Power-Good Enable Threshold	V_{VMON_TH}	**290**	305	**320**	mV
VMON Hysteresis Current			10		µA
SOFT-START					
SS Current	I_{SS}		22		µA
SS Ramp Amplitude		**0.55**		**3.60**	V
SS Threshold for Output Gates Turn-Off		**0.40**			V
REFERENCE AND DAC					
System Accuracy (Industrial Temp. Range)		**-0.8**		**0.8**	%
Internal Reference	V_{REF}		0.6		V
External Reference DC Amplitude Range	V_{REFTRK} (DC)	**0.1**		**2.3**	V

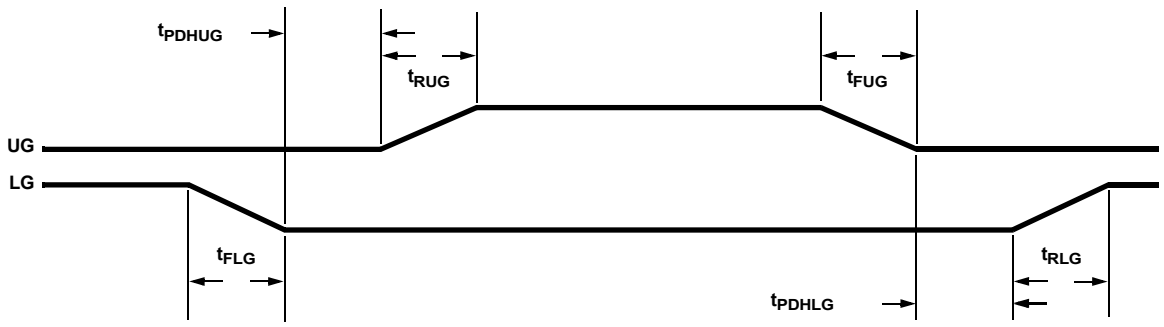
Electrical Specifications Operating Conditions: V_{CC} = 5V, T_J = -40°C to +85°C, unless otherwise specified. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
External Reference DC Offset Range	V_{REFTRK} (DC) offset	**-4.5**		**4.5**	mV
ERROR AMPLIFIER AND REMOTE SENSING					
DC Gain (Note 7)	R_L = 10k to ground		80		dB
Gain-Bandwidth Product (Note 7)	C_L = 10pF		95		MHz
Slew Rate (Note 7)	C_L = 10pF		30		V/µs
Maximum Output Voltage	No load	**4.0**			V
Minimum Output Voltage	No load			**0.7**	V
VSEN+, VSEN- Input Resistance		**140**	225		kΩ
POWER GOOD					
PGD Rising Lower Threshold			92		%
PGD Rising Upper Threshold			112		%
PGD Threshold Hysteresis			2.5		%
PROTECTION					
Overcurrent Trip Level		**80**	103	**120**	µA
Overvoltage Threshold	VDIFF Rising		122		%
Overvoltage Hysteresis	VDIFF Falling		5.5		%
SWITCHING TIME					
UG Rise Time (Note 7)	t_{RUG}; V_{VCC} = 5V, 3nF Load		8		ns
LG Rise Time (Note 7)	t_{RLG}; V_{VCC} = 5V, 3nF Load		8		ns
UG Fall Time (Note 7)	t_{FUG}; V_{VCC} = 5V, 3nF Load		8		ns
LG Fall Time (Note 7)	t_{FLG}; V_{VCC} = 5V, 3nF Load		4		ns
UG Turn-On Non-overlap (Note 7)	t_{PDHUG}; V_{VCC} = 5V, 3nF Load		8		ns
LG Turn-On Non-overlap (Note 7)	t_{PDHLG}; V_{VCC} = 5V, 3nF Load		8		ns
OUTPUT					
Upper Drive Source Resistance	100mA Source Current		1.0	**2.5**	Ω
Upper Drive Sink Resistance	100mA Sink Current		1.0	**2.5**	Ω
Lower Drive Source Resistance	100mA Source Current		1.0	**2.5**	Ω
Lower Drive Sink Resistance	100mA Sink Current		0.4	**1.0**	Ω

NOTES:

7. Parameter magnitude guaranteed by design.
8. Not a tested parameter; range provided for reference only.
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Timing Diagram



Functional Pin Descriptions

VCC (Pin 8)

Bias supply for the IC's small-signal circuitry. Connect this pin to a 5V supply and locally decouple using a quality 0.1µF ceramic capacitor. This pin is monitored for POR purposes. VCC bias may be applied in the absence of PVCC bias.

PVCC (Pin 15)

Power supply pin for the MOSFET drives. Connect this pin to a 5V supply and locally decouple using a quality 1µF ceramic capacitor. This pin is monitored for POR purposes. PVCC bias should not be applied in the absence of VCC bias.

VREG (Pin 7)

This pin is the output of the internal shunt regulator. The internal shunt regulator monitors and regulates the voltage at the VCC pin. In applications where the chip bias, including that necessary to drive the external MOSFETs, is below the current rating of this pin, connect it to VCC and PVCC, then connect this node to the input supply via a properly sized resistor. Should the input voltage vary over a wide range and/or the bias current required exceed the intrinsic capability of the on-board regulator, use this pin in conjunction with an external NPN transistor and a couple of resistors to create a more flexible bias supply for the ISL8121. In any configuration, pay particular attention to the chip's limitations in terms of both current sinking capability of the shunt regulator, as well as the internal power dissipation.

For more information, see "Bias Supply Considerations" on page 16.

GND (Pin 25)

Connect this pad to the circuit ground using the shortest possible path (one to four vias to the internal ground plane, placed on the soldering pad are recommended). All internal small-signal circuitry, as well as the lower gates' return paths are referenced to this pin.

REFTRK (Pin 24)

This pin represents an optional reference input, as well as a clamp voltage for the internal reference. If utilizing the ISL8121's internal 0.6V reference, and desire no special tracking features enabled, electrically connect this pin to the VCC pin, or leave it open. Internal or external reference operation mode is dictated by the VMON pin.

While operating in internal reference mode, this pin represents an internal reference clamp that can be used for implementation of various tracking features. In this operating mode, a small internal current is sourced on this pin, pulling it high if left open.

If utilizing the ISL8121 in conjunction with an external reference, connect the desired stimulus to this pin; the sensed output of the ISL8121 converter follows this input.

While operating with an external reference, the power-good and overvoltage protection functions are disabled while the VMON pin voltage is below its threshold (typically 300mV).

VMON (Pin 3)

The status of this pin is checked every time the chip is enabled or POR is released; should its potential be lower than 3.5V (typical), the REFTRK potential is assumed to be an externally-provided reference and the ISL8121 proceeds to regulate the sensed output voltage to this external reference. When operating using the internal reference voltage, connect this pin to VCC (to bypass the mechanism described above).

While operating with an externally-provided reference, connect this pin to a properly-sized resistor divider off the voltage to be monitored. PGD and OVP functions are enabled when this pin exceeds its monitored threshold (typically 300mV).

This pin is normally floating (high impedance input) until it exceeds its detect threshold. Once the threshold is exceeded, a small current is sourced on this pin; this current, along with a properly sized resistor network, allows the user to adjust the threshold hysteresis.

For more information, refer to "External Reference Operation" on page 13.

EN (Pin 9)

This pin is a precision-threshold (approximately 0.6V) enable pin. Pulled above the threshold, the pin enables the controller for operation, initiating a soft-start. Normally a high impedance input, once it is pulled above its threshold, a small current is sourced on this pin; this current, along with a properly sized resistor network, allows the user to adjust the threshold hysteresis. Pulled below the falling threshold, this pin disables controller operation, by ramping down the SS voltage and discharging the output.

VSEN+, VSEN-, and VDIFF (Pins 2, 1, and 4)

The inputs and output of the on-board unity-gain operational amplifier intended for differential output sensing. Connect VSEN- and VSEN+ to the output load's local GND and VOUT, respectively; VDIFF will reflect the load voltage referenced to the chip's local ground. Connect the feedback network to the voltage thus reflected at the VDIFF pin. Should the circuit not allow implementation of remote sensing, connect the VSEN+ and VSEN- pins to the physical place where voltage is to be regulated.

Connect the resistor divider setting the output voltage at the input of the differential amplifier. To minimize the error introduced by the resistance of differential amplifier's inputs, select resistor divider values smaller than 1kΩ. VDIFF is monitored for overvoltage events and for PGD reporting purposes.

FB and COMP (Pins 5 and 6)

The internal error amplifier's inverting input and output respectively. These pins are connected to the external network used to compensate the regulator's feedback loop.

ISEN1, ISEN2 (Pins 17, 13)

These pins are used to close the current feedback loop and set the overcurrent protection threshold. A resistor connected between each of these pins and their corresponding PHASE pins determine a certain current flow magnitude during the lower MOSFET's conduction interval. The resulting currents established through these resistors are used for channel current balancing and overcurrent protection.

Use Equation 1 to select the proper R_{ISEN} resistor:

$$R_{ISEN} = \frac{r_{DS(ON)} \times I_{OUT}}{50\mu A} \quad \text{(EQ. 1)}$$

where:

$r_{DS(ON)}$ = lower MOSFET drain-source ON resistance (Ω)

I_{OUT} = channel maximum output current (A)

Read "Current Loop" on page 9, "Current Sensing" on page 11, "Channel-Current Balance" on page 11, and "Overcurrent Protection" on page 11 for more information.

UG1, UG2 (Pins 19, 11)

Connect these pins to the upper MOSFETs' gates. These pins are used to control the upper MOSFETs and are monitored for shoot-through prevention purposes. Minimize the impedance of these connections. Maximum individual channel duty cycle is limited to 66%.

BOOT1, BOOT2 (Pins 20, 10)

These pins provide the bias voltage for the upper MOSFETs' drives. Connect these pins to appropriately-chosen external bootstrap capacitors. Internal bootstrap diodes connected to the PVCC pins provide the necessary bootstrap charge. Minimize the impedance of these connections.

PHASE1, PHASE2 (Pins 18, 12)

Connect these pins to the sources of the upper MOSFETs. These pins are the return path for the upper MOSFETs' drives. Minimize the impedance of these connections.

LG1, LG2 (Pins 16, 14)

These pins are used to control the lower MOSFETs and are monitored for shoot-through prevention purposes. Connect these pins to the lower MOSFETs' gates. Minimize the impedance of these connections.

SS (Pin 23)

This pin allows adjustment of the output voltage soft-start ramp rate, as well as the hiccup interval following an overcurrent event. The potential at this pin is used as a clamp voltage for the internal error amplifier's non-inverting input, regulating its rate of rise during start-up. Connect this pin to a capacitor referenced to ground. Small internal current sources linearly charge and discharge this capacitor, leading to similar variation in the ramp up/down of the output voltage. While below 0.3V, all output drives are turned off. As this pin ramps up, the drives are not enabled but only after the first UG pulse emerges (avoid draining the output, if pre-charged). If no UG pulse are generated until the SS exceeds the top of the oscillator ramp, at that time all gate operation is enabled, allowing immediate draining of the output, as necessary.

SS voltage has a ~0.7V offset above the reference clamp, meaning the reference clamp rises from 0V with unity gain correspondence as the SS pin exceeds 0.7V. For more information, please refer to "Soft-Start" on page 11.

FS (Pin 22)

This pin is used to set the switching frequency. Connect a resistor, R_{FS}, from this pin to ground and size it according to the graph in Figure 1 or Equation 2.

$$R_{FS} = 10^{(10.61 - (1.035 \cdot \log(F_{SW})))} \quad \text{(EQ. 2)}$$

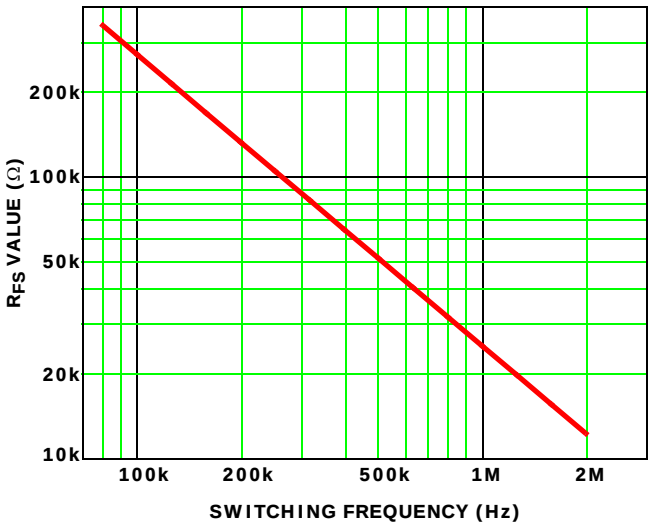


FIGURE 1. SWITCHING FREQUENCY VS. R_{FS} VALUE

PGD (Pin 21)

This pin represents the output of the on-board power-good monitor. Thus, the FB pin is monitored and compared against a window centered around the available reference; an FB voltage within the window disables the open-collector output, allowing the external resistor to pull-up PGD high. Approximate pull-down device impedance is 65Ω.

While operating with an external reference, the power-good function is enabled once the VMON pin amplitude exceeds its monitored threshold (typically 300mV).

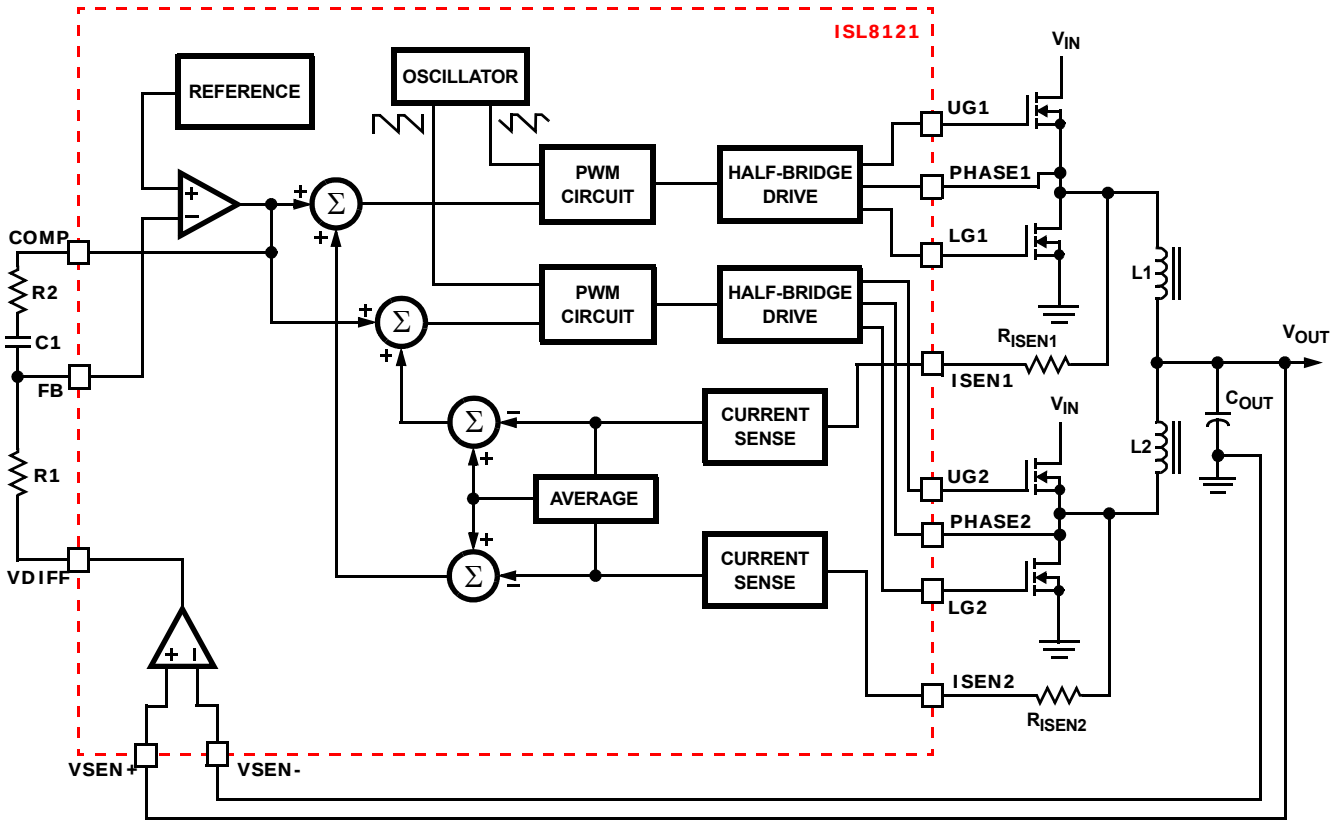


FIGURE 2. SIMPLIFIED BLOCK DIAGRAM OF THE ISL8121 VOLTAGE AND CURRENT CONTROL LOOPS

Operation

Figure 2 shows a simplified diagram of the voltage regulation and current loops. The voltage loop is used to precisely regulate the output voltage, while the current feedback is used to balance the output currents, I_{L1} and I_{L2}, of the two power channels.

VOLTAGE LOOP

Feedback from the output voltage is fed via the on-board differential amplifier and applied via resistor R1 to the inverting input of the Error Amplifier. The signal generated by the error amplifier is summed up with the current correction error signal and applied to the positive inputs of the PWM circuit comparators. Out-of-phase sawtooth signals are applied to the two PWM comparators inverting inputs. Increasing error amplifier voltage results in increased duty cycle. This increased duty cycle signal is passed to the output drivers with no phase reversal to drive the external MOSFETs. Increased duty cycle, translating to increased ON-time for the upper MOSFET transistor, results in increased output voltage, compensating for the low output voltage which lead to the increase in the error signal in the first place.

CURRENT LOOP

The current control loop is only used to finely adjust the individual channel duty cycle, in order to balance the current carried by each phase. The information used for this control is the voltage that is developed across $r_{DS(ON)}$ of each lower MOSFET, while they are conducting. A resistor converts and scales the voltage across each MOSFET to a current that is applied to the current sensing circuits within the ISL8121. Output from these sensing circuits is averaged and used to compute a current error signal. Each PWM channel receives a current signal proportional to the difference between the average sensed current and the individual channel current. When a PWM channel's current is greater than the average current, the signal applied via the summing correction circuit to the PWM comparator reduces the output pulse width (duty cycle) of the comparator to compensate for the detected above average current in the respective channel.

MULTI-PHASE POWER CONVERSION

Multi-phase power conversion provides a cost-effective power solution when load currents are no longer easily supported by single-phase converters. Although its greater complexity presents additional technical challenges, the multi-phase approach offers advantages with improved response time, superior ripple cancellation, and thermal distribution.

INTERLEAVING

The switching of each channel in a ISL8121-based converter is timed to be symmetrically out of phase with the other channel. As a result, the two-phase converter

has a combined ripple frequency twice the frequency of one of its phases. In addition, the peak-to-peak amplitude of the combined inductor currents is proportionately reduced. Increased ripple frequency and lower ripple amplitude generally translate to lower per-channel inductance and/or lower total output capacitance for any given set of performance specification.

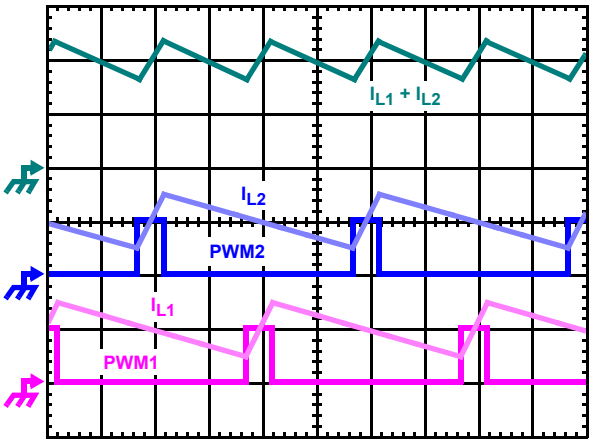


FIGURE 3. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 2-PHASE CONVERTER

Figure 3 illustrates the additive effect on output ripple frequency. The two channel currents (I_{L1} and I_{L2}), combine to form the AC ripple current and the DC load current. The ripple component has two times the ripple frequency of each individual channel current.

To understand the reduction of ripple current amplitude in the multi-phase circuit, examine Equation 3, which represents an individual channel's peak-to-peak inductor current.

$$I_{L,PP} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot f_S \cdot V_{IN}} \quad \text{(EQ. 3)}$$

V_{IN} and V_{OUT} are the input and output voltages, respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multi-phase converters, the capacitor current is the sum of the ripple currents from each of the individual channels.

$$I_{PP} = \frac{(V_{IN} - N \cdot V_{OUT}) \cdot V_{OUT}}{L \cdot f_S \cdot V_{IN}} \quad \text{(EQ. 4)}$$

Peak-to-peak ripple current decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors (should output high-frequency ripple be an important design parameter).

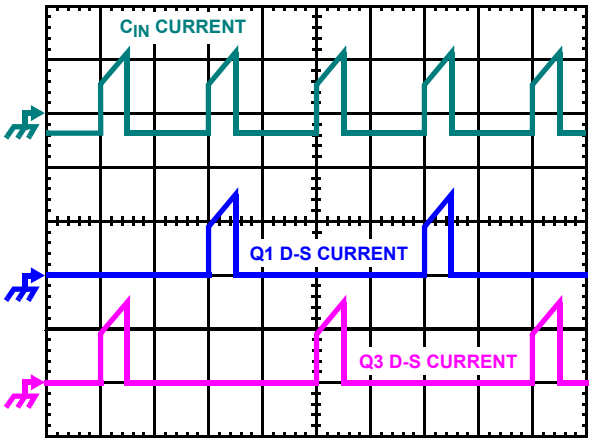


FIGURE 4. INPUT CAPACITOR CURRENT AND INDIVIDUAL CHANNEL CURRENTS IN A 2-PHASE CONVERTER

Another benefit of interleaving is the reduction of input ripple current. Input capacitance is determined in a large part by the maximum input ripple current. Multi-phase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 4 illustrates input currents from a two-phase converter combining to reduce the total input ripple current.

Figure 28, part of "Input Capacitor Selection" on page 24, can be used to determine the input-capacitor RMS current based on load current and duty cycle. The figure is provided as an aid in determining the optimal input capacitor solution.

PWM OPERATION

One switching cycle for the ISL8121 is defined as the time between consecutive PWM pulse terminations (turn-off of the upper MOSFET on a channel). Each cycle begins when a switching clock signal commands the upper MOSFET to go off. The other channel's upper MOSFET conduction is terminated 1/2 of a cycle later.

Once a channel's upper MOSFET is turned off, the lower MOSFET remains on for a minimum of 1/3 cycle. This forced off time is required to assure an accurate current sample. Following the 1/3-cycle forced off time, the controller enables the upper MOSFET output. Once enabled, the upper MOSFET output transitions high when the sawtooth signal crosses the adjusted error-amplifier output signal, as illustrated in Figure 2. Just prior to the upper drive turning the MOSFET on, the lower MOSFET drive turns the freewheeling element off. The upper MOSFET is kept on until the clock signals the beginning of the next switching cycle and the PWM pulse is terminated.

CURRENT SENSING

ISL8121 senses current by sampling the voltage across the lower MOSFET during its conduction interval. MOSFET $r_{DS(ON)}$ sensing is a no-added-cost method to sense current for load line regulation, channel current balance, module current sharing, and overcurrent protection.

The ISEN pins are used as current inputs for each channel. Internally, a virtual ground is created at the ISEN pins. The R_{ISEN} resistors are used to size the current flow through the ISEN pins, proportional to the lower MOSFETs' $r_{DS(ON)}$ voltage, during their conduction periods. The current thus developed through the ISEN pins is internally averaged, then the current error signals resulting from comparing the average to the individual current signals are used for channel current balancing.

Select the value for the R_{ISEN} resistors based on the room temperature $r_{DS(ON)}$ of the lower MOSFETs and the full-load total converter output current, I_{FL}.

$$R_{ISEN} = \frac{r_{DS(ON)}}{50 \times 10^{-6}} \cdot \frac{I_{FL}}{2} \quad \text{(EQ. 5)}$$

As this current sense path is also used for OC detection, ensure that at maximum power train temperature rise and maximum output current loading the OC protection is not inadvertently tripped. OC protection current level through the ISEN pins is listed in the "Electrical Specifications" table on page 6.

CHANNEL-CURRENT BALANCE

Another benefit of multi-phase operation is the thermal advantage gained by distributing the dissipated heat over multiple devices and greater area. By doing this, the designer avoids the complexity of driving multiple parallel MOSFETs and the expense of using expensive heat sinks and exotic magnetic materials.

All things being equal, in order to fully realize the thermal advantage, it is important that each channel in a multi-phase converter be controlled to deliver about the same current at any load level. Intersil's ISL8121 ensure current balance by comparing each channel's current to the average current delivered by both channels and making appropriate adjustments to each channel's pulse width based on the resultant error. The error signal modifies the pulse width to correct any unbalance and force the error toward zero.

Conversely, should a channel-to-channel imbalance be desired, such imbalance can be created by adjusting the individual channel's R_{ISEN} resistor. Asymmetrical layouts, where one phase of the converter is naturally carrying more current than the other, or where one of the two phases is subject to a more stringent thermal environment limiting its current-carrying capability, are instances where this adjustment is particularly useful, helping to cancel out the design-intrinsic thermal or current imbalances.

SOFT-START

The soft-start function allows the converter to bring up the output voltage in a controlled fashion, resulting in a linear ramp-up. As soon as the controller is fully enabled for operation, the SS pin starts to output a small current which charges the external capacitor, C_{SS}, connected to this pin. An internal reference clamp controlled by the potential at the SS pin releases the reference to the input of the error amplifier with a 1:1 correspondence for SS potential exceeding 0.7V (typically). Figure 5 details a normal soft-start start-up. Equation 6 helps determine the approximate time period during which the controlled output voltage is ramped from 0V to the desired DC-set level.

$$t_{SS} = \frac{C_{SS} \cdot V_{REF}}{I_{SS}} \quad \text{(EQ. 6)}$$

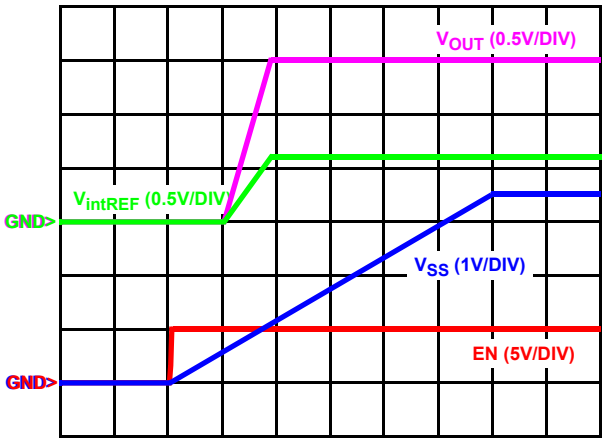


FIGURE 5. NORMAL SOFT-START WAVEFORMS FOR ISL8121-BASED MULTI-PHASE CONVERTER

Whenever the ISL8121's power-on reset falling threshold is tripped, or it is disabled via the EN pin, the SS capacitor is quickly discharged via an internal pull-down device (represented as the 1mA, typical, current source).

As the SS pin's positive excursion is internally clamped to about 3.5V, insure that any external pull-up device does not force more than 3mA into this pin.

Should OC protection be tripped while the ISL8121 is operating in internal-reference mode and the SS pin not be allowed to fully discharge the SS capacitor, the ISL8121 cannot continue the normal SS cycling.

OVERCURRENT PROTECTION

The individual channel currents, as sensed via the PHASE pins and scaled via the ISEN resistors, as well as their combined average are continuously monitored and compared with an internal overcurrent (OC) reference. If the combined channel current average exceeds the reference current, the overcurrent comparator triggers an overcurrent event. Similarly, an OC event is also triggered if either channel's current exceeds the OC reference for seven consecutive switching cycles.

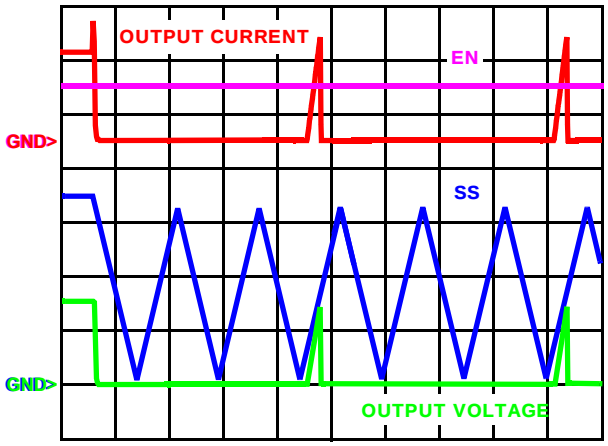


FIGURE 6. OVERCURRENT BEHAVIOR WHILE IN INTERNAL REFERENCE MODE

As a result of an OC event, output drives turn off both upper and lower MOSFETs, and the SS capacitor is discharged via a 20µA current source. The behavior following this standard response varies depending whether the controller is operating in internal (using internal reference; VMON > 3.5V) or external reference mode (using external reference; VMON < 3.5V). As shown in Figure 6, the soft-start capacitor discharge prompted by the OC event is followed by two SS cycles, during which the ISL8121 stays off. Following the dormant SS cycles, the controller attempts to re-establish the output. Should the OC condition been removed, the output voltage is ramped up and operation resumes as normal. Should the OC condition still be present and result in another OC event, the entire behavior repeats until the OC condition is removed or the IC is disabled. Figure 7 details the OC behavior while in external reference mode. Following the OC event, the output drives are turned off, the ISL8121 latches off, and the SS capacitor is discharged to ground. Resetting the OC latch involves removal of bias power or cycling of the EN pin (pictured in Figure 7). Should the OC event been removed, the controller initiates a new SS cycle and restores the output voltage.

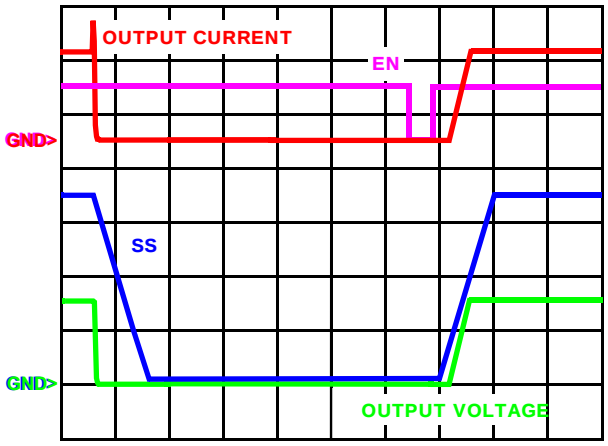


FIGURE 7. OVERCURRENT BEHAVIOR WHILE IN EXTERNAL REFERENCE MODE

SETTING THE OUTPUT VOLTAGE

The ISL8121 uses a precision internal reference voltage to set the output voltage. Based on this internal reference, the output voltage can thus be set from 0.6V up to a level determined by the input voltage, the maximum duty cycle, and the conversion efficiency of the circuit. Equation 7 estimates this maximum amplitude the output voltage can be regulated to.

$$V_{OUTMAX} = d_{MAX} \cdot V_{IN} \cdot \text{Efficiency} \qquad \text{(EQ. 7)}$$

Obviously, ensure that the input voltage and all the voltages sampled by the ISL8121 do not exceed the controller's absolute maximum limits, or any other limits specified in this document.

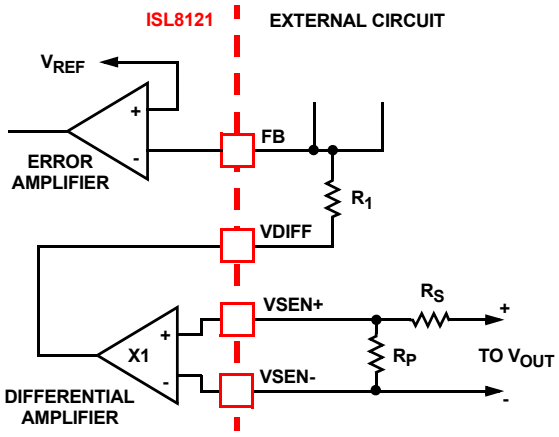


FIGURE 8. SETTING THE OUTPUT VOLTAGE AT THE INPUT OF THE DIFFERENTIAL AMPLIFIER

The output voltage can be set via a simple resistor divider, as shown in Figure 8. It is recommended this resistor divider is connected at the input of the differential amplifier (as this amplifier is powered from the IC's 5V bias and has limited input range).

$$R_P = R \cdot \frac{V_{OUT}}{V_{OUT} - V_{REF}} \qquad R_S = R \cdot \frac{V_{OUT}}{V_{REF}} \qquad \text{(EQ. 8)}$$

To avoid degradation of DC regulation tolerance due to the differential amplifier's input resistance, a size requirement is placed on the combined value of R_P and R_S. Consider R to be the parallel combination of these two resistors, and use a value of 2kΩ or less for R; use the following equations to determine the value of R_P and R_S, based on the desired out-put voltage, the reference voltage, and the chosen value of R.

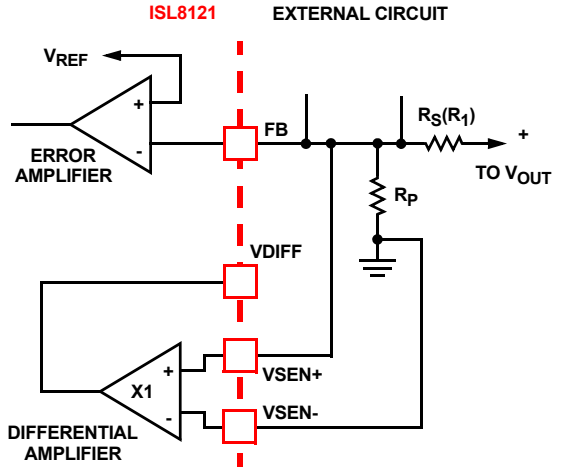


FIGURE 9. SETTING THE OUTPUT VOLTAGE AT THE FB PIN

The differential amplifier can be used even if remote output sensing is not desired or not feasible, simply connect VSEN- to the local ground and connect VSEN+ to the output voltage being monitored. Should one desire to bypass the differential amplifier, the circuit in Figure 9 is recommended as the proper implementation. Since its output is monitored for OVP and PGD purposes, the differential amplifier needs to be connected to the feedback circuit at all times, hence its input connections to FB and local ground. However, its output, VDIFF, can be left open. The resistor divider setting the output voltage is calculated in a manner identical to that already revealed.

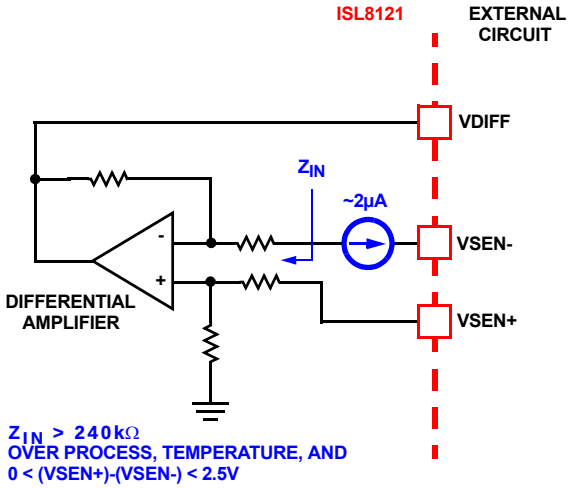


FIGURE 10. SETTING THE OUTPUT VOLTAGE AT THE INPUT OF THE DIFFERENTIAL AMPLIFIER

DIFFERENTIAL AMPLIFIER'S UNITY GAIN NETWORK

The differential amplifier on the ISL8121 utilizes a typical resistive network along with active compensating circuitry to set its unity gain. This resistive network can affect the DC regulation setpoint in proportion to its relative magnitude compared to the external output voltage setting resistor divider. Figure 10 details the internal resistive network. For minimal impact on the output voltage setting, follow the guidelines presented in "Setting the Output Voltage" on page 12.

EXTERNAL REFERENCE OPERATION

The ISL8121 is capable of accepting an external voltage and using it as a reference for its output regulation. To enable this mode of operation, the VMON pin potential has to be below 3.5V and the reference voltage has to be connected to the REFTRK pin. The internal or external reference mode of operation is latched in every time the POR is released or the ISL8121 is enabled. The highest magnitude external reference fed to the REFTRK pin that the ISL8121 can follow is limited to 2.3V. The ISL8121 utilizes a small initial negative offset (typically about 50mV) in the voltage loop at the beginning of it soft-start, to counteract any positive offsets that may have undesirable effects. As this initial offset is phased out as the reference is ramped up to around 200mV, in order to avoid an error in the output regulation level, it is recommended the external reference has an amplitude (final, DC level) exceeding 300mV.

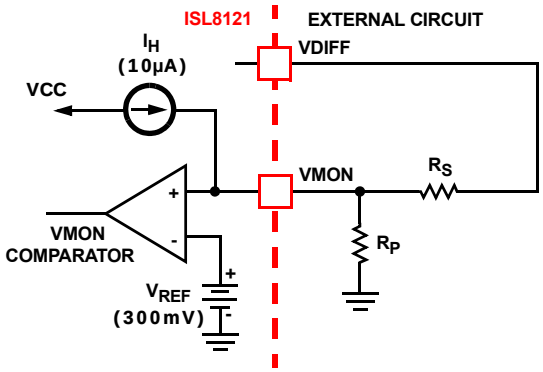


FIGURE 11. SETTING THE MONITORING THRESHOLD AND HYSTERESIS

While in external reference (ER) mode, the threshold sensitive VMON pin can be used to control when the ISL8121 starts to monitor the output for PGD and OVP protection purposes. As shown in Figure 11, connect the VMON pin to the voltage to be monitored via a resistor divider. An internal current source helps set a user-adjustable monitor threshold hysteresis. Choose resistor values according to desired hysteresis voltage, V_H, and desired rising threshold, V_T.

$$R_S = \frac{V_H}{I_H} \qquad R_P = \frac{R_S \cdot V_{REF}}{V_T - V_{REF}} \qquad \text{(EQ. 9)}$$

Make note that, in Equation 9, V_{REF} refers to the reference of the VMON comparator (300mV).

Intersil recommends the VMON threshold is set to be tripped when the external reference voltage reaches at least 90% of the final DC value. Since PGD and OVP monitoring are relative to the external reference

magnitude, it is important to understand that the PGD and OVP thresholds will move in proportion to the moving reference (externally soft-started reference).

ISL8121 POWER-GOOD OPERATION

The open-collector PGD output reports on the quality of the regulated output voltage. Once the ISL8121 is enabled and the VMON pin is above its threshold, PGD goes open circuit when the output enters the power-good window (see “Electrical Specifications” table on page 6), and stays open for as long as the output remains within the specified window. The PGD is immediately pulled low if the ISL8121 is disabled by removal of bias, toggling of the EN pin, or upon encountering of an overcurrent event; PGD is allowed to report the status of the output as soon as operation is resumed following any of these events.

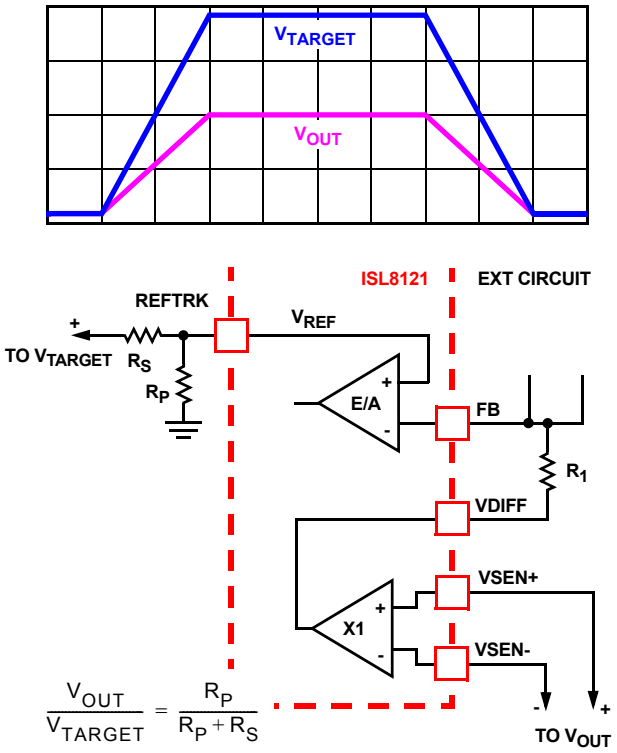


FIGURE 12. RATIOMETRIC VOLTAGE TRACKING

The VMON pin is used in external-reference configurations, where the reference is controlled by a circuit external to the ISL8121. As such, the ISL8121 has no way of ‘knowing’ when the external reference has stabilized to its full value, or is within a certain percentage of its final value. Thus, the VMON pin’s functionality can be used to indicate when a desired threshold has been reached (either by monitoring the reference itself, or the output voltage controlled by the ISL8121). By default, when operating in external reference mode and desiring PGD monitoring as shown in this datasheet, it is recommended the VMON is set to trip its threshold when the output voltage (or reference) reaches 92% of the final set value, choosing the resistor divider as to achieve a 2% hysteresis.

When operating in internal-reference mode, the value of the reference is known to the ISL8121, so the VMON pin function can be bypassed by tying it to VCC potential.

VOLTAGE TRACKING AND SEQUENCING

By making creative use of the reference clamps at the SS and REFTRK pins, and/or the available external reference input, as well as the functionality of the EN pin, the ISL8121 can accommodate the full spectrum of tracking and sequencing options. Figures 13 and 14 offer some implementation suggestions for a few typical situations.

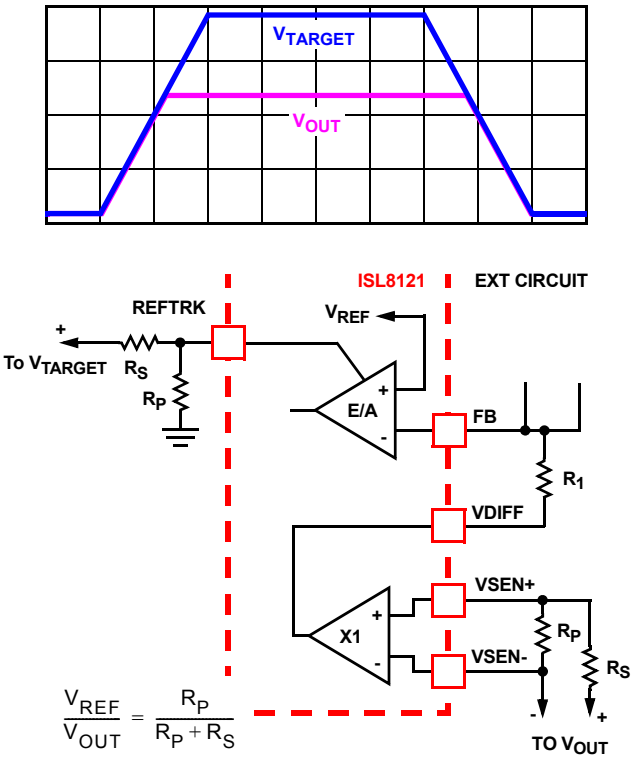


FIGURE 13. COINCIDENTAL VOLTAGE TRACKING

Simple ratiometric external voltage tracking, such as that required by the termination voltage regulator for double data rate (DDR) memory can be implemented by feeding a reference voltage equal to 0.5 of the memory core voltage (VDDQ) to the reference input of the ISL8121, as shown in Figure 12. The resistor divider at the REFTRK pin sets the V_{OUT} level. Select a suitable SS capacitor, such that the SS clamp does not interfere with the desired ramp-up time or slope of V_{OUT}.

Coincidental tracking using the internal reference results in a behavior similar to that presented in Figure 13. The resistor divider at the input of the differential amplifier sets the output voltage, V_{OUT}, to the desired regulation level. The same resistor divider used at the REFTRK pin divides down the voltage to be tracked, effectively scaling it to the magnitude of the internal reference. As a result, the output voltage ramps up at the same rate as the target voltage, its ramp-up leveling off at the programmed regulation level established by the R_S/R_P resistor divider.

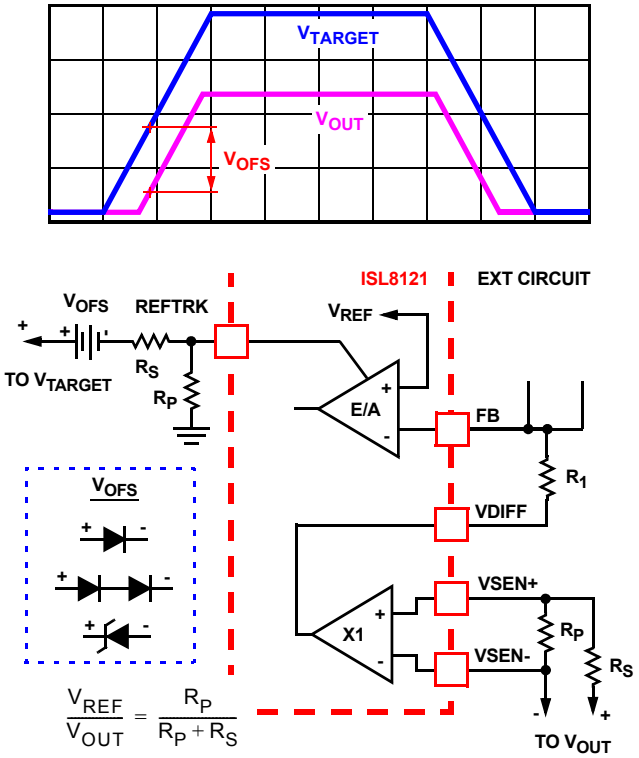


FIGURE 14. OFFSET VOLTAGE TRACKING

Offset tracking can be accomplished via a circuit similar to that used for coincidental tracking (see Figure 14). The desired offset can be implemented via a voltage source inserted in line with the resistor divider present at the REFTRK pin. Since most offset tracking requirements are subject to fairly broad tolerances, simple voltage drop sources can be used. Figure 14 exemplifies the use of various counts of forward-biased diodes or that of a schottky, although other options are available.

Sequential start-up control is easily implemented via the EN pin, using either a logic control signal or the ISL8121's own EN threshold as a power-good detector for the tracked, or sequence-triggering, voltage. See Figure 15 for details of control using the EN pin.

OVERVOLTAGE PROTECTION

Although the normal feedback loop operation naturally counters overvoltage (OV) events the ISL8121 benefits from a secondary, fixed threshold overvoltage protection. Should the output voltage exceed 120% of the reference, the lower MOSFETs are turned on. Once turned on, the lower MOSFETs are only turned off when the sensed output voltage drops below the 110% falling threshold of the OV comparator. The OVP behavior repeats for as long as the ISL8121 is biased, should the sensed output voltage rise back above the designated threshold. The occurrence of an OVP event does not latch the controller; should the phenomenon be transitory, the controller resumes normal operation following such an event.

When operating in external-reference mode, the OVP monitoring is enabled when the VMON pin exceeds its rising threshold. For as long as the ISL8121 is biased, OVP has the highest priority, bypassing all other control mechanisms and acting directly onto the lower MOSFETs, as described. Disabling the IC via the EN pin does not turn off OVP protection.

START-UP INTO A PRE-CHARGED OUTPUT

The ISL8121 also has the ability to start up into a pre-charged output, without causing any unnecessary disturbance. The FB pin is monitored during soft-start, and should it be higher than the equivalent internal ramping reference voltage, the output drives hold both MOSFETs off. Once the internal ramping reference exceeds the FB pin potential, the output drives are enabled, allowing the output to ramp from the pre-charged level to the final level dictated by the circuit setting.

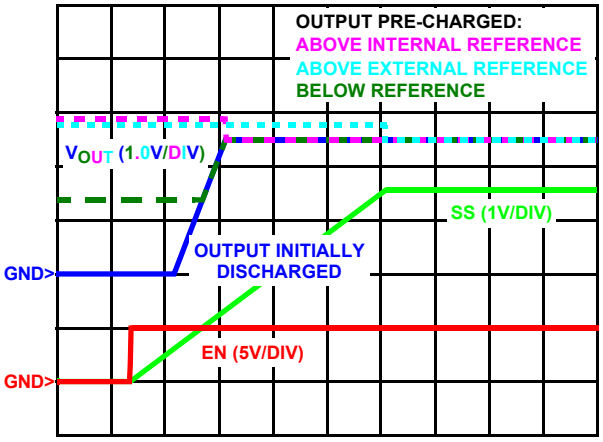


FIGURE 15. SOFT-START WAVEFORMS INTO A PRE-CHARGED OUTPUT CAPACITOR BANK

As shown in Figure 15, while operating in internal reference mode, should the output be pre-charged to a level exceeding the circuit's output voltage setting, the output drives are enabled at the conclusion of the internal reference ramp, leading to an abrupt correction in the output voltage down to the set level.

When operating in external reference mode, should the output voltage be pre-charged above the regulation level driven by the external reference, the output drives are fully enabled when the SS pin levels out at the top of its range.

CONTROL OF ISL8121 OPERATION

The internal power-on reset circuit (POR) prevents the ISL8121 from starting before the bias voltage at VCC and PVCC reach the rising POR thresholds, as defined in "Electrical Specifications" on page 5. The POR levels are sufficiently high to guarantee that all parts of the ISL8121 can perform their functions properly once bias is applied to the part. While bias is below the rising POR thresholds, the controlled MOSFETs are kept in an off state.

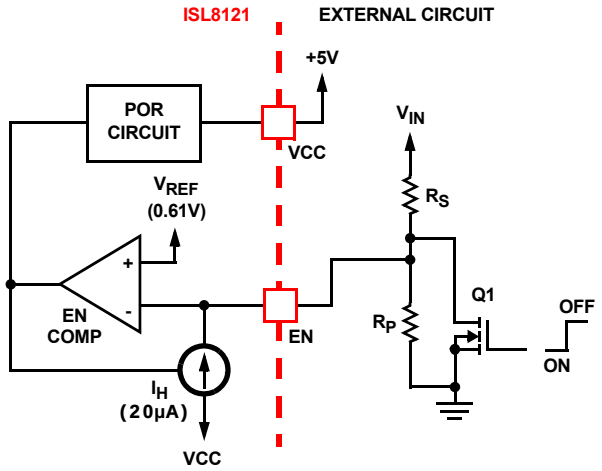


FIGURE 16. START-UP COORDINATION USING THE EN PIN

A secondary disablement feature is available via the threshold-sensitive enable input, the EN. This optional feature prevents the ISL8121 from operating until a certain chosen voltage rail is available and above some selectable threshold. One example would be the input voltage: it may be desirable the ISL8121-based converter does not start up until the input voltage is sufficiently high. The schematic in Figure 16 demonstrates coordination of the ISL8121 start-up with such a rail. The internal current source, I_H, provides the means to a user-adjustable hysteresis. The resistor value selection process follows the same equations as those presented in "External Reference Operation" on page 13.

Additionally, an open-drain or open-collector device (Q1) can be used to wire-AND a second (or multiple) control signal. To defeat the threshold-sensitive enable, connect EN to VCC directly or via a pull-up resistor.

In summary, for the ISL8121 to operate, VCC and PVCC must be greater than their respective POR thresholds and the voltage at EN must be greater than the comparator's reference (see typical threshold in "Electrical Specifications" on page 5). Once these conditions are met, the controller immediately initiates a soft-start sequence.

General Application Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multi-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques in the following sections. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for typical applications.

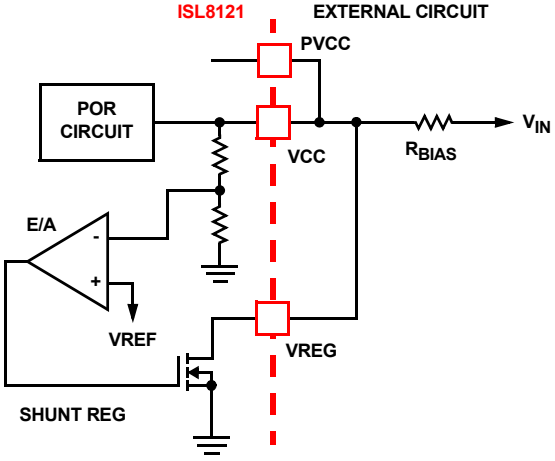


FIGURE 17. INTERNAL SHUNT REGULATOR USE WITH EXTERNAL RESISTOR (PASSIVE CONFIGURATION)

BIAS SUPPLY CONSIDERATIONS

The ISL8121 features an on-board shunt regulator capable of sinking up to 100mA (minimally). This integrated regulator can be used to produce the necessary bias voltage for the controller and the MOSFETs. The integrated regulator can be utilized directly, via a properly sized resistor, as shown in Figure 17, or via an external NPN transistor and additional resistors when either the current needed or the power being dissipated becomes too large to be handled inside the ISL8121 in the given operating environment.

A first step in determining the feasibility and selecting the proper bias regulator configuration consists in determining the maximum bias current required by the circuit. While the bias current required by the ISL8121 is listed in "Electrical Specifications" table on page 5, the bias current required by the controlled MOSFETs needs be calculated. The following equation helps determine this bias current function of the sum of the gate charge of all the controlled MOSFETs at 5V V_{GS}, Q_{GTOTAL}, and the switching frequency, F_{SW}:

$$I_B \cong Q_{GTOTAL} \cdot F_{SW} \quad \text{(EQ. 10)}$$

$$I_{BIAS} = I_{VCC} + I_B$$

Total required bias current, I_{BIAS}, sums up the ISL8121's bias current, I_{VCC}, to that required by the MOSFETs, I_B.

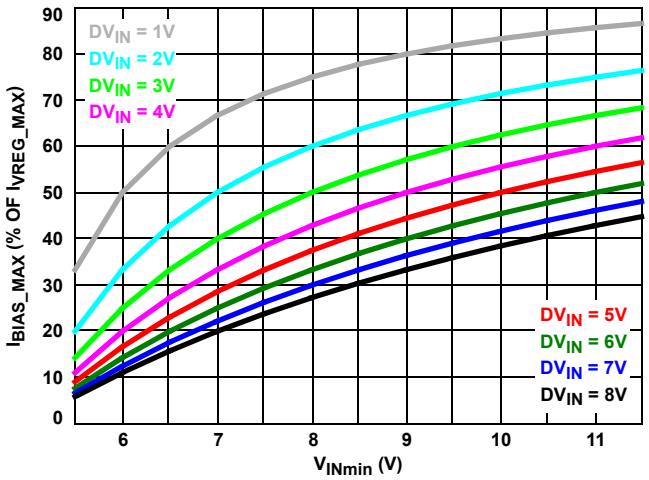


FIGURE 18. NORMALIZED MAXIMUM BIAS CURRENT OBTAINABLE IN PASSIVE CONFIGURATION vs INPUT VOLTAGE RANGE CHARACTERISTIC; V_{VCC} = 5V

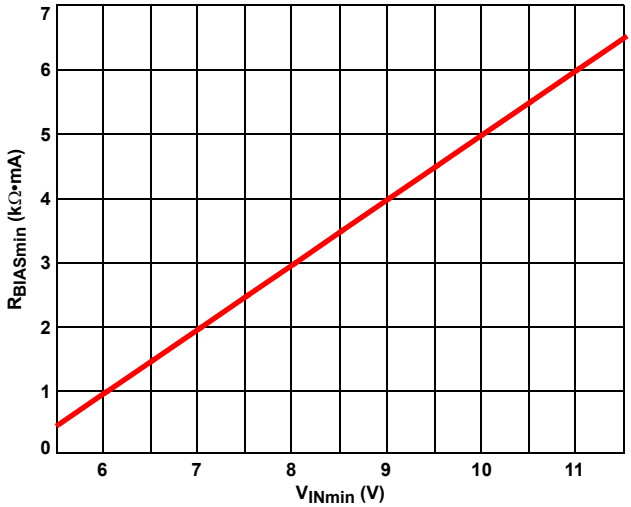


FIGURE 19. NORMALIZED RESISTOR VALUE IN PASSIVE CONFIGURATION; V_{VCC} = 5V

The maximum bias current, I_{BIAS}, that can be obtained via the internal shunt regulator and a simple external resistor is characterized in Figure 18 and can also be determined using Equation 11:

$$I_{BIASMAX} = I_{VREGMAX} \cdot \frac{V_{INMIN} - V_{VCC}}{V_{INMAX} - V_{VCC}} \quad \text{(EQ. 11)}$$

To exemplify the use, for an input voltage ranging from 10V to 14V, find the intersection of the ΔV_{IN} = 4V curve with the V_{INmin} = 10V mark and project the result on the Y axis to find the maximum bias current obtainable (approximately 56% of the maximum current obtainable via the integrated shunt regulator, I_{VREG_MAX}).

Once the maximum obtainable bias current, I_{BIAS_MAX}, is determined, and providing it is greater than the bias current, I_{BIAS}, required by the circuit, R_{SHUNT} can be determined based on the lowest input voltage, V_{INMIN}:

$$R_{BIAS} = \frac{V_{INMIN} - V_{VCC}}{I_{BIAS}} \quad \text{(EQ. 12)}$$

Figure 19 helps with a quick resistor selection based on the previous guidelines presented. Divide the value thus obtained by the maximum desired bias current, I_{BIAS}, to obtain the actual resistor value to be used.

Figure 20 details the normalized maximum power dissipation R_{BIAS} will be subject to in the given application. To use the graph provided, find the power dissipation level corresponding to the minimum input voltage and the input voltage range and multiply it by the maximum desired bias current to obtain the maximum power R_{BIAS} will dissipate.

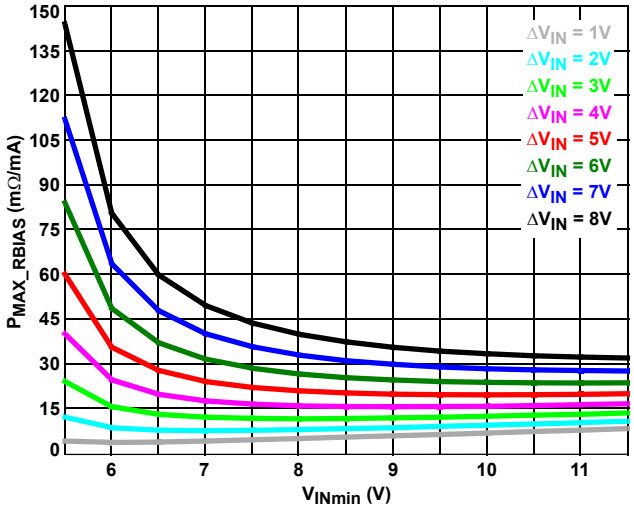


FIGURE 20. NORMALIZED RESISTOR POWER DISSIPATION (AS SELECTED IN FIGURE 17) vs MINIMUM INPUT VOLTAGE; V_{VCC} = 5V

Alternately, the maximum power dissipation inside R_{BIAS} can be calculated using Equation 13:

$$P_{MAXRBIAS} = (V_{INMAX} - V_{VCC}) \cdot I_{BIAS} \quad \text{(EQ. 13)}$$

Maximum power dissipation in the bias resistor will take place at the upper end of the input voltage range. Select a resistor with a power dissipation rating above the calculated value and pay attention to design aspects related to the power dissipation level of this component. Although Figures 18 through 20 assume a VCC voltage of 5V, the design aid curves can be translated to a different VCC voltage by translating them in the amount of the voltage differential, to the left for a lower VCC voltage, or to the right for a higher VCC voltage,

Should the simple series bias resistor configuration fall short of providing the necessary bias current, the internal shunt regulator can be used in conjunction with an external BJT transistor to increase the shunt regulator current. Figure 21 details such an implementation utilizing a PNP transistor. Selection of R1 can be based on the graphs provided for the passive regulator configuration. Maximum power dissipation inside Q1 will take place when maximum voltage is applied to the circuit and the ISL8121 is disabled; determine $I_{VREGMAX}$ by reverse-use of the graph in Figure 18 and use the obtained number to calculate Q1 power dissipation.

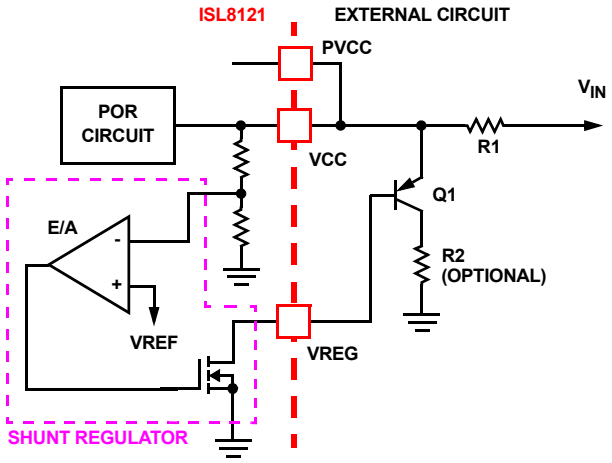


FIGURE 21. INTERNAL SHUNT REGULATOR USE WITH EXTERNAL PNP TRANSISTOR (ACTIVE CONFIGURATION)

An NPN transistor can also be used to increase the maximum available bias current, as shown in Figure 22. Used as a series pass element, Q1 will dissipate the most power when the circuit is enabled and operational, and the input voltage, V_{IN}, is at its highest level.

With the series pass element configuration shown in Figure 22, the difference between the input and the regulation level at the VCC pin has to be higher than the lowest acceptable V_{CE} of Q1 (may choose to run Q1 into saturation, but must consider the reduced gain). Thus, R2 has to be chosen such that it will provide appropriate base current at lowest V_{CE} of Q1. Next, ensure the ISL8121's $I_{VREGMAX}$ is not exceeded when the input voltage swings to its highest extreme (assume base current goes to 0 when the IC is disabled). R1 is an optional circuit element: it can be added to offset some of the power dissipation in Q1, but it also reduces the available V_{CE} for Q1. If utilizing such a series resistor, check that it does not impede on the proper operation at the lowest input voltage and choose a power rating corresponding to the highest bias current that the ISL8121 may require to drive the switching MOSFETs.

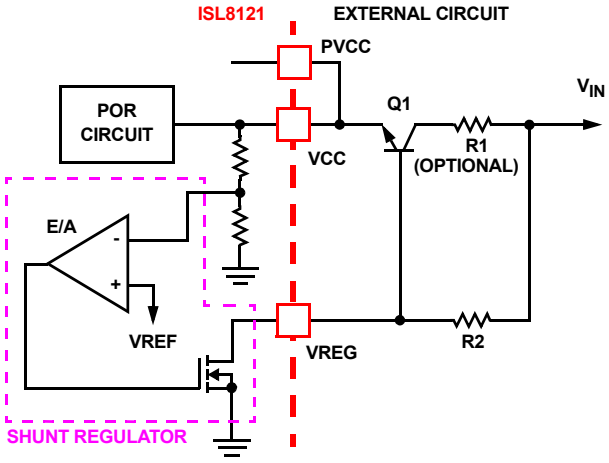


FIGURE 22. INTERNAL SHUNT REGULATOR USE WITH EXTERNAL NPN TRANSISTOR (ACTIVE CONFIGURATION)

FREQUENCY COMPENSATION

The ISL8121 multi-phase converter behaves in a similar manner to a voltage-mode controller. This section highlights the design consideration for a voltage-mode controller requiring external compensation. To address a broad range of applications, a type-3 feedback network is recommended (see Figure 23).

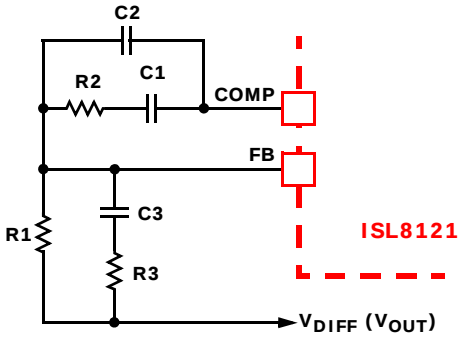


FIGURE 23. COMPENSATION CONFIGURATION FOR ISL8121 CIRCUIT

Figure 24 highlights the voltage-mode control loop for a synchronous-rectified buck converter, applicable, with a small number of adjustments, to the multi-phase ISL8121 circuit. The output voltage (V_{OUT}) is regulated to the reference voltage, VREF, level. The error amplifier output (COMP pin voltage) is compared with the oscillator (OSC) modified saw-tooth wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L and C). The output filter capacitor bank's equivalent series resistance is represented by the series resistor E.

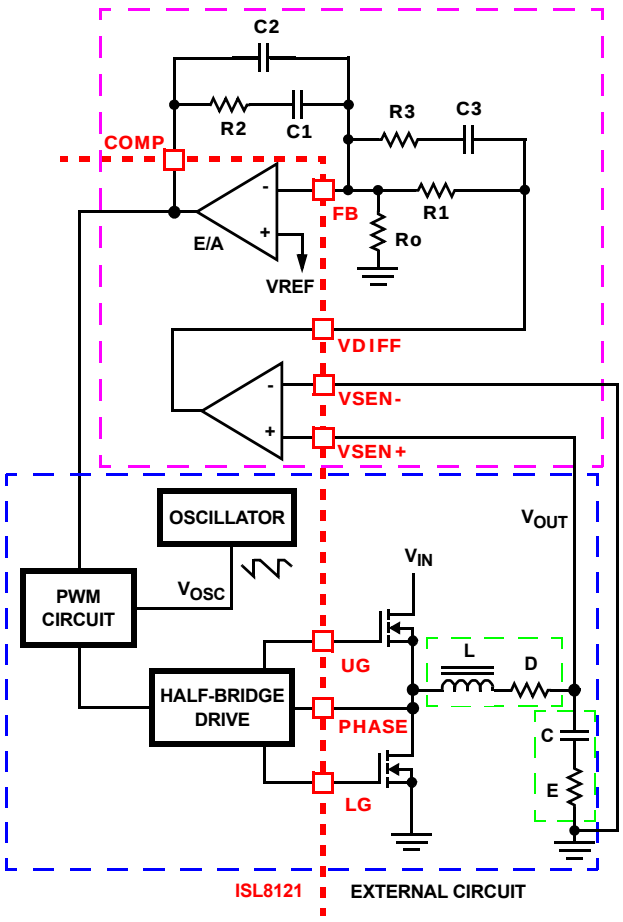


FIGURE 24. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain, given by $d_{MAX}V_{IN}/V_{OSC}$, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis, L and D represent the individual channel inductance and its DCR divided by 2 (equivalent parallel value of the two output inductors), while C and E represents the total output capacitance and its equivalent series resistance.

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \qquad F_{CE} = \frac{1}{2\pi \cdot C \cdot E} \qquad \text{(EQ. 14)}$$

The compensation network consists of the error amplifier (internal to the ISL8121) and the external R1-R3, C1-C3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of F_{SW}) and adequate phase margin (better than 45 degrees). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°. The equations that follow relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 23. Use the following guidelines for locating the poles and zeros of the compensation network:

1. Select a value for R1 (1kΩ to 5kΩ, typically). Calculate value for R2 for desired converter bandwidth (F_0). If setting the output voltage via an offset resistor connected to the FB pin, Ro in Figure 24, the design procedure can be followed as presented. However, when setting the output voltage via a resistor divider placed at the input of the differential amplifier, in order to compensate for the attenuation introduced by the resistor divider, the obtained R2 value needs be multiplied by a factor of $(R_P+R_S)/R_P$. The remainder of the calculations remain unchanged, as long as the compensated R2 value is used.

$$R2 = \frac{V_{OSC} \cdot R1 \cdot F_0}{d_{MAX} \cdot V_{IN} \cdot F_{LC}} \qquad \text{(EQ. 15)}$$

2. Calculate C1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor to desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost at F_{LC}).

$$C1 = \frac{1}{2\pi \cdot R2 \cdot 0.5 \cdot F_{LC}} \qquad \text{(EQ. 16)}$$

3. Calculate C2 such that F_{P1} is placed at F_{CE}.

$$C2 = \frac{C1}{2\pi \cdot R2 \cdot C1 \cdot F_{CE} - 1} \qquad \text{(EQ. 17)}$$

4. Calculate R3 such that F_{Z2} is placed at F_{LC}. Calculate C3 such that F_{P2} is placed below F_{SW} (typically, 0.5 to 1.0 times F_{SW}). F_{SW} represents the per-channel switching frequency. Change the numerical factor to reflect desired placement of this pole. Placement of F_{P2} lower in frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R3 = \frac{R1}{\frac{F_{SW}}{F_{LC}} - 1} \qquad C3 = \frac{1}{2\pi \cdot R3 \cdot 0.7 \cdot F_{SW}} \qquad \text{(EQ. 18)}$$

It is recommended a mathematical model is used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. Equation 19 describes the frequency response of the modulator (G_{MOD}), feedback compensation (G_{FB}) and closed-loop response (G_{CL}):

$$G_{MOD}(f) = \frac{d_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot E \cdot C}{1 + s(f) \cdot (E + D) \cdot C + s^2(f) \cdot L \cdot C}$$

$$G_{FB}(f) = \frac{1 + s(f) \cdot R2 \cdot C1}{s(f) \cdot R1 \cdot (C1 + C2)} \cdot \qquad \text{(EQ. 19)}$$

$$\cdot \frac{1 + s(f) \cdot (R1 + R3) \cdot C3}{(1 + s(f) \cdot R3 \cdot C3) \cdot \left(1 + s(f) \cdot R2 \cdot \left(\frac{C1 \cdot C2}{C1 + C2}\right)\right)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot G_{FB}(f) \qquad \text{where, } s(f) = 2\pi \cdot f \cdot j$$

COMPENSATION BREAK FREQUENCY EQUATIONS

$$F_{Z1} = \frac{1}{2\pi \cdot R2 \cdot C1} \qquad F_{P1} = \frac{1}{2\pi \cdot R2 \cdot \frac{C1 \cdot C2}{C1 + C2}} \quad \text{(EQ. 20)}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R1 + R3) \cdot C3} \qquad F_{P2} = \frac{1}{2\pi \cdot R3 \cdot C3}$$

Figure 25 shows an asymptotic plot of the DC/DC converter's gain vs frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the previously mentioned guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The closed loop gain, G_{CL}, is constructed on the log-log graph of Figure 25 by adding the modulator gain, G_{MOD} (in dB), to the feedback compensation gain, G_{FB} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

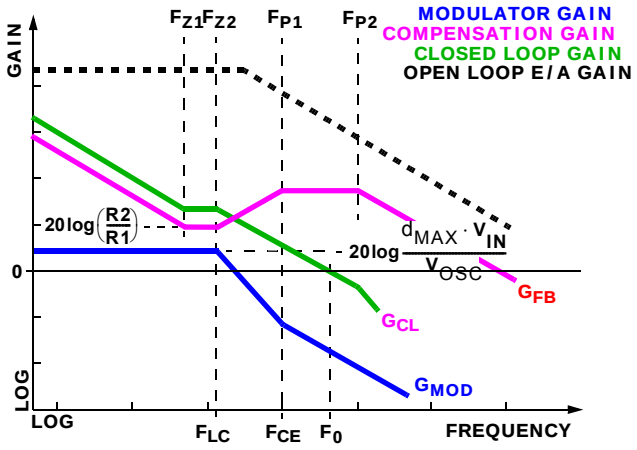


FIGURE 25. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select target crossover frequencies in the range of 10% to 30% of the per-channel switching frequency, F_{SW}.

OUTPUT FILTER DESIGN

The output inductors and the output capacitor bank together form a low-pass filter responsible for smoothing the square wave voltage at the phase nodes. Additionally, the output capacitors must also provide the energy required by a fast transient load during the short interval of time required by the controller and power train to respond. Because it has a low bandwidth compared to the switching frequency, the output filter limits the system transient response leaving the output capacitor bank to supply the load current or sink the inductor currents, all while the current in the output inductors increases or decreases to meet the load demand.

In high-speed converters, the output capacitor bank is amongst the costlier (and often the physically largest) parts of the circuit. Output filter design begins with consideration of the critical load parameters: maximum size of the load step, ΔI, the load-current slew rate, di/dt, and the maximum allowable output voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates according to Equation 21:

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \quad \text{(EQ. 21)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors is also responsible for the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current, a voltage develops across the bulk-capacitor ESR equal to I_{PP}. Thus, once the output capacitors are selected and a maximum allowable ripple voltage, $V_{PP(MAX)}$, is determined from an analysis of the available output voltage budget, Equation 22 can be used to determine a lower limit on the output inductance.

$$L \geq ESR \cdot \frac{(V_{IN} - 2 \cdot V_{OUT}) \cdot V_{OUT}}{f_S \cdot V_{IN} \cdot V_{PP(MAX)}} \quad \text{(EQ. 22)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

$$L \leq \frac{4 \cdot C \cdot V_{OUT}}{(\Delta I)^2} \cdot (\Delta V_{MAX} - \Delta I \cdot ESR) \quad \text{(EQ. 23)}$$

While the previous equation addresses the leading edge, the following equation gives the upper limit on L for cases where the trailing edge of the current transient causes a greater output voltage deviation than the leading edge.

$$L \leq \frac{2.5 \cdot C}{(\Delta I)^2} \cdot (\Delta V_{MAX} - \Delta I \cdot ESR) \cdot (V_{IN} - V_O) \quad \text{(EQ. 24)}$$

Normally, the trailing edge dictates the selection of L, if the duty cycle is less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In all equations in this paragraph, L is the per-channel inductance and C is the total output bulk capacitance.

LAYOUT CONSIDERATIONS

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turnoff transition of the upper PWM MOSFET. Prior to turnoff, the upper MOSFET was carrying channel current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC/DC converter using a ISL8121 controller. The power components are the most critical because they switch large amounts of energy. Next are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

Although the ISL8121 allows for external adjustment of the channel-to-channel current balancing (via the R_{ISEN} resistors), it is desirable to have a symmetrical layout, preferably with the controller equidistantly located from the two power trains it controls. Equally important are the gate drive lines (UG, LG, PHASE): since they drive the power train MOSFETs using short, high current pulses, it is important to size them accordingly and reduce their overall impedance. Equidistant placement of the controller to the two power trains also helps keeping these traces equally long (equal impedances, resulting in similar driving of both sets of MOSFETs).

The power components should be placed first. Locate the input capacitors close to the power switches. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches. Locate the output inductors and output capacitors between the MOSFETs and the load. Locate all the high-frequency decoupling capacitors (ceramic) as close as practicable to their decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND immediately next, or even onto the capacitor's grounded solder pad.

The critical small components include the bypass capacitors for VCC and PVCC. Locate the bypass capacitors, C_{BP}, close to the device. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up. It is important to place the R_{ISEN} resistors close to the respective terminals of the ISL8121.

A multi-layer printed circuit board is recommended. Figure 26 shows the connections of the critical components for one output channel of the converter. Note that capacitors C_{xxIN} and C_{xxOUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually the one underneath the component side of the board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to inductor L_{OUT} short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring.

Size the trace interconnects commensurate with the signals they are carrying. Use narrow (0.005" to 0.008") and short traces for the high-impedance, small-signal connections, such as the feedback, compensation, soft-start, frequency set, enable, reference track, etc. The wiring traces from the IC to the MOSFETs' gates and sources should be wide (0.02" to 0.05") and short, encircling the smallest area possible.

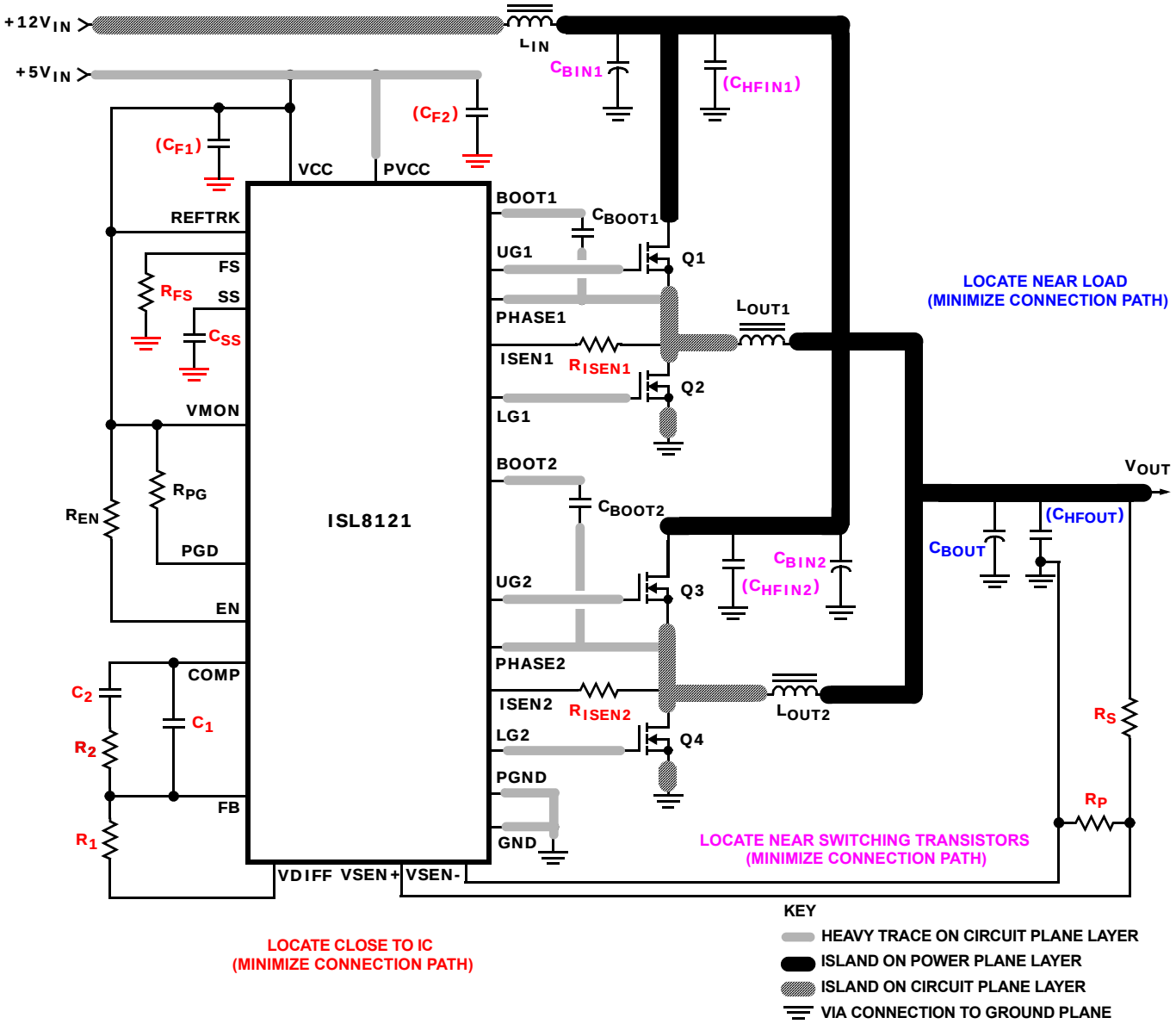


FIGURE 26. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Component Selection Guidelines

MOSFETS

The selection of MOSFETs revolves closely around the current each MOSFET is required to conduct, the switching characteristics, the capability of the devices to dissipate heat, as well as the characteristics of available heat sinking. Since the ISL8121 drives the MOSFETs with a 5V signal, the selection of appropriate MOSFETs should be done by comparing and evaluating their characteristics at this specific V_{GS} bias voltage. The following paragraphs addressing MOSFET power dissipation ignore the driving losses associated with the gate resistance.

The aggressive design of the shoot-through protection circuits, part of the ISL8121 output drivers, is geared toward reducing the deadtime between the conduction of the upper and the lower MOSFET/s. The short deadtimes, coupled with strong pull-up and pull-down output devices driving the UG and LG pins make the ISL8121 best suited to driving low gate resistance (R_G), late-generation MOSFETs. If employing MOSFETs with a nominal gate resistance in excess of 1Ω to 2Ω, check for the circuit's proper operation. A few examples (non exclusive list) of suitable MOSFETs to be used in ISL8121 applications include the D8 (and later) generation from Renesas and the OptiMOS®2 line from Infineon. Along the same line, the use of gate resistors is discouraged, as they may interfere with the circuits just mentioned.

LOWER MOSFET POWER CALCULATION

Since virtually all of the heat loss in the lower MOSFET is conduction loss (due to current conducted through the channel resistance, $r_{DS(ON)}$), a quick approximation for heat dissipated in the lower MOSFET can be found in Equation 25:

$$P_{LMOS1} = r_{DS(ON)}\left[\left(\frac{I_{OUT}}{2}\right)^2(1-D)+\frac{I_{L,PP}^2(1-D)}{12}\right] \quad \text{(EQ. 25)}$$

where: I_M is the maximum continuous output current, $I_{L,PP}$ is the peak-to-peak inductor current, and D is the duty cycle (approximately V_{OUT}/V_{IN}).

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$; the switching frequency, f_S; and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval, respectively.

$$P_{LMOS2} = V_{D(ON)}f_S\left[\left(\frac{I_{OUT}}{2}+\frac{I_{PP}}{2}\right)t_{d1}+\left(\frac{I_{OUT}}{2}-\frac{I_{PP}}{2}\right)t_{d2}\right] \quad \text{(EQ. 26)}$$

Equation 26 assumes the current through the lower MOSFET is always positive; if so, the total power dissipated in each lower MOSFET is approximated by the summation of P_{LMOS1} and P_{LMOS2}.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper-MOSFET losses are switching losses, due to currents conducted through the device while the input voltage is present as V_{DS}. Upper MOSFET losses can be divided into separate components, separating the upper-MOSFET switching losses, the lower-MOSFET body diode reverse recovery charge loss, and the upper MOSFET $r_{DS(ON)}$ conduction loss.

In most typical circuits, when the upper MOSFET turns off, it continues to conduct a decreasing fraction of the output inductor current as the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting (via its body diode or enhancement channel), the current in the upper MOSFET decreases to zero. In Equation 27, the required time for this commutation is $t_1$and the associated power loss is $P_{UMOS,1}$.

$$P_{UMOS,1} \approx V_{IN}\left(\frac{I_{OUT}}{N}+\frac{I_{L,PP}}{2}\right)\left(\frac{t_1}{2}\right)f_S \quad \text{(EQ. 27)}$$

Similarly, the upper MOSFET begins conducting as soon as it begins turning on. Assuming the inductor current is in the positive domain, the upper MOSFET sees approximately the input voltage applied across its drain and source terminals, while it turns on and starts conducting the inductor current. This transition occurs over a time t_2, and the approximate the power loss is $P_{UMOS,2}$.

$$P_{UMOS,2} \approx V_{IN}\left(\frac{I_{OUT}}{N}-\frac{I_{L,PP}}{2}\right)\left(\frac{t_2}{2}\right)f_S \quad \text{(EQ. 28)}$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{RR}. Since the lower MOSFET's body diode conducts the full inductor current before it has fully switched to the upper MOSFET, the upper MOSFET has to provide the charge required to turn off the lower MOSFET's body diode. This charge is conducted through the upper MOSFET across VIN, the power dissipated as a result, $P_{UMOS,3}$ can be approximated as:

$$P_{UMOS,3} = V_{IN}Q_{rr}f_S \quad \text{(EQ. 29)}$$

Lastly, the conduction loss part of the upper MOSFET's power dissipation, $P_{UMOS,4}$, can be calculated using Equation 30:

$$P_{UMOS,4} = r_{DS(ON)}\left[\left(\frac{I_{OUT}}{N}\right)^2 d+\frac{I_{PP}^2}{12}\right] \quad \text{(EQ. 30)}$$

In this case, of course, $r_{DS(ON)}$ is the ON-resistance of the upper MOSFET.

The total power dissipated by the upper MOSFET at full load can be approximated as the summation of these results. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process that involves repetitively solving the loss equations for different MOSFETs and different switching frequencies until converging upon the best solution.

OUTPUT CAPACITOR SELECTION

The output capacitor is selected to meet both the dynamic load requirements and the voltage ripple requirements. The load transient a microprocessor impresses is characterized by high slew rate (di/dt) current demands. In general, multiple high quality capacitors of different size and dielectric are paralleled to meet the design constraints.

Should the load be characterized by high slew rates, attention should be particularly paid to the selection and placement of high-frequency decoupling capacitors (MLCCs, typically multi-layer ceramic capacitors). High frequency capacitors supply the initially transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load, or for that reason, to any decoupling target they are meant for, as physically possible. Attention should be paid as not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient's edge. In most cases, multiple capacitors of small case size perform better than a single large case capacitor.

Bulk capacitor choices include aluminum electrolytic, OS-Con, Tantalum and even ceramic dielectrics. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Consult the capacitor manufacturer and/or measure the capacitor's impedance with frequency to help select a suitable component.

OUTPUT INDUCTOR SELECTION

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. In a multi-phase converter, small inductors reduce the response time with less impact to the total output ripple current (as compared to single-phase converters).

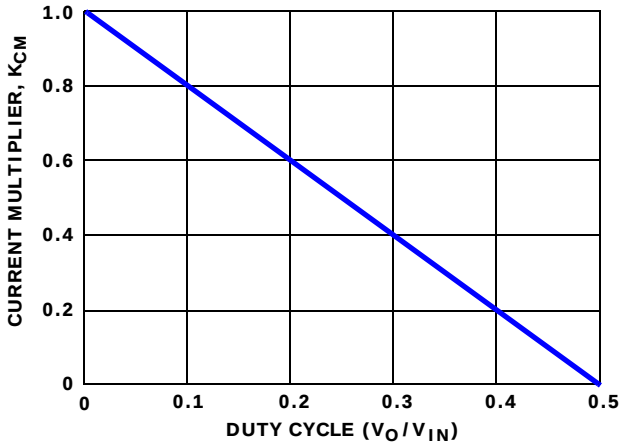


FIGURE 27. RIPPLE CURRENT vs DUTY CYCLE

The output inductor of each power channel controls the ripple current. The control IC is stable for channel ripple current (peak-to-peak) up to twice the average current. A single channel's ripple current is approximated by Equation 31:

$$I_{L,PP} = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot L} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 31)}$$

The current from multiple channels tend to cancel each other and reduce the total ripple current. The total output ripple current can be determined using the curve in Figure 27; it provides the total ripple current as a function of duty cycle and number of active channels, normalized to the parameter K_{NORM} at zero duty cycle.

$$K_{NORM} = \frac{V_{OUT}}{L \cdot F_{SW}} \quad \text{(EQ. 32)}$$

where L is the channel inductor value.

Find the intersection of the active channel curve and duty cycle for your particular application. The resulting ripple current multiplier from the y-axis is then multiplied by the normalization factor, K_{NORM}, to determine the total output ripple current for the given application.

$$\Delta I_{TOTAL} = K_{NORM} \cdot K_{CM} \quad \text{(EQ. 33)}$$

INPUT CAPACITOR SELECTION

The important parameters for the bulk input capacitors are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage. The input RMS current required for a multi-phase converter can be approximated with the aid of Figure 28. For a more exact calculation of the input RMS current use Equation 34:

$$I_{IN(RMS)} = \sqrt{I_O^2 \cdot (D - D^2) + I^2_{L,PP} \cdot \frac{D}{12}} \quad \text{(EQ. 34)}$$

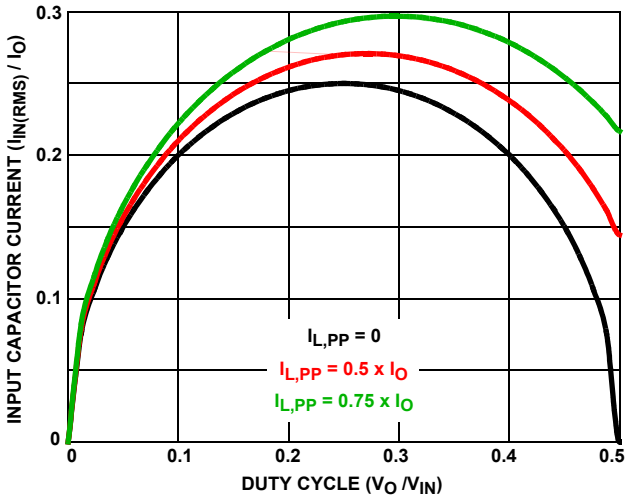


FIGURE 28. NORMALIZED INPUT RMS CURRENT vs DUTY CYCLE FOR A 2-PHASE CONVERTER

As the input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs, their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs. Figure 28 can be used to determine the input-capacitor RMS current function of duty cycle, maximum sustained output current (I_O), and the ratio of the peak-to-peak inductor current ($I_{L,PP}$) to the maximum sustained load current, I_O.

Use a mix of input bypass capacitors to control the input voltage ripple. Use ceramic capacitance for the

high frequency decoupling and bulk capacitors to supply the RMS current. Minimize the connection path inductance of the high frequency decoupling ceramic capacitors (from drain of upper MOSFET to source of lower MOSFET).

For bulk capacitance, several electrolytic or high-capacity MLC capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up.

APPLICATION SYSTEM DC TOLERANCE

Although the ISL8121 features a tight voltage reference, the overall system DC tolerance can be affected by the tolerance of the other components employed. The resistive divider used to set the output voltage will directly influence the system DC voltage tolerance. Figure 29 details the absolute worst case tolerance stack-up for 1% and 0.1% feedback resistors, and assuming the ISL8121 is regulating at 0.8% above its nominal reference. Other component tolerance stack-ups may be investigated using the following equation, where REF_{TM}, R_{PTM}, and R_{STM} are the tolerance multipliers corresponding to V_{REF}, R_S, and R_P, respectively.

$$TOL = \frac{REF_{TM} \cdot \frac{(k-1) \cdot R_{STM} + R_{PTM}}{k \cdot R_{PTM}} - 1}{100} \quad [\%] \qquad \text{(EQ. 35)}$$

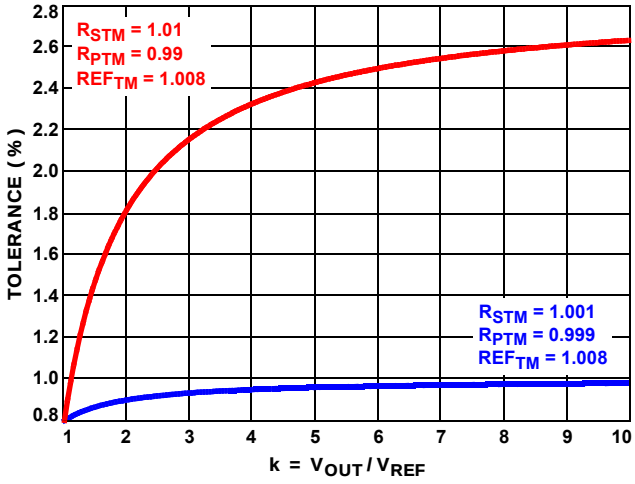
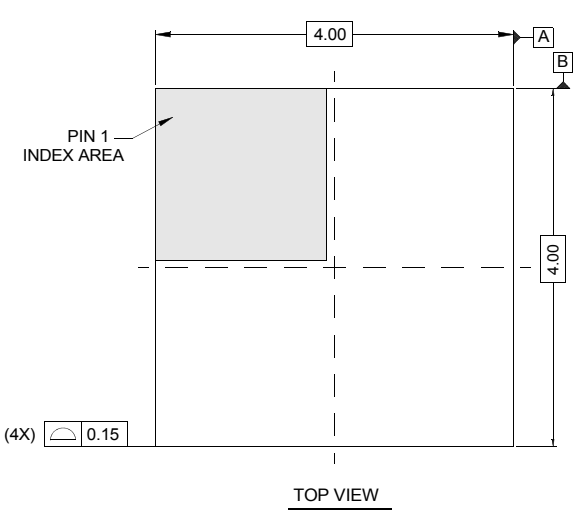


FIGURE 29. WORST CASE SYSTEM DC REGULATION TOLERANCE (V_{REF} AT 0.8% ABOVE NOMINAL)

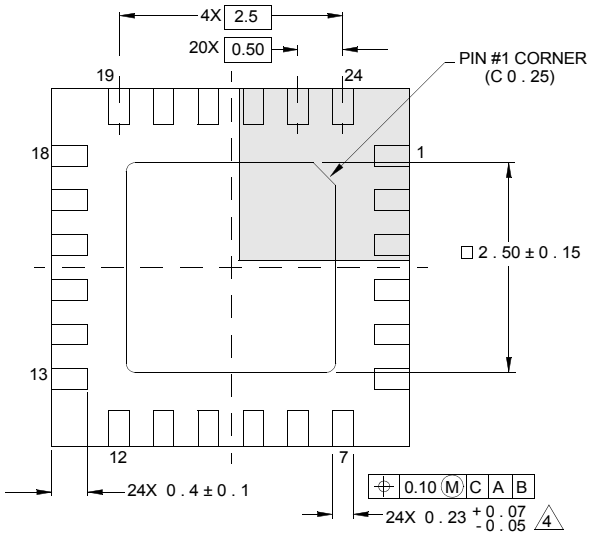
Package Outline Drawing

L24.4x4C

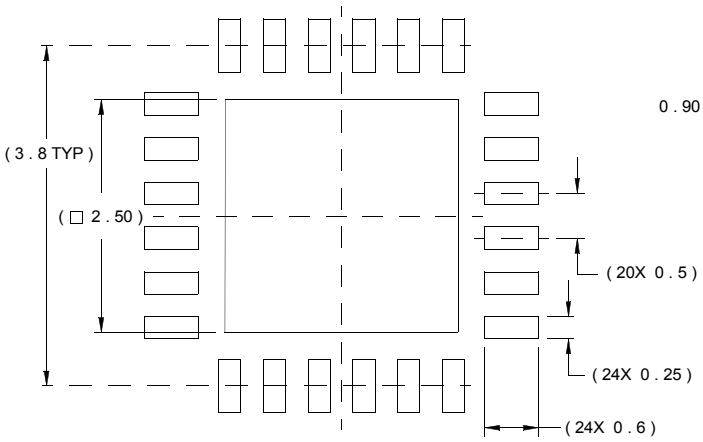
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/06



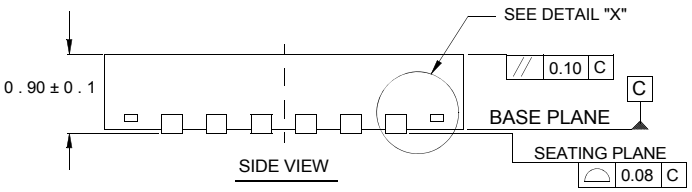
TOP VIEW



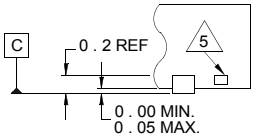
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.