ISL70001SEH, ISL70001SRH

Radiation Hardened and SEE Hardened 6A Synchronous Buck Regulator

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The ISL70001SEH, ISL70001SRH are radiation hardened and SEE hardened high efficiency monolithic synchronous buck regulators with integrated MOSFETs. This single chip power solution operates over an input voltage range of 3V to 5.5V and provides a tightly regulated output voltage that is externally adjustable from 0.8V to ~85% of the input voltage. Output load current capacity is 6A for T_J < +145°C.

High integration and class leading radiation tolerance makes the ISL70001SEH, ISL70001SRH ideal choices to power many of today's small form factor applications. Two devices can be synchronized to provide a complete power solution for large scale digital ICs, like field programmable gate arrays (FPGAs) that require separate core and I/O voltages.

In applications where the ENABLE input is tied high to PVIN we recommend that the input voltage ramp rate be equal to or greater than 10V/ms. This is to prevent unwanted voltage from prematurely appearing on the output.

For a PVIN voltage that has a slower ramp rate or is stepped up we recommend use of the ISL70001ASEH. Ensuring that the ENABLE input is held low until the chosen VINPOR is satisfied will prevent this 'false start'.

Applications

- FPGA, CPLD, DSP, CPU core or I/O voltages
- Low-voltage, high-density distributed power systems

Features

- ±1% reference voltage over line, load, temperature and radiation
- Current mode control for excellent dynamic response
- Full Mil-temp range operation (T_A = -55°C to +125°C)
- High efficiency >90%
- Fixed 1MHz operating frequency
- Available in a thermally enhanced heatsink package - R48.B
- Operates from 3V to 5.5V supply
- Adjustable output voltage
  - Two external resistors set V_{OUT} from 0.8V to ~85% of V_{IN}
- Bidirectional SYNC pin allows two devices to be synchronized 180° out-of-phase
- Starts into prebiased load
- Power-good output voltage monitor
- Adjustable analog soft-start
- Input undervoltage, output undervoltage and output overcurrent protection
- Electrically screened to DLA SMD 5962-09225
- QML qualified per MIL-PRF-38535 requirements
- Radiation acceptance testing - ISL70001SEH
  - HDR (50-300rad(Si)/s): 100krad(Si) (min)
  - LDR (<10mrad(Si)/s): 50krad(Si) (min)
- Radiation acceptance testing - ISL70001SRH
  - HDR (50-300rad(Si)/s): 100krad(Si) (min)
- SEE hardness (see SEE report for details)
  - SEL and SEB LET_{eff} . . . . . 86.4MeV/mg/cm^2 (min)
  - SEFI X-section (LET_{eff} = 86.4MeV/mg/cm^2) 1.4 x 10^{-6} cm^2 (max)
  - SET LET_{eff} (<1 pulse perturbation) 86.4MeV/mg/cm^2 (min)

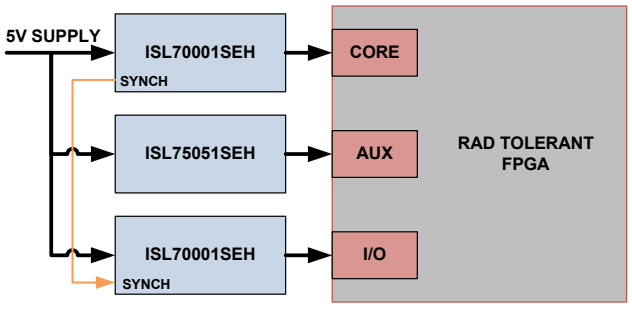

FIGURE 1. TYPICAL APPLICATION

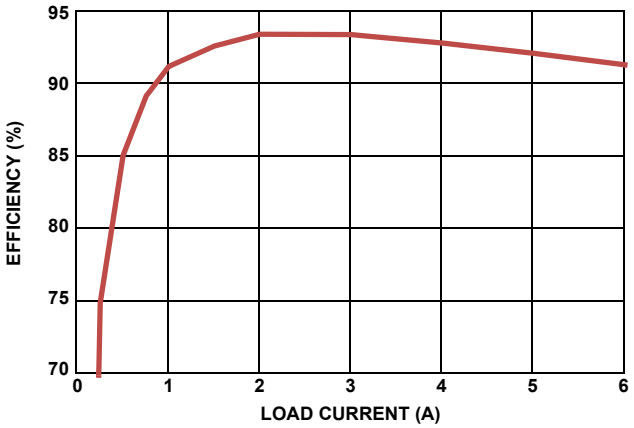

FIGURE 2. EFFICIENCY 5V INPUT TO 3.3V OUTPUT, T_A = +25°C

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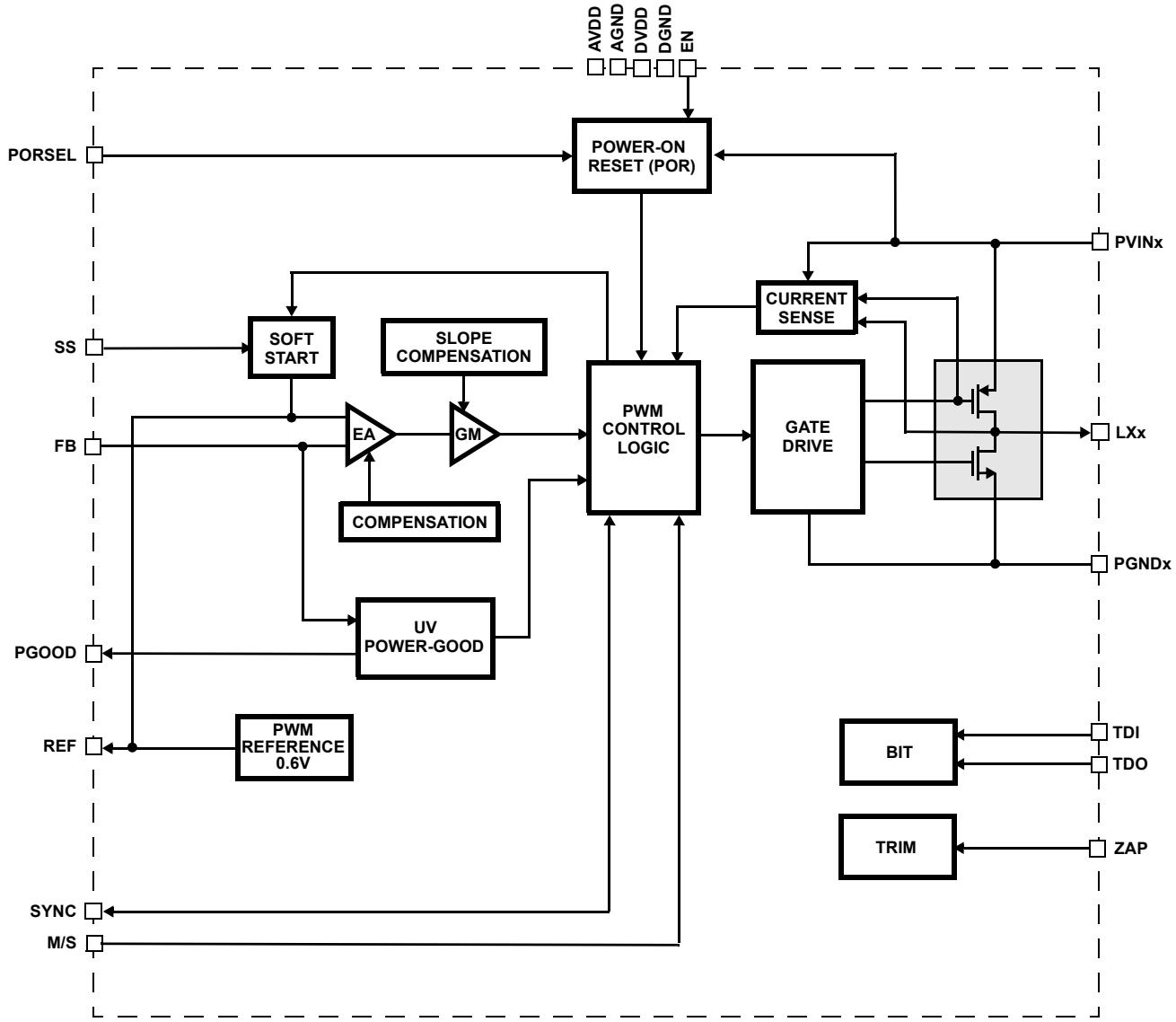


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

Typical Application Schematics

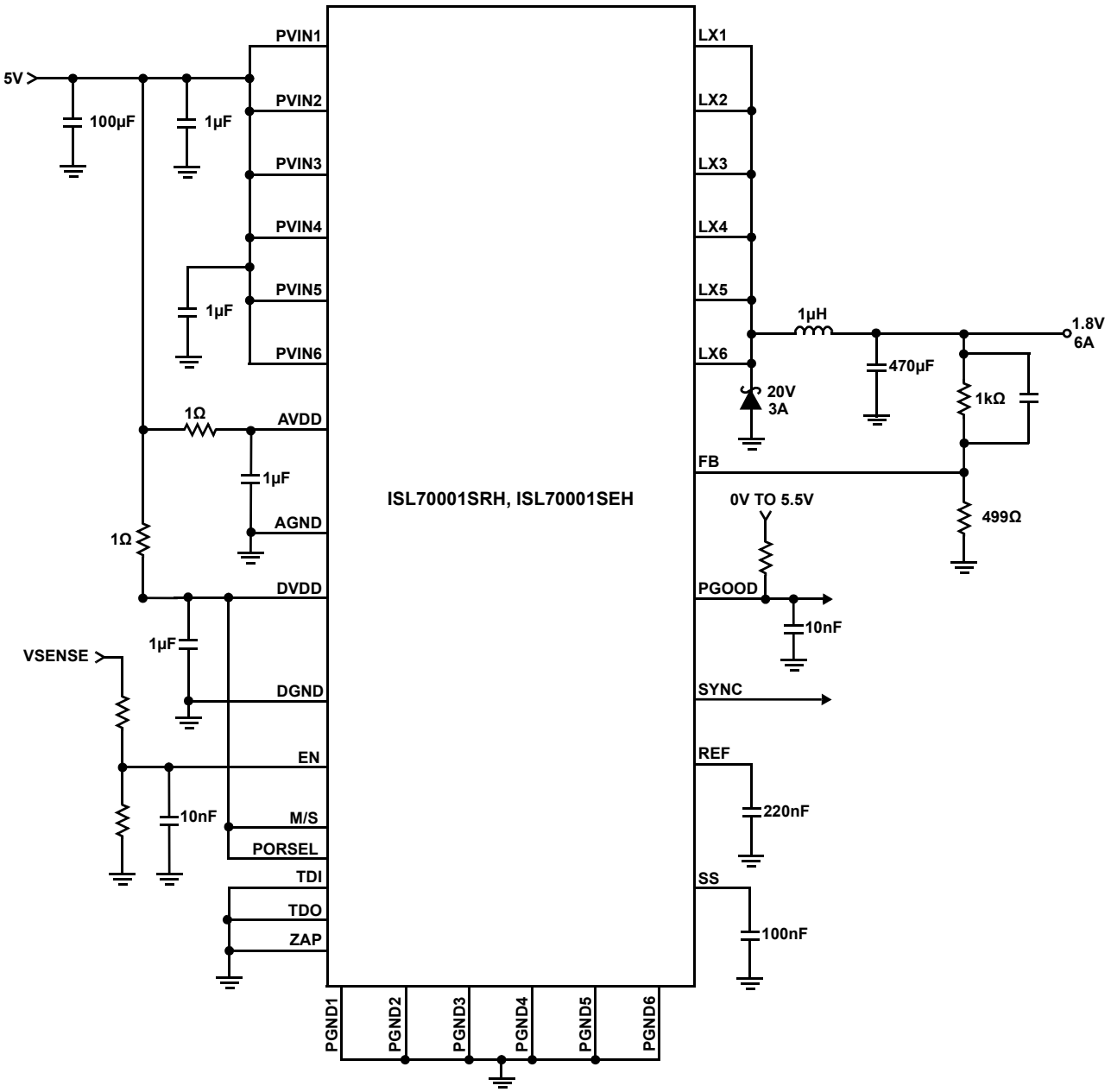


FIGURE 4. 5V INPUT SUPPLY VOLTAGE WITH MASTER MODE SYNCHRONIZATION

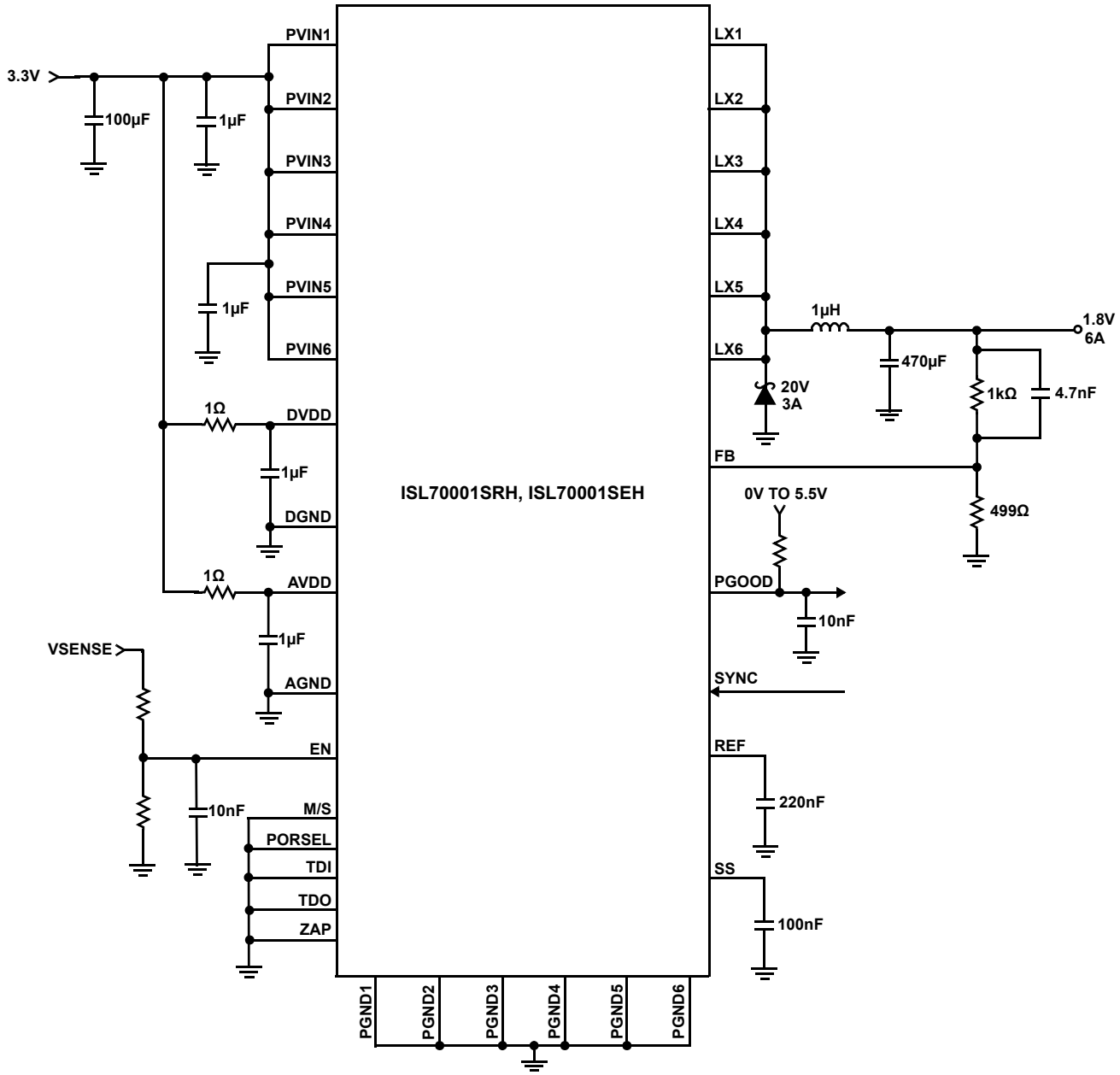


FIGURE 5. 3.3V INPUT SUPPLY VOLTAGE WITH SLAVE MODE SYNCHRONIZATION

Ordering Information

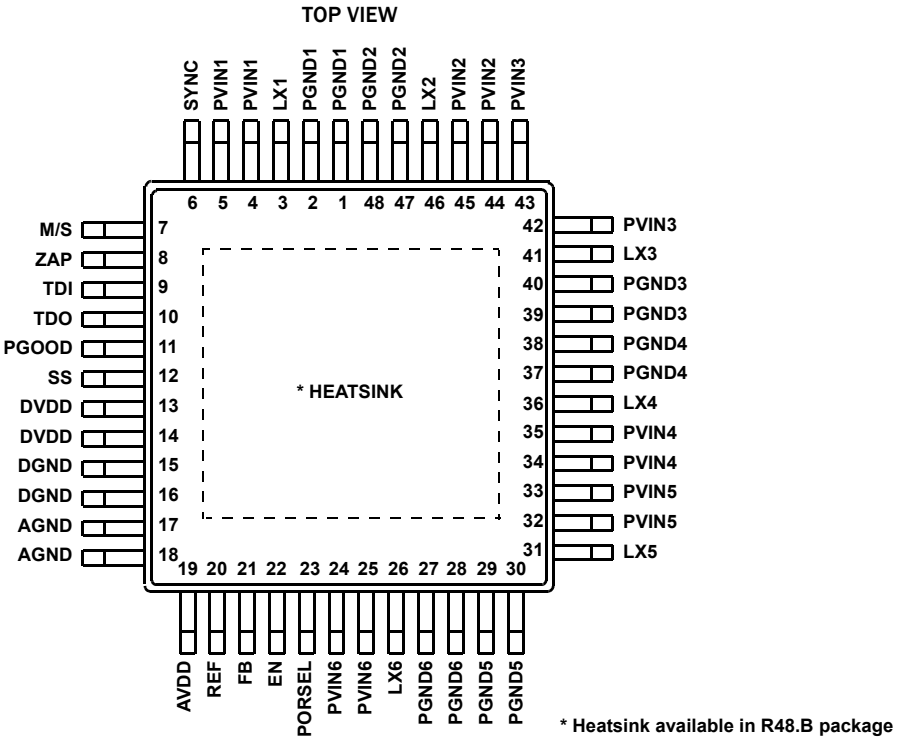
SMD ORDERING NUMBER (Note 2)	PART NUMBER (Note 1)	TEMP. RANGE	RADIATION HARDNESS (Total Ionizing Dose)	PACKAGE DESCRIPTION (RoHS Compliant)	PKG. DWG. #
5962R0922502VXC	ISL70001SEHVF	-55 to +125°C	HDR to 100krad(Si), LDR to 50krad(Si)	48 Ld CQFP	R48.A
5962R0922502VYC	ISL70001SEHVFE			48 Ld CQFP With Heatsink	R48.B
5962R0922502V9A	ISL70001SEHVX (Note 3)			Die	-
5962R0922501VXC	ISL70001SRHVF		LDR to 50krad(Si)	48 Ld CQFP	R48.A
5962R0922501QXC	ISL70001SRHQF				
5962R0922501V9A	ISL70001SRHVX (Note 3)			Die	-
N/A	ISL70001SRHF/PROTO (Note 4)		N/A	48 Ld CQFP	R48.A
N/A	ISL70001SEHFE/PROTO (Note 4)			48 Ld CQFP With Heatsink	R48.B
N/A	ISL70001SRHX/SAMPLE (Notes 3, 4)			Die	-
N/A	ISL70001SRHEVAL1Z (Note 5)	Evaluation Board			

NOTES:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the Ordering Information table on must be used when ordering.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in Electrical Specifications.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
5. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Pin Information

Pin Assignments



* Heatsink available in R48.B package

Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
1, 2, 27, 28, 29, 30, 37, 38, 39, 40, 47, 48	PGNDx	These pins are the power grounds associated with the corresponding internal power blocks. Connect these pins directly to the ground plane. These pins should also connect to the negative terminals of the input and output capacitors. Locate the input and output capacitors as close as possible to the IC.
3, 26, 31, 36, 41, 46	LXx	These pins are the outputs of the corresponding internal power blocks and should be connected to the output filter inductor. Internally, these pins are connected to the synchronous MOSFET power switches. To minimize voltage undershoot, it is recommended that a Schottky diode be connected from these pins to PGNDx. The Schottky diode should be located as close as possible to the IC.
4, 5, 24, 25, 32, 33, 34, 35, 42, 43, 44, 45	PVINx	These pins are the power supply inputs to the corresponding internal power blocks. These pins must be connected to a common power supply rail, which must fall in the range of 3V to 5.5V. Bypass these pins directly to PGNDx with ceramic capacitors located as close as possible to the IC.
6	SYNC	This pin is the synchronization I/O for the IC. When configured as an output (Master mode), this pin drives the SYNC input of another ISL70001SEH, ISL70001SRH. When configured as an input (Slave mode), this pin accepts the SYNC output from another ISL70001SEH, ISL70001SRH or an external clock. Synchronization of the slave unit is 180° out-of-phase with respect to the master unit. If synchronizing to an external clock, the clock must be SEE hardened and the frequency must be within the range of 1MHz ±20%.
7	M/S	This pin is the Master/Slave input for selecting the direction of the bidirectional SYNC pin. For SYNC = Output (Master mode), connect this pin to DVDD. For SYNC = Input (Slave mode), connect this pin to DGND.
8	ZAP	This pin is a trim input and is used to adjust various internal circuitry. Connect this pin to DGND.
9	TDI	This pin is the test data input of the internal BIT circuitry. Connect this pin to DGND.
10	TDO	This pin is the test data output of the internal BIT circuitry. Connect this pin to DGND.
11	PGOOD	This pin is the power-good output. This pin is an open-drain logic output that is pulled to DGND when the output voltage is outside a ±11% typical regulation window. This pin can be pulled up to any voltage from 0V to 5.5V, independent of the supply voltage. A nominal 1kΩ to 10kΩ pull-up resistor is recommended. Bypass this pin to DGND with a 10nF ceramic capacitor to mitigate SEE.
12	SS	This pin is the soft-start input. Connect a ceramic capacitor from this pin to DGND to set the soft-start output ramp time in accordance with Equation 1: $t_{SS} = C_{SS} \cdot V_{REF} / I_{SS}$ (EQ. 1) Where: t_{SS} = Soft-start output ramp time C_{SS} = Soft-start capacitor V_{REF} = Reference voltage (0.6V typical) I_{SS} = Soft-start charging current (23µA typical) Soft-start time is adjustable from approximately 2ms to 200ms. The range of the soft-start capacitor should be 82nF to 8.2µF, inclusive.
13, 14	DVDD	These pins are the bias supply inputs to the internal digital control circuitry. Connect these pins together at the IC and locally filter them to DGND using a 1Ω resistor and a 1µF ceramic capacitor. Locate both filter components as close as possible to the IC.
15, 16	DGND	These pins are the digital ground associated with the internal digital control circuitry. Connect these pins directly to the ground plane.
17, 18	AGND	These pins are the analog ground associated with the internal analog control circuitry. Connect these pins directly to the ground plane. Reference "Metallization Mask Layout" on page 19, pad 13 is labeled PGND and is pin 17 on the packaged device. These 2 pads are to be connected together when using the die product.
19	AVDD	This pin is the bias supply input to the internal analog control circuitry. Locally filter this pin to AGND using a 1Ω resistor and a 1µF ceramic capacitor. Locate both filter components as close as possible to the IC.
20	REF	This pin is the internal reference voltage output. Bypass this pin to AGND with a 220nF ceramic capacitor located as close as possible to the IC. The bypass capacitor is needed to mitigate SEE. No current (sourcing or sinking) is available from this pin.

PIN NUMBER	PIN NAME	DESCRIPTION
21	FB	This pin is the voltage feedback input to the internal error amplifier. Connect a resistor from FB to VOUT and from FB to AGND to adjust the output voltage in accordance with Equation 2: $V_{OUT} = V_{REF} \cdot [1 + (R_T / R_B)]$ (EQ. 2) Where: V_{OUT} = Output voltage V_{REF} = Reference voltage (0.6V typical) R_T = Top divider resistor (Must be 1kΩ) R_B = Bottom divider resistor The top divider resistor must be 1kΩ to mitigate SEE. Connect a 4.7nF ceramic capacitor across RT to mitigate SEE and to improve stability margins.
22	EN	This pin is the enable input to the IC. This is a comparator type input with a rising threshold of 0.6V and programmable hysteresis. Driving this pin above 0.6V enables the IC. Bypass this pin to AGND with a 10nF ceramic capacitor to mitigate SEE.
23	PORSEL	This pin is the input for selecting the rising and falling POR (Power-On-Reset) thresholds. For a nominal 5V supply, connect this pin to DVDD. For a nominal 3.3V supply, connect this pin to DGND. For nominal supply voltages between 5V and 3.3V, connect this pin to DGND.
	Heatsink	The heatsink is electrically isolated and should be connected to a thermal chassis of any potential which offers optimal thermal relief.

Absolute Maximum Ratings

AVDD . . . . . AGND - 0.3V to AGND + 6.5V
DVDD . . . . . DGND - 0.3V to DGND +6.5V
LXx, PVINx . . . . . PGNDx - 0.3V to PGNDx + 6.5V
AVDD - AGND, DVDD - DGND . . . . . PVINx - PGNDx ± 0.3V
Signal Pins (Note 10) . . . . . AGND - 0.3V to AVDD + 0.3V
Digital Control Pins (Note 11) . . . . . DGND - 0.3V to DVDD + 0.3V
PGOOD . . . . . DGND - 0.3V to DGND + 6.5V
SS . . . . . DGND - 0.3V to DGND + 2.5V

Absolute Maximum Ratings (Note 12)

AVDD . . . . . AGND - 0.3V to AGND + 5.7V
DVDD . . . . . DGND - 0.3V to DGND + 5.7V
LXx, PVINx . . . . . PGNDx - 0.3V to PGNDx + 5.7V
AVDD - AGND, DVDD - DGND . . . . . PVINx - PGNDx ± 0.3V
Signal Pins (Note 10) . . . . . AGND - 0.3V to AVDD + 0.3V
Digital Control Pins (Note 11) . . . . . DGND - 0.3V to DVDD + 0.3V
PGOOD . . . . . DGND - 0.3V to DGND + 5.7V
SS . . . . . DGND - 0.3V to DGND + 2.5V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
48 Ld CQFP R48.A (Notes 6, 8)	36.5	3
48 Ld CQFP R48.B (Notes 7, 9)	19	1.3

Maximum Junction Temperature . . . . . +145°C
Storage Temperature Range . . . . . -65°C to +150°C

Recommended Operating Conditions

AVDD . . . . . AGND + 3V to 5.5V
DVDD . . . . . DGND + 3V to 5.5V
PVINx . . . . . PGNDx + 3V to 5.5V
AVDD - AGND, DVDD - DGND . . . . . PVINx - PGNDx ± 0.1V
Signal Pins (Note 11) . . . . . AGND to AVDD
Digital Control Pins (Note 12) . . . . . DGND to DVDD
REF, SS . . . . . Internally Set
GND, TDI, TDO, TPGM . . . . . DGND
I_{LXx} ($T_J \leq +145°C$) . . . . . 0A to 1.0A
Ambient Temperature Range . . . . . -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See TB379 for details.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features. See TB379.
8. For θ_{JC}, the "case temp" location is the center of the package underside.
9. For θ_{JC}, the "case temp" location is the center of the exposed metal heatsink on the package underside.
10. EN, FB, PORSEL and REF pins.
11. M/S, SYNC, TDI, TDO and ZAP pins.
12. For operation in a heavy ion environment tested at LET = 86.4MeV•cm^2/mg with +125°C (T_C).

Electrical Specifications

Unless otherwise noted, V_{IN} = AVDD = DVDD = PVINx = EN = M/S = 3V or 5.5V; GND = AGND = DGND = PGNDx = TDI = TDO = ZAP = 0V; FB = 0.65V; PORSEL = V_{IN} for 4.5V ≤ V_{IN} ≤ 5.5V and GND for V_{IN} < 4.5V, SYNC = LXx = Open Circuit; PGOOD is pulled up to V_{IN} with a 1kΩ resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; I_{OUT} = 0A; T_A = T_J = +25°C. (Note 15). **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total Iodizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total Iodizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

PARAMETER	TEST CONDITIONS	MIN (Note 16)	TYP	MAX (Note 16)	UNIT
POWER SUPPLY					
Operating Supply Current	V_{IN} = 5.5V (Note 13)		40	**65**	mA
	V_{IN} = 3.6V (Note 13)		25	**45**	mA
Shutdown Supply Current	V_{IN} = 5.5V, EN = GND (Note 14)		6	**12**	mA
	V_{IN} = 3.6V, EN = GND (Note 14)		3	**6**	mA
OUTPUT VOLTAGE					
Reference Voltage Tolerance		**0.594**	0.600	**0.606**	V
Output Voltage Tolerance	V_{OUT} = 0.8V to 2.5V for V_{IN} = 4.5V to 5.5V, V_{OUT} = 0.8V to 2.5V for V_{IN} = 3V to 3.6V, I_{OUT} = 0A to 6A (Notes 17, 18)	**-2**	0	**2**	%
Feedback (FB) Input Leakage Current	V_{IN} = 5.5V, V_{FB} = 0.6V	**-1**	0	**1**	µA
PWM CONTROL LOGIC					
Oscillator Accuracy		**0.85**	1	**1.15**	MHz
External Oscillator Range		**0.8**	1	**1.2**	MHz
Minimum LXx On Time	V_{IN} = 5.5V, Test mode		110	**150**	ns

Electrical Specifications Unless otherwise noted, V_{IN} = AVDD = DVDD = PVINx = EN = M/S = 3V or 5.5V; GND = AGND = DGND = PGNDx = TDI = TDO = ZAP = 0V; FB = 0.65V; PORSEL = V_{IN} for 4.5V ≤ V_{IN} ≤ 5.5V and GND for V_{IN} < 4.5V, SYNC = LXx = Open Circuit; PGOOD is pulled up to V_{IN} with a 1kΩ resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; I_{OUT} = 0A; T_A = T_J = +25°C. (Note 15). **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total lodizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total lodizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 16)	TYP	MAX (Note 16)	UNIT
Minimum LXx Off Time	V_{IN} = 5.5V, Test mode		40	**100**	ns
Minimum LXx On Time	V_{IN} = 3V, Test mode		150	**210**	ns
Minimum LXx Off Time	V_{IN} = 3V, Test mode		50	**100**	ns
Master/Slave (M/S) Input Voltage	Input high threshold	**V_{IN} - 0.5**	1.3		V
	Input low threshold		1.2	**0.5**	V
Master/Slave (M/S) Input Leakage Current	V_{IN} = 5.5V, M/S = GND or V_{IN}	**-1**	0	**1**	µA
Synchronization (SYNC) Input Voltage	Input high threshold, M/S = GND	**2.3**	1.7		V
	Input low threshold, M/S = GND		1.5	**1**	V
Synchronization (SYNC) Input Leakage Current	V_{IN} = 5.5V, M/S = GND, SYNC = GND or V_{IN}	**-1**	0	**1**	µA
Synchronization (SYNC) Output Voltage	V_{IN} - V_{OH} at I_{OH} = -1mA		0.15	**0.40**	V
	V_{OL} at I_{OL} = 1mA		0.15	**0.40**	V
POWER BLOCKS					
Upper Device $r_{DS(ON)}$	V_{IN} = 3V, 0.4A per power block, test mode (Note 18)	**122**	215	**346**	mΩ
Lower Device $r_{DS(ON)}$	V_{IN} = 3V, 0.4A per power block, test mode (Note 18)	**77**	146	**236**	mΩ
LXx Output Leakage	V_{IN} = 5.5V, EN = LXx = GND, single LXx output	**-1**	0		µA
	V_{IN} = 5.5V, EN = GND, LXx = V_{IN}, single LXx output		0	**15**	µA
Dead time	Within a single power block or between power blocks (Note 18)	**1.7**	5		ns
Efficiency	V_{IN} = 3.3V, V_{OUT} = 1.8V, I_{OUT} = 3A		90		%
	V_{IN} = 5V, V_{OUT} = 2.5V, I_{OUT} = 3A		92		%
POWER-ON RESET					
POR Select (PORSEL)	Input high threshold	**V_{IN} - 0.5**	1.4		V
	Input low threshold		1.2	**0.5**	V
POR Select (PORSEL) Input Leakage Current	V_{IN} = 5.5V, PORSEL = GND or V_{IN}	**-1**	0	**1**	µA
VIN POR	Rising threshold, PORSEL = V_{IN}	**4.10**	4.25	**4.45**	V
	Hysteresis, PORSEL = V_{IN}	**225**	325	**425**	mV
	Rising threshold, PORSEL = GND	**2.65**	2.80	**2.95**	V
	Hysteresis, PORSEL = GND	**90**	175	**260**	mV
Enable (EN) Input Voltage	Rising/falling threshold	**0.56**	0.60	**0.64**	V
Enable (EN) Input Leakage Current	V_{IN} = 5.5V, EN = GND or V_{IN}	**-3**	0	**3**	µA
Enable (EN) Sink Current	EN = 0.3V	**6.4**	11.0	**16.6**	µA
SOFT-START					
Soft-Start Source Current	SS = GND	**20**	23	**27**	µA
Soft-Start Discharge ON-Resistance			2.2	**4.7**	Ω
Soft-Start Discharge Time			256		Clock Cycles
POWER-GOOD SIGNAL					

Electrical Specifications Unless otherwise noted, V_{IN} = AVDD = DVDD = PVINx = EN = M/S = 3V or 5.5V; GND = AGND = DGND = PGNDx = TDI = TDO = ZAP = 0V; FB = 0.65V; PORSEL = V_{IN} for 4.5V ≤ V_{IN} ≤ 5.5V and GND for V_{IN} < 4.5V, SYNC = LXx = Open Circuit; PGOOD is pulled up to V_{IN} with a 1kΩ resistor; REF is bypassed to GND with a 220nF capacitor; SS is bypassed to GND with a 100nF capacitor; I_{OUT} = 0A; T_A = T_J = +25°C. (Note 15). **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total lodizing dose of 100krad(Si) with exposure at a high dose rate of 50 - 300krad(Si)/s; and over a total lodizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 16)	TYP	MAX (Note 16)	UNIT
Rising Threshold	V_{FB} as a % of V_{REF}, Test mode	**107**	111	**115**	%
Rising Hysteresis	V_{FB} as a % of V_{REF}, Test mode	**2**	3.5	**5**	%
Falling Threshold	V_{FB} as a % of V_{REF}, Test mode	**85**	89	**93**	%
Falling Hysteresis	V_{FB} as a % of V_{REF}, Test mode	**2**	3.5	**5**	%
Power-Good Drive	V_{IN} = 3V, PGOOD = 0.4V, EN = GND	**7.3**	8.2		mA
Power-Good Leakage	V_{IN} = PGOOD = 5.5V		0.001	**1**	µA
PROTECTION FEATURES					
Undervoltage Monitor					
Undervoltage Trip Threshold	V_{IN} = 3V, V_{FB} as a % of V_{REF}, Test mode	**71**	75	**79**	%
Undervoltage Recovery Threshold	V_{IN} = 3V, V_{FB} as a % of V_{REF}, Test mode	**84**	88	**92**	%
Overcurrent Monitor					
Overcurrent Trip Level	LX4 power block, Test mode, (Note 19)	**1.3**	1.9	**2.5**	A
Overcurrent or Short-Circuit Duty-Cycle	V_{IN} = 3V, SS interval = 200µs, Test mode, fault interval divided by hiccup interval		0.8	**5**	%

NOTES:

13. L = 1µH connected to Lx
14. 1kΩ PGOOD pull-up resistor is not populated.
15. Typical values shown are not guaranteed. Guaranteed min/max values are provided in the SMD.
16. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
17. Limits do not include tolerance of external feedback resistors. The 0A to 6A output current range may be reduced by Minimum LXx On Time and Minimum LXx Off Time specifications.
18. Limits established by characterization or analysis and are not production tested.
19. During an output short-circuit, peak current through the power block(s) can continue to build beyond the overcurrent trip level by up to 3A. With all six power blocks connected, peak current through the power blocks and output inductor could reach (6 x 2.5A) + 3A = 18A. The output inductor must support this peak current without saturating.

Functional Description

The ISL70001SEH, ISL70001SRH are monolithic, fixed frequency, current-mode synchronous buck regulators with user configurable power blocks. Two devices can be used to provide a total DC/DC solution for FPGAs, CPLDs, DSPs and CPUs.

The ISL70001SEH, ISL70001SRH utilize peak current-mode control with integrated compensation and switches at a fixed frequency of 1MHz. Two devices can be synchronized 180° out-of-phase to reduce input RMS ripple current. These attributes reduce the number and size of external components required, while providing excellent output transient response. The internal synchronous power switches are optimized for high efficiency and good thermal performance.

The chip features a comparator type enable input that provides flexibility. It can be used for simple digital on/off control or, alternately, can provide undervoltage lockout capability by using two external resistors to precisely sense the level of an external supply voltage. A power-good signal indicates when the output voltage is within ±11% typical of the nominal output voltage.

Regulator start-up is controlled by an analog soft-start circuit, which can be adjusted from approximately 2ms to 200ms by using an external capacitor.

The ISL70001SEH, ISL70001SRH incorporate fault protection for the regulator. The protection circuits include input undervoltage, output undervoltage, and output overcurrent.

Power Blocks

The power output stage of the regulator consists of six 1A capable power blocks that are paralleled to provide full 6A output current capability. The block diagram in Figure 6 shows a top level view of the individual power blocks.

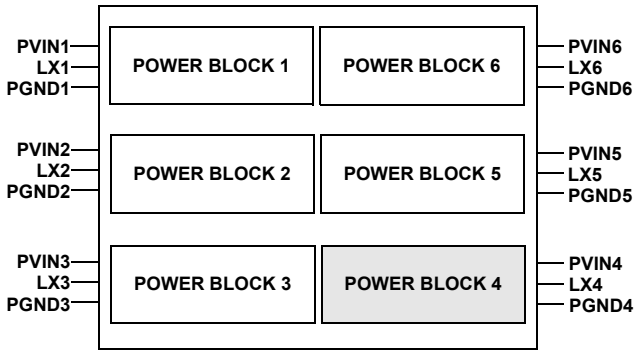


FIGURE 6. POWER BLOCK DIAGRAM

Each power block has a power supply input pin, PVINx, a phase output pin, LXx, and a power supply ground pin, PGNDx. All PVINx pins must be connected to a common power supply rail and all PGNDx pins must be connected to a common ground. LXx pins should be connected to the output inductor based on the required load current, but must include the LX4 pin. For example, if 3A of output current is needed, any three LXx pins can be connected to the inductor as long as one of them is the LX4 pin. The unused LXx pins should be left unconnected. Connecting all six LXx pins to the output inductor provides a maximum 6A of output current. See the Typical Application Schematics for pin connection guidance.

A scaled pilot device associated with each power block provides current feedback. Power block 4 contains the master pilot device and this is why it must be connected to the output inductor.

Main Control Loop

During normal operation, the internal top power switch is turned on at the beginning of each clock cycle. Current in the output inductor ramps up until the current comparator trips and turns off the top power MOSFET. The bottom power MOSFET turns on and the inductor current ramps down for the rest of the cycle.

The current comparator compares the output current at the ripple current peak to a current pilot. The error amplifier monitors V_{OUT} and compares it with an internal reference voltage. The output voltage of the error amplifier drives a proportional current to the pilot. If V_{OUT} is low, the current level of the pilot is increased and the trip off current level of the output is increased. The increased output current raises V_{OUT} until it is in agreement with the reference voltage.

Output Voltage Selection

The output voltage can be adjusted using an external resistor divider as shown in Figure 7.

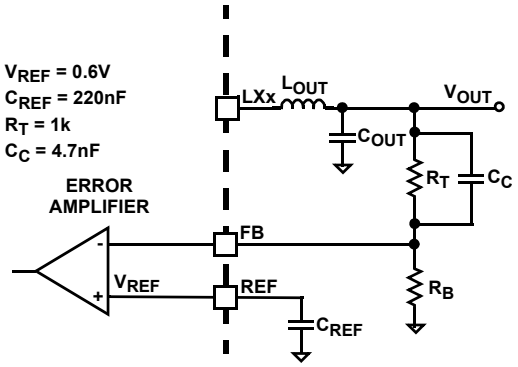


FIGURE 7. OUTPUT VOLTAGE SELECTION

R_T should be selected as 1kΩ to mitigate SEE. R_T should be shunted by a 4.7nF ceramic capacitor, C_C, to mitigate SEE and to improve loop stability margins. The REF pin should be bypassed to AGND with a 220nF ceramic capacitor to mitigate SEE. It should be noted that no current (sourcing or sinking) is available from the REF pin. R_B can be determined from Equation 3. The designer can configure the output voltage from 0.8V to 85% of the input voltage.

$$R_B = R_T \cdot \frac{V_{REF}}{V_{OUT} - V_{REF}} \quad \text{(EQ. 3)}$$

Switching Frequency/Synchronization

The ISL70001SEH, ISL70001SRH feature an internal oscillator running at a fixed frequency of 1MHz ±15% over recommended operating conditions. The regulator can be configured to run from the internal oscillator or can be synchronized to another ISL70001SEH or an SEE hardened external clock with a frequency range of 1MHz ±20%.

To run the regulator from the internal oscillator, connect the M/S pin to DVDD. In this case, the output of the internal oscillator appears on the SYNC pin. To synchronize the regulator to the SYNC output of another regulator or a SEE hardened external

clock, connect the M/S pin to DGND. In this case, the SYNC pin is an input that accepts an external synchronizing signal. When synchronizing multiple devices, slave regulators are synchronized 180° out-of-phase with respect to the SYNC output of a master regulator or an external clock.

When using an ISL70001SEH in clock slave mode and applying an external clock to SYNC (whether from a clock master ISL70001SEH or another external clock), all the clock slaves using the external clock signal must have their switching disabled through their EN input before any stoppage of the clock on the SYNC input. If the external clock signal on the SYNC pin stops or is otherwise removed while the clock slave ISL70001SEH is enabled, the internal lower FET turns on and remains on as the ISL70001SEH control circuit waits for the next rising edge of the external clock that never arrives, as shown in Figure 8. Current from the load then recirculates through the stuck-on lower FET. Figure 8 shows the SYNC stopping at a low level. If the SYNC stops at a level greater than the SYNC voltage threshold (Vth), and then decreases through the SYNC Vth, there is a solitary LX pulse.

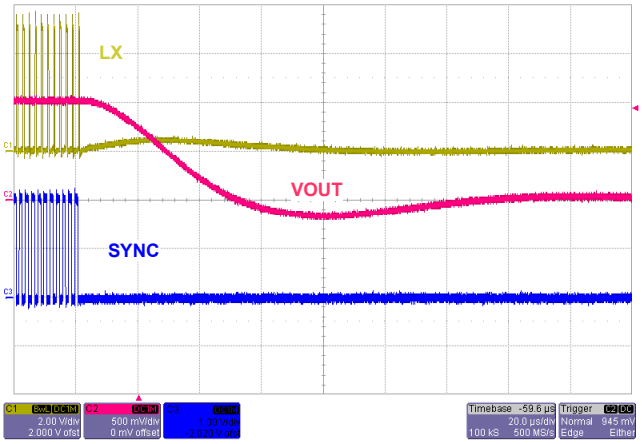


FIGURE 8. SYNC LOSS SHOWING LX PULLED LOW

Operation Initialization

The ISL70001SEH, ISL70001SRH initialize based on the state of the Power-on Reset (POR) monitor of the PVINx inputs and the state of the EN input. Successful initialization prompts a soft-start interval, and the regulator begins slowly ramping the output voltage. Once the commanded output voltage is within the proper window of operation, the power-good signal changes state from LOW to HIGH, indicating proper regulator operation.

Power-On Reset

The POR circuitry prevents the controller from attempting to soft-start before sufficient bias is present at the PVINx pins.

The POR threshold of the PVINx pins is controlled by the PORSEL pin. For a nominal 5V supply voltage, PORSEL should be connected to DVDD. For a nominal 3.3V supply voltage, PORSEL should be connected to DGND. For nominal supply voltages between 5V and 3.3V, PORSEL should be connected to DGND. The POR rising and falling thresholds are shown in the “Electrical Specifications” table on page 10.

Hysteresis between the rising and falling thresholds ensures that small perturbations on PVINx seen during turn-on/turn-off of the regulator do not cause inadvertent turn-off/turn-on of the regulator. When the PVINx pins are below the POR rising threshold, the internal synchronous power MOSFET switches are turned off and the LXx pins are held in a high-impedance state.

Enable and Disable

After the POR input requirement is met, the ISL70001SEH, ISL70001SRH remains in shutdown until the voltage at the enable input rises above the enable threshold. Figure 9 shows the enable circuit features a comparator type input. In addition to simple logic on/off control, the enable circuit allows the level of an external voltage to precisely gate the turn-on/turn-off of the regulator. An internal I_{EN} current sink with a typical value of 11µA is only active when the voltage on the EN pin is below the enable threshold. The current sink pulls the EN pin low. As V_{IN2} rises, the enable level is not set exclusively by the resistor divider from V_{IN2}.

With the current sink active, the enable level is defined by Equation 4. R_1 is the resistor from the EN pin to V_{IN2} and R_2 is the resistor from the EN pin to the AGND pin.

$$V_{ENABLE} = V_R \cdot \left[1 + \frac{R_1}{R_2}\right] + I_{EN} \cdot R_1 \quad \text{(EQ. 4)}$$

Once the voltage at the EN pin reaches the enable threshold, the I_{EN} current sink turns off.

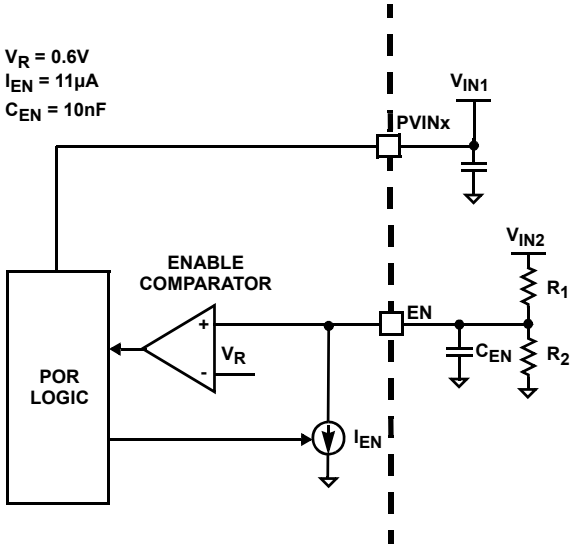


FIGURE 9. ENABLE CIRCUIT

With the part enabled and the I_{EN} current sink off, the disable level is set by the resistor divider. The disable level is defined by Equation 5.

$$V_{DISABLE} = V_R \cdot \left[1 + \frac{R_1}{R_2}\right] \quad \text{(EQ. 5)}$$

The difference between the enable and disable levels provide adjustable hysteresis so that noise on V_{IN2} does not interfere with the enabling or disabling of the regulator.

To mitigate SEE, the EN pin should be bypassed to the AGND pin with a 10nF ceramic capacitor.

Soft-Start

Once the POR and enable circuits are satisfied, the regulator initiates a soft-start. Figure 10 shows that the soft-start circuit clamps the error amplifier reference voltage to the voltage on an external soft-start capacitor connected to the SS pin.

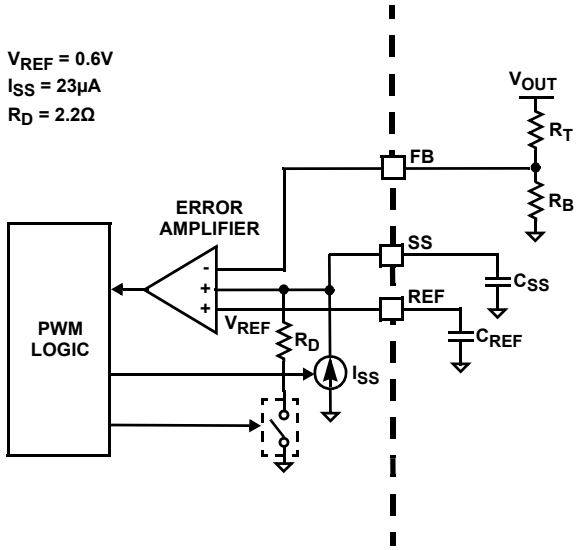


FIGURE 10. SOFT-START CIRCUIT

The soft-start capacitor is charged by an internal I_{SS} current source. As the soft-start capacitor is charged, the output voltage slowly ramps to the set point determined by the reference voltage and the feedback network. Once the voltage on the SS pin is equal to the internal reference voltage, the soft-start interval is complete. The controlled ramp of the output voltage reduces the inrush current during start-up. The soft-start output ramp interval is defined in Equation 6 and is adjustable from approximately 2ms to 200ms. The value of the soft-start capacitor, C_{SS}, should range from 8.2nF to 8.2µF, inclusive. The peak inrush current can be computed from Equation 7. The soft-start interval should be long enough to ensure that the peak in-rush current plus the peak output load current does not exceed the overcurrent trip level of the regulator.

$$t_{SS} = C_{SS} \cdot \frac{V_{REF}}{I_{SS}} \quad \text{(EQ. 6)}$$

$$I_{INRUSH} = C_{OUT} \cdot \frac{V_{OUT}}{t_{SS}} \quad \text{(EQ. 7)}$$

The soft-start capacitor is immediately discharged by a 2.2Ω resistor whenever POR conditions are not met or EN is pulled low. The soft-start discharge time is equal to 256 clock cycles.

Power-Good

The power-good (PGOOD) pin is an open-drain logic output that indicates when the output voltage of the regulator is within regulation limits. The power-good pin pulls low during shutdown and remains low when the controller is enabled. After a successful soft-start, the PGOOD pin releases and the voltage rises with an external pull-up resistor. The power-good signal transitions low immediately when the EN pin is pulled low.

The power-good circuitry monitors the FB pin and compares it to the rising and falling thresholds shown in the “Electrical Specifications” table on page 10. If the feedback voltage exceeds the typical rising limit of 111% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage falls to a typical of 107.5% of the reference voltage. If the feedback voltage drops below a typical of 89% of the reference voltage, the PGOOD pin pulls low. The PGOOD pin continues to pull low until the feedback voltage rises to a typical 92.5% of the reference voltage. The PGOOD pin then releases and signals the return of the output voltage to within the power-good window.

The PGOOD pin can be pulled up to any voltage from 0V to 5.5V, independently from the supply voltage. The pull-up resistor should have a nominal value from 1kΩ to 10kΩ. The PGOOD pin should be bypassed to DGND, with a 10nF ceramic capacitor to mitigate SEE.

Fault Monitoring and Protection

The ISL70001SEH, ISL70001SRH actively monitor output voltage and current to detect fault conditions. Fault conditions trigger protective measures to prevent damage to the regulator and external load device.

Undervoltage Protection

A hysteretic comparator monitors the FB pin of the regulator. The feedback voltage is compared to an undervoltage threshold that is a fixed percentage of the reference voltage. Once the comparator trips, indicating a valid undervoltage condition, a 3-bit undervoltage counter increments. The counter is reset if the feedback voltage rises back above the undervoltage threshold, plus a specified amount of hysteresis outlined in the “Electrical Specifications” table on page 11. If the 3-bit counter overflows, the undervoltage protection logic shuts down the regulator.

After the regulator shuts down, it enters a delay interval equivalent to the soft-start interval, which allows the device to cool. The undervoltage counter is reset when the device enters the delay interval. The protection logic initiates a normal soft-start once the delay interval ends. If the output successfully soft-starts, the power-good signal goes high, and normal operation continues. If undervoltage conditions continue to exist during the soft-start interval, the undervoltage counter must overflow before the regulator shuts down again. This hiccup mode continues indefinitely until the output soft-starts successfully.

Overcurrent Protection

A pilot device integrated into the PMOS transistor of Power Block 4 samples current each cycle. This current feedback is scaled and compared to an overcurrent threshold based on the number of power blocks connected. Each additional power block connected beyond Power Block 4 increases the overcurrent limit by 2A. For example, if three power blocks are connected, the typical current limit threshold would be 3 x 2A = 6A.

If the sampled current exceeds the overcurrent threshold, a 3-bit overcurrent counter increments by one LSB. If the sampled current falls below the threshold before the counter overflows, the counter

is reset. Once the overcurrent counter reaches 111, the regulator shuts down.

After the regulator shuts down, it enters a delay interval, equivalent to the soft-start interval, which allows the device to cool. The overcurrent counter is reset when the device enters the delay interval. The protection logic initiates a normal soft-start once the delay interval ends. If the output successfully soft-starts, the power-good signal goes high, and normal operation continues. If overcurrent conditions continue to exist during the soft-start interval, the overcurrent counter must overflow before the regulator shuts down the output again. This hiccup mode continues indefinitely until the output soft-starts successfully.

Note: To prevent severe negative ringing that can disturb the overcurrent counter, it is recommended that a Schottky diode of appropriate rating be added from the LXx pins to the PGNDx pins.

Feedback Loop Compensation

To reduce the number of external components and to simplify the process of determining compensation components, the ISL70001SEH, ISL70001SRH buck regulators have an internally compensated error amplifier.

Due to the current loop feedback in peak current mode control, the modulator has a single pole response with -20dB slope at a frequency determined by the load (Equation 8):

$$F_{PO} = \frac{1}{2\pi \cdot R_O \cdot C_{OUT}} \quad \text{(EQ. 8)}$$

Where R_O is load resistance and C_{OUT} is the output load capacitance. For this type of modulator, a Type 2 compensation circuit is usually sufficient.

Figure 11 shows a Type 2 amplifier and its response, along with the responses of the current mode modulator and the converter.

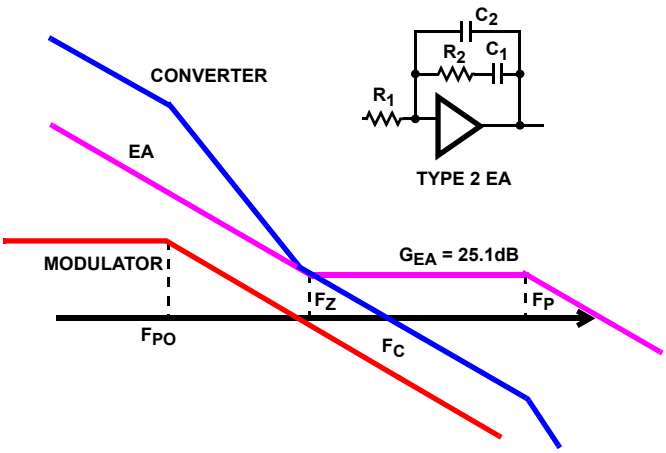


FIGURE 11. FEEDBACK LOOP COMPENSATION

The Type 2 amplifier, in addition to the pole at origin, has a zero-pole pair that causes a flat gain region at frequencies between the zero and the pole (Equations 9 and 10).

$$F_Z = \frac{1}{2\pi \cdot R_2 \cdot C_1} = 8.6\text{kHz} \quad \text{(EQ. 9)}$$

$$F_P = \frac{1}{2\pi \cdot R_1 \cdot C_2} = 546\text{kHz} \quad \text{(EQ. 10)}$$

Zero frequency and amplifier high-frequency gain were chosen to satisfy typical applications. The crossover frequency will appear at the point where the modulator attenuation equals the amplifier high frequency gain. The only task that the system designer has to complete is to specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. Equation 13 approximates the amount of capacitance needed to achieve an optimal pole location depending on the number of LXx pins connected. With this type of compensation, plenty of phase margin is easily achieved due to zero-pole pair phase ‘boost’.

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 1.2kHz to 30kHz range gives some additional phase ‘boost’. Some phase boost is also be achieved by connecting the recommended capacitor C_C in parallel with the upper resistor R_T of the divider that sets the output voltage value, as demonstrated in Figure 7 on page 12.

Component Selection Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a power converter. It is assumed the reader is familiar with many of the basic skills and techniques referenced in the following. In addition to this guide, Renesas provides a complete evaluation board that includes schematic, BOM and an example PCB layout (see “Ordering Information” table on page 6).

Output Filter Design

The output inductor and the output capacitor bank together to form a low-pass filter responsible for smoothing the pulsating voltage at the phase node. The filter must also provide the transient energy until the regulator can respond. Since the filter has low bandwidth relative to the switching frequency, it limits the system transient response. The output capacitors must supply or sink current while the current in the output inductor increases or decreases to meet the load demand.

OUTPUT CAPACITOR SELECTION

The critical load parameters in choosing the output capacitors are the maximum size of the load step (DISTEP), the load-current slew rate (di/dt), and the maximum allowable output voltage deviation under transient loading (DVMAX). Capacitors are characterized according to their capacitance, Equivalent Series Resistance (ESR) and Equivalent Series Inductance (ESL).

At the beginning of a load transient, the output capacitors supply all of the transient current. The output voltage initially deviates by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. Neglecting the contribution of inductor current and regulator

response, the output voltage initially deviates by an amount shown in Equation 11.

$$\Delta V_{MAX} \approx \left[ESL \times \frac{di}{dt}\right] + [ESR \times \Delta I_{STEP}] \quad \text{(EQ. 11)}$$

The filter capacitors selected must have sufficiently low ESL and ESR, such that the total output voltage deviation is less than the maximum allowable ripple.

Most capacitor solutions rely on a mixture of high frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but larger ESR. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

Ceramic capacitors with X7R dielectric are recommended. Alternately, a combination of low ESR solid tantalum capacitors and ceramic capacitors with X7R dielectric may be used.

The ESR of the bulk capacitors is responsible for most of the output voltage ripple. As the bulk capacitors sink and source the inductor AC ripple current, a voltage, $V_{P-P(MAX)}$, develops across the bulk capacitor according to Equation 12.

$$V_{P-P(MAX)} = ESR \times \left[\frac{(V_{IN} - V_{OUT})V_{OUT}}{L_{OUT} \times f_s \times V_{IN}}\right] \quad \text{(EQ. 12)}$$

Another consideration in selecting the output capacitors is loop stability. The total output capacitance sets the dominant pole of the PWM. Because the ISL70001SEH, ISL70001SRH use integrated compensation techniques, it is necessary to restrict the output capacitance in order to optimize loop stability. The recommended load capacitance can be estimated using Equation 13.

$$C_{OUT} = 75\mu F \times \text{Number of LXx Pins Connected} \times \frac{1.8V}{V_{OUT}} \quad \text{(EQ. 13)}$$

Another stability requirement on the selection of the output capacitor is that the 'ESR zero' (f_{ZESR}) be placed at 60kHz to 90kHz. This range is set by an internal, single compensation zero at 8.6kHz. This ESR zero location contributes to increased phase margin of the control loop; therefore (Equation 14):

$$ESR = \frac{1}{2\pi(f_{ZESR})(C_{OUT})} \quad \text{(EQ. 14)}$$

In conclusion, the output capacitors must meet three criteria:

1. They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient.
2. The ESR must be sufficiently low to meet the desired output voltage ripple due to the output inductor current.
3. The ESR zero should be placed, in a rather large range, to provide additional phase margin.

OUTPUT INDUCTOR SELECTION

Once the output capacitors are selected, the maximum allowable ripple voltage, $V_{P-P(MAX)}$, determines the lower limit on the inductance as shown in Equation 15.

$$L_{OUT} \geq ESR \times \left[\frac{(V_{IN} - V_{OUT})V_{OUT}}{f_s \times V_{IN} \times V_{P-P(MAX)}}\right] \quad \text{(EQ. 15)}$$

Since the output capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductor must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

Equation 16 gives the upper limit on output inductance for the case when the trailing edge of the current transient causes a greater output voltage deviation than the leading edge. Equation 17 addresses the leading edge. Normally, the trailing edge dictates the inductance selection because duty cycles are usually <50%. Nevertheless, both inequalities should be evaluated, and inductance should be governed based on the lower of the two results. In each equation, L_{OUT} is the output inductance, C_{OUT} is the total output capacitance, and $\Delta I_{L(P-P)}$ is the peak-to-peak ripple current in the output inductor.

$$L_{OUT} \leq \frac{2 \cdot C_{OUT} \cdot V_{OUT}}{(\Delta I_{STEP})^2}\left[\Delta V_{MAX} - (\Delta I_{L(P-P)} \cdot ESR)\right] \quad \text{(EQ. 16)}$$

$$L_{OUT} \leq \frac{2 \cdot C_{OUT}}{(\Delta I_{STEP})^2}\left[\Delta V_{MAX} - (\Delta I_{L(P-P)} \cdot ESR)\right]\left(V_{IN} - V_{OUT}\right) \quad \text{(EQ. 17)}$$

The other concern when selecting an output inductor is to ensure there is adequate slope compensation when the regulator is operated above 50% duty cycle. Since the internal slope compensation is fixed, output inductance should satisfy Equation 18 to ensure this requirement is met.

$$L_{OUT} \geq \frac{4.32\mu H}{\text{Number of LXx Pins Connected}} \quad \text{(EQ. 18)}$$

Input Capacitor Selection

Input capacitors are responsible for sourcing the AC component of the input current flowing into the switching power devices. Their RMS current capacity must be sufficient to handle the AC component of the current drawn by the switching power devices, which is related to duty cycle. The maximum RMS current required by the regulator is closely approximated by Equation 19.

$$I_{RMS(MAX)} = \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(I_{OUT(MAX)}^2 + \frac{1}{12} \times \left(\frac{V_{IN} - V_{OUT}}{L_{OUT} \times f_s} \times \frac{V_{OUT}}{V_{IN}}\right)^2\right)} \quad \text{(EQ. 19)}$$

The important parameters to consider when selecting an input capacitor are the voltage rating and the RMS ripple current rating. For reliable operation, select capacitors with voltage ratings at least 1.5x greater than the maximum input voltage. The capacitor RMS ripple current rating should be higher than the largest RMS ripple current required by the circuit.

Ceramic capacitors with X7R dielectric are recommended. Alternately, a combination of low ESR solid tantalum capacitors and ceramic capacitors with X7R dielectric may be used. The ISL70001SEH, ISL70001SRH require a minimum effective input capacitance of 100µF for stable operation.

Derating Current Capability

Most space programs issue specific derating guidelines for parts, but these guidelines take the pedigree of the part into account. For instance, a device built to MIL-PRF-38535, such as the ISL70001SEH, ISL70001SRH, is already heavily derated from a current density standpoint. However, a mil-temp or commercial IC that is up-screened for use in space applications may need additional current derating to ensure reliable operation because it was not built to the same standards as the ISL70001SEH, ISL70001SRH.

Figure 12 on page 17 shows the maximum average output current of the ISL70001SEH, ISL70001SRH with respect to junction temperature. These plots take into account the worst-case current share mismatch in the power blocks and the current density requirement of MIL-PRF-38535 (< 2 x 10^5 A/cm^2). The plot clearly shows that the ISL70001SEH, ISL70001SRH can handle 12.1A at +125°C from a worst-case current density standpoint, but the part is limited to 7.8A because that is the lower limit of the current limit threshold with all six power blocks connected.

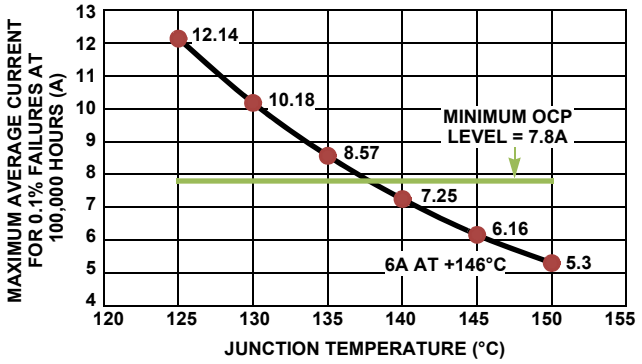


FIGURE 12. CURRENT vs TEMPERATURE

PCB Design

PCB design is critical to high-frequency switching regulator performance. Careful component placement and trace routing are necessary to reduce voltage spikes and minimize undesirable voltage drops. Selection of a suitable thermal interface material is also required for optimum heat dissipation and to provide lead strain relief. See Table 1 on page 19 for layout x-y coordinates.

PCB Plane Allocation

Four layers of 2-ounce copper are recommended. Layer 2 should be a dedicated ground plane with all critical component ground connections made with vias to this layer. Layer 3 should be a dedicated power plane split between the input and output power rails. Layers 1 and 4 should be used primarily for signals but can also provide additional power and ground islands, as required.

PCB Component Placement

Components should be placed as close as possible to the IC to minimize stray inductance and resistance. Prioritize the placement of bypass capacitors on the pins of the IC in the order shown: REF, SS, AVDD, DVDD, PVINx (high frequency capacitors), EN, PGOOD, PVINx (bulk capacitors).

Locate the output voltage resistive divider as close as possible to the FB pin of the IC. The top leg of the divider should connect directly to the POL (Point of Load), and the bottom leg of the divider should connect directly to AGND. The junction of the resistive divider should connect directly to the FB pin.

Locate a Schottky clamp diode as close as possible to the LXx and PGNDx pins of the IC. A small series R-C snubber connected from the LXx pins to the PGNDx pins may be used to damp high frequency ringing on the LXx pins, if desired, see Figure 13.

PCB Layout

Use a small island of copper to connect the LXx pins of the IC to the output inductor on Layers 1 and 4. To minimize capacitive coupling to the power and ground planes, void the copper on Layers 2 and 3 adjacent to the island. Place most of the island of Layer 4 to minimize the amount of copper that must be voided from the ground plane (Layer 2).

Keep all other signal traces as short as possible.

For an example layout, see AN1518.

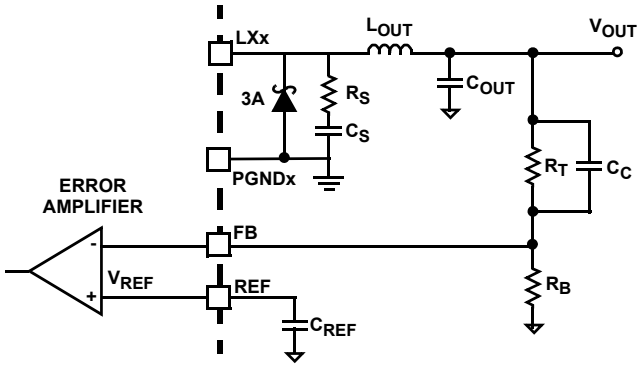


FIGURE 13. SCHOTTKY DIODE AND R-C SNUBBER

Thermal Management for Ceramic Package

For optimum thermal performance, place a pattern of vias and a thermal land on the top layer of the PCB directly underneath the IC. Connect the vias to the plane, which serves as a heatsink. To ensure good thermal contact, thermal interface material such as a Sil-Pad or thermally conductive epoxy should be used to fill the gap between the vias and the bottom of the ceramic package.

Lead Strain Relief

The package leads protrude from the bottom of the package and the leads need forming to provide strain relief. On the ceramic bottom package R48.A, the Sil-pad or epoxy maybe be used to fill the gap left between the PCB board and the bottom of the package when lead forming is completed. On the heat sink option of the package, R48.B, the lead forming should be made so that the bottom of the heatsink and the formed leads are flush.

Heatsink Mounting Guidelines

The R48.B package option has a heatsink mounted on the underside of the package. The following JESD51-5 guidelines may be used to mount the package:

1. Place a thermal land on the PCB under the heatsink.
2. The land should be approximately the same size as to 1mm larger than the 9x9mm heat sink.
3. Place an array of thermal vias below the thermal land.
   - Via array size: ~8 x 8 = 64 thermal vias
   - Via diameter: ~0.3mm drill diameter with plated copper on the inside of each via.
   - Via pitch: ~1.2mm.
   - Vias should drop to and contact as much buried metal area as feasible to provide the best thermal relief.

Heatsink Electrical Potential

The heatsink is electrically isolated and unbiased. The heatsink may be electrically connected to any potential, which offers the best thermal relief through conductive mounting materials (conductive epoxy, solder, etc.) or may be left unbiased through the use of electrically non-conductive mounting materials (non-conductive epoxy, Sil-pad, kapton film, etc.).

Weight Characteristics

Weight of Packaged Device

1.602 Grams typical - R48.A Package

2.440 Grams typical - R48.B Package

Die Characteristics

Die Dimensions

5720µm x 5830µm (225.2 mils x 229.5 mils)
Thickness: 483µm ± 25.4µm (19.0 mils ± 1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Oxide and Silicon Nitride
Thickness: 0.3µm ± 0.03µm to 1.2µm ± 0.12µm

TOP METALLIZATION

Type: AlCu (0.5%)
Thickness: 2.7µm ±0.4µm

SUBSTRATE

Type: Silicon
Isolation: Junction

BACKSIDE FINISH

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential - Package R48.A and R48.B: PGND

Metal Lid Potential

Electrically Isolated -Package R48.A
PGND - Package R48.B

ADDITIONAL INFORMATION

Worst Case Current Density

$< 2 \times 10^5$ A/cm^2

Transistor Count

25030

Layout Characteristics

Step and Repeat

5720µm x 5830µm
Connect PGND to PGNDx

Metallization Mask Layout

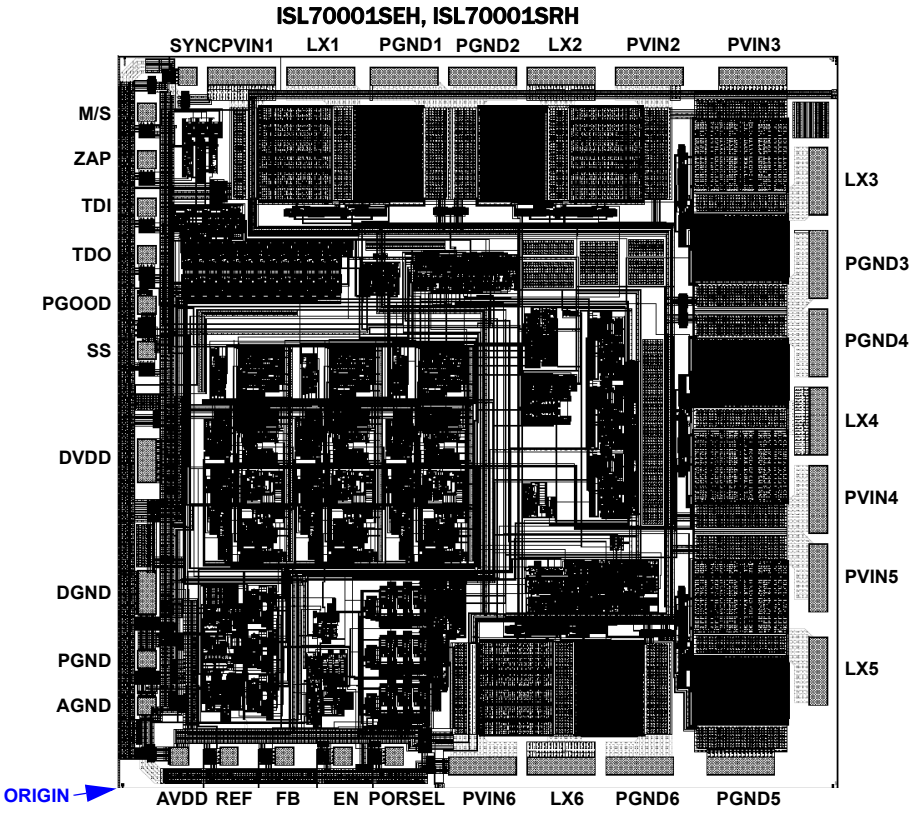


TABLE 1. LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES PER PAD
AVDD	15	478	263	135	135	1
REF	16	865	263	135	135	1
FB	17	1295	263	135	135	1
EN	18	1751	263	135	135	1
PORSEL	19	2151	263	135	135	1
PVIN6	20	2838	188	521	135	3
LX6	21	3449	188	521	135	3
PGND6	22	4060	188	521	135	3
PGND5	23	4845	188	521	135	3
LX5	24	5449	925	135	521	3
PVIN5	25	5449	1651	135	521	3
PVIN4	26	5449	2263	135	521	3
LX4	27	5449	2874	135	521	3
PGND4	28	5449	3485	135	521	3
PGND3	29	5449	4096	135	521	3
LX3	30	5449	4745	135	521	3
PVIN3	31	4941	5559	521	135	3
PVIN2	32	4137	5559	521	135	3
LX2	33	3449	5559	521	135	3

TABLE 1. LAYOUT X-Y COORDINATES (Continued)

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES PER PAD
PGND2	34	2838	5559	521	135	3
PGND1	1	2227	5559	521	135	3
LX1	2	1578	5559	521	135	3
PVIN1	3	962	5559	521	135	3
SYNC	4	544	5559	135	135	1
M/S	5	226	5280	135	135	1
ZAP	6	226	4910	135	135	1
TDI	7	226	4540	135	135	1
TDO	8	226	4170	135	135	1
PGOOD	9	226	3777	135	135	1
SS	10	226	3425	135	135	1
DVDD	11	226	2566	135	333	2
DGND	12	226	1538	135	333	2
PGND	13	226	1018	135	135	1
AGND	14	226	654	135	135	1

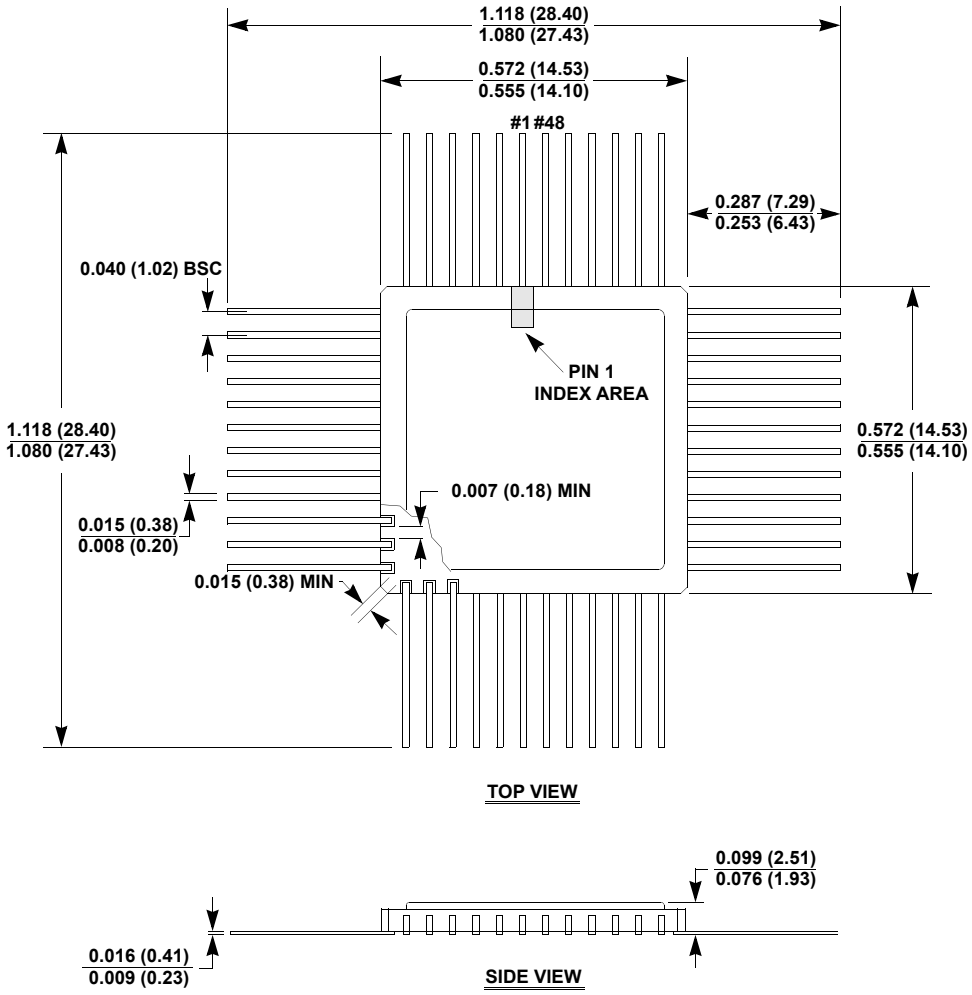
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Apr 15, 2021	3.1	Updated Radiation acceptance features bullets. Updated Ordering information table by adding standard notes and Rad Assurance testing values. Updated Switching Frequency/Synchronization section. Removed About Intersil section.
Feb 22, 2016	3.0	Added text after 2nd paragraph on page 1. Clarified the package vs die pad name (AGND vs PGND) differences and how to use them in the Pin Assignments section. Updated Ordering Information by removing the ISL70001ASEH evaluation board.
Feb 24, 2014	2.0	Added Note 13 on page 11. Added Note 14 on page 11. Removed MSL note from the ordering information on page 2 as it is not applicable to hermetic packages. Added Note 2 for ordering information table on page 6. Added ISL70001SRH throughout datasheet. page 6: Added ISL70001SRHQF and ISL70001SRHVX to the odering information table.
May 20, 2013	1.0	Added heat sink mounting guidelines on page 18. Added “Weight Characteristics” on page 18. Added label “Origin” to Metallization Mask Layout on page 19. page 6, ordering information table: Removed the word “(HEATSINK)” under the first column, and added to rows 2 & 6 in the fourth column “48 ld CQFP with Heatsink”. page 9, thermal information table: Changed note 6, from removed exposed metal pad to exposed metal Heatsink. Updated ordering information table on page 6 as follow: Added ISL7000SRHVF. Added “Heatsink” to help distinguish between the two package types. Thermal Resistance on page 9 as follow: changed note 3 from “low” to “high” effective” thermal conductivity test board type and added note 4 “direct attach”. Page 2: Added ISL70001SEHVFE, ISL70001SEHFE/PROTO parts to ordering information table and added Package DWG# column to table. Added POD: R48.A and R48.
Nov 30, 2011	0.0	Initial Release

Package Outline Drawings

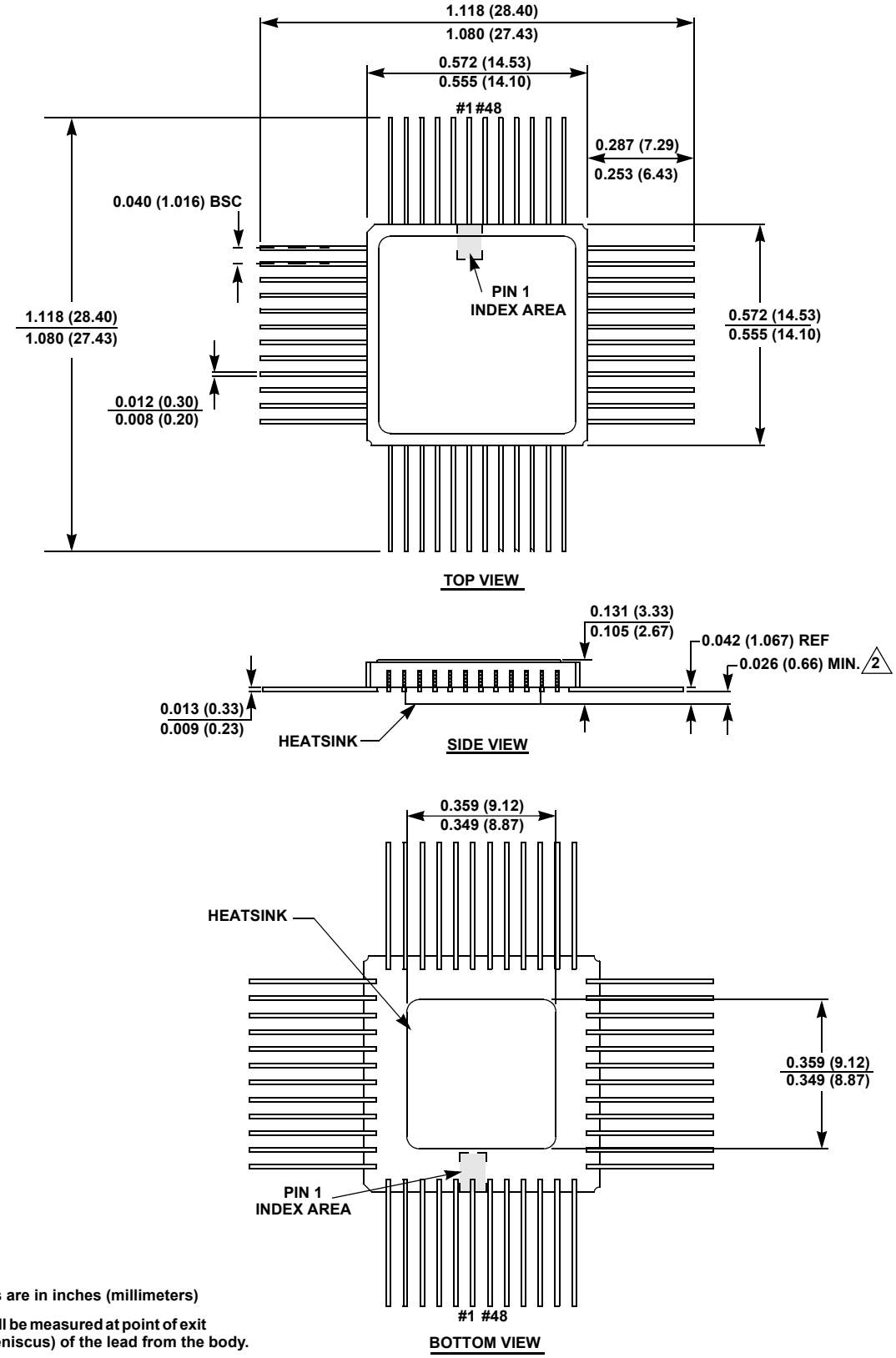
R48.A
48 Ceramic Quad Flatpack Package (CQFP)
Rev 3, 10/12



NOTE:

1. **All dimensions are in inches (millimeters).**

R48.B
48 Ceramic Quad Flatpack Package (CQFP) with Bottom Heatsink
Rev 0, 10/12



NOTES:
1. **All dimensions are in inches (millimeters)**
2. **Dimension shall be measured at point of exit (beyond the meniscus) of the lead from the body.**

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