

32-bit RISC CPU Datasheet M32R CPU

Overview

• M32R is a 32-bit RISC CPU.

Key Features

- RISC architecture
- 32-bit general purpose register x 16
- Number of instructions 83
- 5 stage pipeline
- Two formats of 16 bit length instruction and 32 bit instruction are adopted
 - The code size of the program can be suppressed by the instruction format of 16 bit length
- Multiply-accumulate function
 - Built-in 32-bit x 16-bit multiplier enables execution of 32-bit x 32-bit integer multiplication instruction with 3 CPUCLK
 - Execute multiply-accumulate instruction with 56-bit accumulator
- Peripheral circuit
 - SRAM, cache, bus control circuit, interrupt controller, multifunction timer, serial I / O, watchdog timer

SDI Interrupt Controller Multi-function Timer M32R CPU core Watchdog Timer Built-in Multiply-Serial I/O Accumulator Port Instruction cache SDRAM Controller DMAC Built-in SRAM Block Select Controller **Bus Control Circuit** (A8~A29) 22 32 (D0~D31) (A8~A30) 23 16 (D0~D15)

Block diagram