Description

This document describes the specifications for the F0440 400MHz to 2700MHz Dual RF Digital Variable Gain Amplifier designed for use in receivers.

F0440 Dual RF DVGA provides two independent receiver paths each with 11.6dB typical maximum gain and 4.7dB noise figure in the low-band configuration designed to operate with a single +5V supply. For each path Gain control is split into 3 separate attenuators; DSA0 is a single 6dB step using a single control pin, DSA1 includes 23dB SPI-controlled gain adjustment in 1dB steps, and DSA2 includes 18dB attenuation in 6dB steps controlled using two control pins. F0440 offers +40dBm nominal output IP3 using 245mA total I_{CC}.

This device is packaged in a 6mm x 6mm, 36-pin TQFN with 50 ohm single-ended RF input and RF output impedances for ease of integration into the signal-path lineup for each of the two paths.

Competitive Advantage

- High Reliability
- High Linearity
- Low DC current
- Zero Distortion™ technology
- GlitchFree™ technology

Typical Applications

- Multi-mode, Multi-carrier Receivers
- PCS1900 Base Stations
- DCS1800 Base Stations
- WiMAX and LTE Base Stations
- UMTS/WCDMA 3G Base Stations
- PHS/PAS Base Stations
- Distributed Antenna Systems
- Digital Radio

Table 1. Typical Band Performance Summary

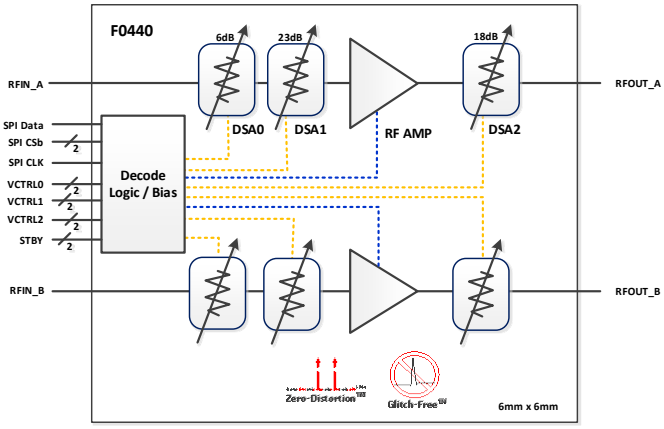
RF Frequency (MHz)	900	2000	2700
Max Gain (dB)	11.6	11.4	11.6
NF at max gain (dB)	4.7	4.9	5.2
OIP3 at max gain (dBm)	+40	+41	+38
OP1dB at max gain (dBm)	+20.2	+19.8	+18.9
DC current (mA)	245	245	245
Power Dissipation (mW)	1225	1225	1225

Features

- Dual Path RF amp and DSAs for Diversity / MIMO Receivers
- RF: 400MHz to 2700MHz
- < 2dB overshoot between DSA transitions
- 11.6dB typical max gain at 900MHz
- DSA0 is a single 6dB coarse step
- DSA1 has 23dB total gain range in 1dB steps
- DSA2 has 18dB gain range in 6dB steps
- +41dBm OIP3 at 2000MHz
- 4.7dB Noise Figure at 900MHz
- +5V Supply Voltage
- I_{CC} = 245mA
- Independent standby: 7mA standby current
- SPI interface for DSA1
- 1-bit control for DSA0
- 2-bit control for DSA2
- 50Ω input and output impedance
- Broadband, Internally Matched
- 6 x 6 mm, 36-TQFN package

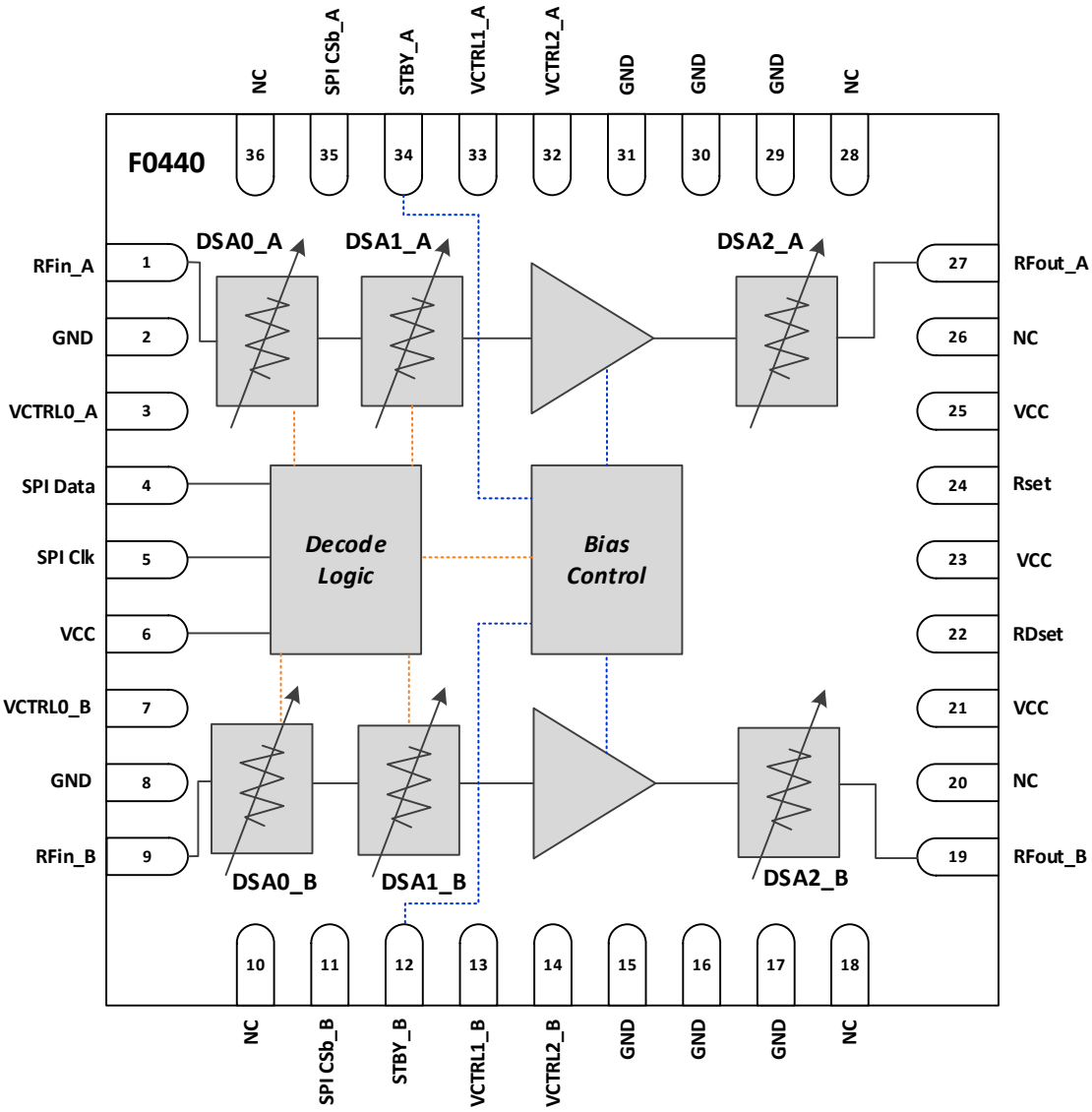
Block Diagram

Figure 1. Block Diagram



Pin Assignments

Figure 2. Pin Assignments for 6 x 6 mm 36-TQFN Package – Top View



Pin Descriptions

Table 2. Pin Descriptions

Number	Name	Description
1	RFin_A	RF Path A input internally matched to 50Ω. Must use external DC block.
2, 8, 15, 16, 17, 29, 30, 31	GND	Ground these pins.
3	VCTRL0_A	1bit DSA0 6dB attenuator control for path A
4	SPI Data[a]	Data input: 3.3V or 1.8V CMOS compatible.
5	SPI Clk[a]	Clock input: 3.3V or 1.8V CMOS compatible.
6, 21, 23, 25	VCC	+5V Power Supply. Use bypass capacitors as close to pin as possible.
7	VCTRL0_B	1bit DSA0 6dB attenuator control for path B
9	RFin_B	RF Path B input internally matched to 50Ω. Must use external DC block.
10, 18, 20, 26, 28, 36	NC	No internal connection. Can be either left open or connected to GND (recommended)
11	SPI CSb_B[a]	Chip Select bar input path B: 3.3V or 1.8V CMOS compatible. Logic LOW shifts data.
12	STBY_B	Standby (Low/Open = device power ON, High = device power OFF with SPI still powered ON). A pull-down resistor connects between input and GND.
13	VCTRL1_B	See separate attenuation logic table for Path B DSA2.
14	VCTRL2_B	See separate attenuation logic table for Path B DSA2.
19	RFout_B	RF output Path B. Use external DC block as close to the pin as possible.
22	RDset	Connect external resistor to GND to optimize amplifier bias. Used with pin 24.
24	Rset	Connect external resistor to GND to optimize amplifier bias. Used with pin 22.
27	RFout_A	RF output Path A. Use external DC block as close to the pin as possible.
32	VCTRL2_A	See separate attenuation logic table for Path A DSA2.
33	VCTRL1_A	See separate attenuation logic table for Path A DSA2.
34	STBY_A	Standby (Low/Open = device power ON, High = device power OFF with SPI still powered ON). A pull-down resistor connects between input and GND.
35	SPI CSb_A[a]	Chip Select bar input path A: 3.3V or 1.8V CMOS compatible. Logic LOW shifts data.
	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple ground vias are also required to achieve the noted RF performance.

a. See Serial Control Mode section for description.

Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the F0440 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
VCC to GND	V_{CC}	-0.3	+5.5	V
SPI Data, SPI CSb_A, CSb_B, SPI Clk, VCTRL0_A, VCTRL0_B	V_{Ctrl1}	-0.3	Minimum (VCC, 3.6)	V
STBY_A, STBY_B, VCTRL1_A, VCTRL1_B, VCTRL2_A, VCTRL2_B	V_{Ctrl2}	-0.3	VCC + 0.25	V
RDset	I_{R1}		+1.5	mA
Rset	I_{R2}		+0.8	mA
RFin_A, RFin_B externally applied DC voltage	V_{RFin}	+1.4	+3.6	V
RFout_A, RFout_B, externally applied DC voltage	V_{RFout}	+1.4	+3.6	V
RF Input Power (RFin_A, RFin_B) applied for 24 hours maximum[a]	P_{in1}		+22	dBm
Continuous Power Dissipation	P_{diss}		1.5	W
Junction Temperature	T_j		150	°C
Storage Temperature Range	T_{st}	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C
ElectroStatic Discharge – HBM (JEDEC/ESDA JS-001-2012)			Class 1C (1500 V)	
ElectroStatic Discharge – CDM (JEDEC 22-C101F)			Class C3 (1000 V)	

a. Exposure to these maximum RF levels can result in significant V_{cc} current draw due to overdriving the amplifier stages.

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Supply Voltage(s)	V_{CC}	All VCC pins	4.75		5.25	V
Operating Temperature Range	T_{CASE}	Exposed Paddle Temperature	-40		+105	°C
RF Frequency Range	F_{RF}	Operating Range	400		2700	MHz
RF Source Impedance	Z_{RFI}	Single Ended		50		Ω
RF Load Impedance	Z_{RFO}	Single Ended		50		Ω

Electrical Characteristics

Table 5. Electrical Characteristics

See F0440 Typical Application Circuit. V_{CC} = +5V, T_C = +25°C, Specifications apply operated as a dual-path RF DVGA unless otherwise noted, Max gain setting, output power = 0dBm, Z_{RFI} = Z_{RFO} = 50Ω, unless otherwise noted.

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Logic Input High	V_{IH}	These apply for 5V, 3.3V, and 1.8V logic levels		*1.1* [a]			V
Logic Input Low	V_{IL}					*0.63*	
Logic Current (per pin)	I_{IH}, I_{IL}	STBY_A, STBY_B	5V logic	*-5*		127[b]	µA
			3.3V logic	*-5*		*87*	
			1.8V logic	*-5*		47	
		SPI_, VCTRL0, VCTRL1, VCTRL2	3.3V logic	*-5*		*5*	
			1.8V logic	*-5*		5	
Supply Current	I_{CC_LB}	Low Band Configuration			245		mA
	I_{CC_MB}	Mid Band Configuration			245	*270*	
	I_{CC_HB}	High Band Configuration			245		
	I_{CC_STBY}	Standby Mode[c]			7	*14*	
Startup time	Tstart	50% of STBY going low to Gain within ±1dB with no attenuation.			74		ns
DSA0 Adjust Range / Step	G_{STEP0}				6		dB
DSA1 Adjustment Range	G_{ADJ1}				23		dB
DSA1 Step	G_{STEP1}				1		dB
DSA2 Adjustment Range	G_{ADJ2}				18		dB
DSA2 Step	G_{STEP2}				6		dB
Max Attenuation Glitch	$ATTN_G$				2		dB
DSA0 Gain Settling Time [d]	$ATT0\_{SW\_0to6}$	50% CTL to within 0.1dB final value, 0 dB state to 6dB state			24	35	ns
	$ATT0\_{SW\_6to1}$	50% CTL to within 0.1dB final value, 6dB state to 0dB state			18	35	ns
DSA2 Gain Settling Time	$ATT2\_{SW\_0to18}$	50% CTL to within 0.1dB final value, 0dB state to 18dB state			16	35	ns
	$ATT2\_{SW\_18to0}$	50% CTL to within 0.1dB final value, 18 dB state to 0dB state			15	35	ns
DSA1 Gain Settling Time	$DSA1_{ST}$	50% of CSb to within 0.1dB final value			300		ns
DSA2 Phase Settling Time	$ATT2\_{PH\_0to18}$	50% CTL to within 1 degree of final value, 0dB state to 18dB state			16	35	ns
	$ATT2\_{PH\_18to0}$	50% CTL to within 1 degree of final value, 18dB state to 0dB state			15	35	ns
Stability K Factor	K_{FACT}	Over entire temperature range		1.4			unit

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Serial Clock Speed	SPI_{CLK}				*10*	MHz
CSb_A, CSb_B to First Serial Clock Rising Edge	A	SPI 3 wire Bus. 50% of CSb falling edge to 50% of CLK rising edge.	10			ns
Serial Data Hold Time	B	SPI 3 wire Bus. 50% of CLK rising edge to 50% of Data falling edge.	10			ns
Final Serial Clock Rising Edge to CSb	C	SPI 3 wire Bus. 50% of CLK rising edge to 50% of CSb rising edge.	10			ns
DSA0 Phase Settling Time	$ATT0\_{PH\_0to6}$	50% CTL to within 1 degree of final value, 0dB state to 6dB state		24	35	ns
	$ATT0\_{PH\_6to0}$	50% CTL to within 1 degree of final value, 6dB state to 0dB state		18	35	ns

a. Items in min/max columns in ***bold italics*** are confirmed by Test.
b. Items in min/max columns that are not bold/italics are confirmed by Design Characterization.
c. During standby mode, SPI is to be left ON and previous state shall be maintained when device is powered up.
d. Time for the gain to settle within ±0.1dB and relative to SPI command latch.

Table 6. Electrical Characteristics – 450MHz Performance

See F0440 Typical Application Circuit. Specifications apply operated as a dual-path RF DVGA unless otherwise noted, V_{CC} = +5V, T_C = +25°C, F_{RF} = 450MHz, Max gain setting, output power = 0dBm / tone, $Z_{RFI} = Z_{RFO}$ = 50Ω, the evaluation board and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
RF Input Return Loss	RL_{IN_450}			11		dB
RF Output Return Loss	RL_{Out_450}			14.5		dB
Gain	G_{MAX_450}			11		dB
	G_{MIN_450}	Maximum attenuation		-35		
	G_{TEMP_450}	Variation over Temperature		0.7		
DSA0 Absolute Error	G_{DSA0SE_450}	Relative to maximum gain		±0.07		dB
DSA1 Step Error	G_{DSA1SE_450}	Between adjacent states		±0.05		dB
DSA1 Absolute Error	$G_{DSA1ABS\_450}$	Relative to maximum gain		±0.15		dB
DSA2 Step Error	G_{DSA2SE_450}	Between adjacent states		±0.11		dB
DSA2 Absolute Error	$G_{DSA2ABS\_450}$	Relative to maximum gain		±0.25		dB
Relative Phase DSA0	$G_{PH\_DSA0\_450}$			1.7		Deg
Phase Deviation DSA1	$G_{PH\_DSA1\_450}$	Between adjacent states		0.16		Deg
Relative Phase DSA2	$G_{PH\_DSA2\_450}$	Between any two states		7.7		Deg
Noise Figure	NF_{450}			5		dB
	NF_{450_HOT}	T_{case} = +105°C		5.7		
	NF_{450_RG}	DSA1 22dB attenuation		27.7		
Output Third Order Intercept Point	$OIP3_{450-1}$	1MHz tone separation		38		dBm

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
	$OIP3_{450-2}$	1MHz tone separation Pout = -10dBm/tone		35		
	$OIP3_{450-6dB}$	1MHz tone separation DSA0 full attenuation		38		
	$OIP3_{450-3}$	1MHz tone separation Worst case over temp range		37		
	$OIP3_{450\_18dB}$	Pout = -18dBm / tone 1MHz tone separation DSA2 full 18dB attenuation		20		
Input 1dB Compression [d]	$IP1dB_{450}$	Full attenuation		30		dBm
Output 1dB Compression	$OP1dB_{450}$			19.4		dBm
Output 1dB Compression Degradation	$OP1_{DEG\_450}$	$OP1dB\_DEG_{450}$= $OP1dB_{450}$ (DSA2 =0dB atten) - $ATTN_{450\_DSA2\_MAX}$ - $OP1dB_{450}$ (DSA2=max atten)		0.4		dB
Output 0.2dB Compression	$OP0.2dB_{450}$			18.2		dBm
Output Saturated Power	$PSAT_{450}$	3dB compression		20.1		dBm
Reverse Isolation	REV_{ISO_450}			21		dB
Path Isolation	$PATH_{ISO\_450}$	RFOUT_B vs. RFOUT_A w/ signal applied to RFIN_A		39		dB
		Same gain settings over PVT		39		

a. Items in min/max columns in ***bold italics*** are confirmed by Test.
b. Items in min/max columns that are not bold/italics are confirmed by Design Characterization.
c. Including frequency and ripple variations valid within each individual 3GPP band.
d. Input 1dB compression point is a linearity figure of merit. Refer to Abs Max Ratings table for maximum RF input power.

Table 7. Electrical Characteristics – Lowband Performance

See F0440 Typical Application Circuit. Specifications apply operated as a dual-path RF DVGA unless otherwise noted, V_{CC} = +5V, T_C = +25°C, F_{RF} = 900MHz, Max gain setting, output power = 0dBm / tone, $Z_{RFI} = Z_{RFO}$ = 50Ω, the evaluation board and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
RF Input Return Loss	RL_{IN_LB}			16		dB
RF Output Return Loss	RL_{Out_LB}			20		dB
Gain	G_{MAX_LB}		*10.9*	11.6	*12.2*	dB
	G_{MIN_LB}	Maximum attenuation	*-36.4*	-34.9	*-33.4*	
	G_{TEMP_LB}	Variation over Temperature		0.6		
	G_{VAR_LB}	Variation over frequency[c]		0.1		
DSA0 Absolute Error	G_{DSA0SE_LB}	Relative to maximum gain		± 0.2		dB
DSA1 Step Error	G_{DSA1SE_LB}	Between adjacent states		± 0.03		dB
DSA1 Absolute Error	$G_{DSA1ABS\_LB}$	Relative to maximum gain		± 0.35		dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
DSA2 Step Error	G_{DSA2SE_LB}	Between adjacent states		± 0.03		dB
DSA2 Absolute Error	$G_{DSA2ABS\_LB}$	Relative to maximum gain		± 0.06		dB
Relative Phase DSA0	$G_{PH\_DSA0\_LB}$			0.7		Deg
Phase Deviation DSA1	$G_{PH\_DSA1\_LB}$	Between adjacent states		0.26		Deg
Relative Phase DSA2	$G_{PH\_DSA2\_LB}$	Between any two states		2.5		Deg
Noise Figure	NF_{LB}			4.7		dB
	NF_{LB_HOT}	T_{case} = +105°C		5.4		
	NF_{LB_RG}	DSA1 22dB attenuation		27		
Output Third Order Intercept Point	$OIP3_{\_LB-1}$	1MHz tone separation	38.5	40		dBm
	$OIP3_{\_LB-2}$	1MHz tone separation Pout = -10dBm/tone		39		
	$OIP3_{\_LB-6dB}$	1MHz tone separation DSA0 full attenuation		40		
	$OIP3_{\_LB-3}$	1MHz tone separation Worst case over temp range	38	39		
	$OIP3_{\_LB\_18dB}$	Pout = -18dBm / tone 1MHz tone separation DSA2 full 18dB attenuation		22		
Input 1dB Compression [d]	$IP1dB_{\_LB}$	Full attenuation		27		dBm
Output 1dB Compression	$OP1dB_{\_LB}$		*18.4*	20.2		dBm
Output 1dB Compression Degradation	$OP1_{\_DEG\_LB}$	$OP1dB\_DEG_{LB}$= $OP1dB_{LB}$ (DSA2 =0dB atten) - $ATTN_{LB\_DSA2\_MAX}$ - $OP1dB_{LB}$ (DSA2=max atten)		0.05	0.5	dB
Output 0.2dB Compression	$OP0.2dB_{\_LB}$			18.7		dBm
Output Saturated Power	$PSAT_{\_LB}$	3 dB compression		20.9		dBm
Reverse Isolation	REV_{ISO_LB}		20	20.5		dB
Path Isolation	$PATH_{ISO\_LB}$	RFOUT_B vs. RFOUT_A w/ signal applied to RFIN_A	43	45		dB
		Same gain settings over PVT		45		

a. Items in min/max columns in ***bold italics*** are confirmed by Test.
b. Items in min/max columns that are not bold/italics are confirmed by Design Characterization.
c. Including frequency and ripple variations valid within each individual 3GPP band.
d. Input 1dB compression point is a linearity figure of merit. Refer to Abs Max Ratings table for maximum RF input power.

Table 8. Electrical Characteristics – Midband Performance

See F0440 Typical Application Circuit. Specifications apply operated as a dual-path RF DVGA unless otherwise noted, VCC = +5V, T_C = +25°C, FRF = 2000MHz, Max gain setting, output power = 0dBm / tone, $Z_{RFI} = Z_{RFO} = 50\Omega$, the evaluation board and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
RF Input Return Loss	RL_{IN_MB}			20		dB
RF Output Return Loss	RL_{Out_MB}			20		dB
Gain	G_{MAX_MB}		*10.6*	11.6	*12.3*	dB
	G_{MIN_MB}	Maximum attenuation	-37.0	-35.3	-33.5	
	G_{TEMP_MB}	Variation over Temperature		0.4		
	G_{VAR_MB}	Variation over frequency[c]		0.02		
DSA0 Absolute Error	G_{DSA0SE_MB}	Relative to maximum gain		± 0.05		dB
DSA1 Step Error	G_{DSA1SE_MB}	Between adjacent states		± 0.03		dB
DSA1 Absolute Error	$G_{DSA1ABS\_MB}$	Relative to maximum gain	*-0.6*	± 0.1	*0.6*	dB
DSA2 Step Error	G_{DSA2SE_MB}	Between adjacent states		± 0.075		dB
DSA2 Absolute Error	$G_{DSA2ABS\_MB}$	Relative to maximum gain		± 0.15		dB
Relative Phase DSA0	$G_{PH\_DSA0\_MB}$			2.9		Deg
Phase Deviation DSA1	$G_{PH\_DSA1\_MB}$	Between adjacent states		0.88		Deg
Relative Phase DSA2	$G_{PH\_DSA2\_MB}$	Any State		10		Deg
Noise Figure	NF_{MB}			4.9		dB
	NF_{MB_HOT}	T_{case} = +105°C		5.6		
	NF_{MB_RG}	DSA1 22dB attenuation		27		
Output Third Order Intercept Point	$OIP3_{\_MB-1}$	1MHz tone separation	37.5	41		dBm
	$OIP3_{\_MB-2}$	1MHz tone separation Pout = -10dBm/tone		40.5		
	$OIP3_{\_MB-6dB}$	1MHz tone separation DSA0 full attenuation		41		
	$OIP3_{\_MB-3}$	1MHz tone separation Worst case over temp range	37.5	39.5		
	$OIP3_{\_MB\_18dB}$	Pout = -18dBm / tone 1 MHz tone separation DSA2 full 18dB attenuation		21		
Input 1dB Compression[d]	$IP1dB_{\_MB}$	Full attenuation		29		dBm
Output 1dB Compression	$OP1dB_{\_MB}$			19.8		dBm
Output 1dB Compression Degradation	$OP1_{\_DEG\_MB}$	$OP1dB\_DEG_{MB}$= $OP1dB_{MB}$ (DSA2 =0dB atten) - $ATTN_{MB\_DSA2\_MAX}$ - $OP1dB_{MB}$ (DSA2=max atten)		0.1	0.5	dB

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Output 0.2dB Compression	$OP0.2dB_{\_MB}$			18.8		dBm
Output Saturated Power	$PSAT_{\_MB}$	3dB compression		20.5		dBm
Reverse Isolation	REV_{ISO_MB}		20	20.5		dB
Path Isolation	$PATH_{ISO\_MB}$	RFOUT_B vs. RFOUT_A w/ signal applied to RFIN_A	44	45		dB
		Same gain settings over PVT		45		

a. Items in min/max columns in ***bold italics*** are confirmed by Test.
b. Items in min/max columns that are not bold/italics are confirmed by Design Characterization.
c. Including frequency and ripple variations valid within each individual 3GPP band.
d. Input 1dB compression point is a linearity figure of merit. Refer to Abs Max Ratings table for maximum RF input power.

Table 9. Electrical Characteristics – Highband Performance

See F0440 Typical Application Circuit. Specifications apply operated as a dual-path RF DVGA unless otherwise noted, VCC = +5V, T_C = +25°C, FRF = 2700MHz, Max gain setting, output power = 0dBm / tone, $Z_{RFI} = Z_{RFO} = 50\Omega$, the evaluation board and connector losses are de-embedded, unless otherwise noted.

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
RF Input Return Loss	RL_{IN_HB}			20		dB
RF Output Return Loss	RL_{Out_HB}			20		dB
Gain	G_{MAX_HB}		*10.6*	11.6	*12.6*	dB
	G_{MIN_HB}	Maximum attenuation	-37.0	-35.4	-33.7	
	G_{TEMP_HB}	Variation over Temperature		0.32		
	G_{VAR_HB}	Variation over frequency[c]		0.05		
DSA0 Absolute Error	G_{DSA0SE_HB}	Relative to maximum gain		± 0.2		dB
DSA1 Step Error	G_{DSA1SE_HB}	Between adjacent states		± 0.04		dB
DSA1 Absolute Error	$G_{DSA1ABS\_HB}$	Relative to maximum gain		± 0.23		dB
DSA2 Step Error	G_{DSA2SE_HB}	Between adjacent states		± 0.11		dB
DSA2 Absolute Error	$G_{DSA2ABS\_HB}$	Relative to maximum gain		± 0.24		dB
Relative Phase DSA0	$G_{PH\_DSA0\_HB}$			4.1		Deg
Phase Deviation DSA1	$G_{PH\_DSA1\_HB}$	Between adjacent states		1.27		Deg
Relative Phase DSA2	$G_{PH\_DSA2\_HB}$	Any State		16		Deg
Noise Figure	NF_{HB}			5.2		dB
	NF_{HB_HOT}	T_{case} = +105°C		5.9		
	NF_{HB_RG}	DSA1 22dB attenuation		28		

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Units
Output Third Order Intercept Point	$OIP3_{HB-1}$	1MHz tone separation	35.2	38		dBm
	$OIP3_{HB-2}$	1MHz tone separation Pout = -10dBm/tone	34	37		
	$OIP3_{HB-6dB}$	1MHz tone separation DSA0 full attenuation		38		
	$OIP3_{HB-3}$	1MHz tone separation Worst case over temp range	34	37		
	$OIP3_{HB\_18dB}$	Pout = -18dBm / tone 1MHz tone separation DSA2 full 18dB attenuation		19		
Input 1dB Compression [d]	$IP1dB_{HB}$	Full attenuation		24		dBm
Output 1dB Compression	$OP1dB_{HB}$			18.9		dBm
Output 1dB Compression Degradation	$OP1_{DEG\_HB}$	$OP1dB\_DEG_{HB}$= $OP1dB_{HB}$ (DSA2 =0dB atten) - $ATTN_{HB\_DSA2\_MAX}$ - $OP1dB_{HB}$ (DSA2=max atten)		0.3	0.5	dB
Output 0.2dB Compression	$OP0.2dB_{HB}$			18.2		dBm
Output Saturated Power	$PSAT_{HB}$	3dB compression		19.4		dBm
Reverse Isolation	REV_{ISO_HB}		19	20.5		dB
Path Isolation	$PATH_{ISO\_HB}$	RFOUT_B vs. RFOUT_A w/ signal applied to RFIN_A	42	44		dB
		Same gain settings over PVT		43		

a. Items in min/max columns in ***bold italics*** are confirmed by Test.
b. Items in min/max columns that are not bold/italics are confirmed by Design Characterization.
c. Including frequency and ripple variations valid within each individual 3GPP band.
d. Input 1dB compression point is a linearity figure of merit. Refer to Abs Max Ratings table for maximum RF input power.

Thermal Characteristics

Table 10. Package Thermal Characteristics

Parameter	Symbol	Value	Units
Junction to Ambient Thermal Resistance	θ_{JA}	40	°C/W
Junction to Case Thermal Resistance (case is defined as the exposed Paddle)	θ_{JC}	4	°C/W
Moisture Sensitivity Rating (Per J-STD-020)		MSL 1	

Typical Operating Conditions

Unless otherwise noted, for the TOC graphs on the following pages, the following conditions apply:

- Vcc = +5V
- Pout = 0dBm / Tone
- 1 MHz Tone Spacing
- T_{CASE} = +25°C
- ATTN setting = 0 dB (Max Gain)
- EVkit losses (traces and connectors) fully de-embedded

Typical Performance Characteristics [Output IP3, EVkit Losses]

Figure 3. Output IP3 for Pout = 0dBm/tone

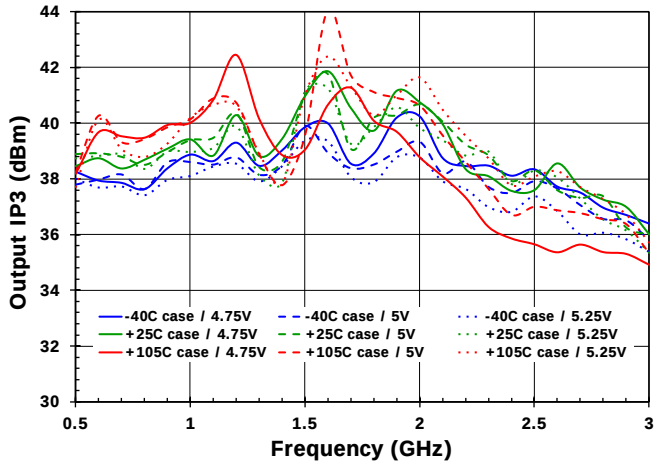


Figure 4. Output IP3 for Pout =-10dBm/tone

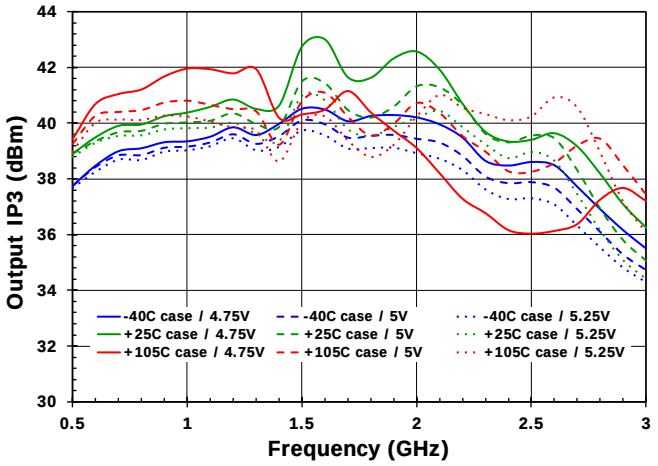


Figure 5. Output IP3 for DSA0=6dB, DSA1=0dB, DSA2 = 0dB, and Pout = 0dBm/tone

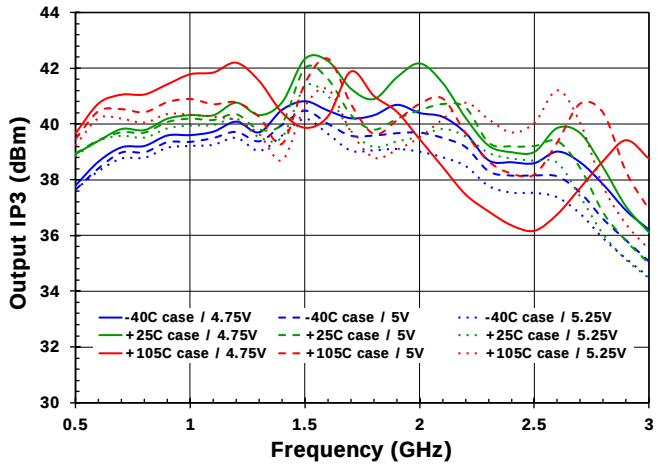


Figure 6. Output IP3 for DSA0=0dB, DSA1=0dB, DSA = 18dB, and Pout =-18dBm/tone

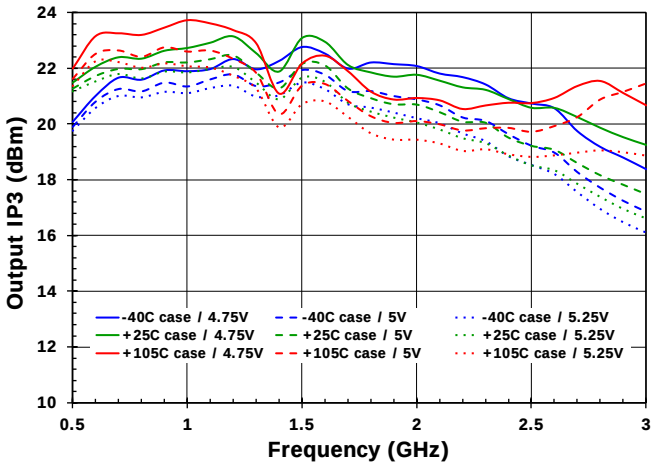


Figure 7. Output IP3 Versus Tone Spacing

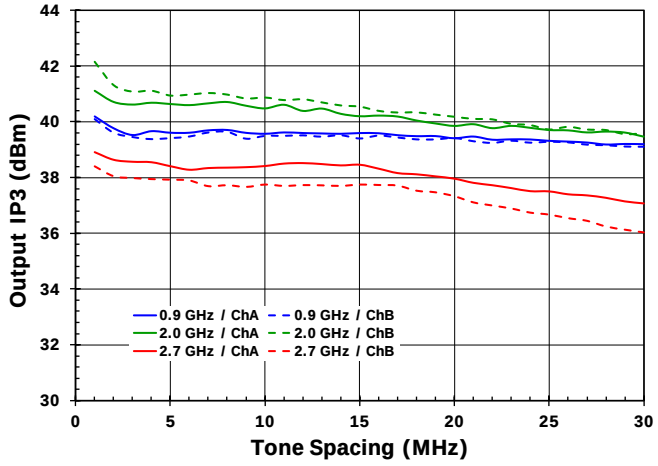
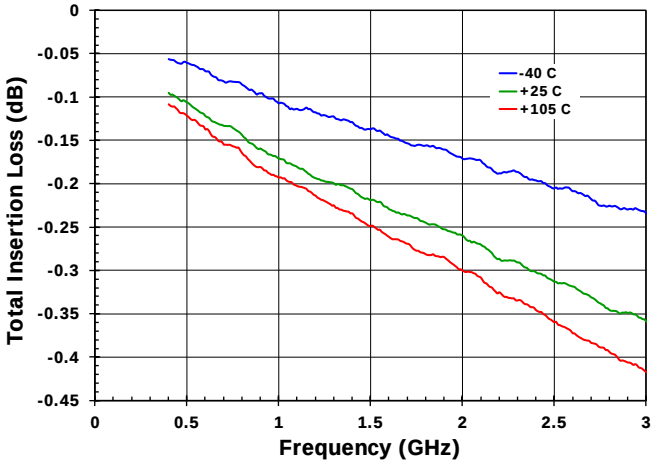


Figure 8. EVkit Losses [connectors and traces])



Typical Performance Characteristics [Compression]

Figure 9. Gain Compression [900MHz]

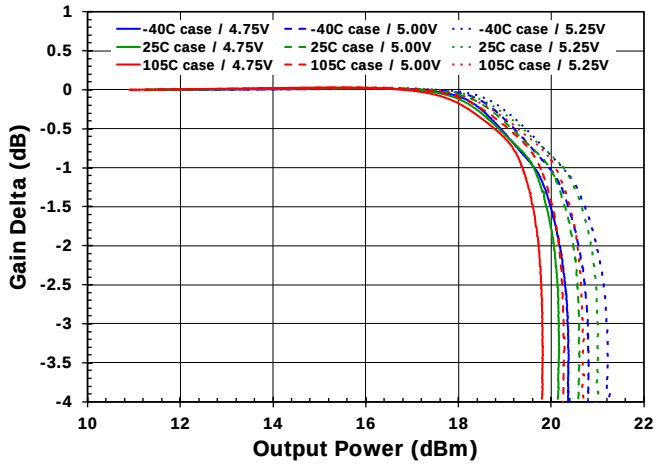


Figure 10. Phase Compression [900MHz]

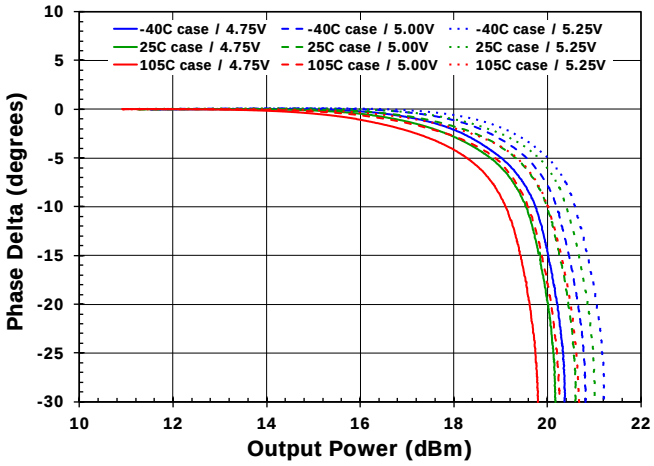


Figure 11. Gain Compression [2000MHz]

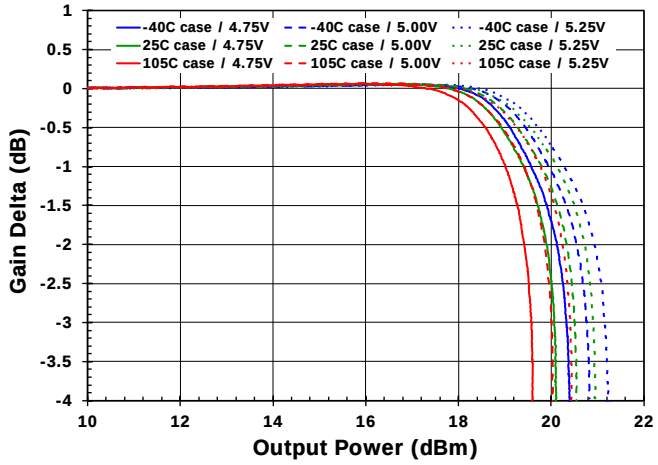


Figure 12. Phase Compression [2000MHz]

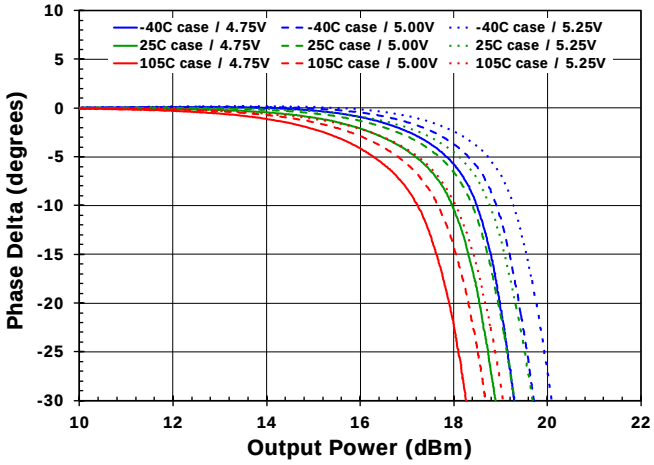


Figure 13. Gain Compression [2700MHz]

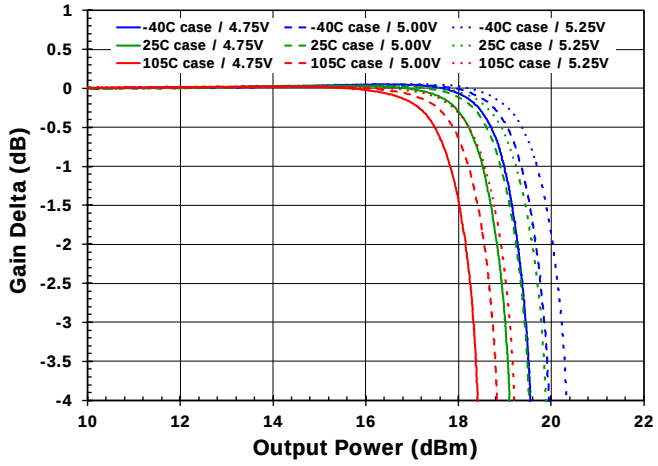
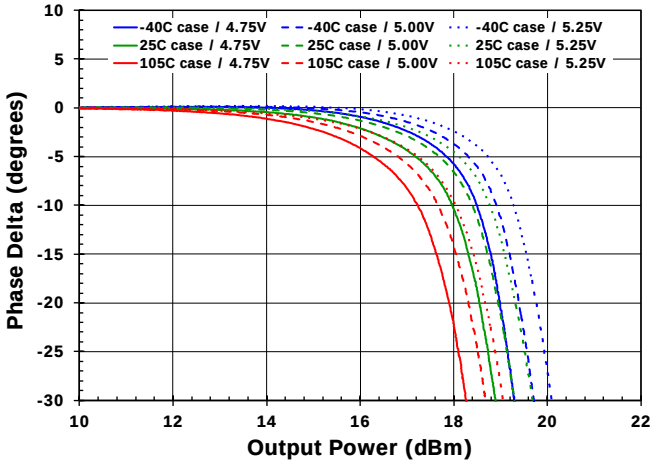


Figure 14. Phase Compression [2700MHz]



Typical Performance Characteristics [Output IP2, Stability, Noise Figure]

Table 11. Wideband OIP2 [Tcase = 25°C, Pout = -10dBm/Tone]

F1 (MHz)	F2 (MHz)	IMD_2- (MHz)	IMD_2+ (MHz)	IMD_2- (dBm)	OIP_2- (dBm)	IMD_2+ (dBm)	OIP_2+ (dBm)
700	1720	1020	2420	-70.1	**50.1**	-70.7	**50.7**
700	1950	1250	2650	-69.9	**49.9**	-70.8	**50.8**
700	2650	1950	3350	-71.1	**51.1**	-72.9	**52.9**
824	900	----	1724	----	----	-71.2	**51.2**
900	1720	820	2620	-69.7	**49.7**	-71.4	**51.4**
1755	2600	845	4355	-67.8	**47.8**	-76.2	**56.2**
1900	2600	700	4500	-67.7	**47.7**	-75.7	**55.7**

Table 12. Wideband OIP2 [Tcase = 25°C, Pout = 0dBm/Tone]

F1 (MHz)	F2 (MHz)	IMD_2- (MHz)	IMD_2+ (MHz)	IMD_2- (dBm)	OIP_2- (dBm)	IMD_2+ (dBm)	OIP_2+ (dBm)
700	1720	1020	2420	-49.7	**49.7**	-50.5	**50.5**
700	1950	1250	2650	-49.8	**49.8**	-50.6	**50.6**
700	2650	1950	3350	-50.7	**50.7**	-53.1	**53.1**
824	900	----	1724	----	----	-50.7	**50.7**
900	1720	820	2620	-49.5	**49.5**	-51.2	**51.2**
1755	2600	845	4355	-47.4	**47.4**	-57.2	**57.2**
1900	2600	700	4500	-47.2	**47.2**	-56.8	**56.8**

Figure 15. Stability Versus Temperature and Voltage [DSA1 = 0dB]

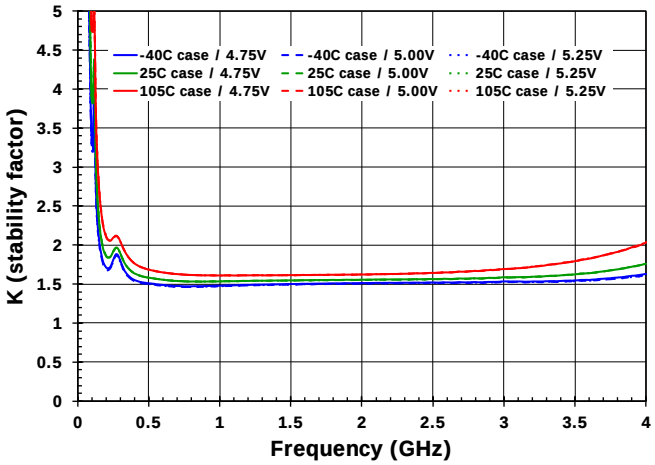


Figure 16. Stability Versus DSA1 Attenuation

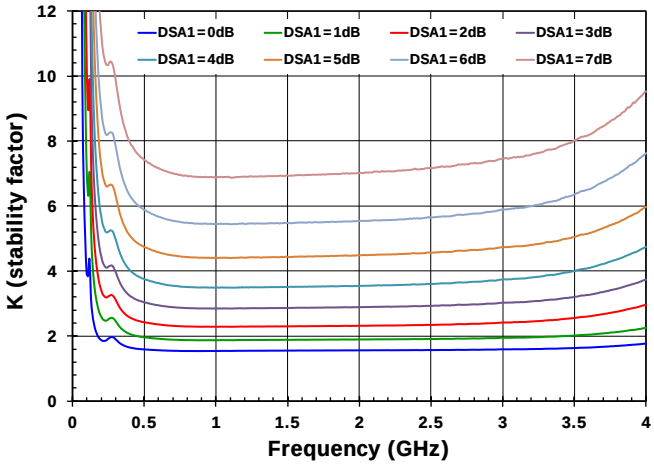


Figure 17. Noise Figure versus Voltage and Temperature

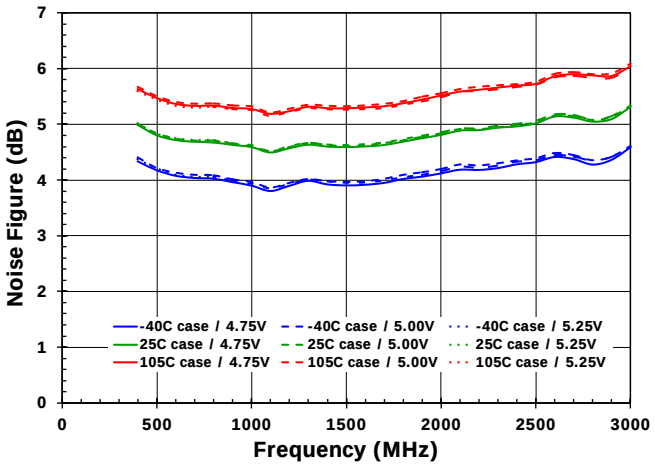
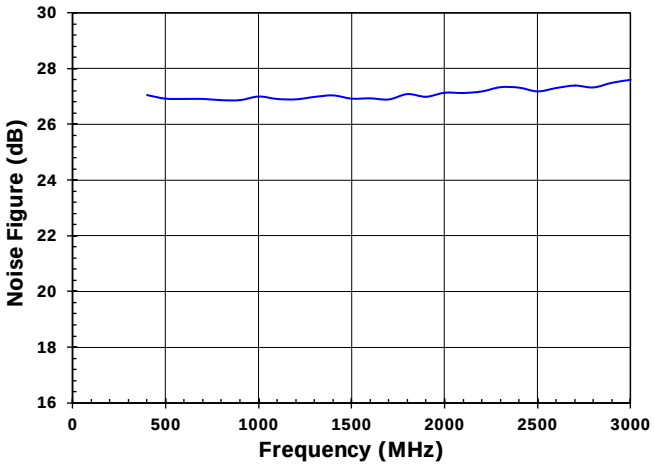


Figure 18. Noise Figure with DSA1 = 22dB



Typical Performance Characteristics [Gain, S-Parameters, Phase Change]

Figure 19. Maximum Gain [S21, DSA0 = 0dB, DSA1 = 0dB, DSA2 = 0dB]

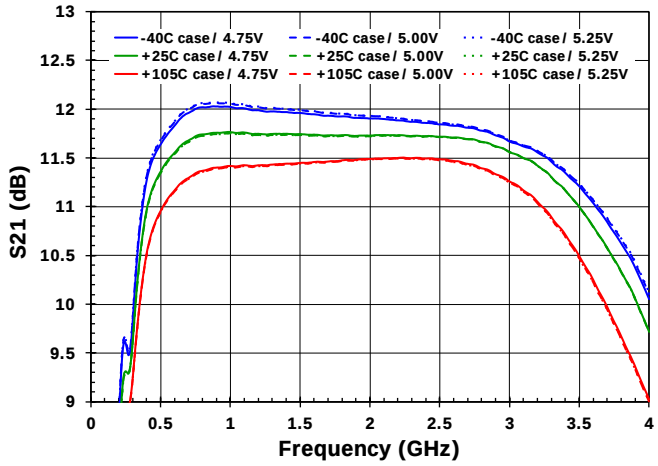


Figure 20. S21 [DSA0 = 0dB, DSA1 varied, DSA2 = 0dB]

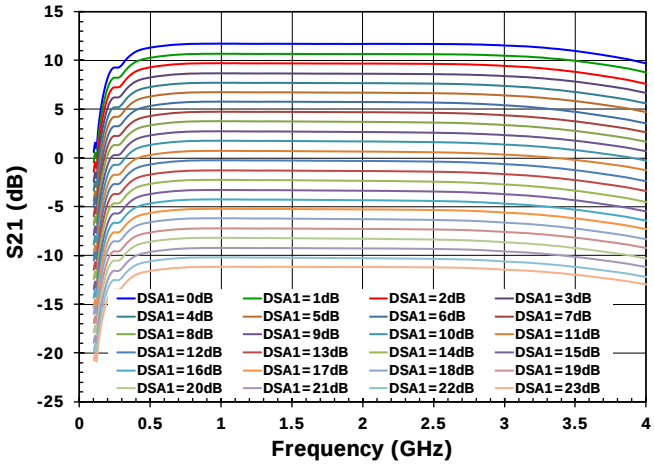


Figure 21. S11 [DSA0 = 0dB, DSA1 varied, DSA2 = 0dB]

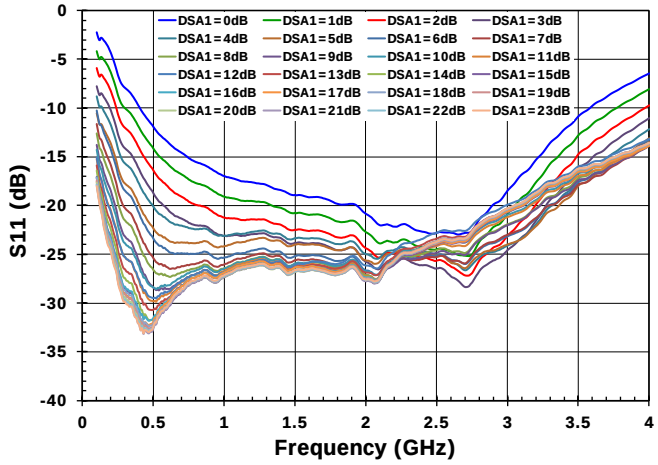


Figure 22. S22 [DSA0 = 0dB, DSA1 varied, DSA = 0dB]

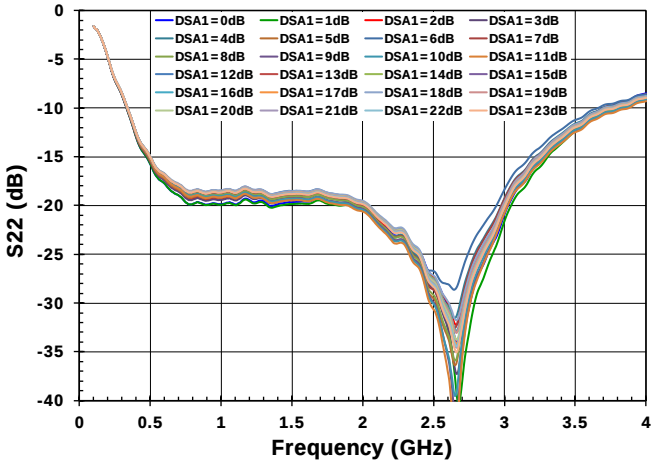


Figure 23. S12 [DSA0 = 0dB, DSA1 varied, DSA2 = 0dB]

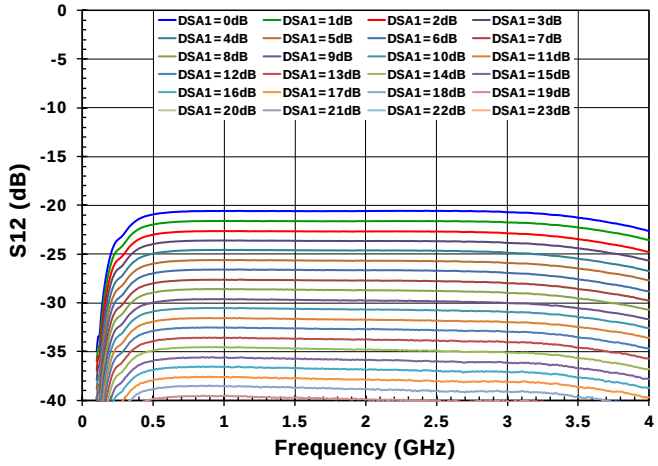
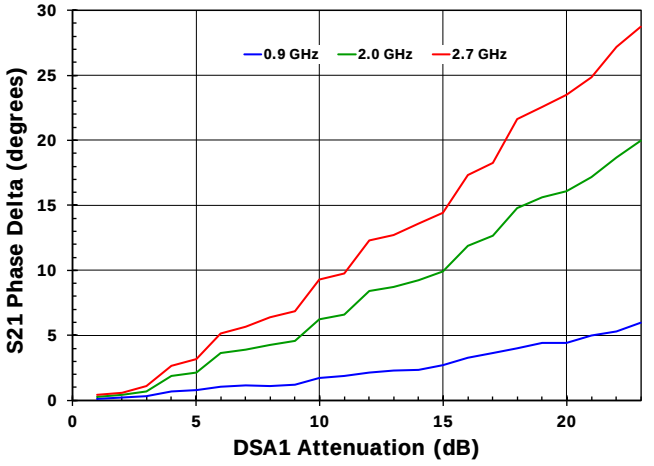


Figure 24. Phase Change as DSA1 varied [DSA0 = 0dB, DSA2 = 0dB]



Typical Performance [DSA1 Errors, S-parameters with varied DSA2]

Figure 25. DSA1 Absolute Attenuation Error [DSA0 = 0dB, DSA2 = 0dB]

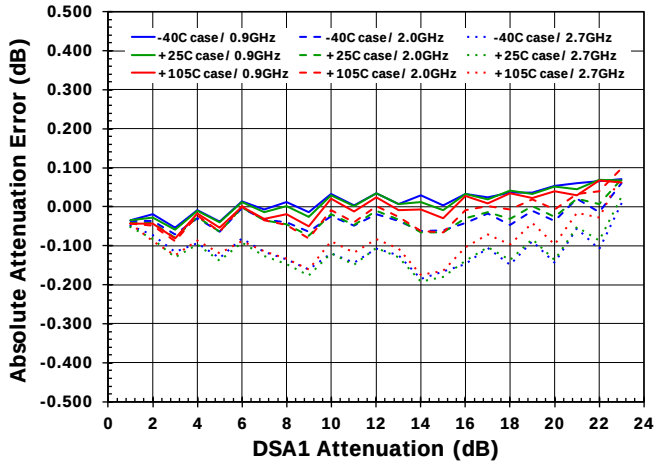


Figure 26. DSA1 Attenuator Step Error [DSA0 = 0dB, DSA2 = 0dB]

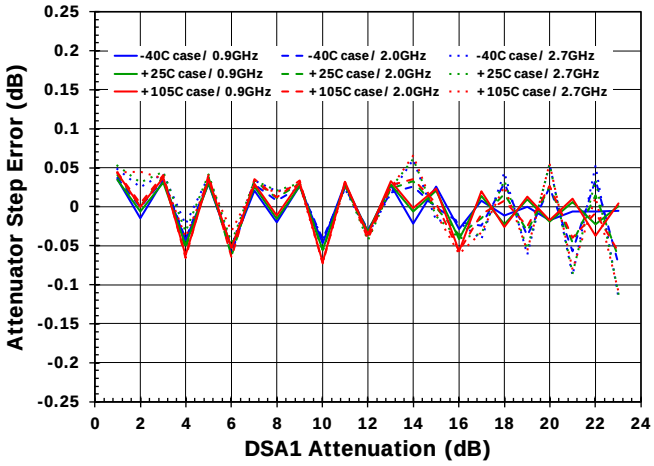


Figure 27. S21 [DSA0 = 0dB, DSA1 = 0dB, DSA2 varied]

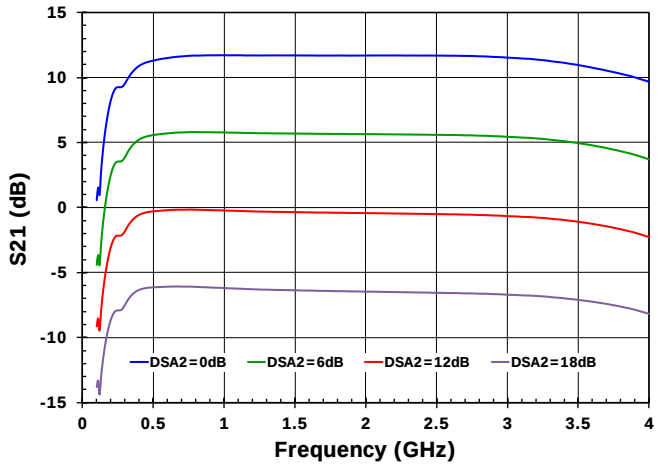


Figure 28. S12 [DSA0 = 0dB, DSA1 =0dB, DSA2 varied]

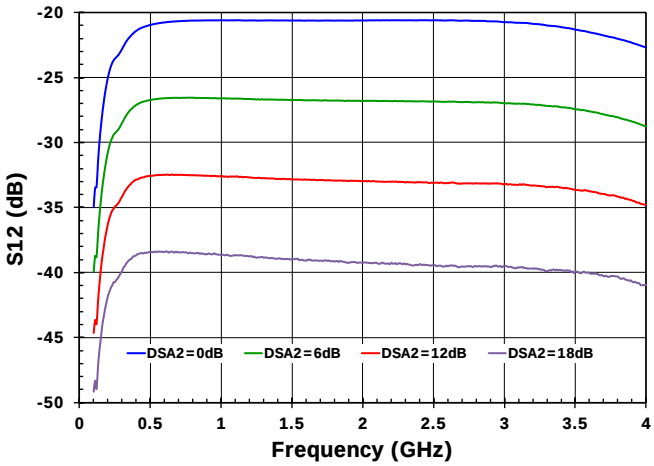


Figure 29. S11 [DSA0 = 0dB, DSA1 = 0dB, DSA2 varied]

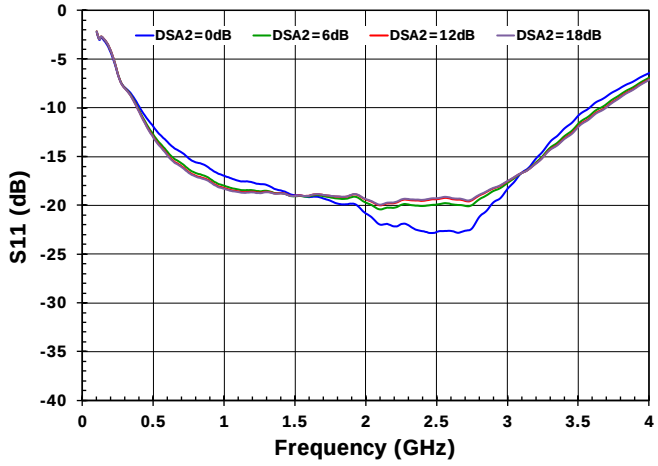
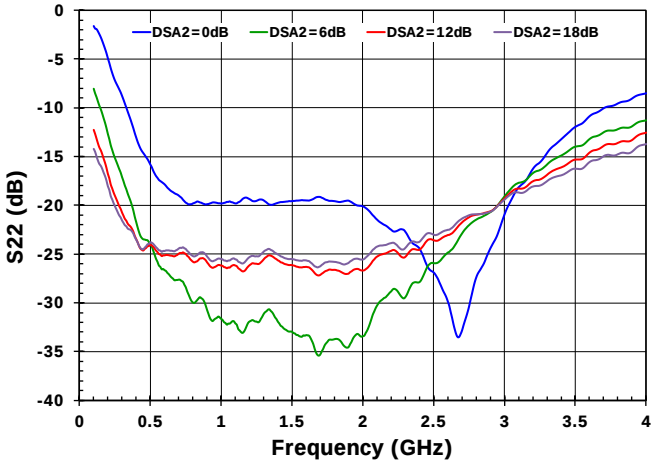


Figure 30. S22 [DSA0 = 0dB, DSA1 = 0dB, DSA2 varied]



Typical Performance [Phase vs. DSA2, DSA2 Errors, S-Param. vs. DSA0]

Figure 31. Phase Change as DSA2 varied [DSA0 = 0dB, DSA1 = 0dB]

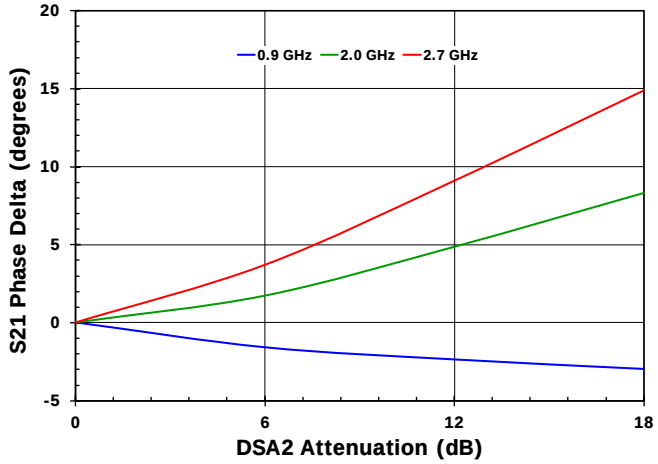


Figure 32. DSA2 Absolute Attenuation Error [DSA0 = 0dB, DSA1 = 0dB]

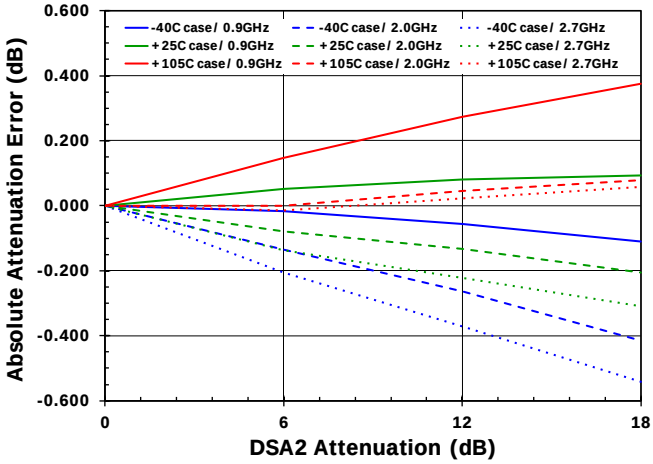


Figure 33. DSA2 Attenuator Step Error [DSA0 = 0dB, DSA1 = 0dB]

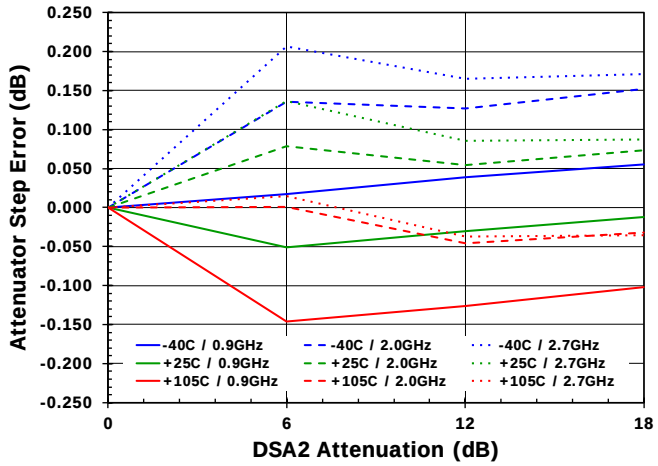


Figure 34. S21 [DSA0 = 0, 6dB, DSA1 = 0dB, DSA2 = 0dB]

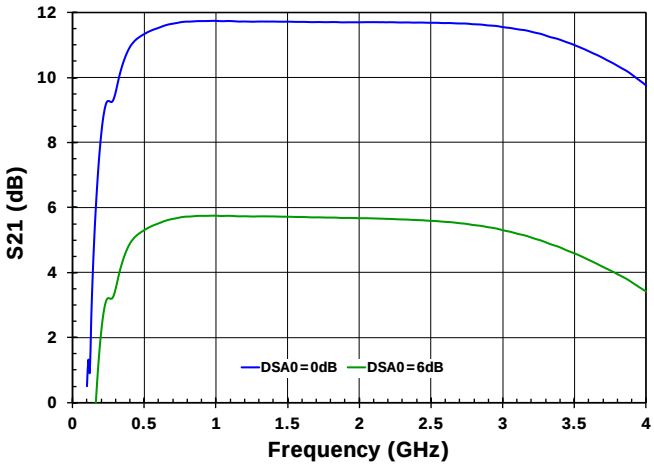


Figure 35. S12 [DSA0 = 0, 6dB, DSA1 = 0dB, DSA2 = 0dB]

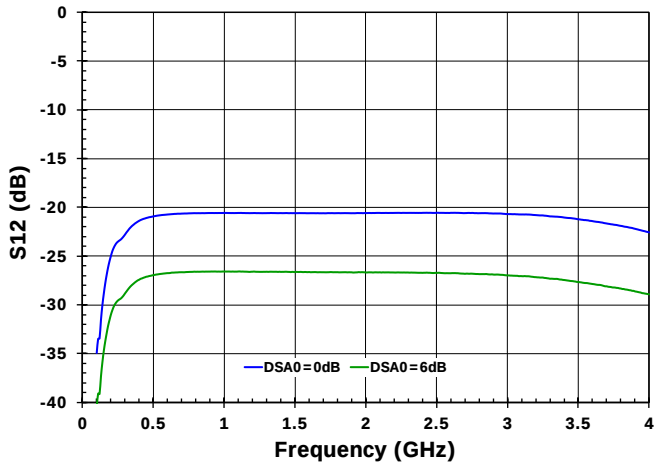
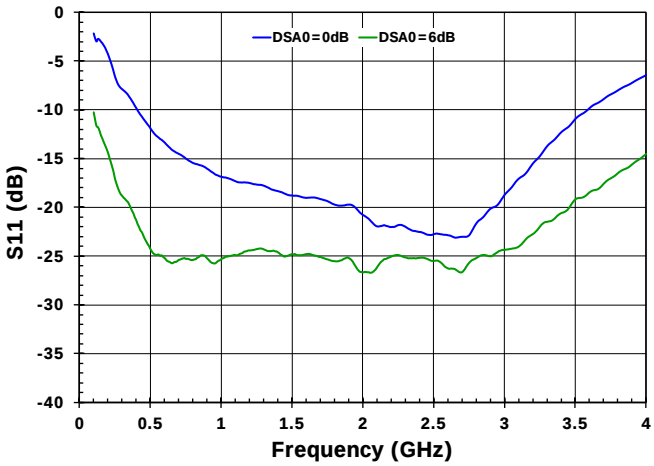


Figure 36. S11 [DSA0 = 0, 6dB, DSA1 = 0dB, DSA2 = 0dB]



Typical Performance [S22 versus DSA0, OIP3 with Swept Pout]

Figure 37. S22 [DSA0 = 0, 6dB, DSA1 = 0dB, DSA2 = 0dB]

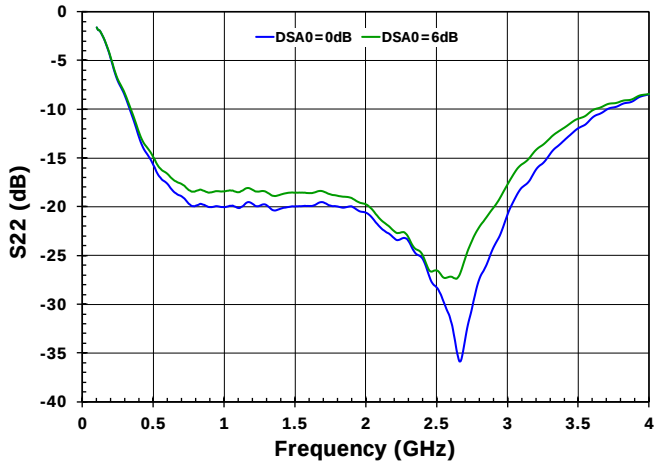


Figure 38. Output IP3 with Swept Pout [DSA0 = 0 dB]

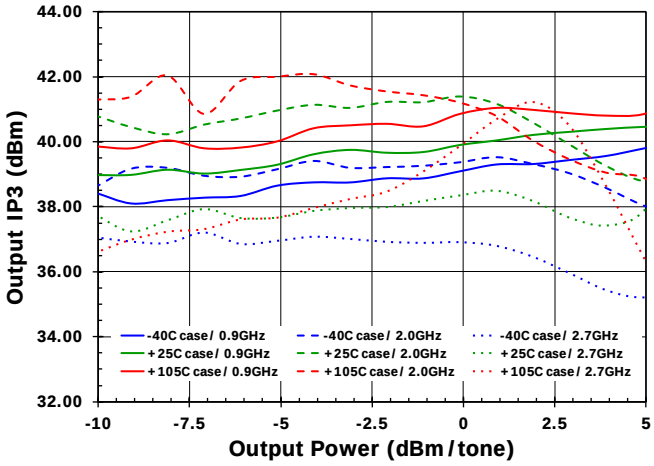


Figure 39. Output IP3 with Swept Pout [DSA0 = 6dB]

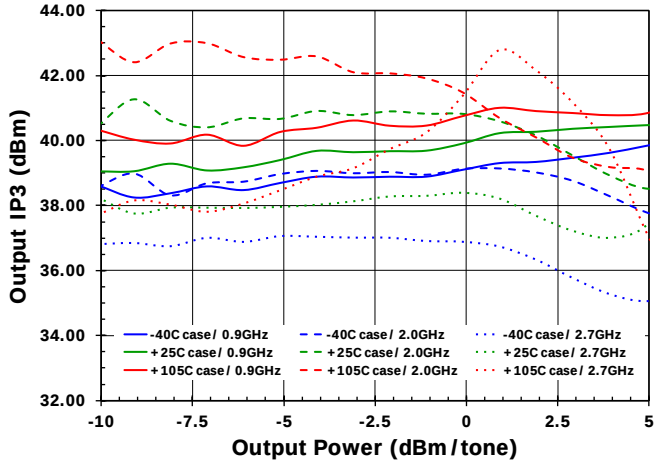
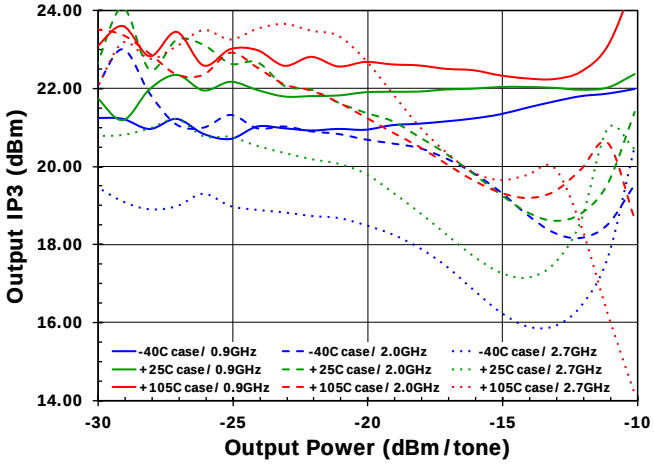


Figure 40. Output IP3 with Swept Pout [DSA2 = 18 dB]



Typical Performance [Low frequency Performance]

Figure 41. LB Output IP3 for Pout = 0dBm/tone

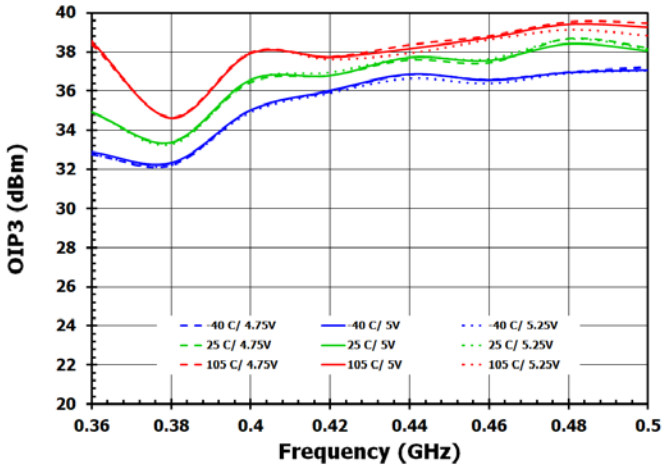


Figure 42. LB Output IP3 for Pout =-10dBm/tone

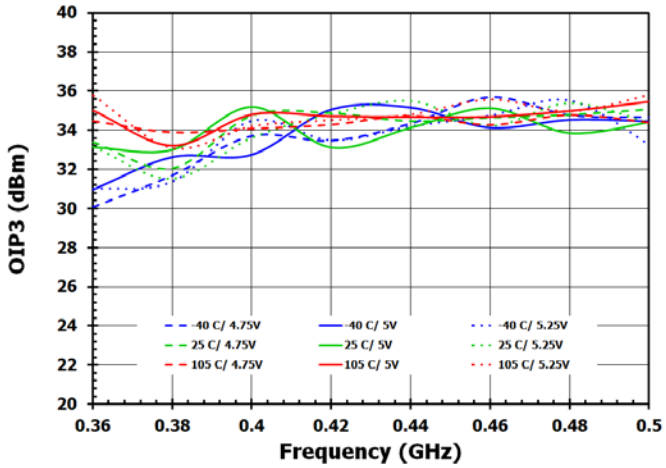


Figure 43. LB Output IP3 for DSA0 = 6dB, DSA1 = 0dB, DSA2 = 0dB, and Pout = 0dBm/tone

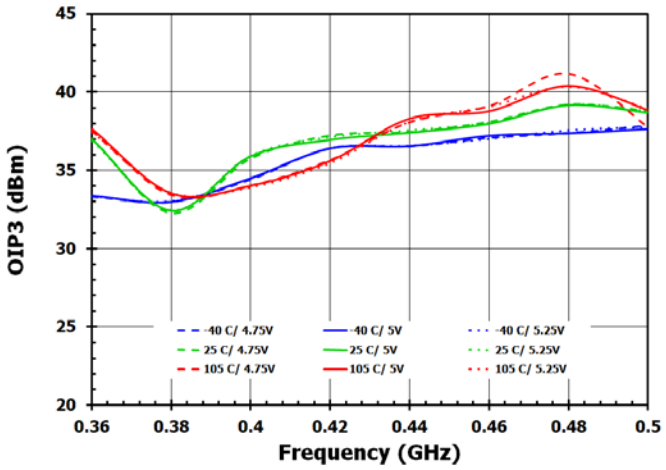


Figure 44. LB Output IP3 for DSA0 = 0dB, DSA1 = 0dB, DSA2 = 18dB, and Pout =-18dBm/tone

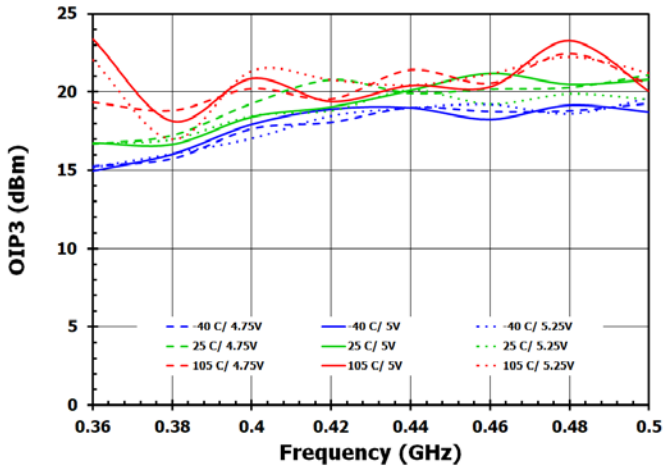


Figure 45. LB Output IP3 Versus Tone Spacing

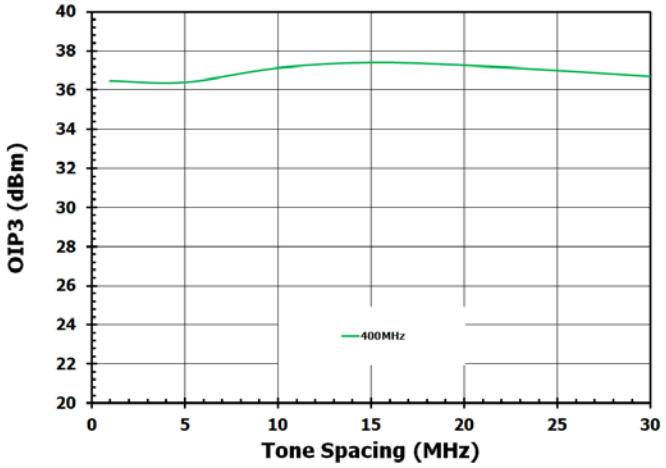
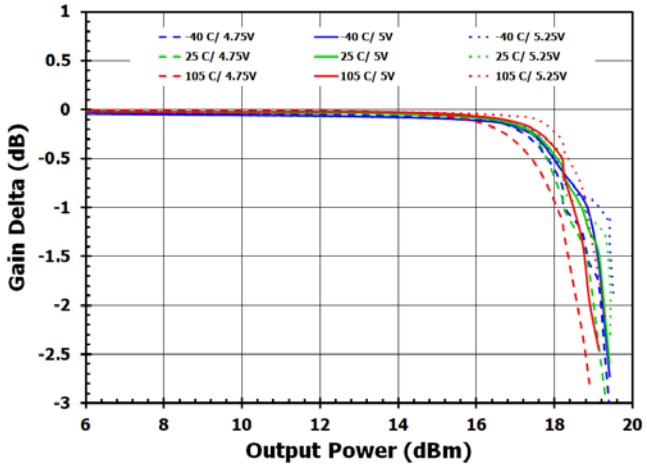


Figure 46. Gain Compression [400MHz]



Programming

Serial Control Mode

Figure 47. Serial Register Timing Diagram (LSB-FIRST)

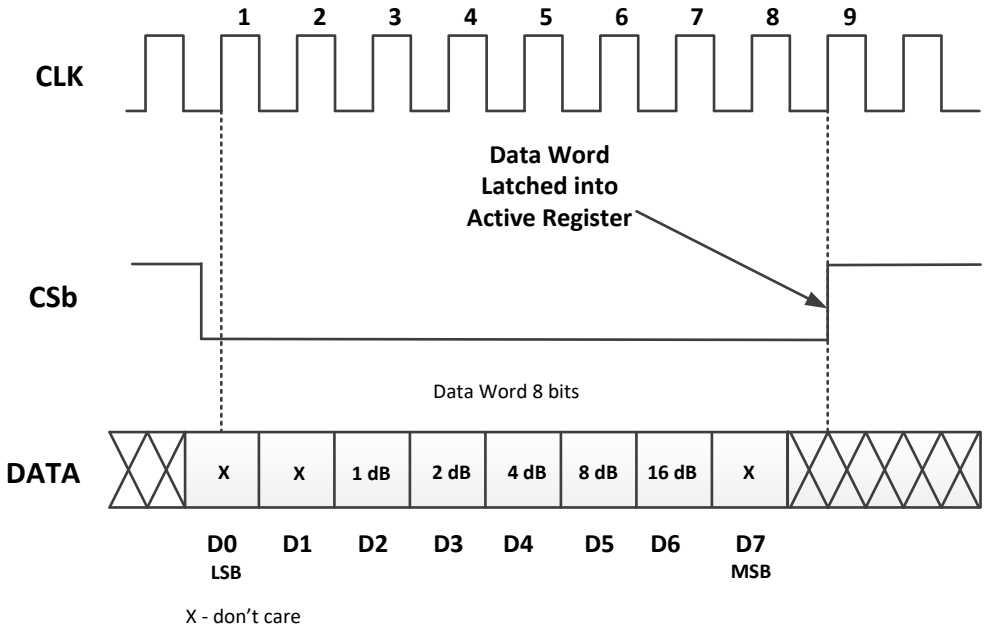


Table 13. DSA1 Serial Mode Default Condition

When the device is first powered up, DS1 will default to the Maximum Attenuation setting as shown.

Default Register Setting

x	x	1	1	1	1	1	x
D0 LSB	D1	D2	D3	D4	D5	D6	D7 MSB

Note – *F0440 includes a CLK inhibit feature designed to minimize sensitivity to CLK bus noise when the device is not being programmed. When CSb is high (> V_{IH}), the CLK input is disabled and serial data (DATA) is not clocked into the shift register. It is recommended that CSb be pulled high (>V_{IH}) when the device is not being programmed.*

Table 14. DSA1 Attenuation Word Truth Table (LSB = first in)

Don't Care	Attenuation Word					Don't Care		Attenuation Setting
D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)	
x	Low	Low	Low	Low	Low	x	x	0dB
x	Low	Low	Low	Low	High	x	x	1dB
x	Low	Low	Low	High	Low	x	x	2dB
x	Low	Low	High	Low	Low	x	x	4dB
x	Low	High	Low	Low	Low	x	x	8dB
x	High	Low	Low	Low	Low	x	x	16dB
x	High	Low	High	High	Low	x	x	22dB
x	High	Low	High	High	High	x	x	23dB (max)
x	High	High	Low	Low	Low	x	x	23dB (max)
x	High	High	Low	Low	High	x	x	23dB (max)
x	High	High	Low	High	Low	x	x	23dB (max)
x	High	High	Low	High	High	x	x	23dB (max)
x	High	High	High	Low	Low	x	x	23dB (max)
x	High	High	High	Low	High	x	x	23dB (max)
x	High	High	High	High	Low	x	x	23dB (max)
x	High	High	High	High	High	x	x	23dB (max)

Table 15. DSA0 Attenuator Truth Table

VCTRL0_A, VCTRL0_B	Attenuation Setting (DB)
0	0 (Reference IL)
1	6

Table 16. DSA2 Truth Table

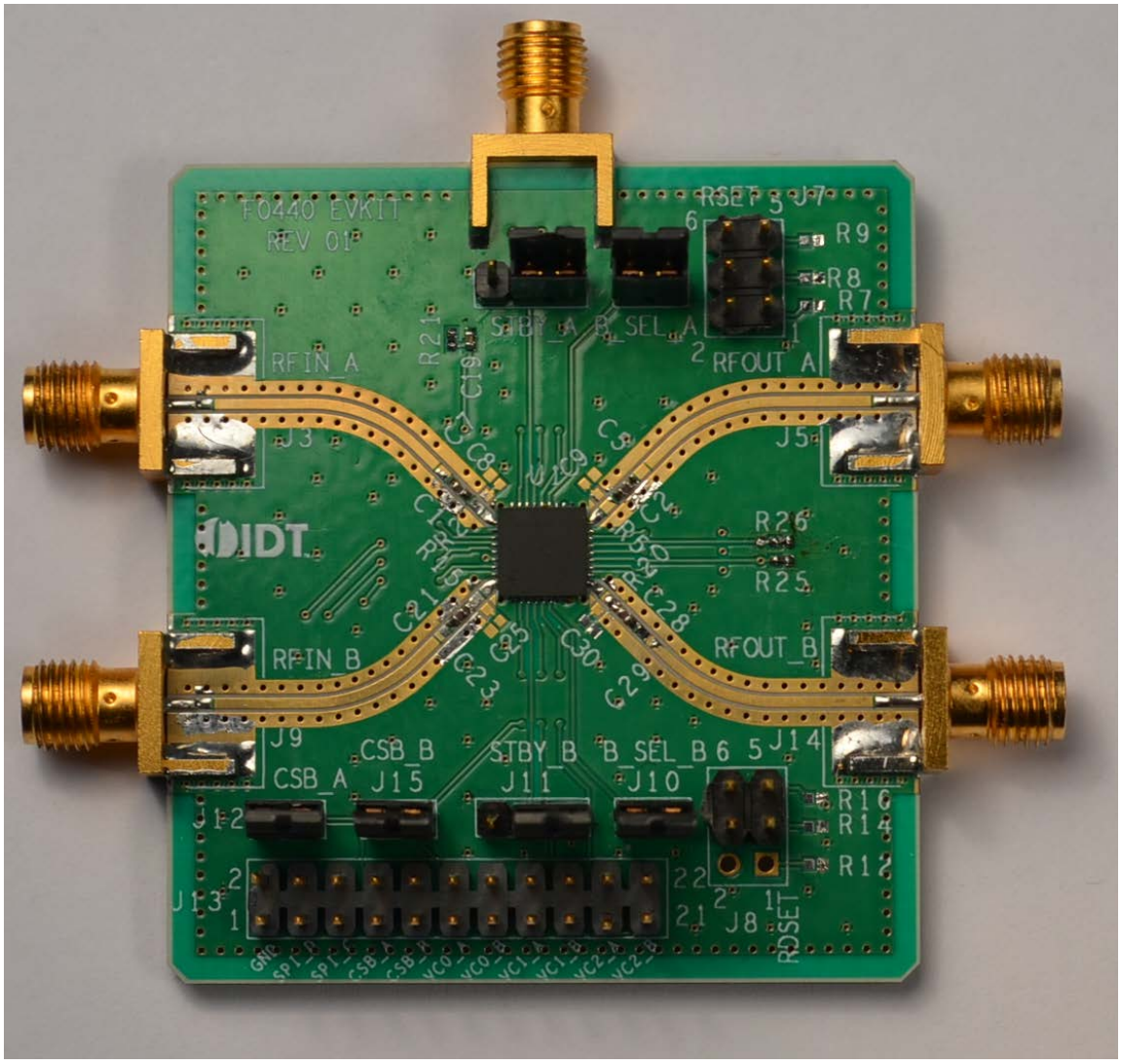
VCTRL1_A, VCTRL1_B	VCTRL2_A, VCTRL2_B	Attenuation Setting G (DB)
0	0	0 (Reference IL)
1 (NC)	0	6
0	1 (NC)	12
1 (NC)	1 (NC)	18

Table 17. Standby Truth Table

Parameter	Logic Level	Function
STBY	Low or NC	Power On
	High	Power Off

Evaluation Kit Picture

Figure 48. Top View



Evaluation Kit / Applications Circuit

Figure 49. Schematic

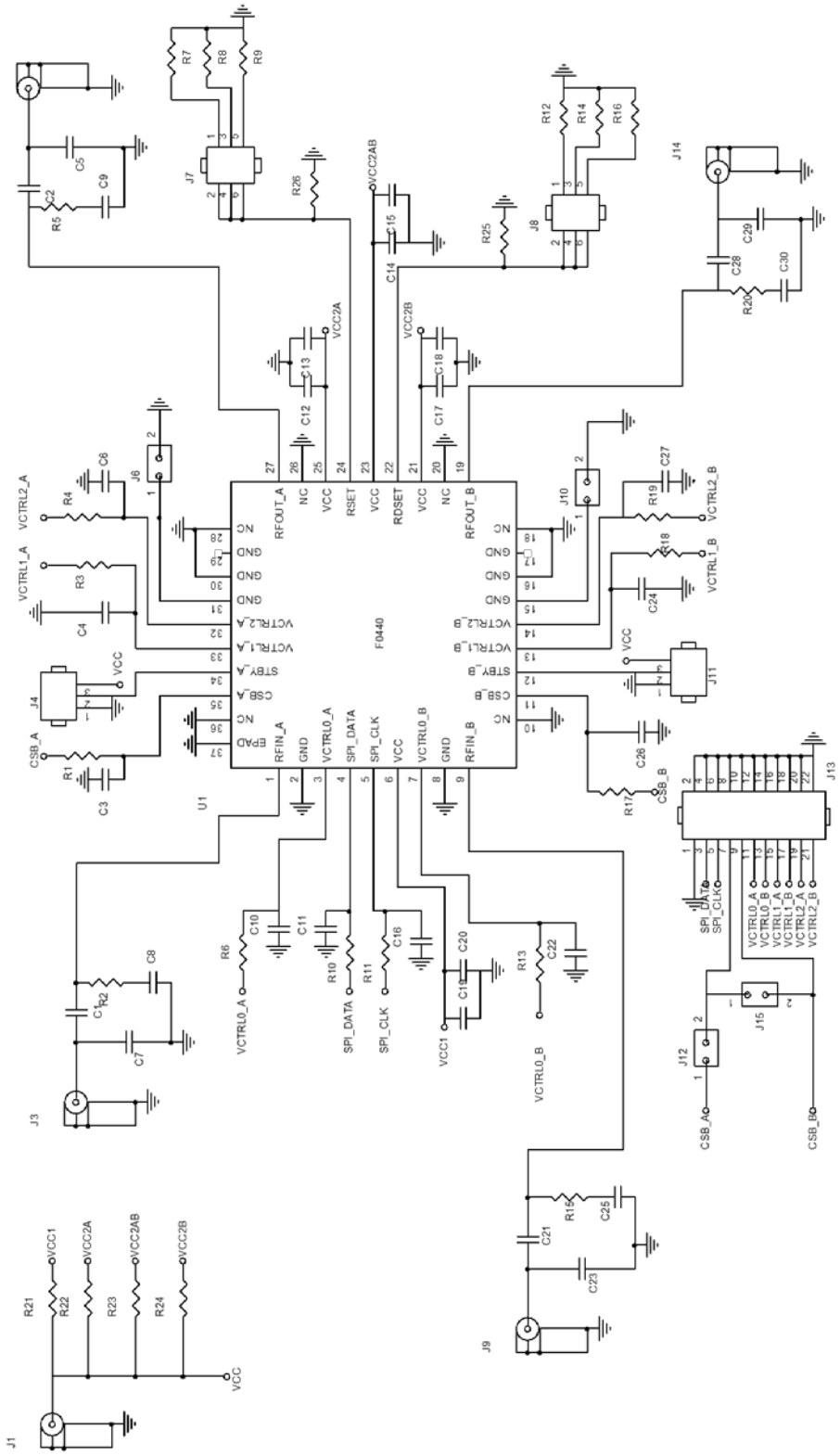


Table 18. Bill of Material (BOM)

Part Reference	QTY	Description	Mfr. Part #	Mfr.
C1, C2, C21, C28	4	47pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H470J	Murata
C3, C4, C6, C10, C11, C16, C22, C24, C26, C27	10	2pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H2R0B	Murata
C12, C14, C17, C20	4	1000pF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM1555C1H102J	Murata
C13, C15, C18, C19	4	0.1uF ±10%, 16V, X7R Ceramic Capacitor (0402)	GRM155R71C104K	Murata
R1, R3, R4, R6, R10, R11, R13, R17, R18, R19	10	5.11kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF5111X	Panasonic
R21, R22, R23, R24	4	0Ω Resistors (0402)	ERJ-2GE0R00X	Panasonic
R25	1	6.04kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF6041X	Panasonic
R26	1	2.37kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2371X	Panasonic
J1, J3, J5, J9, J14	5	Edge Launch SMA (0.375 inch pitch ground tabs)	142-0701-851	Emerson Johnson
J4, J11	2	CONN HEADER VERT SGL 3 X 1 POS GOLD, Mount jumpers to GND	961103-6404-AR	3M
J6, J10, J12, J15	4	CONN HEADER VERT SGL 2 X 1 POS GOLD Mount jumpers	961102-6404-AR	3M
J7, J8	2	DNP	67997-106HLF	FCI
J13	1	CONN HEADER VERT SGL 11 X 2 POS GOLD	67997-122HLF	FCI
C5, C7, C8, C9, C23, C25, C29, C30, R2, R5, R15, R20, R7, R8, R9, R12, R14, R16		DNP		
U1	1	DVGA	F0440NGBI	IDT
	1	Printed Circuit Board	F0440 EVKIT REV 01	IDT
	1	PCB Schematic (Rev 01)		IDT

Applications Information

F0440 has been optimized for use in high performance RF applications from 400MHz to 2700MHz.

Power Supplies

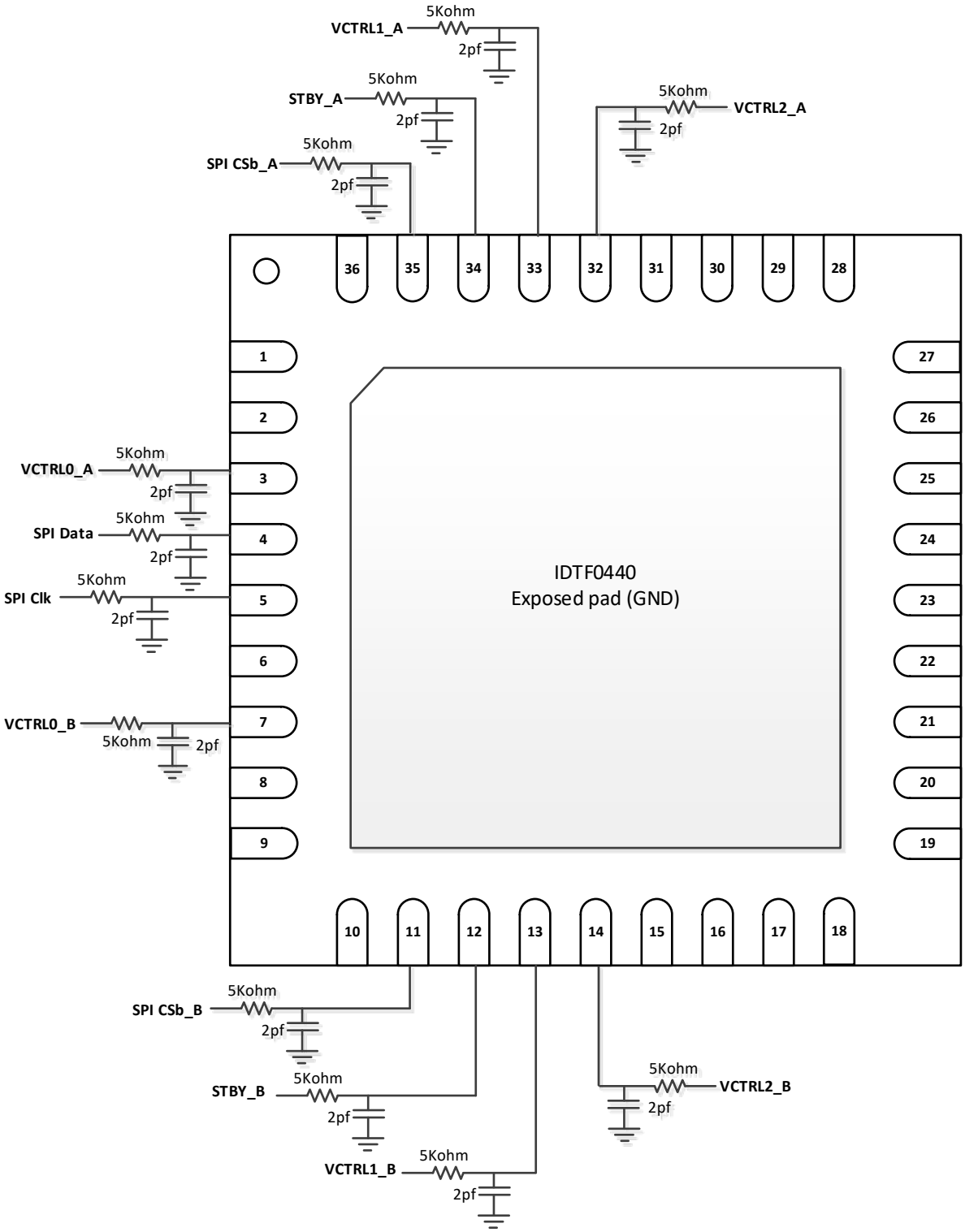
A common VCC power supply should be used for all pins requiring DC power. All supply pins should be bypassed with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figure and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µS. In addition, all control pins should remain at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

GND Jumpers

Jumpers J6 and J10 must be grounded (header in place) for optimum RF performance.

Figure 50. Control Pin Interface

If control signal integrity is a concern and clean signals cannot be guaranteed due to overshoot, undershoot, ringing, etc., the following circuit at the input of each control pin is recommended. This applies to all SPI and control pins as shown below. Note the recommended resistor and capacitor values do not necessarily match the EV kit BOM for the case of poor control signal integrity.



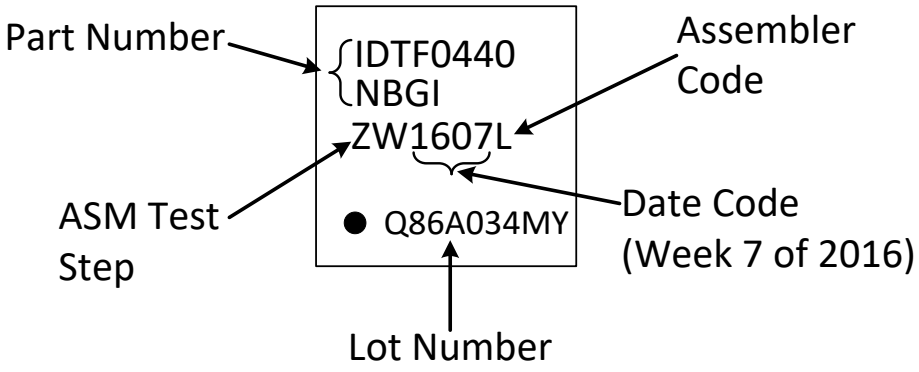
Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

Ordering Information

Orderable Part Number	Package	MSL Rating	Shipping Packaging	Temperature
F0440NBGI	6 × 6 × 0.75 mm 36-TQFN	1	Tray	-40° to +105°C
F0440NBGI8	6 × 6 × 0.75 mm 36-TQFN	1	Tape and Reel	-40° to +105°C
F0440EVBI	Evaluation Board	-	-	-

Marking Diagram

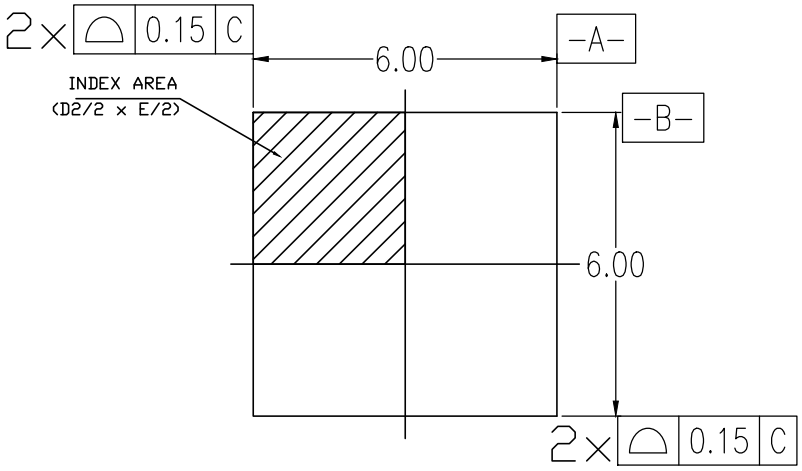


Revision History

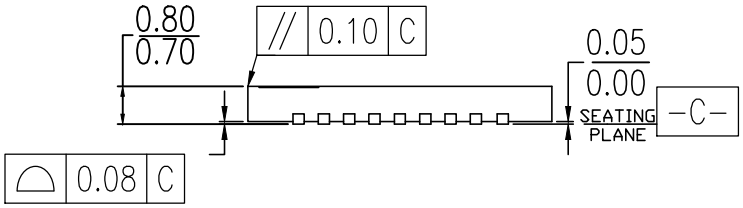
Revision Date	Description of Change
November 4, 2021	▪ Updated Package Outline Drawings section and added POD links in the Ordering Information table. ▪ Added Low Band Plots; updated operating range down to 400MHz.
August 13, 2020	Added Spec Table at 450MHz.
May 13, 2020	Rebranded datasheet.
July 27, 2016	First release (Rev O) of the F0440 datasheet.

36-VFQFPN, Package Outline Drawing

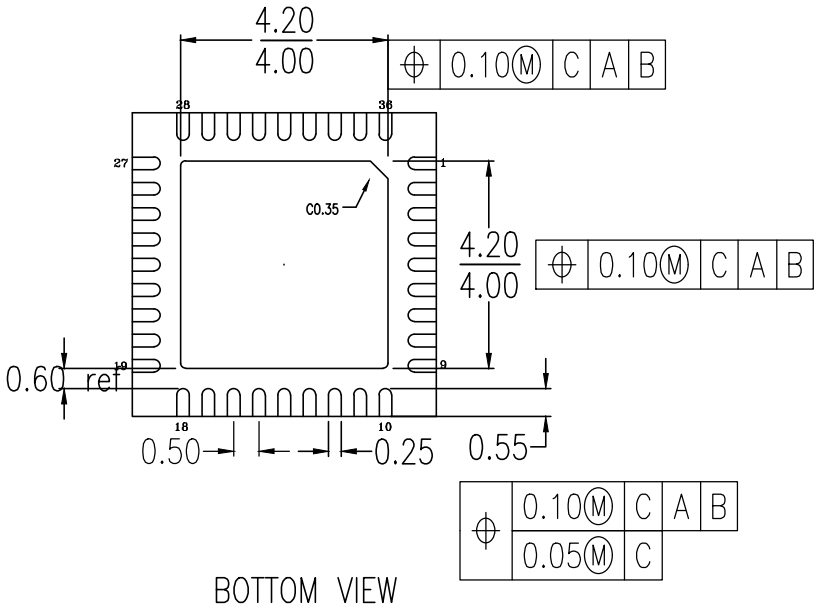
6.00 x 6.00 x 0.75 mm Body, 4.10 x 4.10 mm Epad, 0.5mm Pitch



TOP VIEW



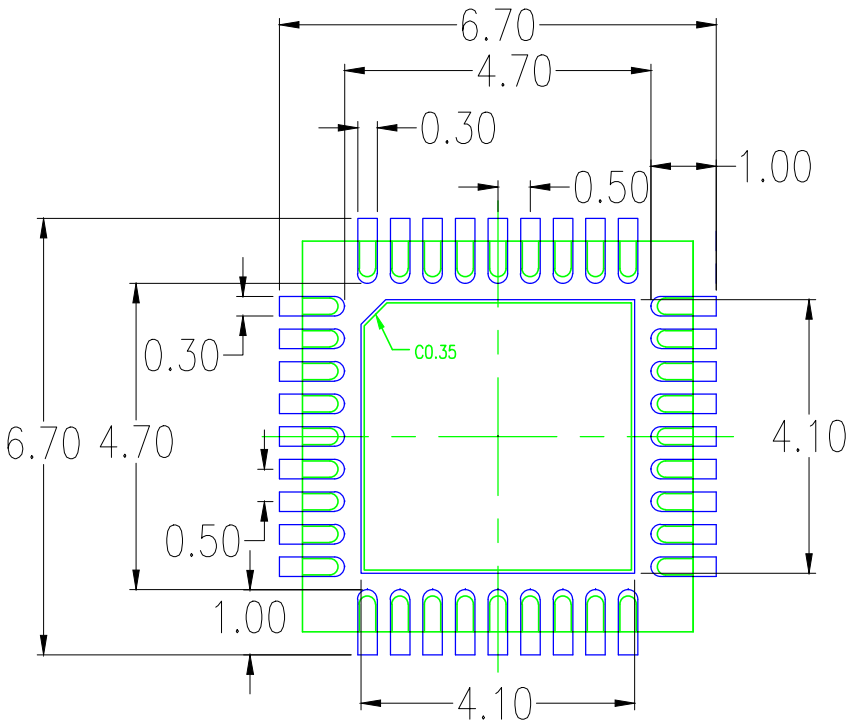
SIDE VIEW



BOTTOM VIEW

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M–1982
2. ALL DIMENSIONS ARE IN MILLIMETERS.



RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSION ARE IN mm. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Nov 8, 2021	01	Update IDT format to Renesas format
Apr 6, 2016	00	Initial Release

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