

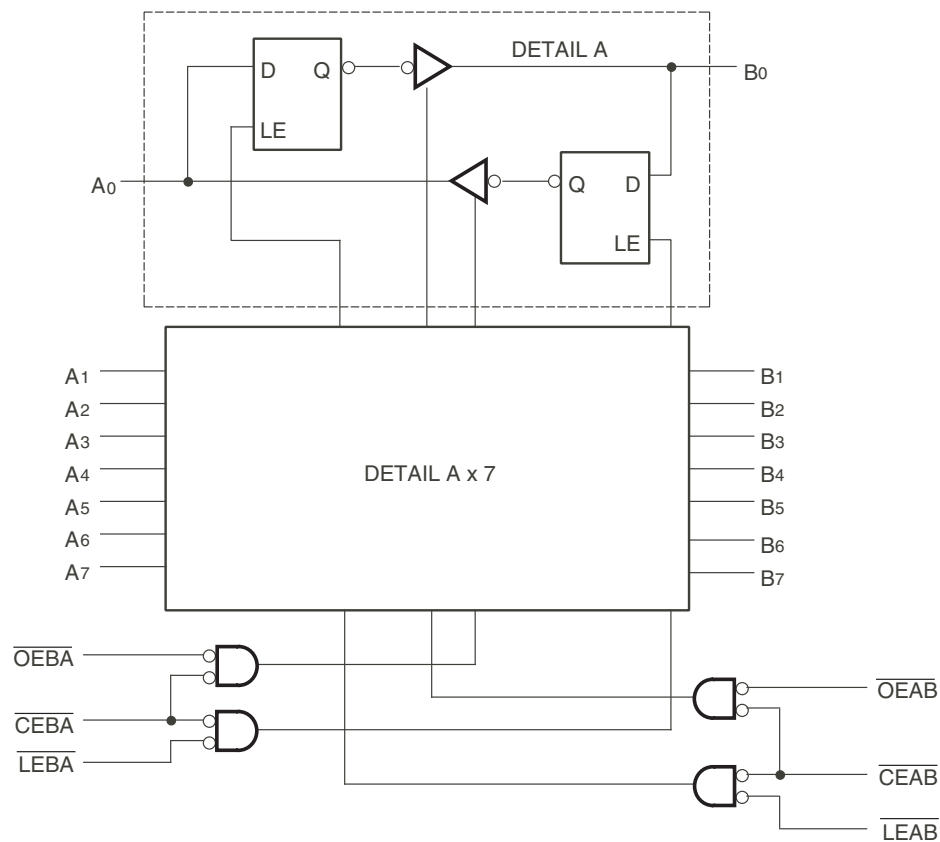
FEATURES:

- A and C grades
- Low input and output leakage  $\leq 1\mu\text{A}$  (max.)
- CMOS power levels
- True TTL input and output compatibility:
  - $V_{OH} = 3.3V$  (typ.)
  - $V_{OL} = 0.3V$  (typ.)
- High Drive outputs (-15mA  $I_{OH}$ , 64mA  $I_{OL}$ )
- Meets or exceeds JEDEC standard 18 specifications
- Power off disable outputs permit "live insertion"
- Available in SOIC and QSOP packages

DESCRIPTION:

The FCT543T is a non-inverting octal transceiver built using an advanced dual metal CMOS technology. This device contains two sets of eight D-type latches with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ( $\overline{\text{CEAB}}$ ) input must be low in order to enter data from A0–A7 or to take data from B0–B7, as indicated in the Function Table. With  $\overline{\text{CEAB}}$  low, a low signal on the A-to-B Latch Enable ( $\overline{\text{LEAB}}$ ) input makes the A-to-B latches transparent; a subsequent low-to-high transition of the  $\overline{\text{LEAB}}$  signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With  $\overline{\text{CEAB}}$  and  $\overline{\text{OEAB}}$  both low, the 3-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses the  $\overline{\text{CEBA}}$ ,  $\overline{\text{LEBA}}$  and  $\overline{\text{OEBA}}$  inputs.

FUNCTIONAL BLOCK DIAGRAM



INDUSTRIAL TEMPERATURE RANGE

## PIN CONFIGURATION



TOP VIEW

Package Type	Package Code	Order Code
QSOP	PCG24	QG
SOIC	PSG24	SOG

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Symbol	Description	Max	Unit
VTERM <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +7	V
VTERM <sup>(3)</sup>	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5	V
TSTG	Storage Temperature	-65 to +150	°C
IOUT	DC Output Current	-60 to +120	mA

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed VCC by +0.5V unless otherwise noted.
- Inputs and VCC terminals only.
- Output and I/O terminals only.

## CAPACITANCE (TA = +25°C, F = 1.0MHz)

Symbol	Parameter <sup>(1)</sup>	Conditions	Typ.	Max.	Unit
CIN	Input Capacitance	VIN = 0V	6	10	pF
COUT	Output Capacitance	VOU = 0V	8	12	pF

### NOTE:

- This parameter is measured at characterization but not tested.

## PIN DESCRIPTION

Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A0-A7	A-to-B Data Inputs or B-to-A 3-State Outputs
B0-B7	B-to-A Data Inputs or A-to-B 3-State Outputs

FUNCTION TABLE<sup>(1, 2)</sup>

For A-to-B (Symmetric with B-to-A)

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A-to-B	Bo-B7
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous* A Inputs

## NOTES:

- \* Before LEAB LOW-to-HIGH Transition  
H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Don't Care
- A-to-B data flow shown; B-to-A flow control is the same, except using  $\overline{CEBA}$ ,  $\overline{LEBA}$  and  $\overline{OEBA}$ .

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5.0\text{V} \pm 5\%$ 

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{IH}$	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
$V_{IL}$	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
$I_{IH}$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{IL}$	Input LOW Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZH}$	High Impedance Output Current (3-State output pins) <sup>(4)</sup>	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	$\pm 1$	$\mu\text{A}$
$I_{OZL}$			$V_O = 0.5\text{V}$	—	—	$\pm 1$	
$I_I$	Input HIGH Current <sup>(4)</sup>	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	$\pm 1$	$\mu\text{A}$
$V_{IK}$	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
$V_H$	Input Hysteresis	—		—	200	—	mV
$I_{CC}$	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	0.01	1	mA

## OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$V_{OH}$	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -8\text{mA}$	2.4	3.3	—	V
			$I_{OH} = -15\text{mA}$	2	3	—	
$V_{OL}$	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 64\text{mA}$	—	0.3	0.55	V
$I_{OS}$	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-225	mA
$I_{OFF}$	Input/Output Power Off Leakage <sup>(5)</sup>	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$		—	—	$\pm 1$	$\mu\text{A}$

## NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0\text{V}$ ,  $+25^\circ\text{C}$  ambient.
- Not more than one output should be tested at one time. Duration of the test should not exceed one second.
- The test limit for this parameter is  $\pm 5\mu\text{A}$  at  $T_A = -55^\circ\text{C}$ .
- This parameter is guaranteed but not tested.

## POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions <sup>(1)</sup>		Min.	Typ. <sup>(2)</sup>	Max.	Unit
$\Delta I_{CC}$	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
$I_{CCD}$	Dynamic Power Supply Current <sup>(4)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/ MHz
$I_C$	Total Power Supply Current <sup>(6)</sup>	$V_{CC} = \text{Max.}$ , Outputs Open $f_{CP} = 10\text{MHz}$ ( $\overline{LEAB}$ ) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% duty cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	2	5.5	
		$V_{CC} = \text{Max.}$ , Outputs Open $f_{CP} = 10\text{MHz}$ ( $\overline{LEAB}$ ) 50% Duty Cycle $\overline{CEAB}$ and $\overline{OEAB} = \text{GND}$ $\overline{CEBA} = V_{CC}$ Eight Bits Toggling at $f_i = 2.5\text{MHz}$ 50% duty cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3.8	7.3 <sup>(5)</sup>	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	6	16.3 <sup>(5)</sup>	

## NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at  $V_{CC} = 5.0V$ ,  $+25^\circ\text{C}$  ambient.
- Per TTL driven input; ( $V_{IN} = 3.4V$ ). All other inputs at  $V_{CC}$  or  $\text{GND}$ .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of  $\Delta I_{CC}$  formula. These limits are guaranteed but not tested.
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$

$$I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$$

$I_{CC}$  = Quiescent Current

$\Delta I_{CC}$  = Power Supply Current for a TTL High Input ( $V_{IN} = 3.4V$ )

$D_H$  = Duty Cycle for TTL Inputs High

$N_I$  = Number of TTL Inputs at  $D_H$

$I_{CCD}$  = Dynamic Current caused by an Input Transition Pair (HLH or LHL)

$f_{CP}$  = Clock Frequency for Register Devices (Zero for Non-Register Devices)

$f_i$  = Output Frequency

$N_i$  = Number of Outputs at  $f_i$

All currents are in milliamps and all frequencies are in megahertz.

## SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Condition <sup>(1)</sup>	74FCT543AT		74FCT543CT		Unit
			Min. <sup>(2)</sup>	Max.	Min. <sup>(2)</sup>	Max.	
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Transparent Mode Ax to Bx or Bx to Ax	C <sub>L</sub> = 50pF R <sub>L</sub> = 500Ω	1.5	6.5	1.5	5.3	ns
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay $\overline{LEBA}$ to Ax, $\overline{LEAB}$ to Bx		1.5	8	1.5	7	ns
t <sub>PZH</sub> t <sub>PZL</sub>	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to Ax or Bx $\overline{CEBA}$ or $\overline{CEAB}$ to Ax or Bx		1.5	9	1.5	8	ns
t <sub>PHZ</sub> t <sub>PLZ</sub>	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to Ax or Bx $\overline{CEBA}$ or $\overline{CEAB}$ to Ax or Bx		1.5	7.5	1.5	6.5	ns
t <sub>SU</sub>	Set-up Time, HIGH or LOW Ax or Bx to $\overline{LEBA}$ or $\overline{LEAB}$		2	—	2	—	ns
t <sub>H</sub>	Hold Time, HIGH or LOW Ax or Bx to $\overline{LEBA}$ or $\overline{LEAB}$		2	—	2	—	ns
t <sub>w</sub>	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW		5	—	5	—	ns

**NOTES:**

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested.

TEST CIRCUITS AND WAVEFORMS



Octal Link

Test Circuits for All Outputs



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Set-Up, Hold, and Release Times



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Propagation Delay

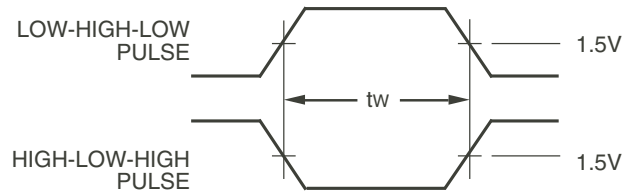
SWITCH POSITION

Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.

RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

Octal Link



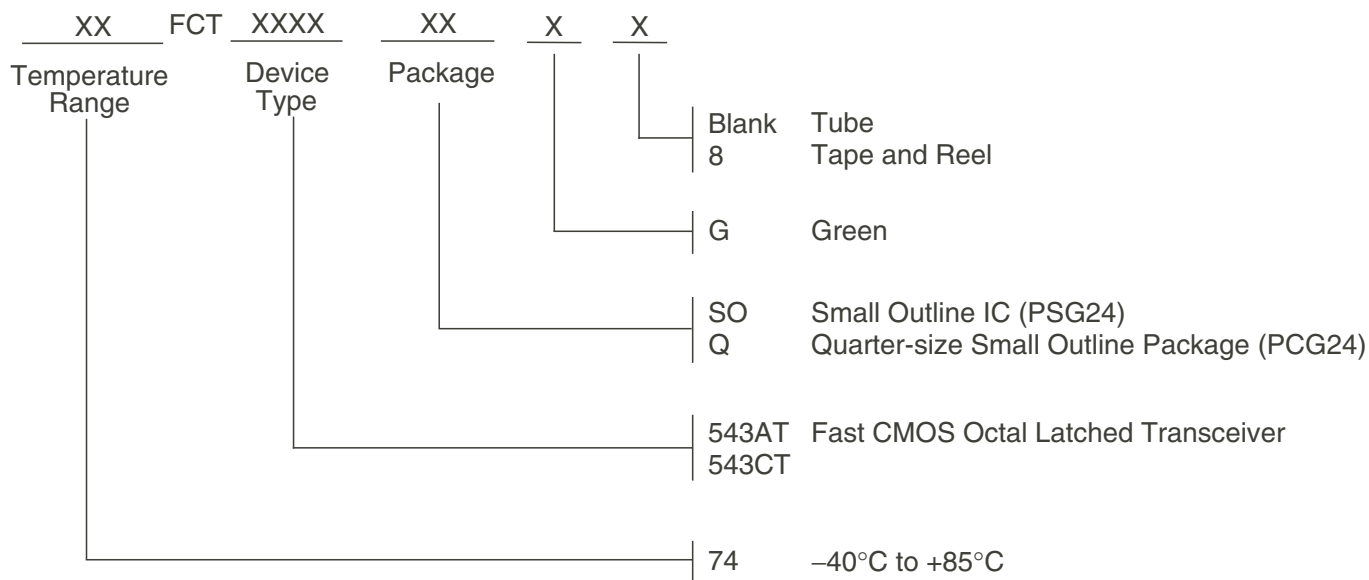
Octal Link

Enable and Disable Times

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
2. Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.

## ORDERING INFORMATION



## Orderable Part Information

Speed (ns)	Orderable Part ID	Pkg. Code	Pkg. Type	Temp. Grade
A	74FCT543ATQG	PCG24	QSOP	I
	74FCT543ATQG8	PCG24	QSOP	I
	74FCT543ATSOG	PSG24	SOIC	I
	74FCT543ATSOG8	PSG24	SOIC	I
C	74FCT543CTQG	PCG24	QSOP	I
	74FCT543CTQG8	PCG24	QSOP	I
	74FCT543CTSOG	PSG24	SOIC	I
	74FCT543CTSOG8	PSG24	SOIC	I

## Datasheet Document History

10/10/2009	Pg. 6	Updated the ordering information by removing the "IDT" notation and non RoHS part.
05/16/2018	Pgs. 2, 7	Added table under pin configuration diagram with detailed package information. Updated the ordering information diagram adding Tube, Tape and Reel. Added new table of orderable part information.
05/10/2019	Pg. 7	Updated ordering information diagram.
02/11/2020	Pgs. 1-8	Rebranded as Renesas datasheet.

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