IDT82V3011 Data Sheet Change Notice

Supplemental Information

This notice describes the differences between the updated version and its previous version of the IDT82V3011 Data Sheet. It helps readers to identify the changes when the data sheet is upgraded.

Revision History

Revision Date	PCN Number (if applicable)	Date Code	Changed Items
November 18, 2004	-	-	Item 5 to 4
October 22, 2003	-	-	Item 3 to 1

Changed Items

November 18, 2004

Item 5: Added green package option (page 1, 30)

Item 4: Changed descriptions on State Control Circuit (2nd paragraph on page 10)

Old: "When changing the operating mode, the TIE control block is enabled/disabled automatically by the state control circuit as shown in Figure - 3, except for the changes from Normal (S1) to Auto-Holdover (S2), and from Auto-Holdover (S2) and Holdover (S3) to Normal (S1). During these three changes, the TIE control block can be enabled or disabled, depending on the logic level on the TIE_en pin."

New: "When the operating mode is changed from one to another, the TIE control block is automatically disabled as shown in Figure - 3, except the changes from Holdover (S3) or Auto-Holdover (S2) to Normal (S1). In the case of changing from S3 or S2 to S1, the TIE control block is enabled or disabled by the TIE_en pin."

October 22, 2003

Item 3: **8.2 Input/Output Timing has been changed. (Page 25)**

Old:

8.2 Input/Output Timing

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t_{RW}	Reference input pulse width high or low	100			ns	8 kHz, 1.544 MHz or 2.048 MHz reference input
		5			ns	19.44 MHz reference input
t_{IRF}	Reference input rise or fall time			10	ns	
t_{R8D}	8 kHz reference input to F8o delay	0		25	ns	
t_{R15D}	1.544 MHz reference input to F8o delay	326		342	ns	
t_{R2D}	2.048 MHz reference input to F8o delay	248		264	ns	
t_{R19D}	19.44 MHz reference input to F8o delay		5		ns	
t_{FOD}	F8o to $\overline{F0o}$ delay	111		130	ns	
t_{F16S}	$\overline{F16o}$ setup to $\overline{C16o}$ falling	25		40	ns	
t_{F16H}	$\overline{F16o}$ hold to $\overline{C16o}$ falling	25		40	ns	

8.2 Input/Output Timing (Continued)

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t_{F19S}	F19o setup to C19o falling		25		ns	
t_{F19H}	F19o hold to C19o falling		25		ns	
t_{C15D}	F8o to C1.5o delay	-10		10	ns	
t_{C3D}	F8o to $\overline{C3o}$ delay	-10		10	ns	
t_{C6D}	F8o to C6o delay	-10		10	ns	
t_{C2D}	F8o to C2o	-11		5	ns	
t_{C4D}	F8o to $\overline{C4o}$	-11		5	ns	
t_{C8D}	F8o to C8o delay	-11		5	ns	
t_{C16D}	F8o to $\overline{C16o}$ delay	-11		5	ns	
t_{C19D}	F8o to C19o delay	-11		5	ns	
t_{C32D}	F8o to $\overline{C32o}$ delay	-11		5	ns	
t_{TSPD}	F8o to TSP delay	-6		10	ns	
t_{RSPD}	F8o to RSP delay	-8		8	ns	
t_{C15W}	C1.5o pulse width high or low	309		339	ns	
t_{C3W}	$\overline{C3o}$ pulse width high or low	154		169	ns	
t_{C6W}	C6o pulse width high or low	70		86	ns	
t_{C2W}	C2o pulse width high or low	232		258	ns	
t_{C4W}	$\overline{C4o}$ pulse width high or low	111		133	ns	
t_{C8W}	C8o pulse width high or low	52		70	ns	
t_{C16W}	$\overline{C16o}$ pulse width high or low	24		35	ns	
t_{C19W}	C19o pulse width high or low		25		ns	
t_{C32W}	$\overline{C32o}$ pulse width high or low	14		16.78	ns	
t_{TSPW}	TSP pulse width high	478		494	ns	
t_{RSPW}	RSP pulse width high	474		491	ns	
t_{F0WL}	$\overline{F0o}$ pulse width low	234		254	ns	
t_{F8WH}	F8o pulse width high	109		135	ns	
t_{F16WL}	$\overline{F16o}$ pulse width low	47		72	ns	
t_{F19WH}	F19o pulse width low		25		ns	
t_{0RF}	Output clock and frame pulse rise or fall time			9	ns	
t_S	Input controls setup Time	100			ns	
t_H	Input controls hold Time	100			ns	
t_{F16D}	F8o to $\overline{F16o}$ delay	24		38	ns	

8.2 Input/Output Timing (Continued)

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t_{F19D}	F8o to F19o delay		25		ns	
t_{F32D}	F8o to $\overline{F32o}$ delay	12		19	ns	
t_{F32S}	$\overline{F32o}$ setup to $\overline{C32o}$ falling	11			ns	
t_{F32H}	$\overline{F32o}$ hold to $\overline{C32o}$ falling	11			ns	
t_{F32WL}	$\overline{F32o}$ pulse width low	15		31	ns	

New:

8.2 Input/Output Timing

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t_{RW}	Reference input pulse width high or low	**51**			ns	8 kHz, 1.544 MHz or 2.048 MHz reference input
		5			ns	19.44 MHz reference input
t_{IRF}	Reference input rise or fall time			10	ns	
t_{R8D}	8 kHz reference input to F8o delay		**8**		ns	
t_{R15D}	1.544 MHz reference input to F8o delay		**332**		ns	
t_{R2D}	2.048 MHz reference input to F8o delay		**253**		ns	
t_{R19D}	19.44 MHz reference input to F8o delay		**8**		ns	
t_{F0D}	F8o to $\overline{F0o}$ delay	**118**	**121**	**124**	ns	
t_{F16S}	$\overline{F16o}$ setup to $\overline{C16o}$ falling	25		40	ns	
t_{F16H}	$\overline{F16o}$ hold to $\overline{C16o}$ falling	25		40	ns	
t_{F19S}	F19o setup to C19o falling	**20**		**35**	ns	
t_{F19H}	F19o hold to C19o falling	**20**		**35**	ns	
t_{C15D}	F8o to C1.5o delay	**-3**	**0**	**+3**	ns	
t_{C3D}	F8o to $\overline{C3o}$ delay	**-3**	**1.6**	**+3**	ns	
t_{C6D}	F8o to C6o delay	**-3**	**1.6**	**+3**	ns	
t_{C2D}	F8o to C2o	**-2**	**0**	**+2**	ns	
t_{C4D}	F8o to $\overline{C4o}$	**-2**	**0**	**+2**	ns	
t_{C8D}	F8o to C8o delay	**-2**	**0**	**+2**	ns	
t_{C16D}	F8o to $\overline{C16o}$ delay	**-2**	**0**	**+2**	ns	
t_{C19D}	F8o to C19o delay	**-8**	**0**	**8**	ns	
t_{C32D}	F8o to $\overline{C32o}$ delay	**-2**	**2**	**+2**	ns	
t_{TSPD}	F8o to TSP delay	**-3**	**0**	**+3**	ns	
t_{RSPD}	F8o to RSP delay	**-3**	**0**	**+3**	ns	
t_{C15W}	C1.5o pulse width high or low		**323**		ns	

8.2 Input/Output Timing (Continued)

Parameter	Description	Min	Typ	Max	Units	Test Conditions
t_{C3W}	$\overline{C3o}$ pulse width high or low		**161**		ns	
t_{C6W}	C6o pulse width high or low		**82**		ns	
t_{C2W}	C2o pulse width high or low		**244**		ns	
t_{C4W}	$\overline{C4o}$ pulse width high or low		**122**		ns	
t_{C8W}	C8o pulse width high or low		**61**		ns	
t_{C16W}	$\overline{C16o}$ pulse width high or low		**30.5**		ns	
t_{C19W}	C19o pulse width high or low		25		ns	
t_{C32WH}	$\overline{C32o}$ pulse width high		**14.4**		ns	
t_{TSPW}	TSP pulse width high		**486**		ns	
t_{RSPW}	RSP pulse width high		**490**		ns	
t_{F0WL}	$\overline{F0o}$ pulse width low		**243**		ns	
t_{F8WH}	F8o pulse width high		**123.6**		ns	
t_{F16WL}	$\overline{F16o}$ pulse width low		**60.9**		ns	
t_{F19WH}	F19o pulse width high		25		ns	
t_{0RF}	Output clock and frame pulse rise or fall time		**3**		ns	
t_S	Input controls setup Time	100			ns	
t_H	Input controls hold Time	100			ns	
t_{F16D}	F8o to $\overline{F16o}$ delay	**27.1**	**30.1**	**33.1**	ns	
t_{F19D}	F8o to F19o delay	**17**	25	**33**	ns	
t_{F32D}	F8o to $\overline{F32o}$ delay	12	**15.8**	19	ns	
t_{F32S}	$\overline{F32o}$ setup to $\overline{C32o}$ falling	11			ns	
t_{F32H}	$\overline{F32o}$ hold to $\overline{C32o}$ falling	11			ns	
t_{F32WL}	$\overline{F32o}$ pulse width low		**30.6**		ns	

Item 2: **7.5 C19o (19.44 MHz) Intrinsic Jitter Filtered Table has been updated. (page 20)**

Old:

7.5 C19o (19.44 MHZ) INTRINSIC JITTER FILTERED

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see “Notes” on page 23)
Intrinsic jitter (500 Hz to 1.3 MHz filter)			2	nspp	1-13, 20-23, 35
Intrinsic jitter (65 kHz to 1.3 MHz filter)			0.5	nspp	1-13, 20-23, 35

New:

7.5 C19o (19.44 MHZ) INTRINSIC JITTER FILTERED

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 23)
Intrinsic jitter (500 Hz to 1.3 MHz filter)		**0.4**	**0.5**	nspp	1-13, 20-23, 35
Intrinsic jitter (65 kHz to 1.3 MHz filter)		**0.2**	**0.3**	nspp	1-13, 20-23, 35

Item 1: **Holdover frequency accuracy has been updated.**

Old: Holdover frequency accuracy of 0.00625 ppm (page 1)

New: Holdover frequency accuracy of 0.025 ppm

Old: The frequency accuracy in the Holdover mode is ±0.00625 ppm, which corresponds to a worst case of 18 frame (125 µs per frame) slips in 24 hours. (page 10)

New: The frequency accuracy in the Holdover mode is ±0.025 ppm, which corresponds to a worst case of 18 frame (125 µs per frame) slips in 24 hours.

Old: The amount of phase drift while in holdover can be negligible because the Holdover mode is very accurate (e.g., 0.00625 ppm). (page 10)

New: The amount of phase drift while in holdover can be negligible because the Holdover mode is very accurate (e.g., 0.025 ppm).

Old: (page 19)

Performance

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 23)
Holdover Mode accuracy with OSCi at: 0 ppm	-0.00625		+0.00625	ppm	2, 4-7, 41, 42
Holdover Mode accuracy with OSCi at: ±32 ppm	-0.00625		+0.00625	ppm	2, 4-7, 41, 42
Holdover Mode accuracy with OSCi at: ±100 ppm	-0.00625		+0.00625	ppm	2, 4-7, 41, 42

New:

Performance

Description	Min.	Typ.	Max.	Units	Test Conditions / Notes (see "Notes" on page 23)
Holdover Mode accuracy with OSCi at: 0 ppm	-0.025		+0.025	ppm	2, 4-7, 41, 42
Holdover Mode accuracy with OSCi at: ±32 ppm	-0.025		+0.025	ppm	2, 4-7, 41, 42
Holdover Mode accuracy with OSCi at: ±100 ppm	-0.025		+0.025	ppm	2, 4-7, 41, 42

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.