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H8/300H Super Low Power Series

Waiting for Stabilization of Sub-Oscillator with Minimum Supply Current

Introduction

This application note describes two methods of waiting for the oscillation of the sub-oscillator to be stabilized with minimized supply current: one uses a timer and the other uses the time constant of the R-C network.

In the method using a timer, the H8/38099 waits in power-down mode until oscillation of the sub-oscillator becomes stable. The module standby function is used during power-down mode.

To check the oscillation of the sub-oscillator, timer C is activated with supply of a subclock and made to produce 1-second toggle output on port pin 92.

Target Device

H8/38099

Contents

1. Specifications

1.1 Waiting for Oscillation Stabilization by Software

1. The H8/38099 directly enters sleep (medium-speed) mode after a reset is canceled.
2. The operating clock frequency is ϕ/64 in sleep (medium-speed) mode.
3. Modules except for the 16-bit timer pulse unit (TPU) are deactivated in sleep (medium-speed) mode.
4. The oscillation stabilization waiting time of the subclock is counted by the TPU.
5. The H8/38099 switches from sleep (medium-speed) mode to active (medium-speed) mode using a TPU interrupt.
6. To check the oscillation of the subclock, timer C is activated with supply of a subclock.

1.2 Waiting for Oscillation to be Stabilized by Time Constant of R and C

Rising of the $\overline{\text{RES}}$ signal can be delayed by attaching an external capacitor to the reset pin and the built-in resistor of the pin.

2. Oscillation Stabilization Time and Reset Timing

2.1 Subclock Oscillation Stabilization Time

This section describes the oscillation stabilization time of the subclock. Figure 1 shows the subclock oscillation stabilization timing. The subclock takes more oscillation stabilization time than the main clock. When the subclock is used as the operating clock of the CPU before the subclock becomes stable, the system may malfunction.

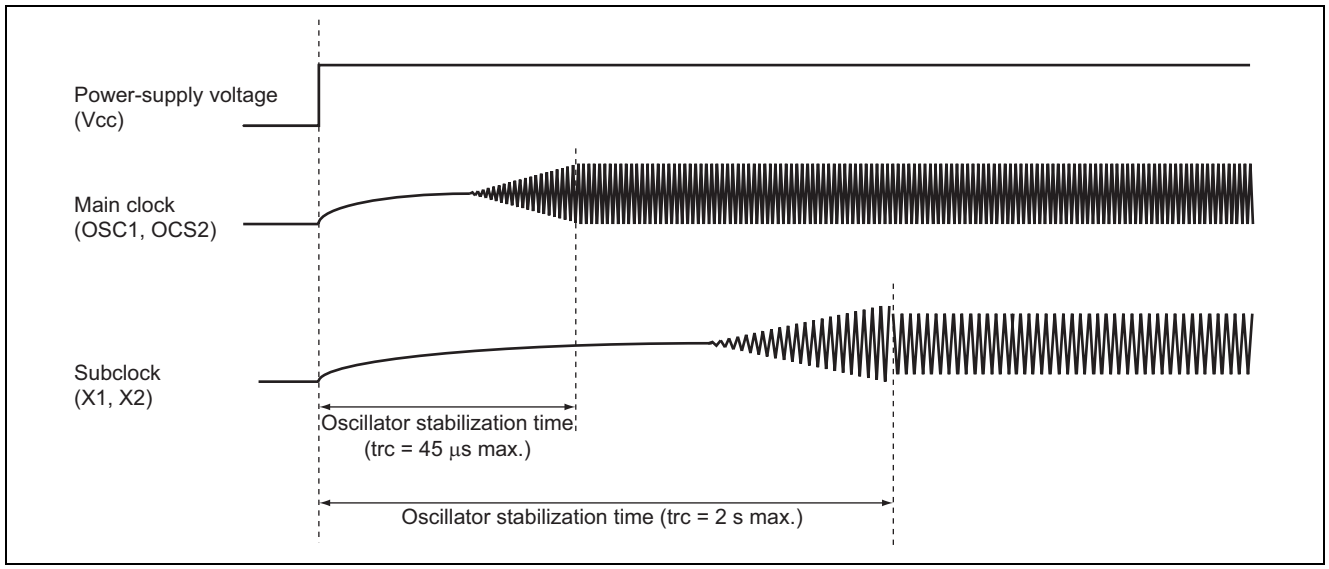


Figure 1 Oscillation Stabilization Time of Main Clock and Subclock

2.2 Timing of Reset Cancellation by Power-On Reset Circuit

The H8/300H-Super Low Power microcontroller incorporates a power-on reset circuit that generates an internal reset signal at power-on with an external capacitor connected. Figure 2 shows the power-on reset circuit.

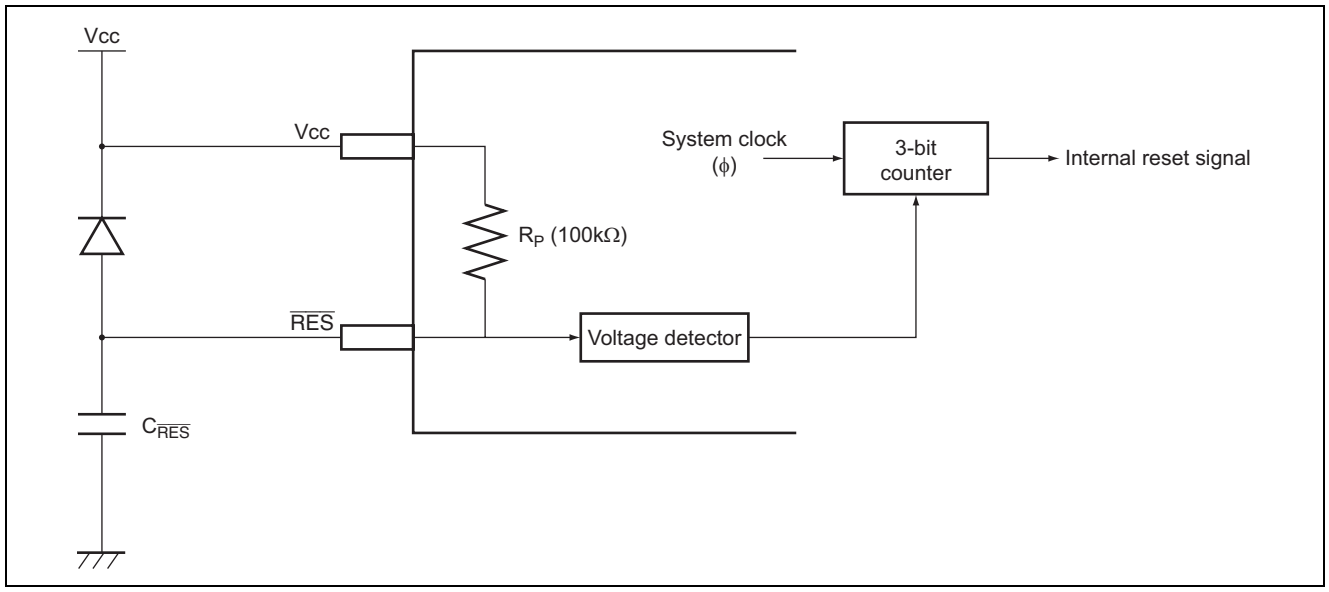


Figure 2 Power-On Reset Circuit

The rising time (t) of the $\overline{RES}$ pin signal is found by the following equation.

$$t = C_{\overline{RES}} \times R_P\ (100\ k\Omega)$$

The oscillation stabilization time of the subclock is specified as 2 seconds at maximum in the hardware manual. Therefore, when waiting for the subclock oscillation to become stable using a timer, determine the subclock usage disabled time considering the capacitance of the external capacitor.

When delaying the reset signal negation with an external capacitor, use a 22 µF capacitor considering the internal pull-up resistor. In this case, the rising time (t) is found as follows:

$$t = 22\ \mu F \times 100\ k\Omega \text{ (internal pull-up resistance)}$$
$$= 2.2\ (s)$$

3. Description of Functions Used

3.1 Functions

The following describes the functions used in waiting for oscillation stabilization of the subclock using the timer.

This sample task generates an interrupt every 1.958 seconds by using the TPU. For details of bits in each register, see section 5.3, Internal Registers Used.

3.2 Power-Down Modes

As the operating mode after a reset is canceled, there are seven types of power-down modes, which remarkably reduce power consumption, in addition to normal active (high-speed) mode. Further, the H8/38099 is provided with a module standby function that reduces power consumption by selectively stopping the operation of on-chip modules. In this sample task, the H8/38099 is made to enter sleep (medium-speed) mode after reset cancellation where the modules other than the TPU are placed in standby mode in order to reduce supply current.

- System Control Registers 1 to 3 (SYSCR1 to SYSCR3)
  SYSCR1 to SYSCR3 control power-down modes.
- Clock Stop Registers 1 to 3 (CKSTPR1 to CKSTPR3)
  CKSTPR1 to CKSTPR3 drive the individual on-chip peripheral modules into the standby state.

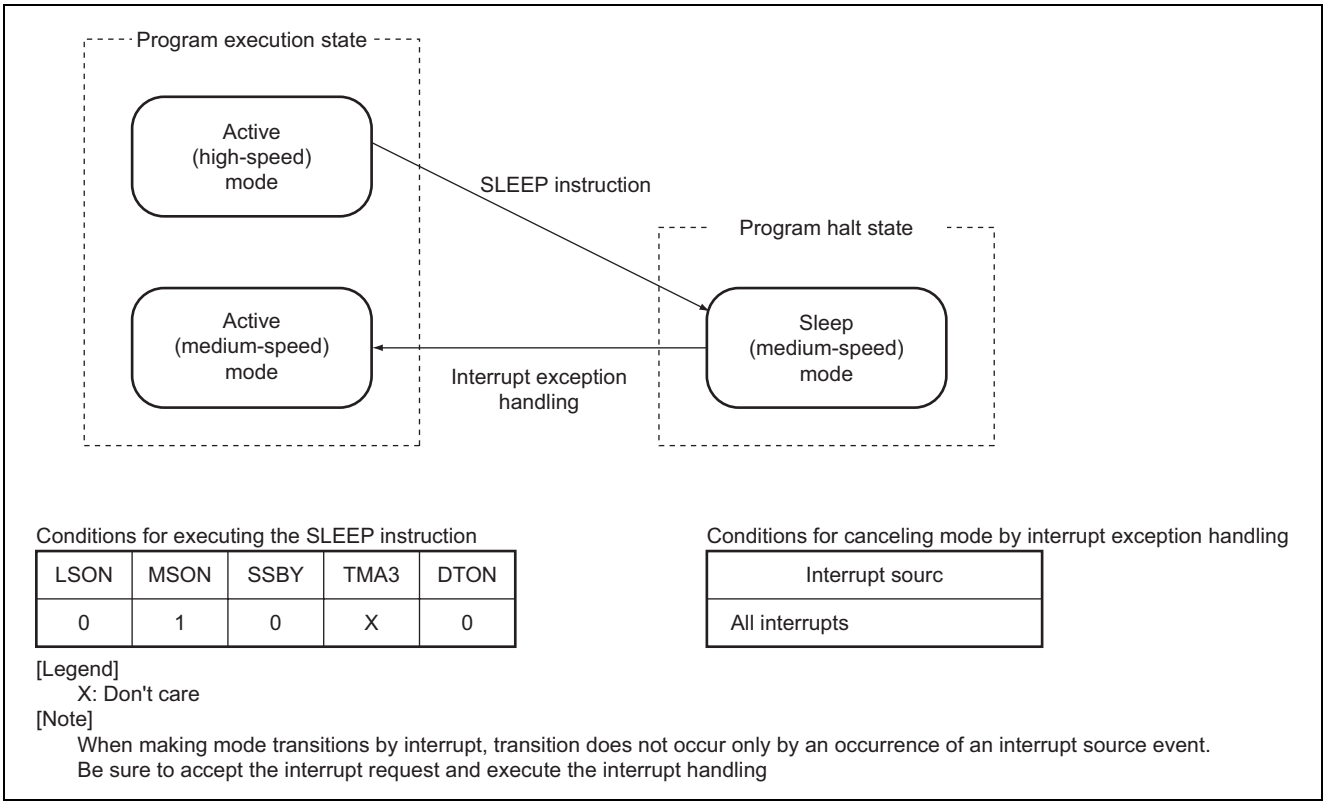
3.2.1 Sleep (Medium-Speed) Mode

- Power-down mode (sleep (medium-speed) mode) function:
  In sleep (medium-speed) mode, the CPU is stopped but the system clock oscillator, on-chip oscillator for the system clock, subclock oscillator, and the on-chip peripheral modules operate. In this mode, the on-chip peripheral modules operate with the clock at the frequency specified by the MA1 and MA0 bits in SYSCR1, and the data stored in the CPU registers is retained. Sleep mode is canceled by an interrupt. When an interrupt request is generated, sleep mode is exited and the interrupt exception handling starts. When the I bit in CCR is 1 or an interrupt is masked by the interrupt enable bit, sleep mode cannot be canceled. After exiting sleep (medium-speed) mode, the H8/38099 enters active (medium-speed) mode.
  When the $\overline{\text{RES}}$ pin level is turned low during sleep mode, the H8/38099 exits sleep mode and enters the reset state.
  Note that there may be a delay of up to 2/ϕ seconds from the occurrence of the interrupt request signal until the interrupt exception handling is started because the interrupt request signal is synchronized with the system clock.

Table 1 shows the state of the LSI in sleep (medium-speed) mode. Figure 3 illustrates transitions from active mode to sleep (medium-speed) mode.

Table 1 State of LSI in Sleep (Medium-Speed) Mode

Function		Sleep (Medium-Speed) Mode
System clock oscillator		Run
Subclock oscillator		Run/stop
CPU	Instruction	Stop
	RAM	Retain
	Register	Retain
	I/O	Retain
External interrupt	NMI	Run
	IRQ0	Run
	IRQ1	Run
	IRQ3	Run
	IRQ4	Run
	IRQAEC	Run
	WKP0 to WKP7	Run
Peripheral module	Timer C	Run
	Timer F, timer G	Run
	Asynchronous event counter	Run
	RTC	Run
	TPU	Run
	WDT	Run
	SCI3/IrDA	Run
	IIC2	Run
	PWM	Run
	A/D converter	Run
	LCD	Run
	Address break	Retain



Conditions for executing the SLEEP instruction

LSON	MSON	SSBY	TMA3	DTON
0	1	0	X	0

Conditions for canceling mode by interrupt exception handling

Interrupt sourc
All interrupts

[Legend]
X: Don't care
[Note]
When making mode transitions by interrupt, transition does not occur only by an occurrence of an interrupt source event. Be sure to accept the interrupt request and execute the interrupt handling

Figure 3 Mode Transitions

- Transition to sleep (medium-speed) mode
  1. Clear the SSBY and LSON bits in SYSCR1 to 0.
  2. Clear the DTON bit in SYSCR2 to 0, and set the MSON bit in SYSCR2 to 1.
  3. Execute the SLEEP instruction.
- Exiting sleep (medium-speed) mode
  1. Accept an interrupt request in sleep (medium-speed) mode.
  2. Execute the interrupt handling processing (The LSI enters active (medium-speed) mode when it wakes up by an interrupt).

3.2.2 Module Standby Mode

The module standby function can be set for all peripheral modules. The clock supply to modules that are set to module standby mode is halted, and the modules enter the power-down state. When the bit in CKSTPR1 to CKSTPR3 corresponding to each module is set to 0, the module enters module standby mode. When the bit is set to 1, module standby mode is canceled.

3.3 16-Bit Timer Pulse Unit (TPU)

The H8/38099 group has an internal 16-bit timer pulse unit (TPU) composed of 2 channels of 16-bit timers.

- Timer control register (TCR)
  The TCR controls the timer counter (TCNT) of each channel. The TPU is provided with two TCRs (one for each channel). Set the TCR while the TCNT is not working. In this sample task, the internal clock ϕ/256 is selected as the counter clock source.
- Timer interrupt enable register (TIER)
  The TIER enables or disables interrupt requests of each channel. The TPU is provided with two TIERs (one for each channel).
- Timer status register (TSR)
  The TSR indicates the status of each channel. The TPU is provided with two TSRs (one for each channel).
- Timer counter (TCNT)
  The TCNT is a 16-bit readable/writable counter. The TPU is provided with two TCNTs (one for each channel). The TCNT is initialized to H'0000 by a reset or when the H8/38099 enters hardware standby mode. Accesses to the TCNT in 8-bit units are prohibited. Only 16-bit access is allowed.
- Timer general register (TGR)
  The TGR is a 16-bit readable/writable register that can be used for either output comparison or input capture. The TPU is provided with four TGRs (two for each channel). The TGR is initialized to H'FFFF by a reset. Accesses to the TGR in 8-bit units are prohibited. Only 16-bit access is allowed. In this sample task, TGRs are set to H'04C5 to generate a compare-match in two seconds.
- Timer start register (TSTR)
  The TSTR starts or stops counting by TCNT on channels 1 and 2. The TCNT of the channel for which the corresponding bit is set to 1 starts counting. TCNT operation should be stopped before setting operating mode in TMDR or setting the clock source for TCNT in TCR.

3.4 Timer C

Timer C is an 8-bit timer that increments or decrements at each input clock. Timer C has the interval function and auto-reload function.

- Timer mode register C (TMC)
  TMC is an 8-bit readable/writable register that selects the auto-reload function, controls count-up/count-down of timer counter C (TCC), and selects an input clock. For the TCC count-up/count-down control, either hardware control driven by the UD pin input or usage as a software-controlled up-counter or down-counter is selectable. The TMC is initialized to H'10 by a reset.

- Timer counter C (TCC)
  TCC is an 8-bit readable up/down-counter that is incremented or decremented by an input internal clock or an external event. An input clock can be selected from among ten types of clock: the system clock divided by 8192, 2048, 512, 64, 16, and 4, the subclock divided by 1024, 256, and 4, and an external clock. In this sample task, the TCC is configured as an up-counter, and the subclock divided by 1024 is selected for the TCC input clock.

- Timer load register C (TLC)
  TLC is an 8-bit write-only register used to set a value to be reloaded to TCC. When a value written to TLC, the value is also loaded to TCC at the same time, and TCC starts counting up or down from that value. When TCC overflows or underflows during auto-reloading operation, the TLC value is loaded to TCC. This allows TCC to overflow/underflow periodically within a range from 1 to 256 cycles of the input clock. TLC is allocated to the same address as TCC and initialized to H'00 by a reset.
  In this sample task, the H'E0 is set in TLC to allow the TCC to overflow in two seconds.

3.5 Interrupt Controller

The H8/38099 controls interrupts using the interrupt controller.

- Interrupt request register 2 (IRR2) shows timer C interrupt request statuses.
- Interrupt enable register 2 (IENR2) enables timer C interrupts.

3.6 Watchdog Timer Function

The H8/38099 has an 8-bit internal watchdog timer (WDT). After a reset, the watchdog timer is turned on. The inside of the H8/38099 is reset when the WDT counter overflows because of the CPU being unable to rewrite the counter value due to a system runaway or other reasons. In this sample task, the watchdog timer function is deactivated because it is not used.

- Timer control/status register WD1 (TCSRWD1)
  Timer control/status register WD1 (TCSRWD1) controls writing to TCSRWD1 itself and to TCWD. TCSRWD1 also controls the operation of the watchdog timer and indicates its operating status. To rewrite this register, use the MOV instruction. Bit manipulation instructions cannot be used to change its setting.

3.7 Assignment of Functions

Table 2 lists the function assignment of this sample task. With the functions assigned as shown in table 2, the wait time for subclock oscillation stabilization is ensured using the TPU.

Table 2 Assignment of Functions

Function	Description
SYSCR1	Controls transition to sleep (medium-speed) mode in combination with SYSCR2 and SYSCR3.
SYSCR2	Controls transition to sleep (medium-speed) mode in combination with SYSCR1 and SYSCR3.
CKSTPR1	Controls module standby state as well as CKSTPCR2 and CKSTPR3.
CKSTPR2	Controls module standby state as well as CKSTPCR1 and CKSTPR3.
CKSTPR3	Controls module standby state as well as CKSTPCR1 and CKSTPR2.
PSS	A 17-bit up-counter that operates with input of the system clock.
TCR1	Selects the input clock of TCNT1.
TGIEA1	Enables TPU interrupt requests.
TGFA1	Reflects whether a TPU interrupt request has been generated or not.
TCNT1	A 16-bit counter that operates with input of the system clock divided by 256.
TGRA1	Sets the value for comparison-match interrupt.
TSTR	Controls TCNT1 counting operation.
TCC	An 8-bit counter that operates with input of the subclock divided by 256.
TMC	Selects the auto-reload function, controls counting up/down, and selects the input clock.
TLC	Sets the value to be reloaded to TCC.
IRRTC	Reflects whether a timer C interrupt request has been generated or not.
IENTC	Enables timer C interrupt requests.
TCRWD1	Stops the watchdog timer.

4. Principles of Operation

Figure 4 illustrates the method of waiting for the oscillation stabilization of the subclock using the TPU. Though the hardware and software processing shown in this figure, the H8/38099 enters sleep (medium-speed) mode and after two seconds, recovers from sleep (medium-speed) mode triggered by interrupt processing to active (medium-speed) mode after waiting for two seconds by the interrupt handling.

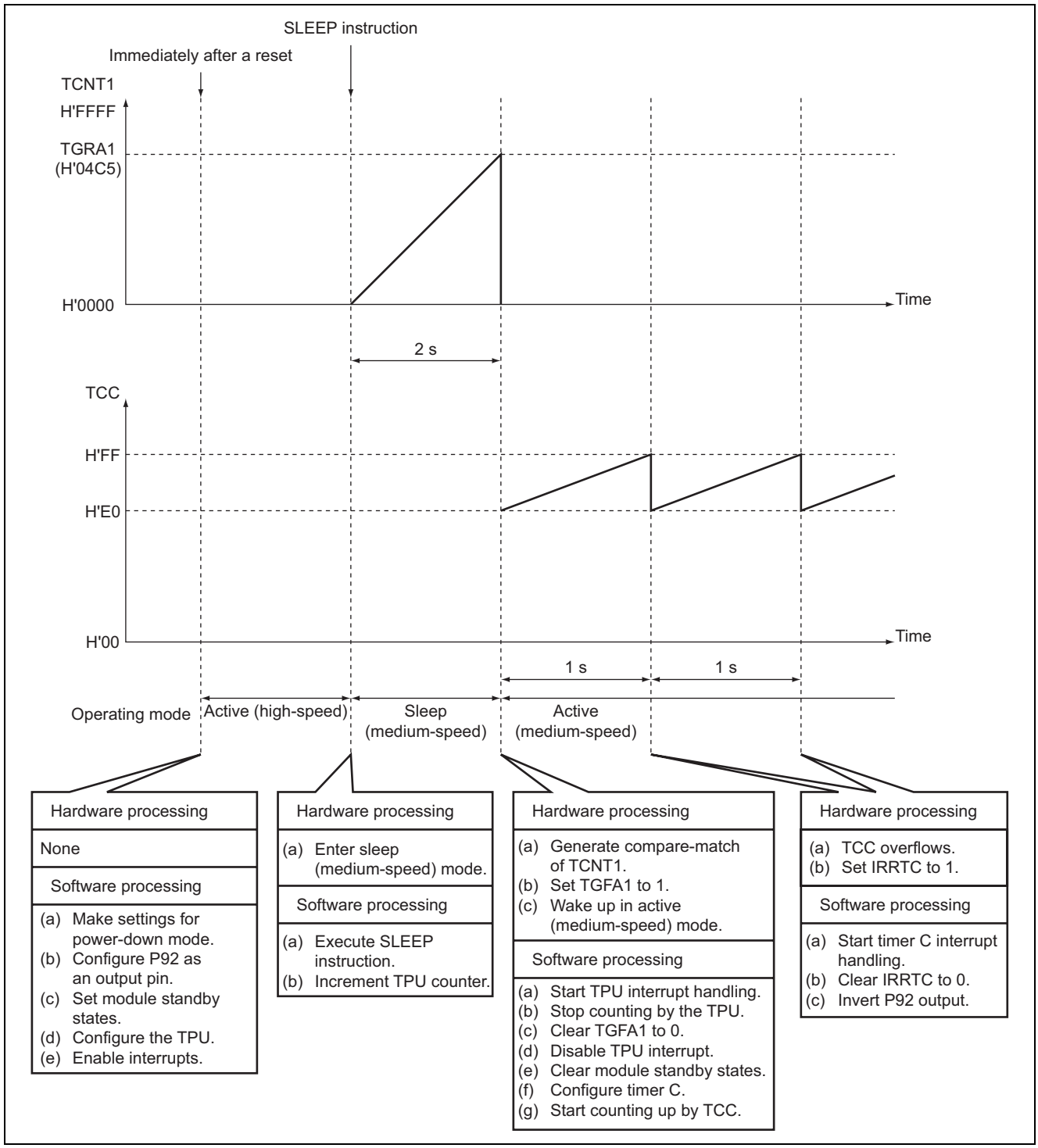


Figure 4 Waiting for Subclock Oscillation Stabilization Using TPU

5. Description of Software

5.1 Modules

Table 3 lists the modules of this sample task.

Table 3 Description of Modules

Module Name	Label Name	Function
Main routine	main	Make settings for the TPU, power-down mode, and the module standby function, and enables interrupts.
TPU interrupt	tpu1int	Interrupt handling routine executed when the H8/38099 switches from sleep (medium-speed) mode to active (medium-speed) mode, which configures timer C and makes settings for the module standby function.
Timer C interrupt	tcint	Performs timer C interrupt handling processing.

5.2 Argument

No argument is used in this sample task.

5.3 Internal Registers Used

This section describes the internal registers used in this sample task.

- System Control Register 1 (SYSCR1) Address: H'FFFFF0

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	SSBY	0	0	R/W	Software Standby Selects the mode to enter after executing the SLEEP instruction. 0: Sleep mode or sub-sleep mode. 1: Standby mode or watch mode.
3	LSON	0	0	R/W	Selects the system clock (ϕ) or subclock (ϕ_{SUB}) as the CPU operating clock when watch mode is exited. 0: Uses the system clock (ϕ) as the CPU operating clock. 1: Uses the subclock (ϕ_{SUB}) as the CPU operating clock.
2	TMA3	0	0	R/W	Selects the mode to enter after executing the SLEEP instruction in combination with SSBY/LSON in SYSCR1 and DTON/MSON in SYSCR2.
1	MA1	1	1	R/W	Active Mode Clock Select 1, 0
0	MA0	1	1	R/W	Select an operating clock frequency for active (medium-speed) mode or sleep (medium-speed) mode. These bits should be modified in active (high-speed) mode or sub-active mode. 00: $\phi_{OSC}/8$ 01: $\phi_{OSC}/16$ 10: $\phi_{OSC}/32$ 11: $\phi_{OSC}/64$

- System Control Register 2 (SYSCR2) Address: H'FFFFF1

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
3	DTON	0	0	R/W	Direct Transfer On Flag Selects the mode to enter after executing the SLEEP instruction in combination with the SSBY, TMA3, and LSON bits in SYSCR1 and the MSON bit in SYSCR2.
2	MSON	0	1	R/W	Middle Speed On Flag Selects whether to enter active (high-speed) mode or active (medium-speed) mode after exiting standby mode, watch mode, and sleep mode. 0: Active (high-speed) mode. 1: Active (medium-speed) mode.

- Clock Stop Register 1 (CKSTPR1) Address: H'FFFFFA

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	S4CKSTP*1*3	1	0/1	R/W	SCI4 Module Standby When this bit is cleared to 0, the SCI4 enters the standby state.
6	S31CKSTP	1	0/1	R/W	SCI3_1 Module Standby*2 When this bit is cleared to 0, the SCI3_1 enters the standby state.
5	S32CKSTP	1	0/1	R/W	SCI3_2 Module Standby*2 When this bit is cleared to 0, the SCI3_2 enters the standby state.
4	ADCKSTP	1	0/1	R/W	A/D Converter Module Standby When this bit is cleared to 0, the A/D converter enters the standby state.
3	—	1	1/1	R/W	Reserved Readable/writable reserved bit.
2	TFCKSTP	1	0/1	R/W	Timer F Module Standby When this bit is cleared to 0, timer F enters the standby state.
1	FROMCKSTP*1*3	1	1	R/W	Flash Memory Module Standby When this bit is cleared to 0, the flash memory enters the standby state. When a flash memory area (H'000000 to H'0000FF) is accessed while this bit is 0, the RAM emulation function is enabled and the RAM area (H'FFFC00 to H'FFFCFF) is accessed.
0	RTCCKSTP	1	0/1	R/W	RTC Module Standby When this bit cleared to 0, the RTC enters the standby state.

Notes: *1. This bit is always read as 1 and cannot be modified in the mask ROM version.
*2. When this bit is set to put the SCI3 module in standby state, all SCI3 registers are reset.
*3. When using the on-chip emulator, be sure to set this bit to 1.

- Clock Stop Register 2 (CKSTPR2) Address: H'FFFFFFB

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	ADBCKSTP	1	0/1	R/W	Address Break Module Standby When this bit is cleared to 0, the address break enters the standby state.
6	TPUCKSTP	1	1	R/W	TPU Module Standby When this bit is cleared to 0, the TPU enters the standby state.
5	IICCKSTP	1	0/1	R/W	IIC2 Module Standby When this bit is cleared to 0, the IIC2 enters the standby state.
4	PW2CKSTP	1	0/1	R/W	PWM2 Module Standby When this bit is cleared to 0, the PWM2 enters the standby state.
3	AECCKSTP	1	0/1	R/W	Asynchronous Event Counter Module Standby When this bit is cleared to 0, the asynchronous event counter enters the standby state.
2	WDCKSTP	1	0/1	R/W*	Watchdog Timer Module Standby When this bit is cleared to 0, the watchdog timer enters the standby state.
1	PW1CKSTP	1	0/1	R/W	PWM1 Module Standby When this bit is cleared to 0, the PWM1 enters the standby state.
0	LDCKSTP	1	0/1	R/W	LCD Module Standby When this bit is cleared to 0, the LCD controller/driver enters the standby state.

Notes: * WDCKSTP is valid when the WDON bit in TCSRW is 0. When WDCKSTP is set to 0 while WDON is 1 (WDT is operating), WDCKSTP is cleared to 0 but the WDT does not enter module standby mode continuing the watchdog function. At the same time when the WDON bit is set to 0 by software, the WDCKSTP bit becomes valid and the WDT enters module standby mode.

- Clock Stop Register 3 (CKSTPR3) Address: H'FFFFFFC

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	S33CKSTP	1	0/1	R/W	SCI3_3 Module Standby* When this bit is cleared to 0, the SCI3_3 enters the standby state.
6	TCCKSTP	1	0/1	R/W	Timer C Module Standby When this bit is cleared to 0, timer C enters the standby state.
5	TGCKSTP	1	0/1	R/W	Timer G Module Standby When this bit is cleared to 0, timer G enters the standby state.
4	PW4CKSTP	1	0/1	R/W	PWM4 Module Standby When this bit is cleared to 0, the PWM4 enters the standby state.
3	PW3CKSTP	1	0/1	R/W	PWM3 Module Standby When this bit is cleared to 0, the PWM3 enters the standby state.
2	—	0	0	—	Reserved
1	—	0	0	—	These bits are always read as 0 and cannot be modified.
0	—	0	0	—	

Notes: * When this bit is set to put the SCI3 module in standby state, all SCI3 registers are reset.

- Timer Control Register 1 (TCR1) Address: H'FFFF040

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
2	TPSC2	0	1	R/W	Timer Prescaler 2 to 0
1	TPSC1	0	1	R/W	Selects the TCNT counter clock. A clock source can be selected independently for each channel. For details, see table 4.
0	TPSC0	0	0	R/W	

Table 4 TPSC2 to TPSC0

Channel	Bit 2 TPSC2	Bit 1 TPSC1	Bit 0 TPSC0	Description
1	0	0	0	Counts with input of the Internal clock φ/1.
	0	0	1	Counts with input of the Internal clock φ/4.
	0	1	0	Counts with input of the Internal clock φ/16.
	0	1	1	Counts with input of the Internal clock φ/64.
	1	0	0	Counts with input of the external clock input from the TCLKA pin.
	1	0	1	Counts with input of the external clock input from the TCLKB pin.
	1	1	0	Counts with input of the Internal clock φ/256.
	1	1	1	Counts the occurrence of TCNT2 overflow.

- Timer Interrupt Enable Register 1 (TIER1) Address: H'FFF044

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
0	TGIEA1	0	0/1	R/W	TGR1 Interrupt Enable A Enables or disables generation of an interrupt request (TGIA1) when the TGFA1 bit in TSR1 is set to 1. 0: Disables the interrupt (TGIA1) by the TGFA1 bit. 1: Enables the interrupt (TGIA1) by the TGFA1 bit.

- Timer Status Register 1 (TSR1) Address: H'FFF045

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
0	TGFA1	0	0/1	R/(W)*	Input Capture/Output Compare Flag A1 Indicates whether an input capture or compare-match of TGRA1 has been generated. [Setting conditions] • The TCNT1 value matches TGRA1 while TGRA1 is functioning as an output compare register. • The TCNT1 value is transferred to TGRA1 by the input capture signal while TGRA1 is functioning as an input capture register. [Clearing condition] • Writing 0 to TGFA1 after reading TGFA1 while it is 1.

Note: * Only writing 0 to clear the flag is enabled.

- Timer Counter 1 (TCNT1) Address: H'FFF046

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
15 to 0	Bit 15 to Bit 0	H'0000	—	R/W	TCNT is a readable/writable counter. Two TCNTs (one for each channel) are provided. The TCNT is initialized to H'0000 by a reset or when the H8/38099 enters hardware standby mode. Accesses to the TCNT in 8-bit units are prohibited. Be sure to make accesses to the TCNT in 16-bit units.

- Timer General Register A1 (TGRA1) Address: H'FFF048

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
15 to 0	Bit 15 to Bit 0	H'FFFF	H'04C5	R/W	TGR is a 16-bit readable/writable register for both output compare and input capture. Four TGR registers (two for each channel) are provided. The TGR is initialized to H'FFFF by a reset. Accesses to the TGR in 8-bit units are prohibited. Be sure to make accesses to the TGR in 16-bit units.

- Timer Start Register (TSTR) Address: H'FFF030

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
1	CST1	0	0 or 1	R/W	Counter Start 1 Starts or stops the TCNT operation. 0: Stops the TCNT1 counter operation. 1: Starts the TCNT1 counter operation.

- Timer Mode Register C (TMC) Address: H'FFFFB4

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	TMC7	0	1	R/W	Auto-Reload Function Select Selects the auto-reload function of timer C. 0: Selects the interval function. 1: Selects the auto-reload function.
6	TMC6	0	0	R/W	Counter Up/Down Control
5	TMC5	0	0	R/W	Select whether TCC operates as an up-counter or down-counter, or its up/down operation is controlled by hardware using the UD pin input. 00: TCC is an up-counter. 01: TCC is a down-counter. 1x: Hardware control using the UD pin input. High UD pin input level: Down-counter. Low UD pin input level: Up-counter.
4	—	1	1	—	Reserved This bit is always read as 0 and cannot be modified.
3	TMC3	0	0	R/W	Clock Select
2	TMC2	0	1	R/W	Select a clock to be input to TCC. The rising edge or falling edge can be selected for an external event input.
1	TMC1	0	1	R/W	
0	TMC0	0	0	R/W	x000: Counts by the internal clock ϕ/8192. x001: Counts by the internal clock ϕ/2048. x010: Counts by the internal clock ϕ/512. x011: Counts by the internal clock ϕ/64. x100: Counts by the internal clock ϕ/16. 0101: Counts by the internal clock ϕ/4. 0110: Counts by the internal clock ϕ_W/1024. 1101: Counts by the internal clock ϕ_W/256. 1110: Counts by the internal clock ϕ_W/4. 0111: Counts falling edges of the external event signal (TMIC).* 1111: Counts rising edges of the external event signal (TMIC).*

Legend:
x: Don't care
Notes: * Be sure to set the TMIC bit in the port mode register E (PMRE) to 1 before setting TMC3 to TMC0 to B'x111.

- Timer Counter C (TCC) Address: H'FFFFB5

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	TCC7	0	—	R	TCC is an 8-bit readable up/down counter that is incremented or decremented with input of an internal clock or an external event. The input clock is selected by the TMC3 to TMC0 bits in TMC. The value of TCC can always be read by the CPU. When TCC overflows (H'FF to H'00 or H'FF to TLC value) or underflows (H'00 to H'FF or H'00 to TLC value), IRRTC in IRR2 is set to 1. TCC is allocated to the same address as TLC and initialized to H'00 by a reset.
6	TCC6	0	—	R	
5	TCC5	0	—	R	
4	TCC4	0	—	R	
3	TCC3	0	—	R	
2	TCC2	0	—	R	
1	TCC1	0	—	R	
0	TCC0	0	—	R	

- Timer Load Register C (TLC) Address: H'FFFFB5

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
7	TLC7	0	1	W	TLC is an 8-bit write-only register used to set a value to be reloaded to TCC. When a value written to TLC, the value is also loaded to TCC at the same time, and TCC starts counting up or down from that value. When TCC overflows or underflows during auto-reloading operation, the TLC value is loaded to TCC. This allows TCC to overflow/underflow periodically within a range from 1 to 256 cycles of the input clock. TLC is allocated to the same address as TCC and initialized to H'00 by a reset.
6	TLC6	0	1	W	
5	TLC5	0	1	W	
4	TLC4	0	0	W	
3	TLC3	0	0	W	
2	TLC2	0	0	W	
1	TLC1	0	0	W	
0	TLC0	0	0	W	

- Interrupt Enable Register 2 (IENR2) Address: H'FFFFF4

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
1	IENTC	0	1	R/W	Timer C Interrupt Enable Enables timer C interrupt requests.

- Interrupt Request Register 2 (IRR2) Address: H'FFFFF7

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
1	IRRTC	0	0/1	R/W	Timer C Interrupt Request Flag [Setting condition] • Timer C overflows or underflows [Clearing condition] • Writing 0

- Port Data Register 9 (PDR9) Address: H'FFFFDC

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
2	P92	1	0/1*	R/W	When port 9 is read when the corresponding bit of the PCR9 register is 1, the value of PDR9 is directly read. The pin state therefore has no effect on reading. When port 9 is read when PCR9 is 0, the pin state is read.

Note * This bit is toggled every second by the timer C interrupt handling routine.

- Port Control Register 9 (PCR9) Address: H'FFFFEC

Bit	Bit Name	Initial Value	Setting Value	R/W	Function
2	PCR92	0	1	W	Setting a PCR9 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR9 and PDR9 registers are valid when the corresponding pin is set as a general I/O pin. PCR9 is a write-only register. This bit is always read as 1.

- Timer Control/Status Register WD1 (TCSRWD1) Address: H'FFFFB1

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
7	B6WI	1	1	R/W	Bit 6 Write Disable Writing to bit 6 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
6	TCWE	0	0	R/W	Timer Counter W Write Enable Writing to TCWD is enabled when this bit is set to 1. When writing to this bit, 0 must be written to bit 7.
5	B4WI	1	*	R/W	Bit 4 Write Disable Writing to bit 4 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
4	TCSRWE	0	*	R/W	Timer Control/Status Register W Write Enable Writing to bits 2 and 0 of this register is enabled when this bit is set to 1. When writing to this bit, 0 must be written to bit 5.
3	B2WI	1	*	R/W	Bit 2 Write Disable Writing to bit 2 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
2	WDON	1	*	R/W	Watchdog Timer On Setting this bit to 1 causes TCWD to start counting up. Clearing it to 0 causes TCWD to stop counting up. [Clearing condition] • 0 is written to B2WI and WDON while TCSRWE is 1. [Setting conditions] • A reset is made. • 0 is written to B2WI and 1 is written to WDON while TCSRWE is 1.

Bit	Bit Name	Initial Value	Setting Value	R/W	Description
1	B0WI	1	1	R/W	Bit 0 Write Disable Writing to bit 0 of this register is enabled only when 0 is written to this bit. This bit is always read as 1.
0	WRST	0	0	R/W	Watchdog Timer Reset [Clearing conditions] • A reset is made with the $\overline{\text{RES}}$ pin. • 0 is written to B0WI and WRST while TCSRWE is 1. [Setting condition] • TCWD overflows and an internal reset signal is generated.

Note: * These bits are manipulated so as to stop the watchdog timer. See the flowchart for the main routine.

5.4 RAM Usage

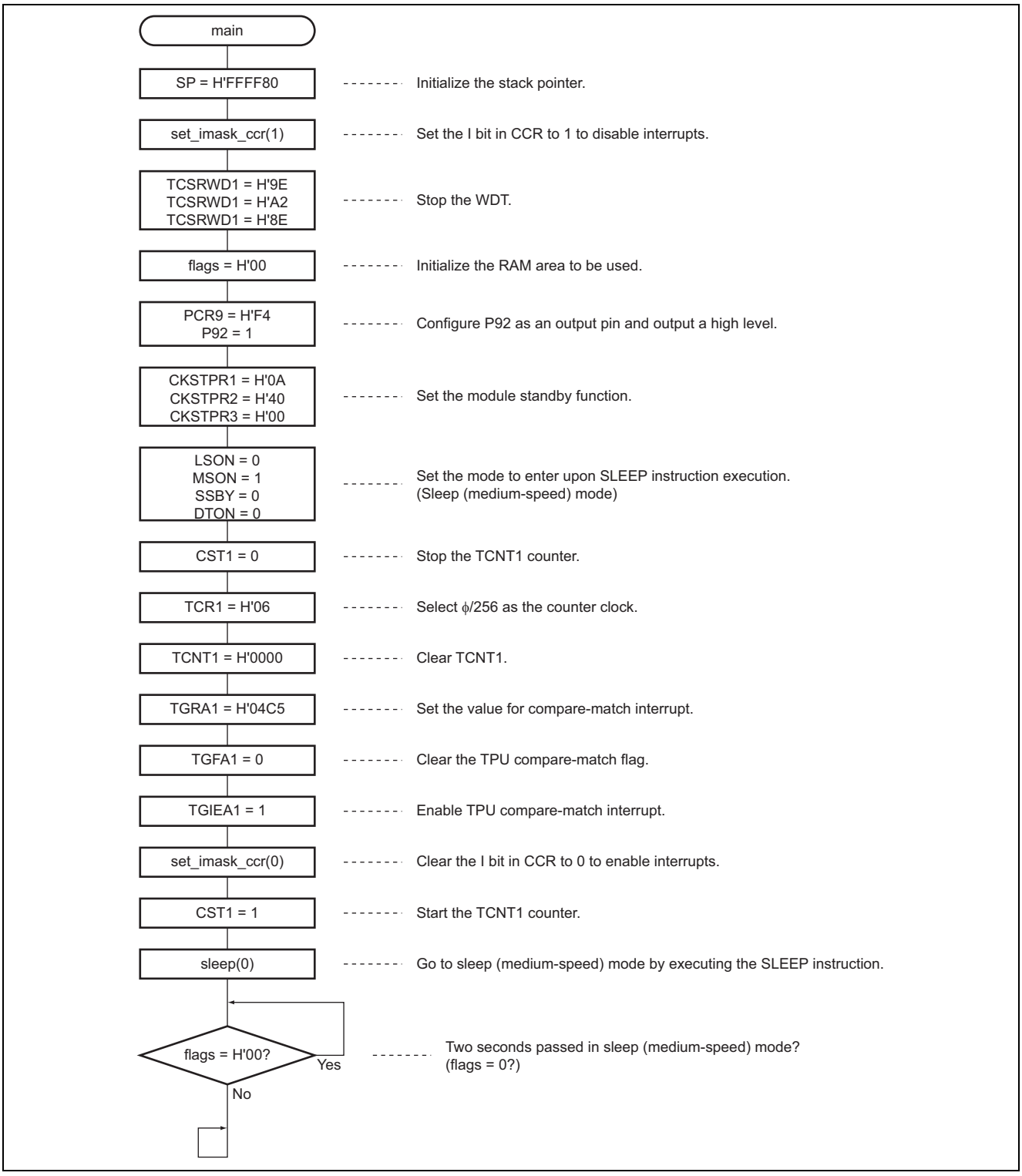
Table 5 shows the RAM usage in this sample task.

Table 5 RAM Usage

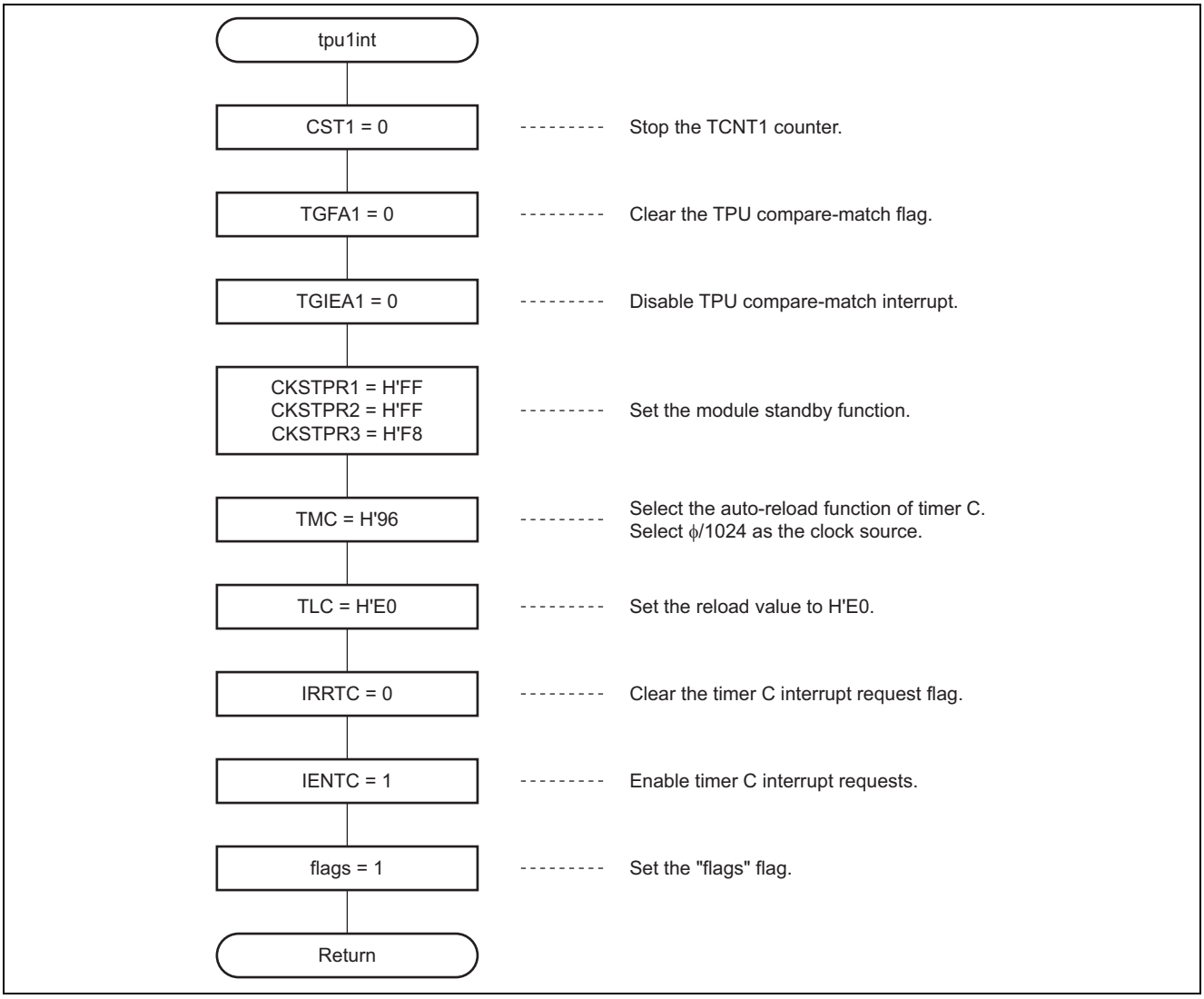
Type	Label Name	Description	Used In
unsigned char	flags	A flag that indicates that two seconds passed in sleep (medium-speed) mode. flags = H'00: 2 seconds not passed flags = H'01: 2 seconds passed	main, tpu1int

6. Flowcharts

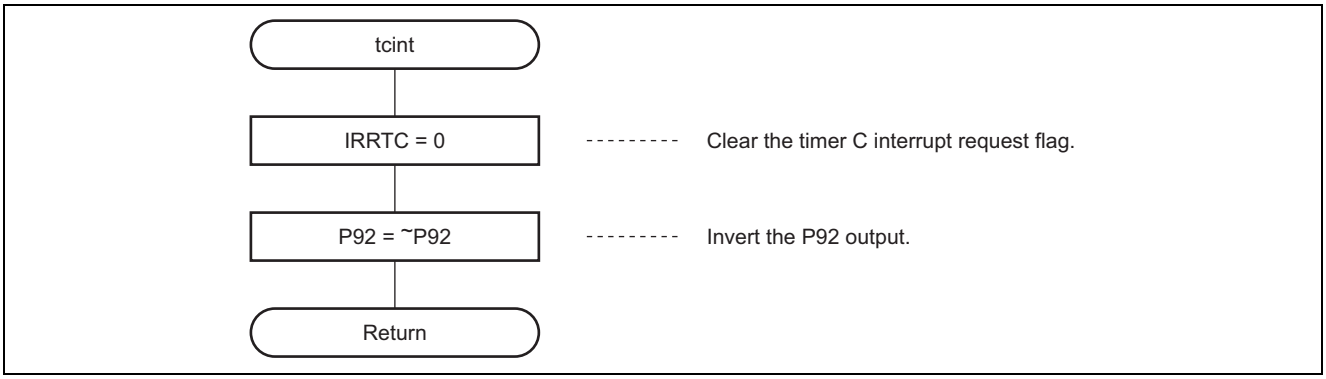
6.1 main Function



6.2 tpu1int Function



6.3 tcint Function



7. Link Address Specifications

Section Name	Address
CV1	H'000000
CV2	H'000074
CV3	H'0000D4
P	H'000800
B	H'FFF380

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Revision Record

		Description	
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