

VersaClock 7 RC21/RC31 Series – Measurement of Hitless Switching

This document provides the steps needed to setup Hitless Switching on VersaClock 7 (VC7) RC21/RC31 Series using Renesas IC Toolbox (RICBox).

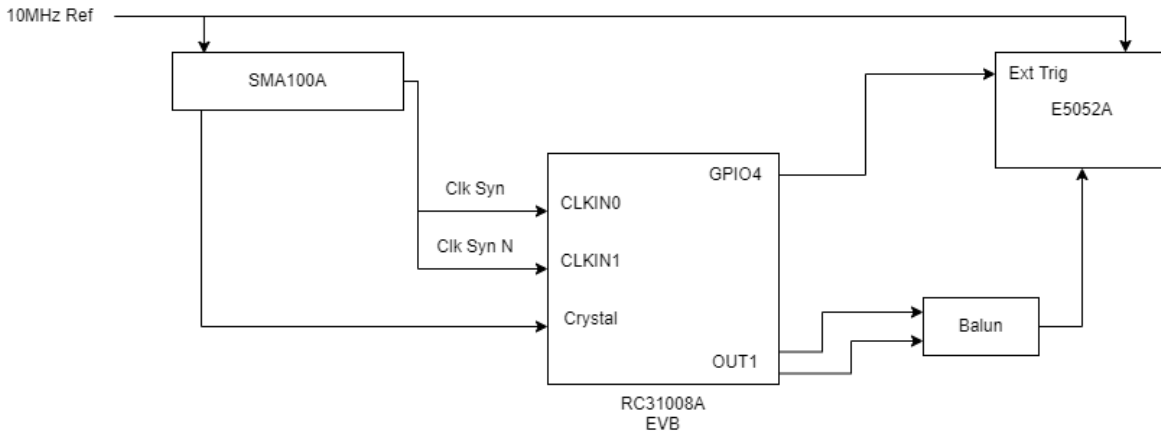
For more information about RICBox, see the [Renesas IC Toolbox User Guide](#). The measurement of hitless switching will be done using the E5052A Signal Source Analyzer.

Contents

1. Bench Setup	2
1.1 RC21008A/RC31008A EVB Setup	2
1.2 SMA100A Setup	2
1.3 E5052A Setup	3
2. RICBox Installation	5
3. Creating the Settings File	5
4. CLKIN Switching	5
4.1 Non Hitless Switching vs Hitless Switching	6
4.2 Hitless Switching	7
4.3 Non Hitless Switching.....	9
4.4 Phase Slope Limit.....	11
5. Revision History	13
Appendix A – Creating a New Configuration	14
Appendix B – Setting Up Hitless Switching	18
Appendix C – Setting up GPIO for E5052A External Trigger	21
Appendix D – Confirming Revertive Switching	24

1. Bench Setup

Equipment used for this measurement are the RC21008A/RC31008A Evaluation Kit (EVK), Rohde & Schwarz SMA100A with the SMA-B29 module, and Agilent E5052A. The 10MHz Ref signal is needed to synchronize the SMA100A and the E5052A in order for the phase plot to be as flat as possible. Similar equipment and differential clock sources can be used as well.



1.1 RC21008A/RC31008A EVB Setup

Connect the USB-C cable to the host PC. Communications will be I²C. Ensure there is a method to connect a GPIO to the E5052A External Trigger.

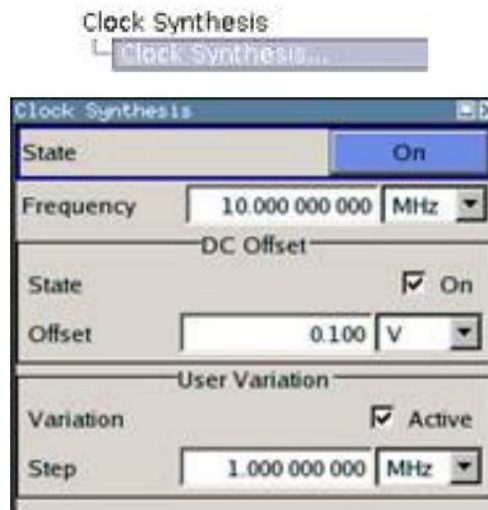
1.2 SMA100A Setup

There are three elements to be setup:

- RF out
- clk syn
- External reference enable

To setup the RF out, first push the **Frequency** button and enter the desired value. Second, push the **Level** button and enter **600mV**. Turn on the output.

To setup the clk syn, push the **Menu** button on the front panel. Navigate down to **Clock Synthesis**. Navigate down to Clock Synthesis and push the main knob to display the configuration menu.

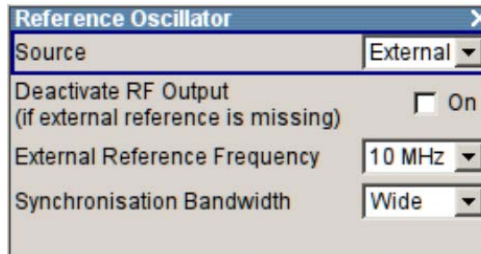


Enter the desired **Frequency** and set the **DC Offset** to 1.2V. For this example, we will be using 100MHz. The true signal is connected to CLKIN0 and the complimentary signal is connected to CLKIN1. The 180 degree phase offset is the worst case scenario. Enable the outputs by setting the state to **On**.

To setup the external reference, do one of the following:

- In the block diagram, select "RF > config... > RF Frequency > Reference Oscillator"
- Press the MENU key and select "RF > RF Frequency > Reference Oscillator"
- Press the SETUP key and select "Setup > System > Reference Oscillator"

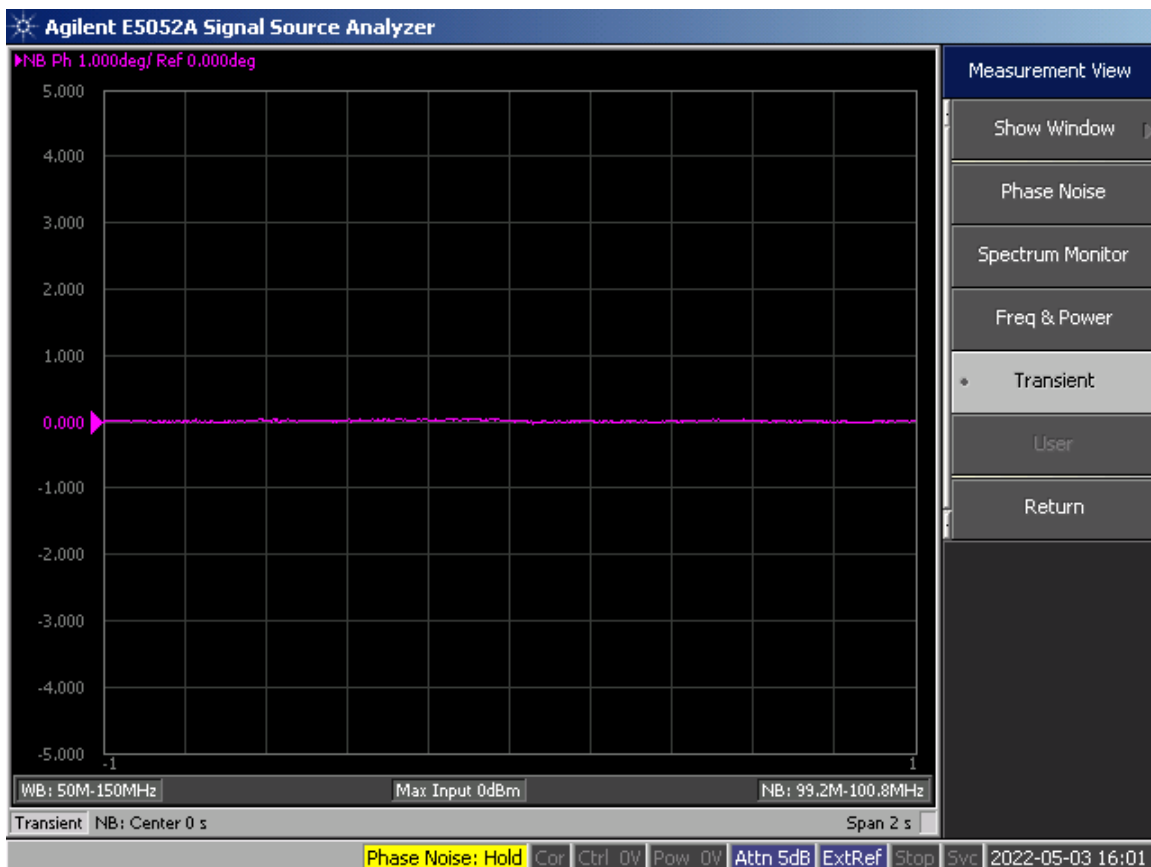
Select **External** for the "Source".



1.3 E5052A Setup

In order to measure hitless switching, the Transient feature of the E5052A will be used.

1. From the root menu, click on **Measurement View**.
2. Next, click **Transient**. By double-clicking the lower right of the screen, NB Ph, the plot will become full screen.
3. The full screen view of the Transient plot is now visible. Click **Return**.



The span for capturing data needs to be set.

1. Click the **Span** button.
2. For the Narrow Span setting, a value of 2 seconds will be used. Click on **Return** when done.

The scale of the y axis needs to be set.

1. Click the **Scale** button.
 - a. The typical specification for hitless switching is 100ps. To convert into degrees, use the following formula:
$$100 \text{ ps} \times 360^\circ \times (\text{output frequency})$$
 - b. The output frequency will be set to 100MHz which makes the datasheet specification limit 3.6 degrees. As a result, the deg/div will be set to '1'.

The X axis will need to be adjusted.

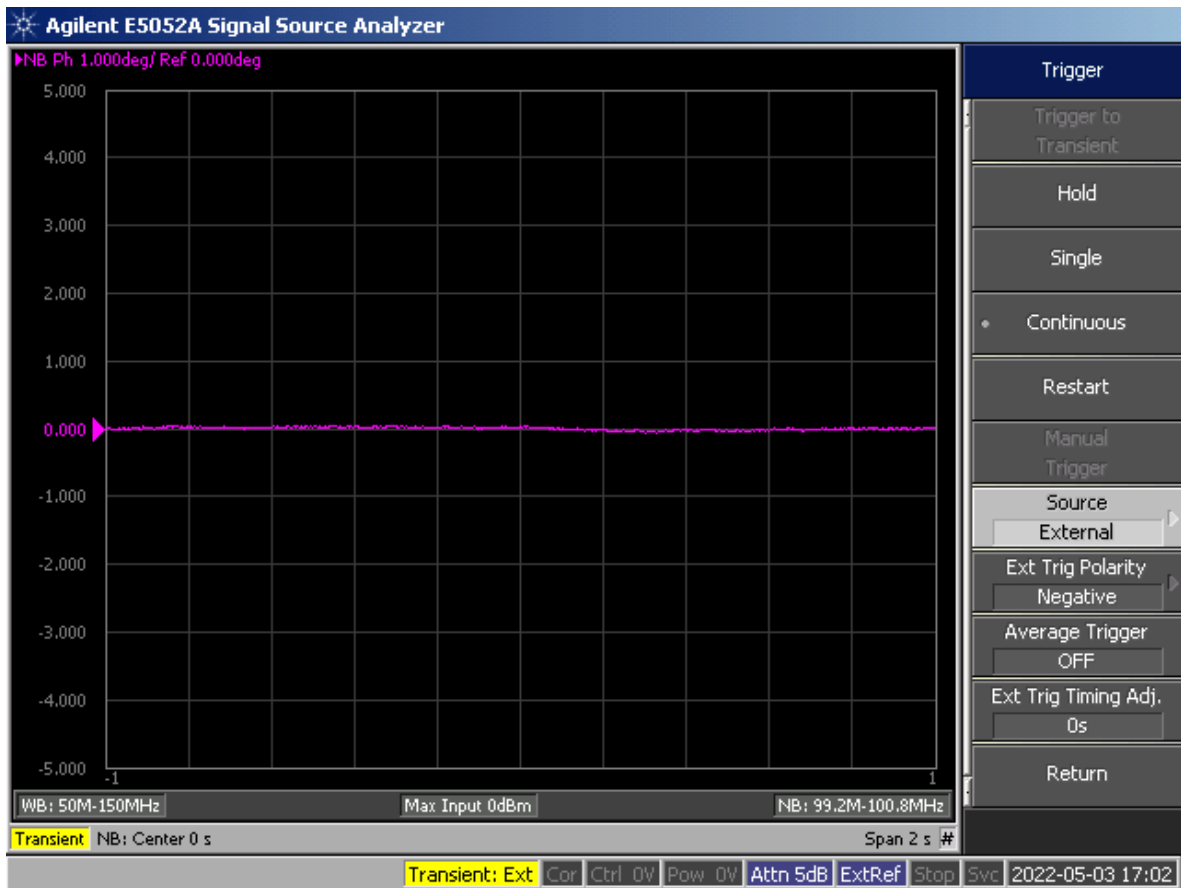
1. Click the X Axis button.
2. The Auto setting needs to be set to OFF, Left set to '-1', and Right set to '1'.

The next step is to setup the Transient measurement for the expected frequency of 100MHz.

1. Click **Setup**.
2. For this sub-menu, the WB Frequency will be set to 50MHz – 150MHz.
3. Target Frequency will be set to 100MHz.
4. Frequency Range will be set to 1.6MHz.
5. Phase Reference will be set to 100MHz.
6. Click **Return** when done.

The final step is to setup the Trigger to use Ext Trig.

1. Click the **Trigger** button.
2. Click Trigger to Transient.
3. Click **Continuous**. The phase plot should be very flat around 0 degrees.
4. Click **Source** and select **External**.
5. Select **Negative** for Ext Trig Polarity.



The last step is to connect GPIO4 of the EVB to the Ext Trig of E5052A. As the clock switch is occurring, the DPLL Lock Status will momentarily go Low.

2. RICBox Installation

For more information on installing RICBox software for VC7, see the [Renesas IC Toolbox User Guide](#).

3. Creating the Settings File

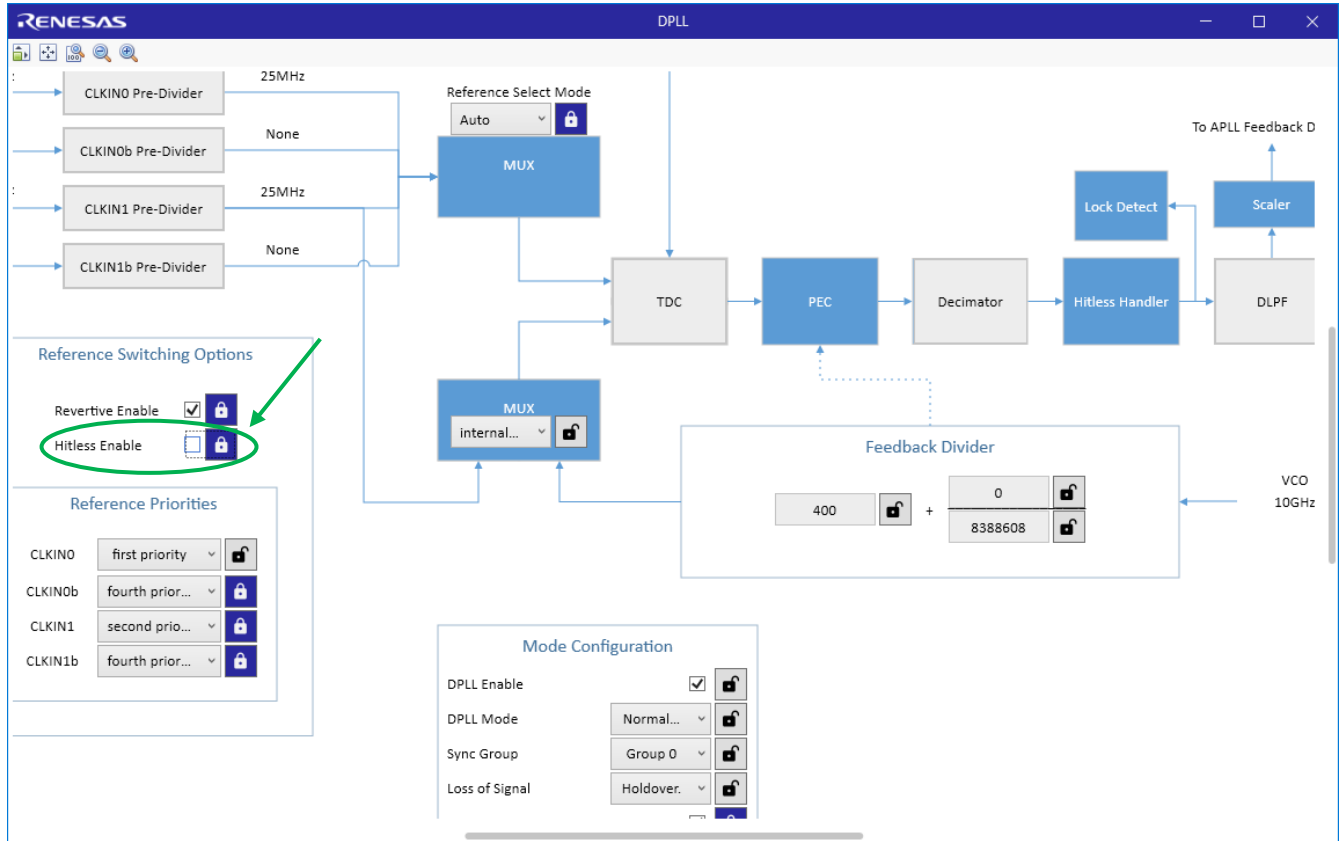
RICBox settings files or '.rbs' files are used to save and distribute custom device configurations. Each settings file contains all of the register settings for a given device. For more information, see Appendix A, Appendix B, and Appendix C.

4. CLKIN Switching

In order to cause a switch, the clock signal connected to CLKIN0 must be removed. One way to accomplish this is to remove the cable connected to CLKIN0. Another way is to disable the clock generator connected to CLKIN0. The method used in this example will be to disable/enable the input buffer using RICBox. For more information, see Appendix D.

4.1 Non-Hitless Switching vs Hitless Switching

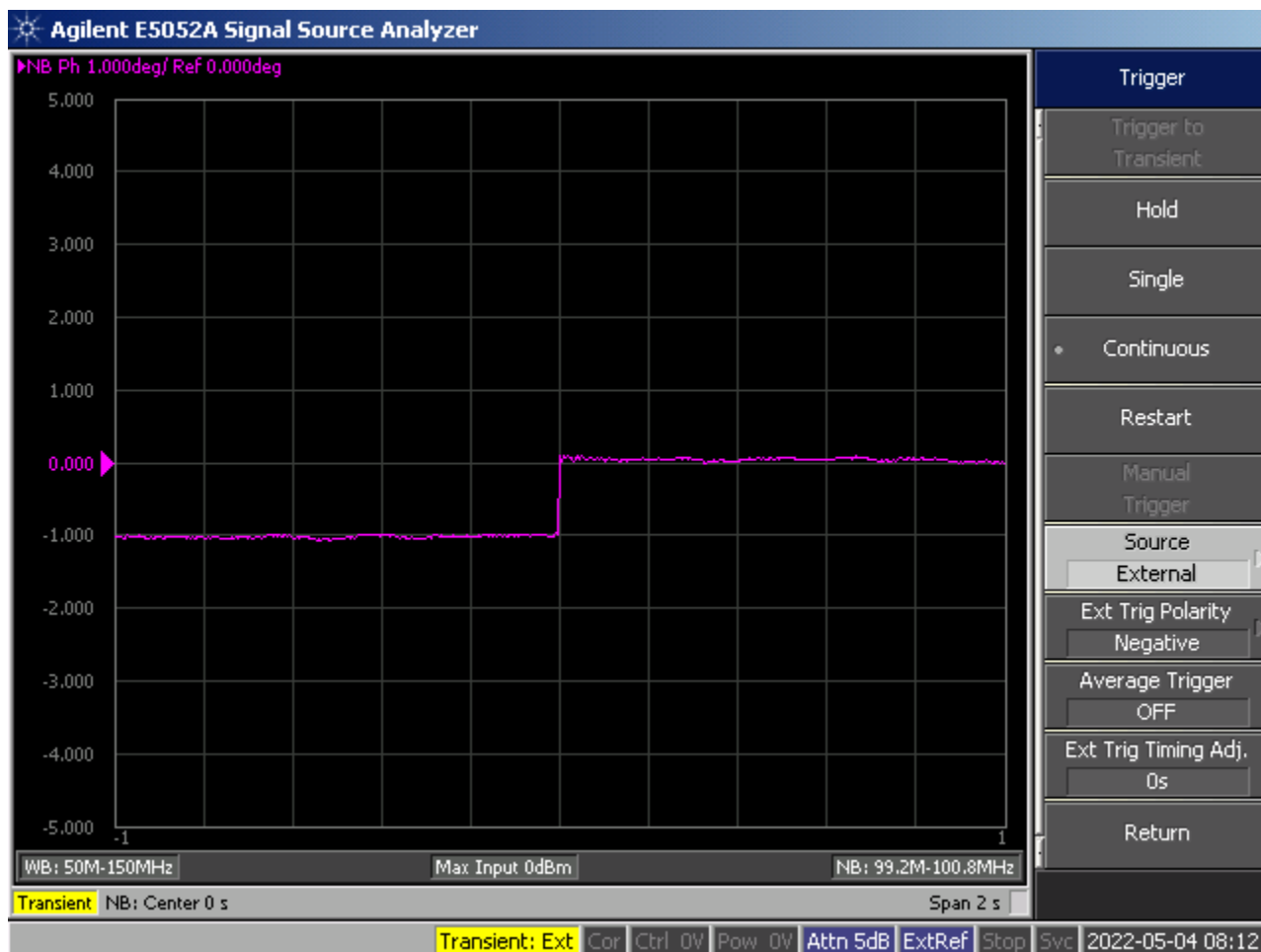
Hitless Switching can be disabled by un-checking Hitless Enable in the DPLL sub diagram.



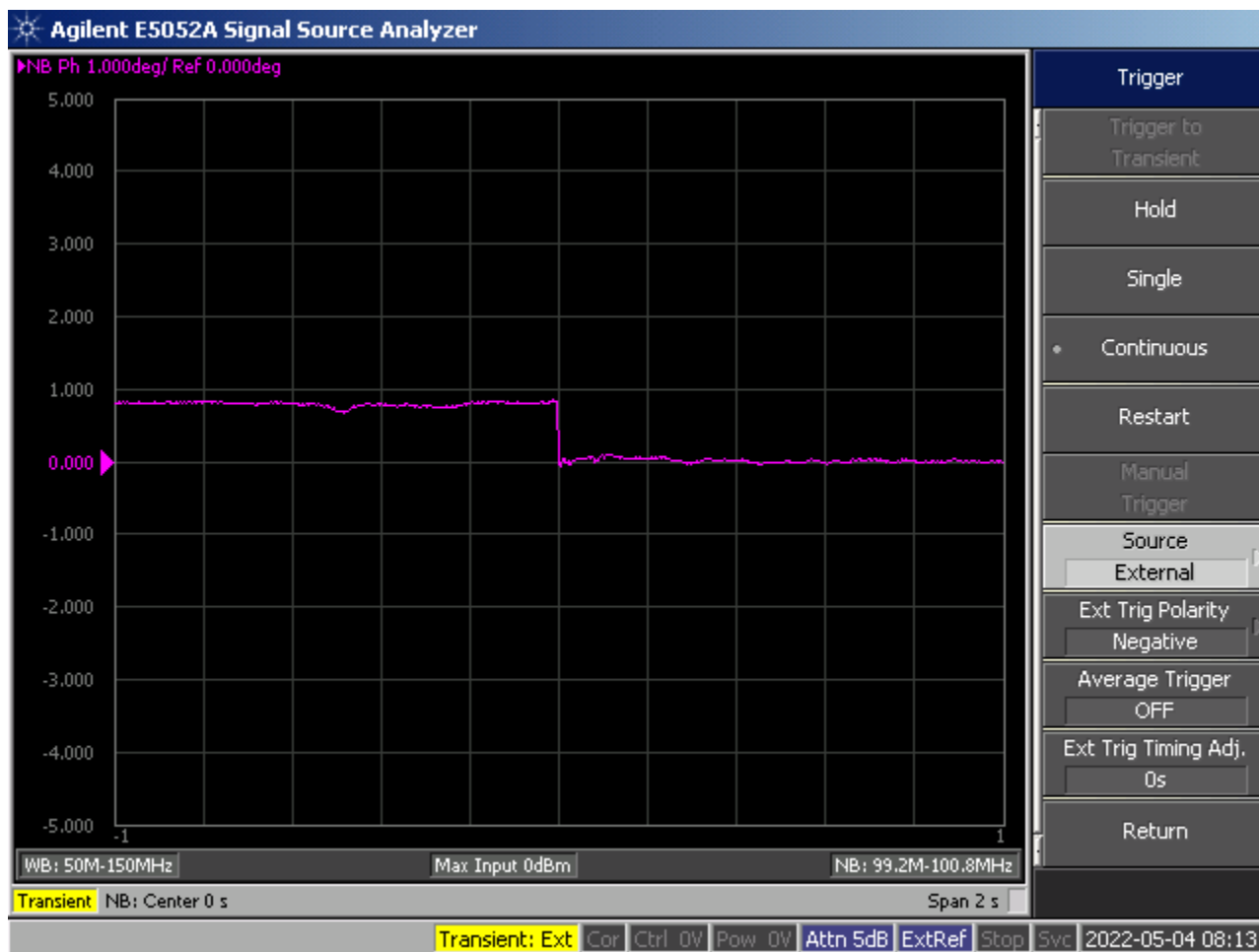
4.2 Hitless Switching

Force a switch using one of the methods mentioned in [CLKIN Switching](#).

- CLKIN0 to CLKIN1



- CLKIN1 to CLKIN0

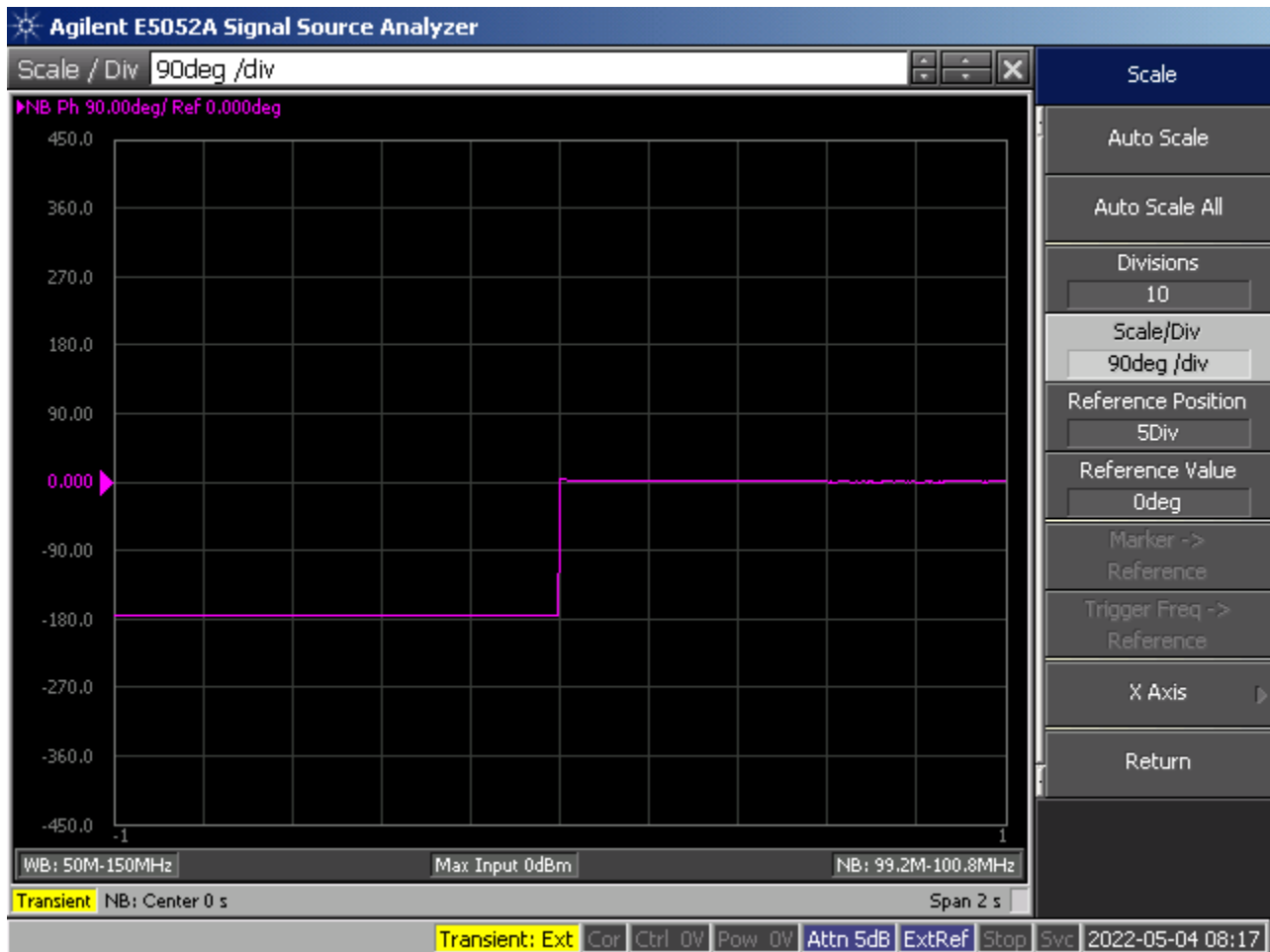


With Hitless enabled, the delta in degrees will be around or less than the datasheet typical specification of 3.6 degrees.

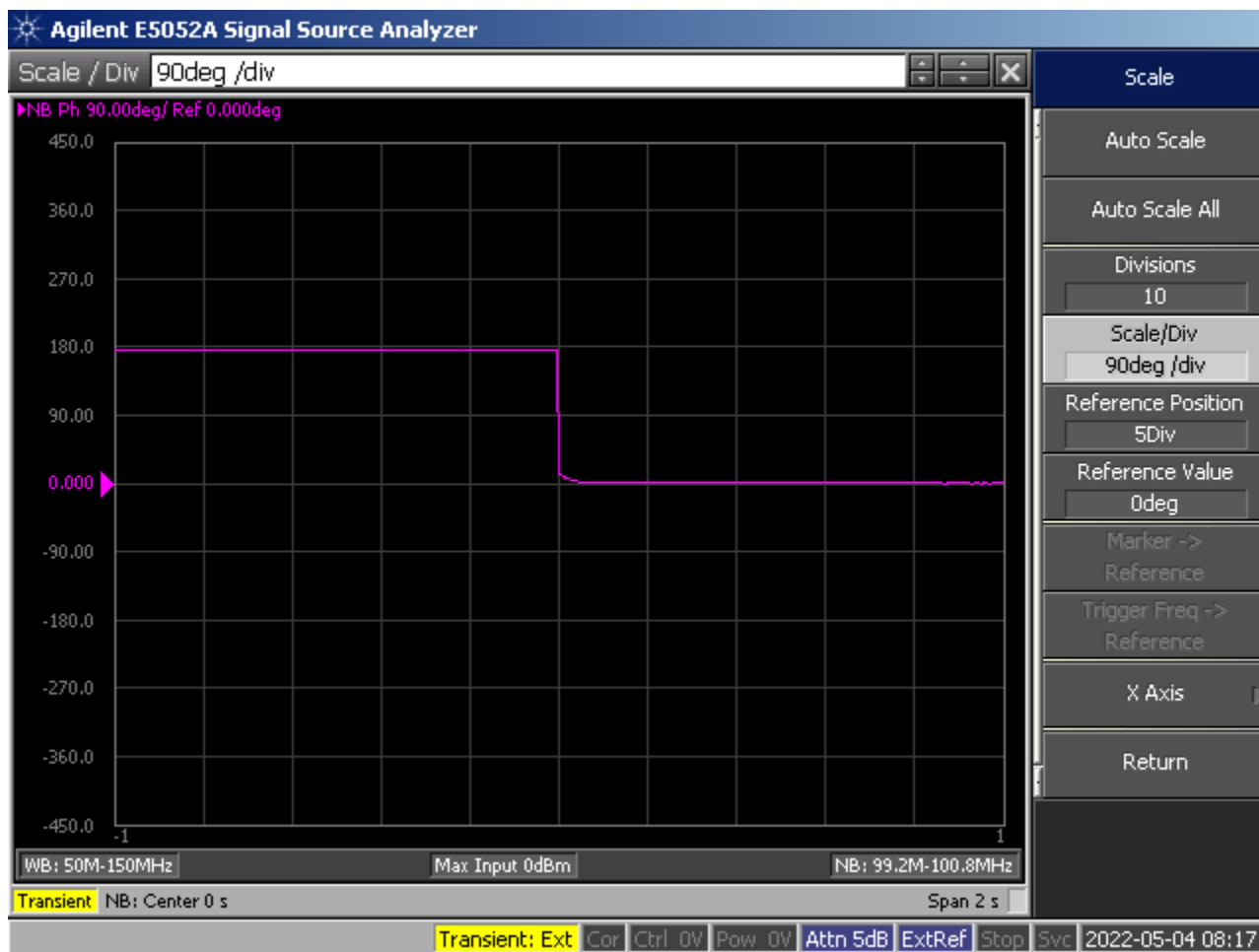
4.3 Non-Hitless Switching

To view this transition, the E5052A Scale/Div setting was set to 90 deg/div. As mentioned earlier, a single LVDS clock source was used to supply CLKIN0 and CLKIN1. The true side of the LVDS signal is connected to CLKIN0 while the complementary side is connected to CLKIN1. This creates a worst case scenario as the input clocks are 180 degrees out of phase. Next, force a switch to CLKIN1 and then back to CLKIN0.

- CLKIN0 to CLKIN1



- CLKIN1 to CLKIN0

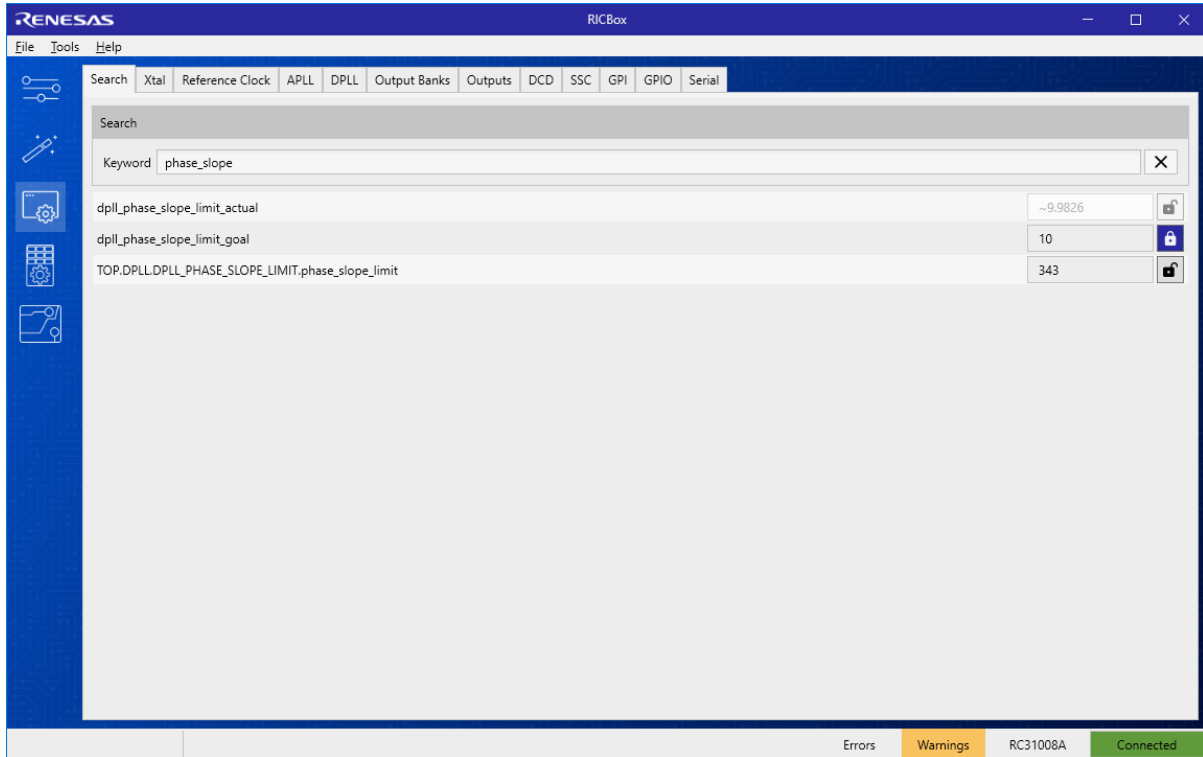


4.4 Phase Slope Limit

During a hitless switch from one input clock to another, the transition is “abrupt”. The phase slope limiter can be used to limit how fast a transition is allowed.

To set the phase slope limit:

1. Click on **Configuration** view in RICBox.
2. Enter ‘phase_slope’ in the **Keyword** field and click enter.
3. In the field called ‘dpll_phase_slope_limit_goal’, enter ‘10’.



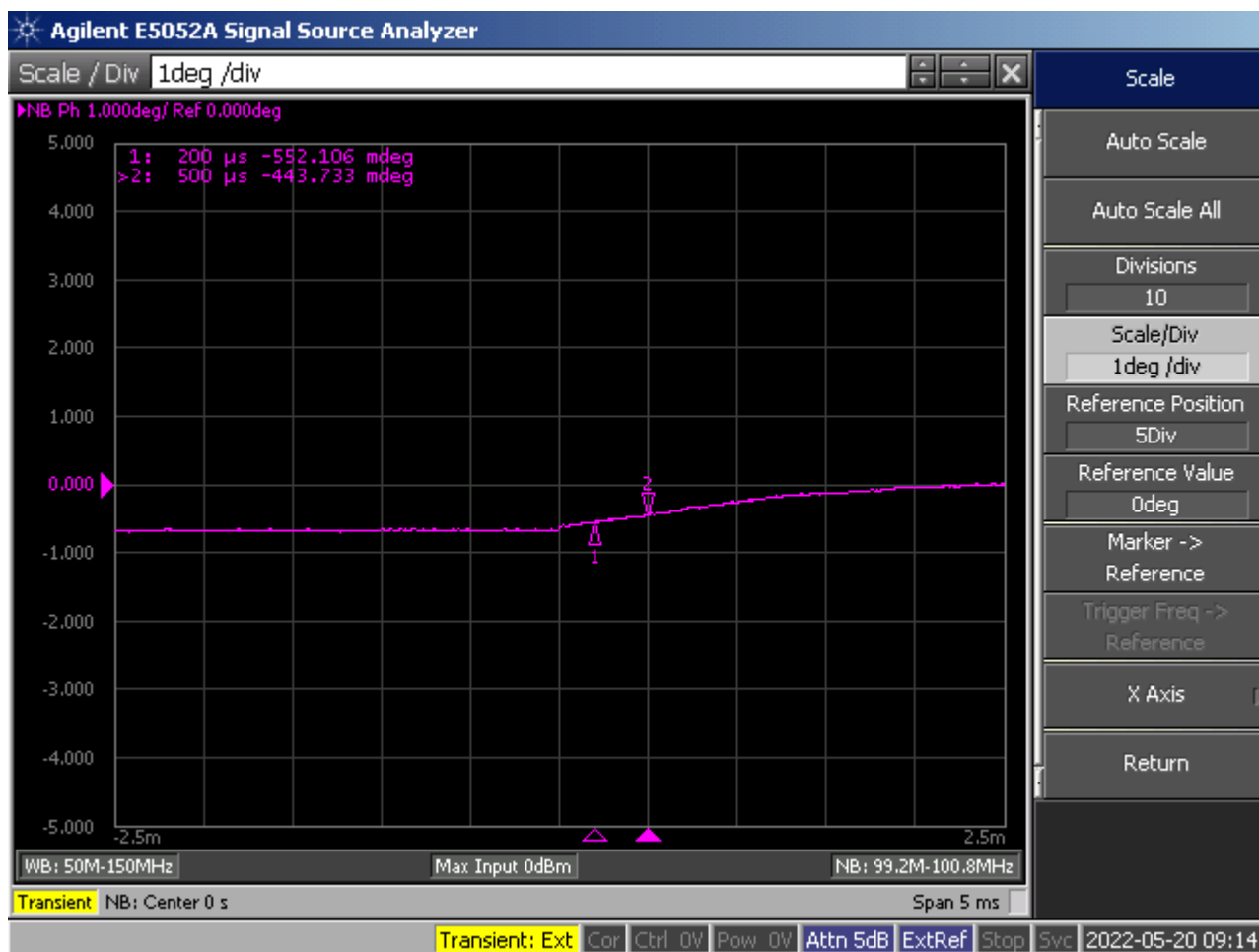
4. Move to the E5052A and set the Span to 5ms and adjust the X axis to display -2.5ms to 2.5ms.
5. Cause a hitless switch.
6. Add two markers to measure the phase.
7. Use the following formula to convert to ns/s:

$$\frac{(y_2 - y_1)}{(x_2 - x_1)} \times \frac{10^9}{(360^\circ \times output_frequency)}$$

where the y values are phase measurement in degrees and the x values are time in seconds.

For this measurement, we have the following data.

X	Y
200e-6 seconds	-0.552106 degrees
500e-6 seconds	-0.443733 degrees



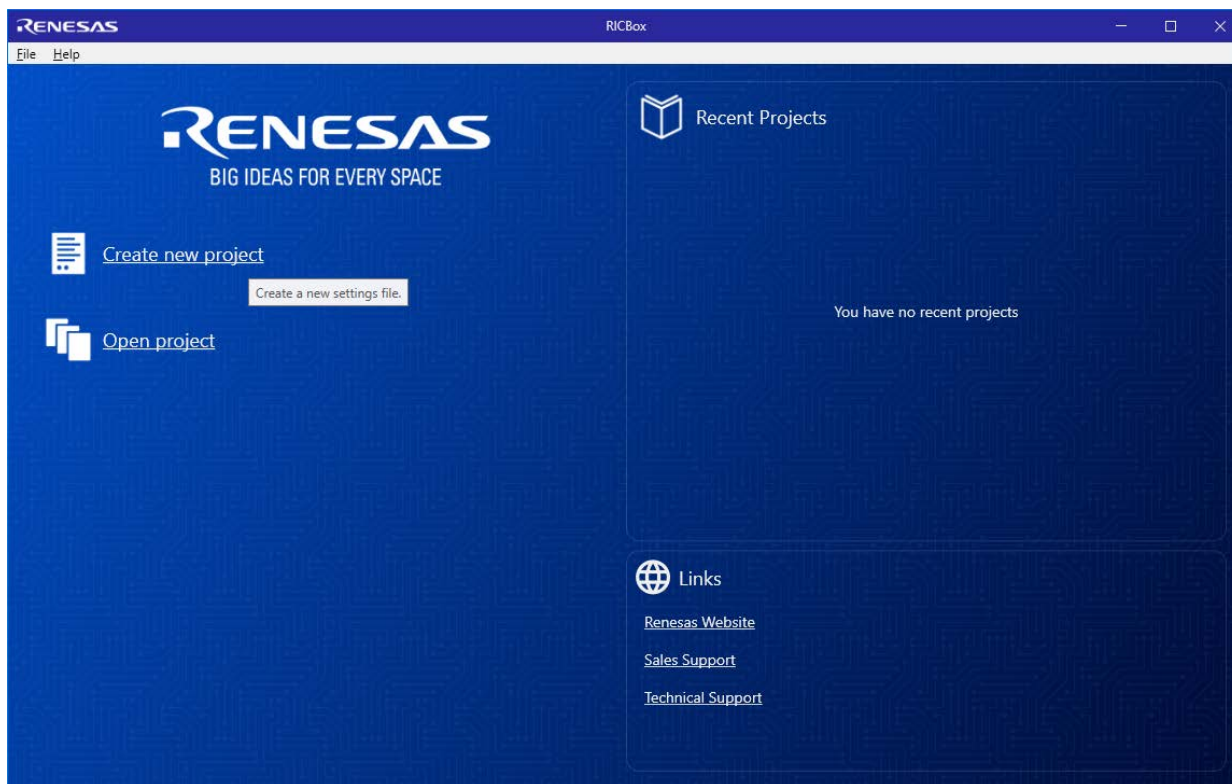
$$\frac{(-0.443733 - -0.552106)}{(500 - 200) \times 10^{-6}} \times \frac{10^9}{(360^\circ \times 100 \times 10^6 \text{Hz})} = 10.035 \text{ ns/s}$$

5. Revision History

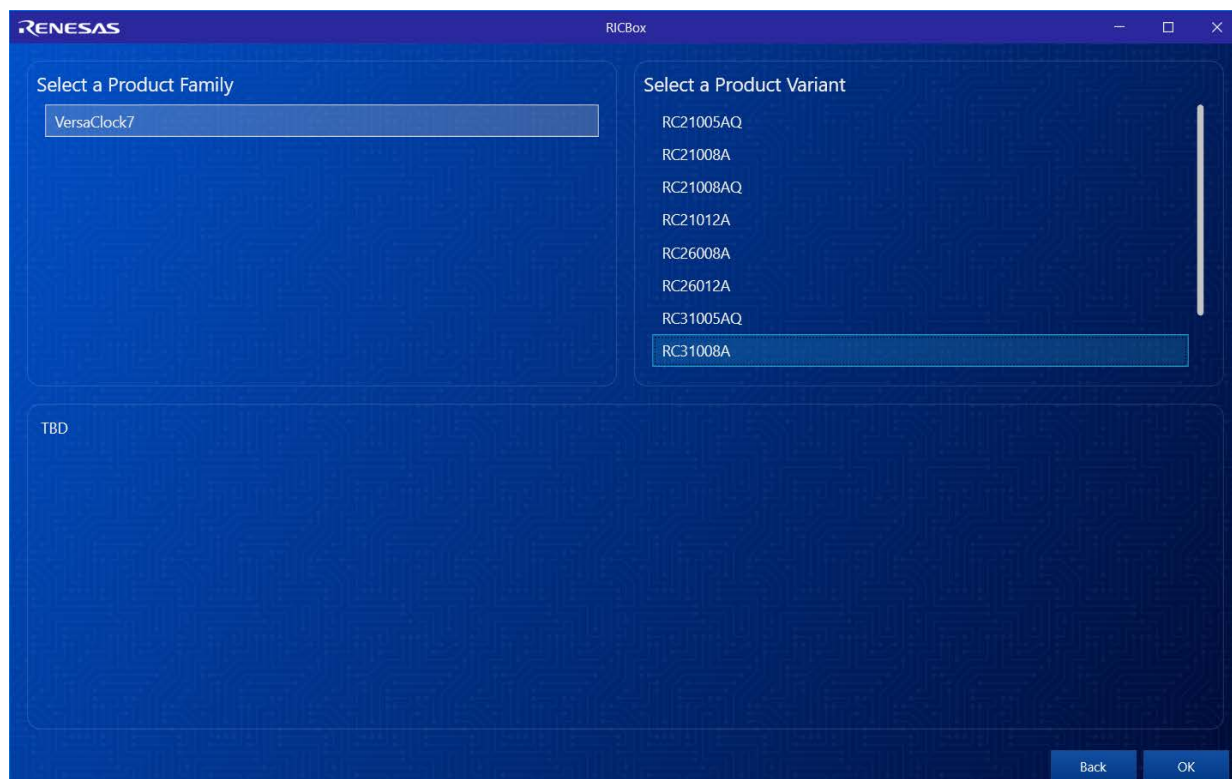
Revision	Date	Description
1.00	Aug 5, 2022	Initial release.

Appendix A – Creating a New Configuration

To create a new configuration, open RICBox and click on **Create new project**.



Choose RC31 device to be configured and push OK.



VersaClock 7 RC21/RC31 Series – Measurement of Hitless Switching

Configure the RC31 for **Jitter Attenuator** mode and enter the information to match your setup. For this example, the input clock will be 100MHz LVDS. The True signal will be connected to CLKIN0 and the Complimentary signal will be connected to CLKIN1. Click **Next** to go to the DPLL page.

Configuring RC31008A 1 of 4 Inputs

Crystal

Operation Mode	Jitter Attenuator	🔒
Mode	Xtal	🔒
Frequency	60MHz	🔒
Load Capacitance (pF)	10.26	🔒

Reference Clocks

CLKIN0	100MHz	🔒	LVDS	🔒
CLKIN0b	None	🔒		
CLKIN1	100MHz	🔒	LVDS	🔒
CLKIN1b	None	🔒		

• XIN_REFIN / XOUT_REFINb supports fundamental crystals or can be overdriven with a differential or single-ended input.

• CLKIN0/CLKIN0b and CLKIN1/CLKIN1b support differential or single-ended input clocks.

Cancel **Next** Finish

Errors Warnings RC31008A Not Connected

VersaClock 7 RC21/RC31 Series – Measurement of Hitless Switching

DPLL settings can be adjusted here. Click **Next** to go to Spread Spectrum. Click **Next** to go to the Outputs page.

Configuring RC31008A 2 of 4 DPLL

Bandwidth

Normal Bandwidth Goal: 25Hz
Actual: ~23.8203Hz

Acquire Bandwidth Goal: 250Hz
Actual: ~222.3227Hz

Decimator

Decimator Bandwidth Goal: 2.5kHz
Actual: ~1.9428kHz

Gain Peaking

Normal Gain Peaking Goal: 0.2
Actual: ~0.1804

Acquire Gain Peaking Goal: 0.2
Actual: ~0.192 (-3.9756% from goal of 0.2)

Phase Slope Limit

Phase Slope Limit Goal: None
Actual: maximum

Cancel Previous **Next** Finish

Errors Warnings RC31008A Not Connected

The DPLL profile drop-down allows for quick configuration of the Renesas timing device for specific ITU-T equipment clock recommendations. Selecting a specific profile will configure the device the same way Renesas tests for ITU-T equipment clock compliance in our labs. Modifications to the configuration can be made, but care must be taken to make sure compliance is not broken.

For more complex clock trees, please contact Renesas for additional support.

Jitter Attenuator
=====

This profile configures the device for jitter attenuation of an input clock.

Key requirements:

- * DPLL Loop Filter Bandwidth: 25Hz (acceptable range is 0.1Hz ~ 12kHz)
- * DPLL Phase Slope Limit: Unlimited
- * DPLL Damping Goal: < 0.2dB

G.8262 EEC1 Sync Profile
=====

This profile configures the device for synchronous equipment clock (Option 1). This allows for proper network operation when timed from another network equipment clock or a higher-quality clock. The G.8262 recommendation contains two options for synchronous equipment clocks. The first option, referred to as Option 1, applies to synchronous equipment designed to interwork with networks optimized for the 2048 kbit/s hierarchy. These networks allow the worst-case synchronization reference chain as specified in Figure 8-5 of ITU-T G.8031.

Bank1 will be configured to source from IOD0 and output 100MHz. Click **Finish** when done.

Configuring RC31008A 4 of 4 Outputs

APLL Frequency: 10GHz

Bank 1

Power Down: []

Source: IOD0
Goal Frequency: 100MHz
Actual Frequency: 100MHz

Output 1
Mode: LPHC...
Settings: []

Bank 2

Power Down: [x]

Source: FOD1
Goal Frequency: None
Actual Frequency: 100MHz

Output 2
Mode: LPHC...
Settings: []

Output 3
Mode: LPHC...
Settings: []

Bank 3

Power Down: [x]

Source: FOD1
Goal Frequency: None

Output 6
Mode: LPHC...
Settings: []

Output 7
Mode: LPHC...
Settings: []

Cancel Previous **Finish**

Errors Warnings RC31008A Not Connected

Outputs are arranged in output banks and some output banks share multiple outputs.

Each output bank gets its frequency from the selected clock source.

VersaClock 7 RC21/RC31 Series – Measurement of Hitless Switching

Window showing a summary of the settings.

The screenshot displays the Renesas software interface for configuring the RC31008A. The window title is 'Untitled - RICBox'. The main settings panel is organized as follows:

- Settings**
 - Mode**
 - Operational Mode: JA
 - Input**
 - XTAL: 60MHz
 - XTAL load capacitance: 10.26 (0.0002ppt from goal of 10.26)
 - CLKIN0: 100MHz
 - CLKIN0b: None
 - CLKIN1: 100MHz
 - CLKIN1b: None
 - SysClock**
 - Quad sys clock: ~227.2727MHz
 - APLL**
 - APLL Frequency: 10GHz (29.8023ppt from goal of 10GHz)
 - Divider: ~83.3333 (83+44739243/2^27)
 - Loop Bandwidth: ~942.2456kHz
 - Phase Margin (degrees): ~59.2687
 - Third Pole Frequency: ~28.4205MHz
 - DPLL**
 - Enabled: yes
 - DPLL Frequency: 10GHz
 - Divider: 400 (400+0/8388608)
 - Normal Bandwidth: ~23.8203Hz
 - Acquire Bandwidth: ~222.3227Hz
 - Decimator Bandwidth: ~1.9428kHz
 - Outputs**
 - OUT1: 100MHz [LPHCSL]
 - OUT2: powered down (Hi-Z)
 - OUT3: powered down (Hi-Z)
 - OUT6: powered down (Hi-Z)
 - OUT7: powered down (Hi-Z)
 - OUT8: powered down (Hi-Z)
 - OUT10: powered down (Hi-Z)
 - OUT11: powered down (Hi-Z)
 - Output Banks**

The status bar at the bottom indicates: Errors | Warnings | RC31008A | Not Connected.

Appendix B – Setting Up Hitless Switching

Click the **Block Diagram** icon to view block diagram.

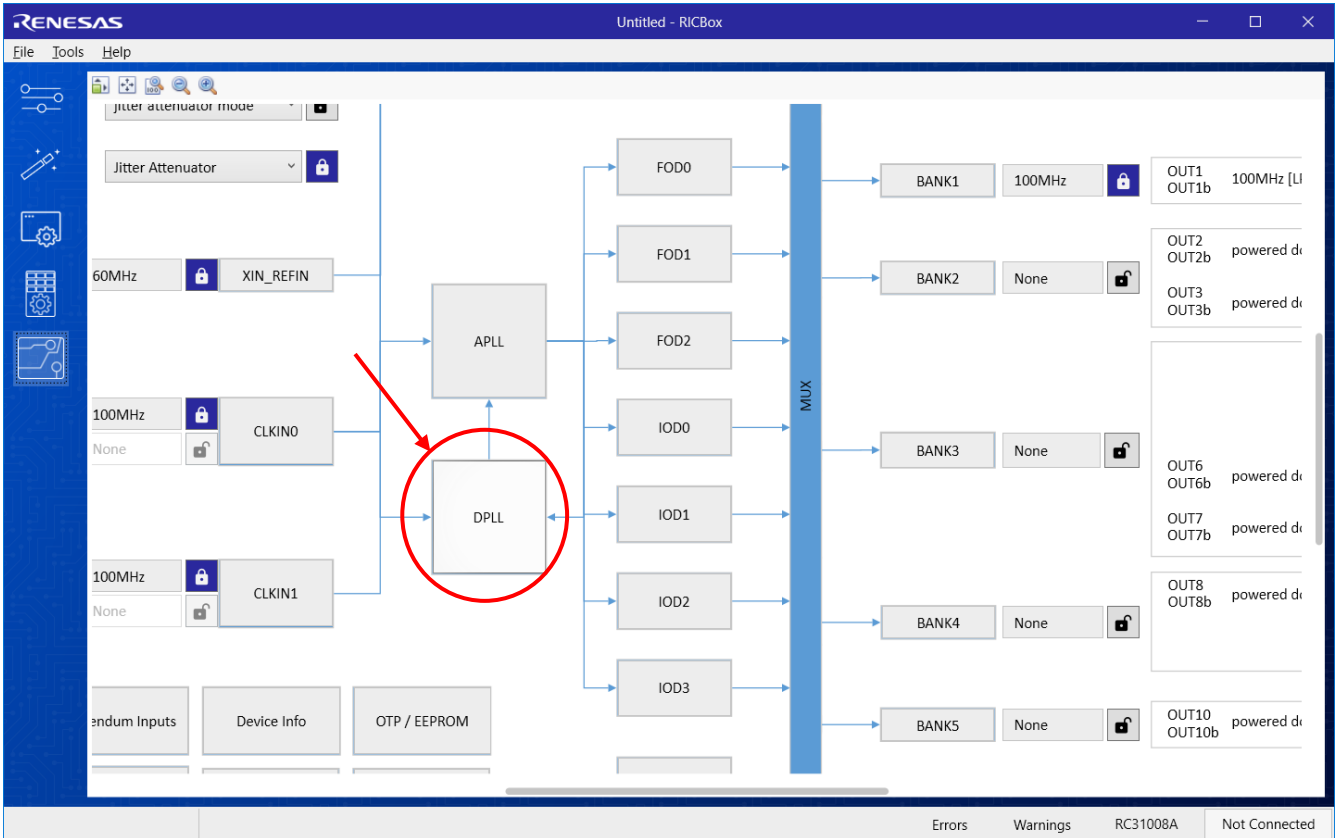
The screenshot shows the RENESAS RICBox software interface for device RC31008A. The 'SysClock' section is highlighted with a red circle and arrow, indicating the 'Quad sys clock' setting.

Section	Parameter	Value	
Settings	Mode	Operational Mode: JA	
	Input	XTAL: 60MHz	
Input	XTAL load capacitance	10.26 (0.0002ppt from goal of 10.26)	
	CLKIN0	100MHz	
	CLKIN0b	None	
	CLKIN1	100MHz	
	CLKIN1b	None	
SysClock	Quad sys clock	~227.2727MHz	
	APLL	APLL Frequency: 10GHz (29.8023ppt from goal of 10GHz)	
APLL	Divider	~83.3333 (83+44739243/2^27)	
	Loop Bandwidth	~942.2456kHz	
	Phase Margin (degrees)	~59.2687	
	Third Pole Frequency	~28.4205MHz	
DPLL	Enabled	yes	
	DPLL Frequency	10GHz	
	Divider	400 (400+0/8388608)	
	Normal Bandwidth	~23.8203Hz	
	Acquire Bandwidth	~222.3227Hz	
	Decimator Bandwidth	~1.9428kHz	
Outputs	OUT1	100MHz [LPHCSL]	
	OUT2	powered down (Hi-Z)	
	OUT3	powered down (Hi-Z)	
	OUT6	powered down (Hi-Z)	
	OUT7	powered down (Hi-Z)	
	OUT8	powered down (Hi-Z)	
	OUT10	powered down (Hi-Z)	
	OUT11	powered down (Hi-Z)	
	Output Banks		

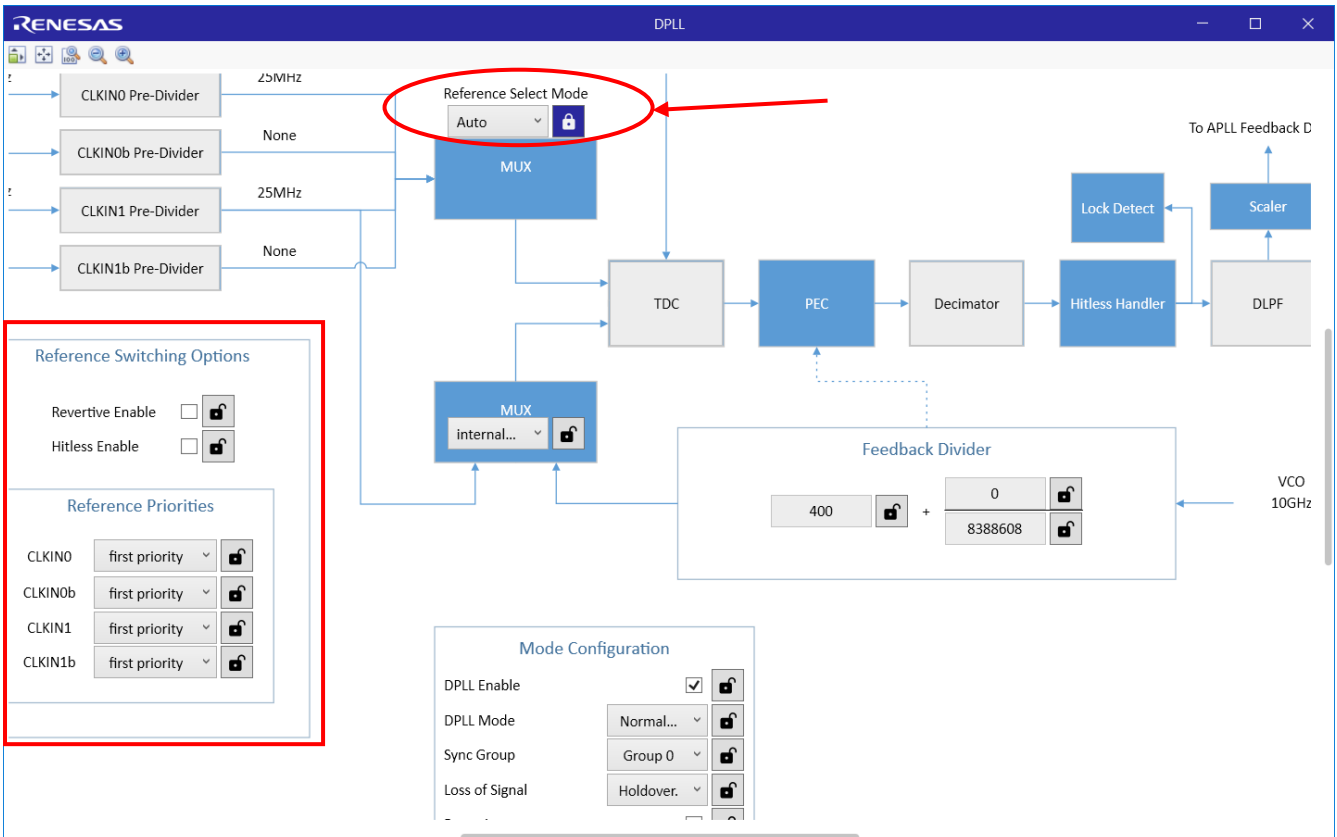
Errors Warnings RC31008A Not Connected

VersaClock 7 RC21/RC31 Series – Measurement of Hitless Switching

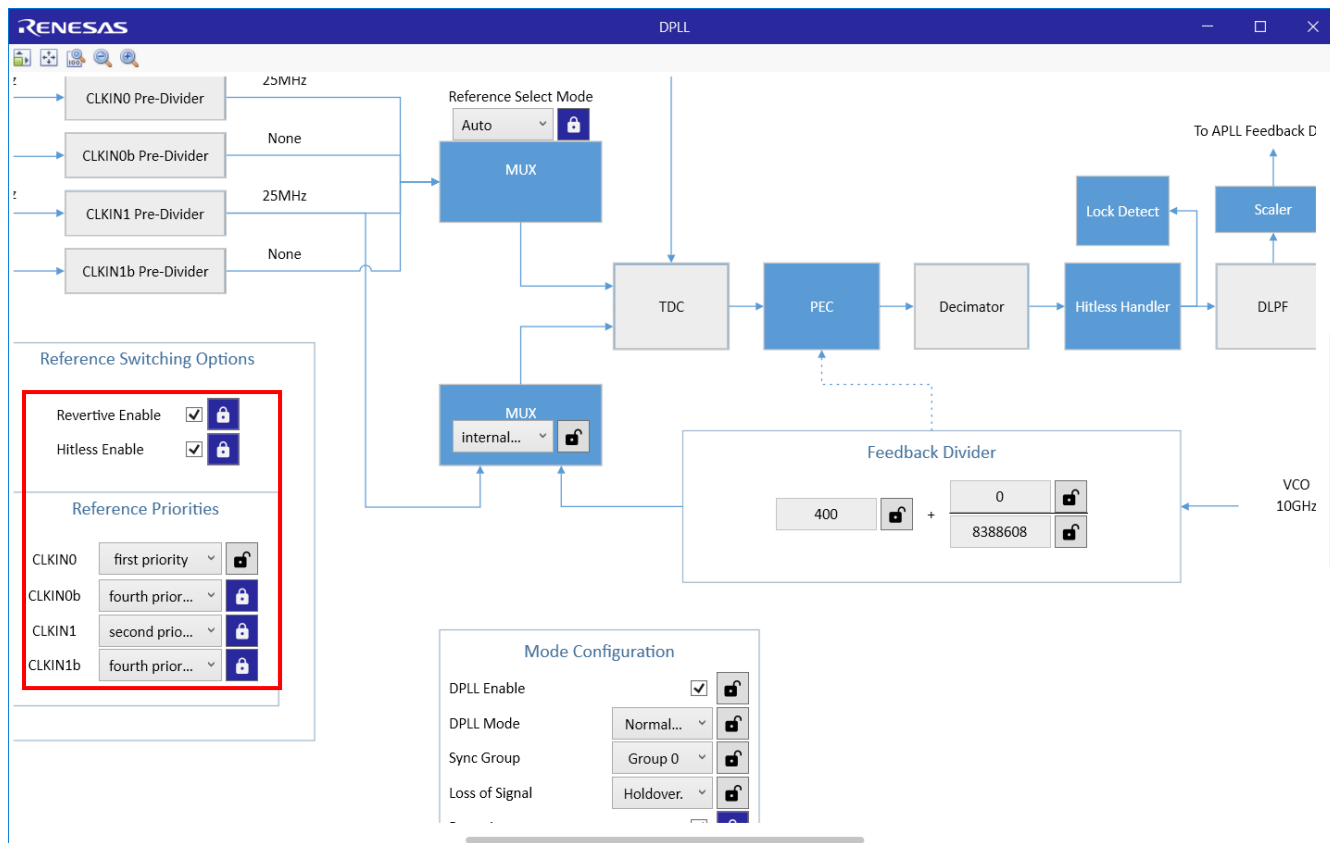
Click on the **DPLL** block to bring up the DPLL sub diagram.



For the **Reference Select Mode**, select **Auto**. This will display the **Reference Switching Options**.

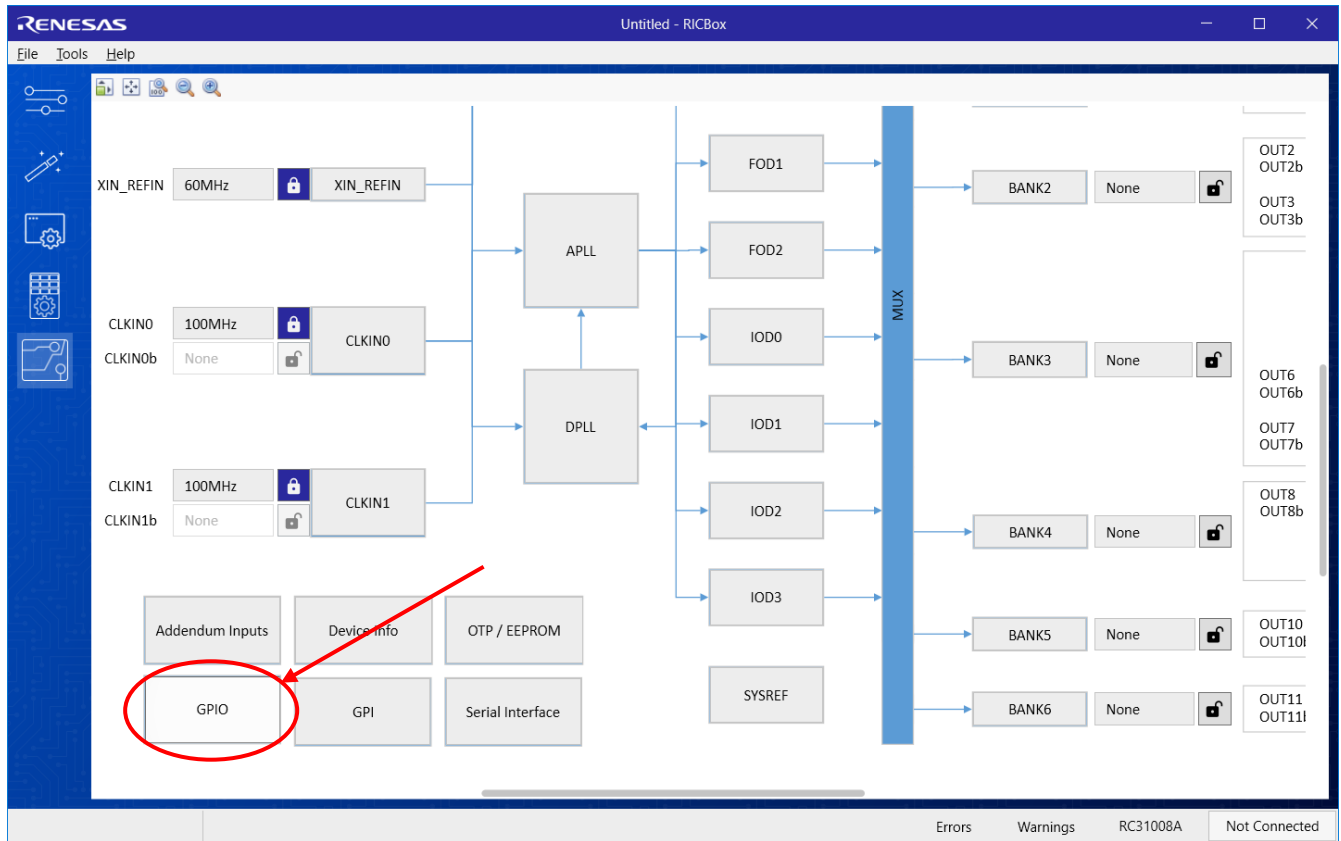


Next, click the boxes for **Revertive Enable** and **Hitless Enable**. Change CLKIN0b and CLKIN1b to **fourth priority**, and CLKIN1 to **second priority**.

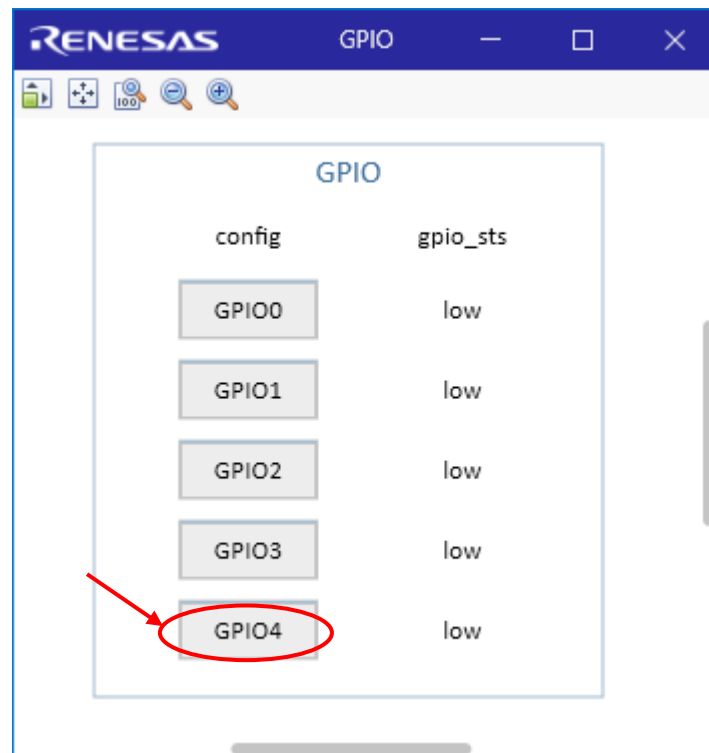


Appendix C – Setting up GPIO for E5052A External Trigger

For this example, GPIO4 is used as the External Trigger for the E5052A. To configure GPIO4, click the **GPIO** button.

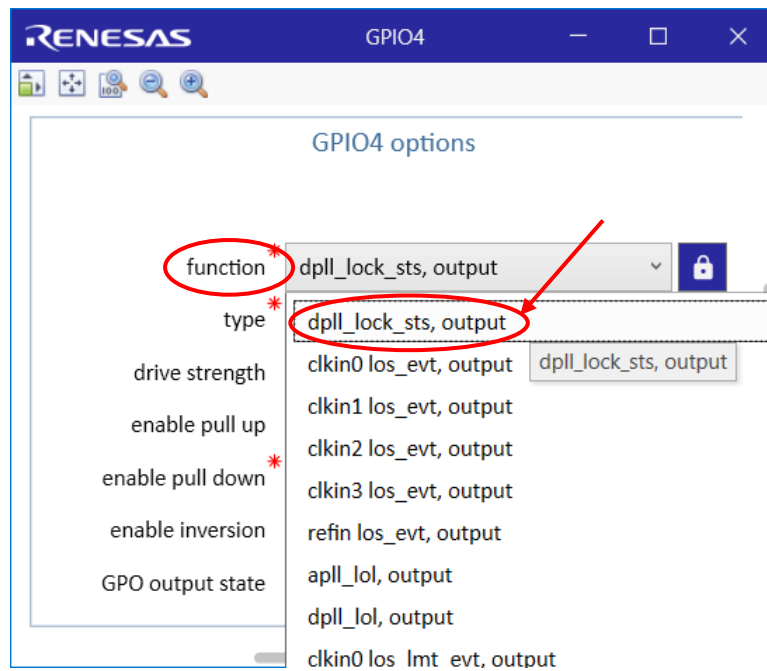


Click the **GPIO4** button.



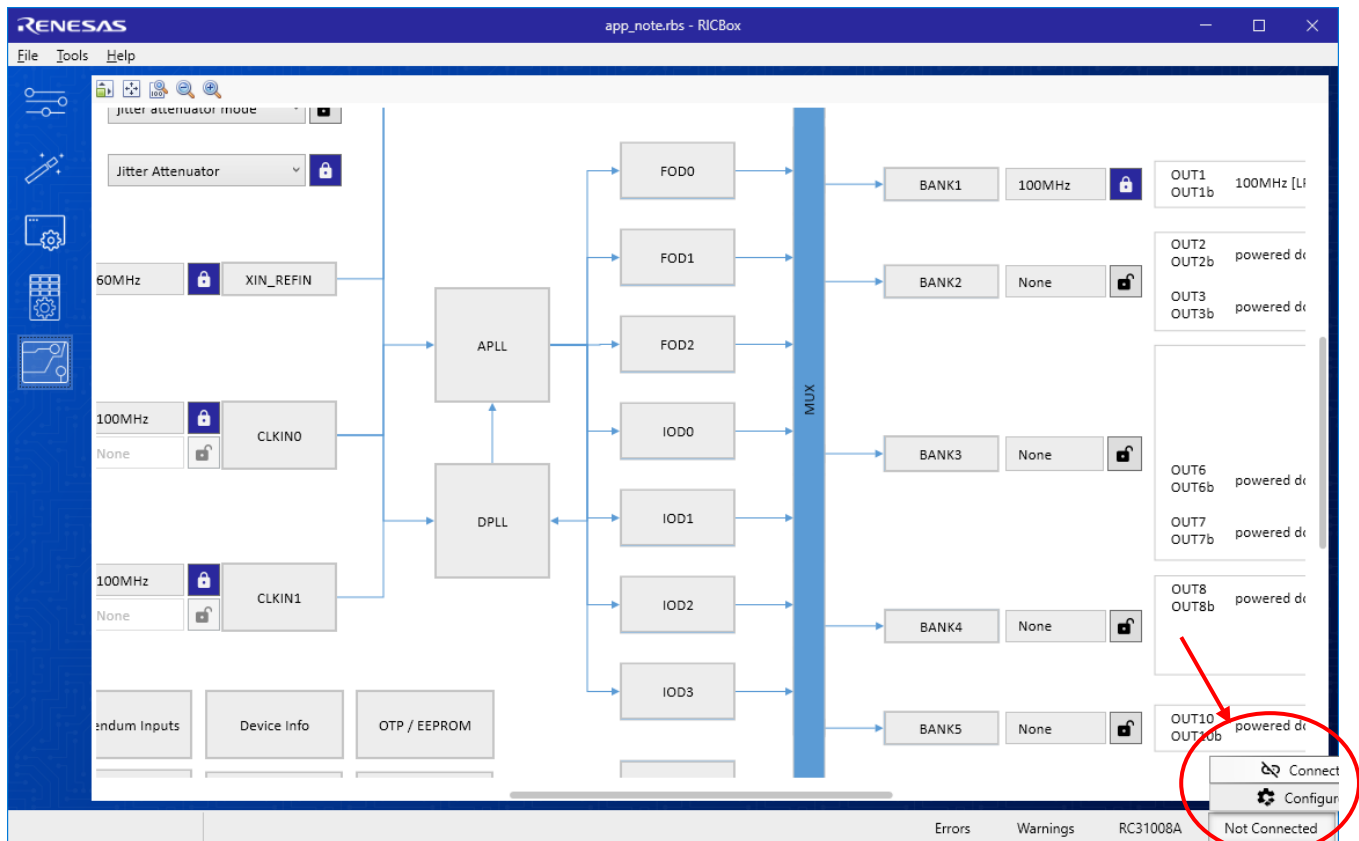
VersaClock 7 RC21/RC31 Series – Measurement of Hitless Switching

Find the **function** pull-down list and select 'dpll_lock_sts'. Close the GPIO4 window and close the GPIO window.

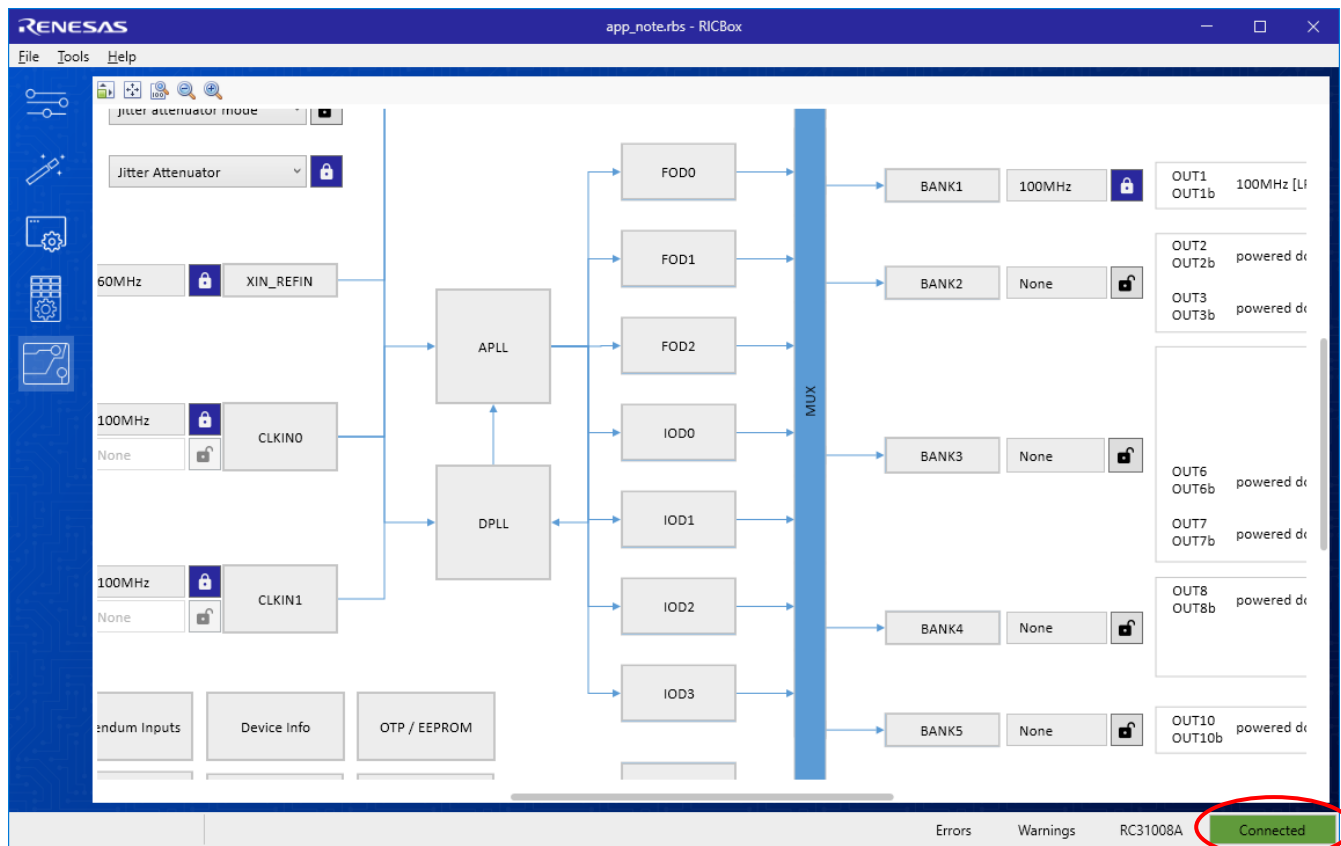


The 'dpll_lock_sts' will momentarily go from high to low as the clkln are switching. This transition will be used to trigger the E5052A.

After all settings are entered, click the **Not Connected** button in the lower right of the window and click **Connect**.

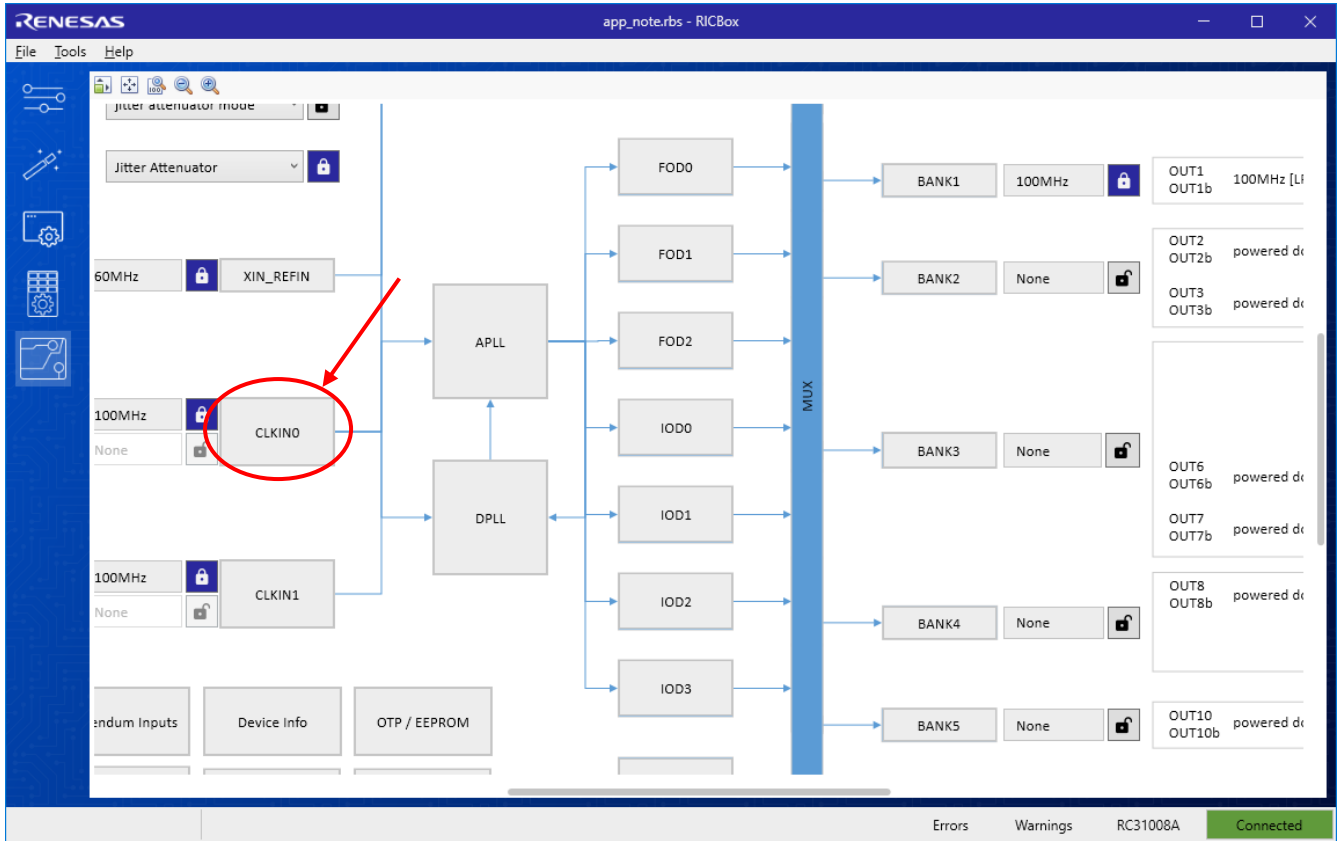


The button will turn **GREEN** and display **Connected**.

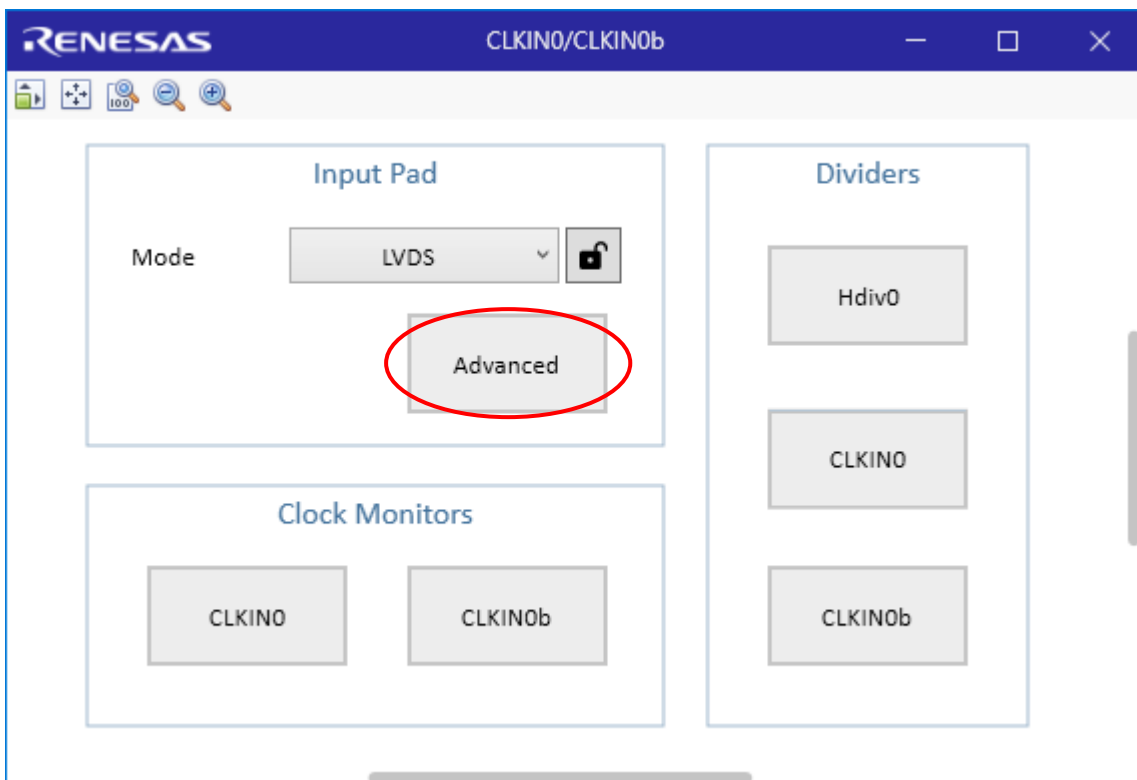


Appendix D – Confirming Revertive Switching

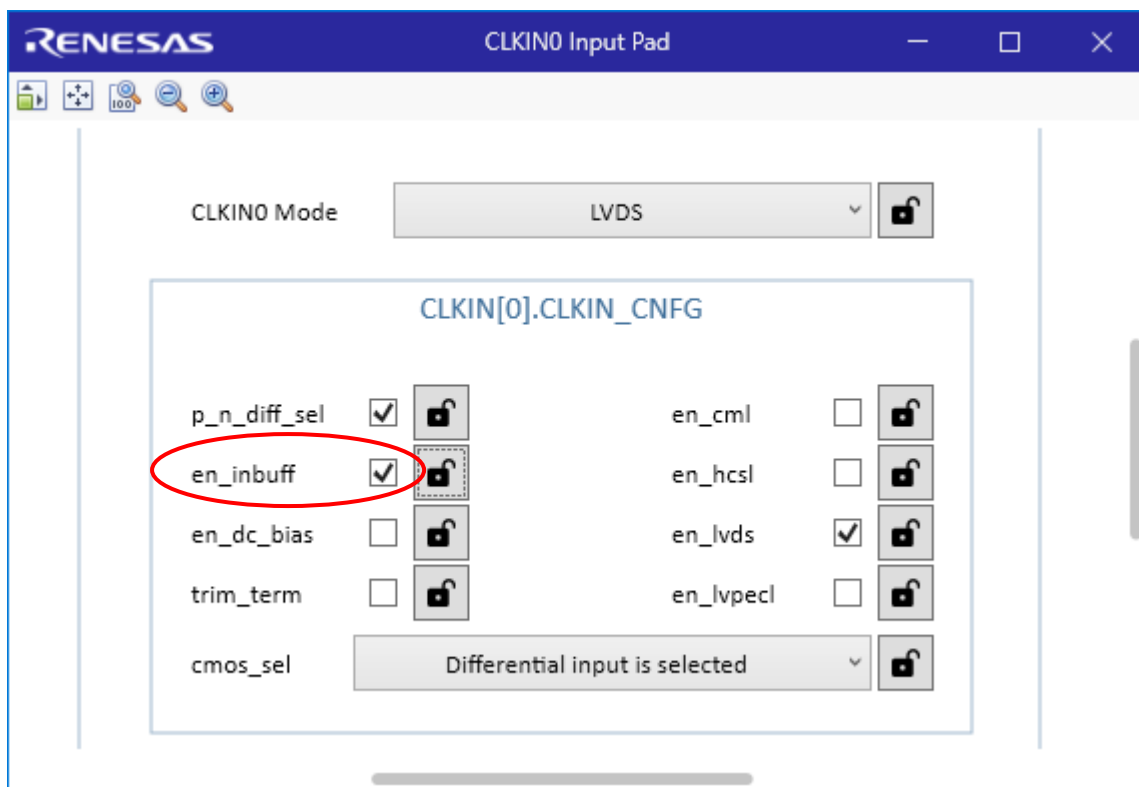
First, click on the **CLKIN0** block.



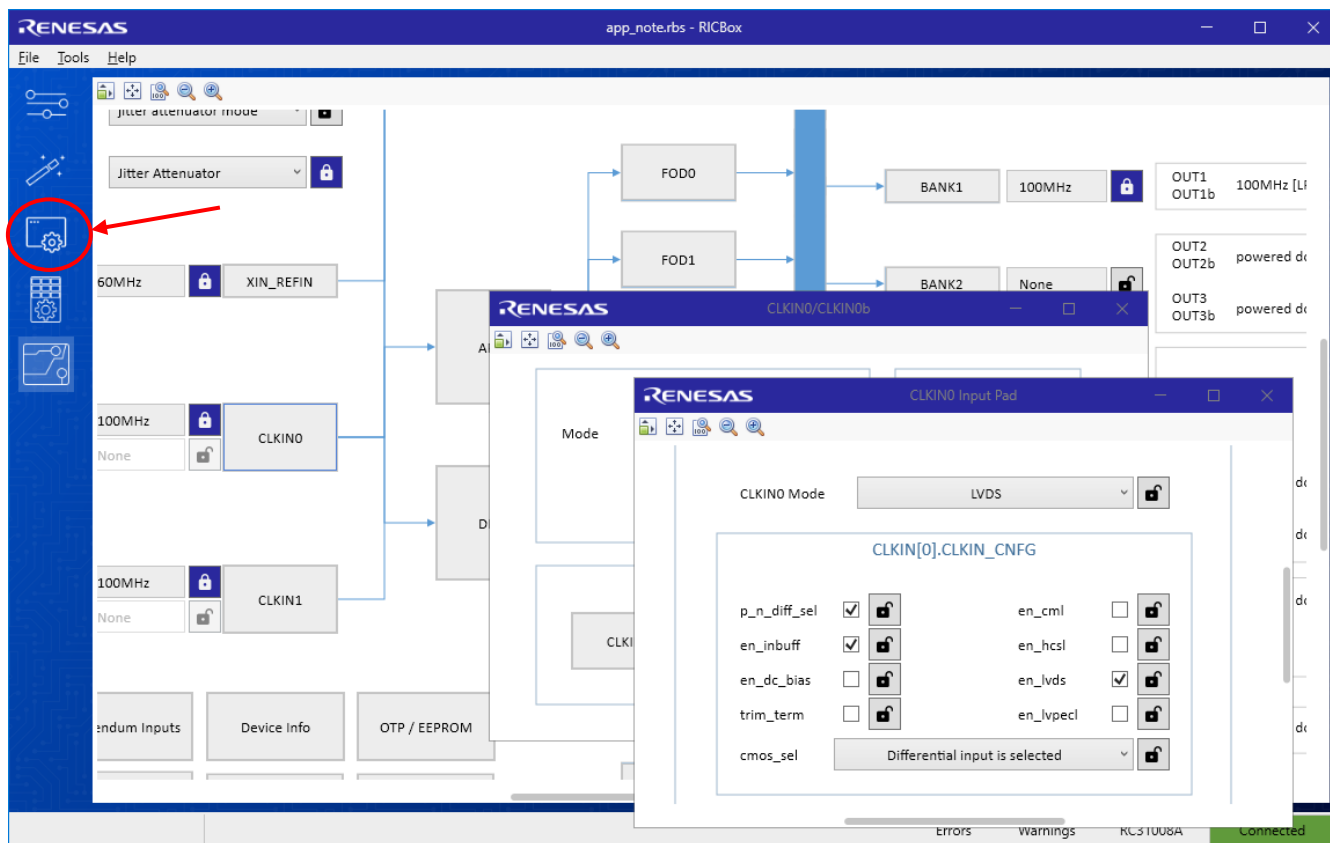
Next, click the **Advanced** button.



The control of interest is called 'en_inbuff'.

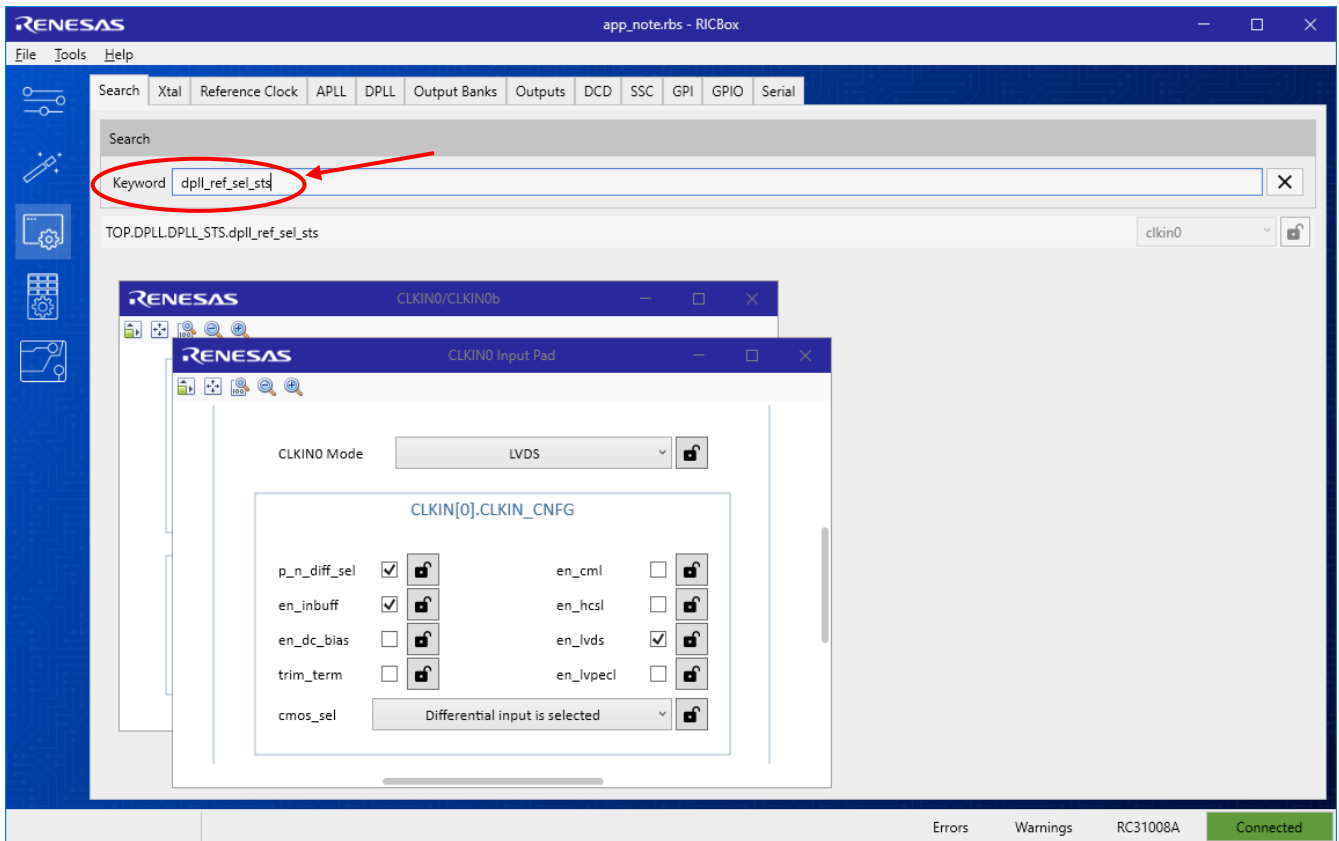


Click the icon shown below to switch over to Configuration view.

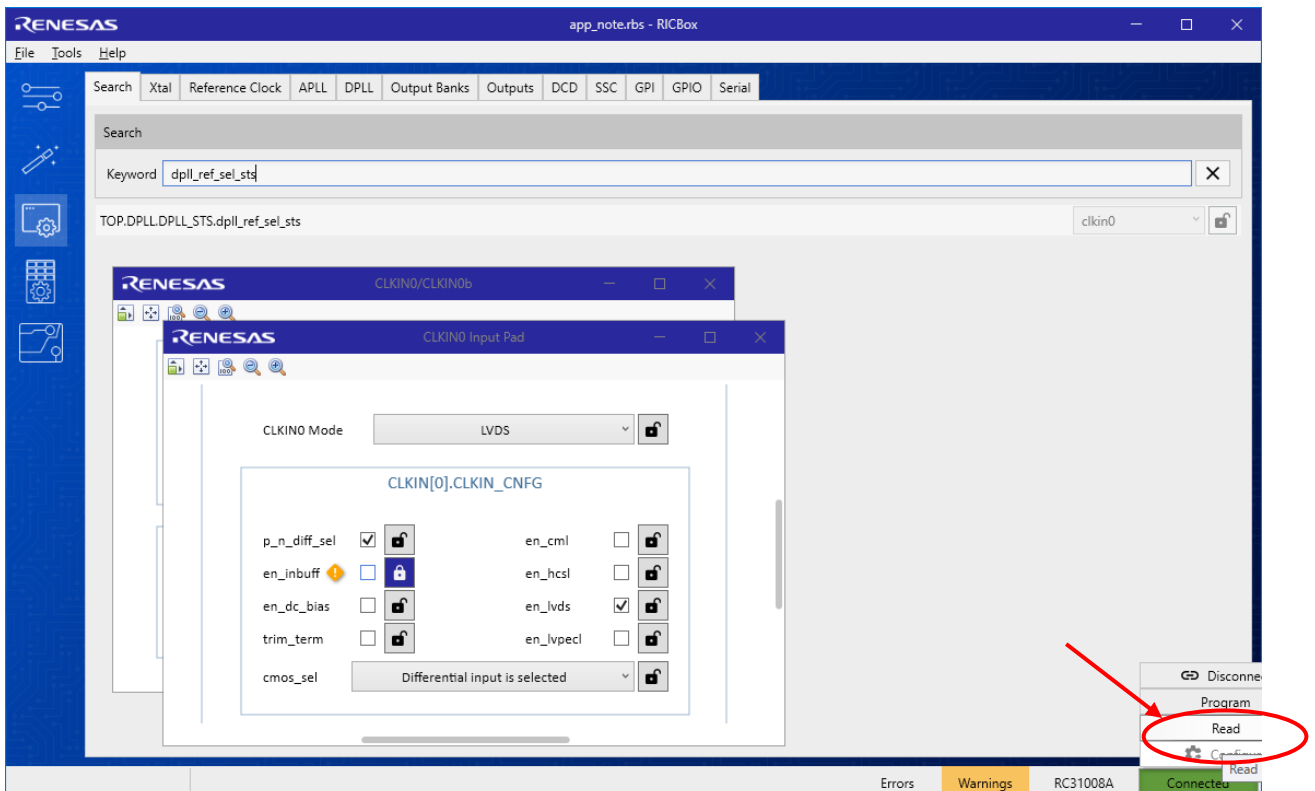


VersaClock 7 RC21/RC31 Series – Measurement of Hitless Switching

In the **Keyword** field, enter 'dpll_ref_sel_sts' and click enter. This register field will reflect the current selected reference that the DPLL is using.

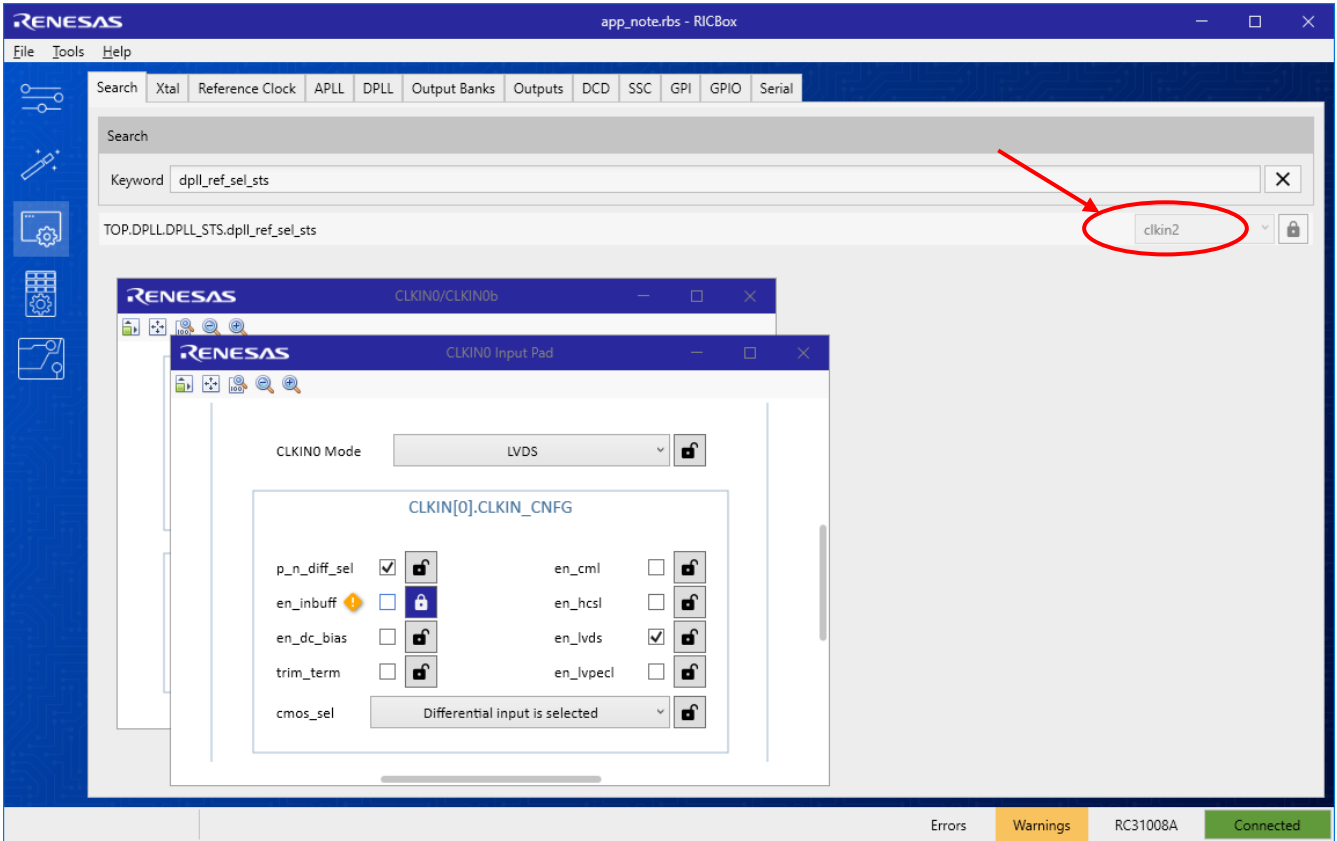


To force a switch, simply un-check 'en_inbuff' control. An updated transient plot on the E5052A will appear. Now click the green **Connected** button then click **Read**.

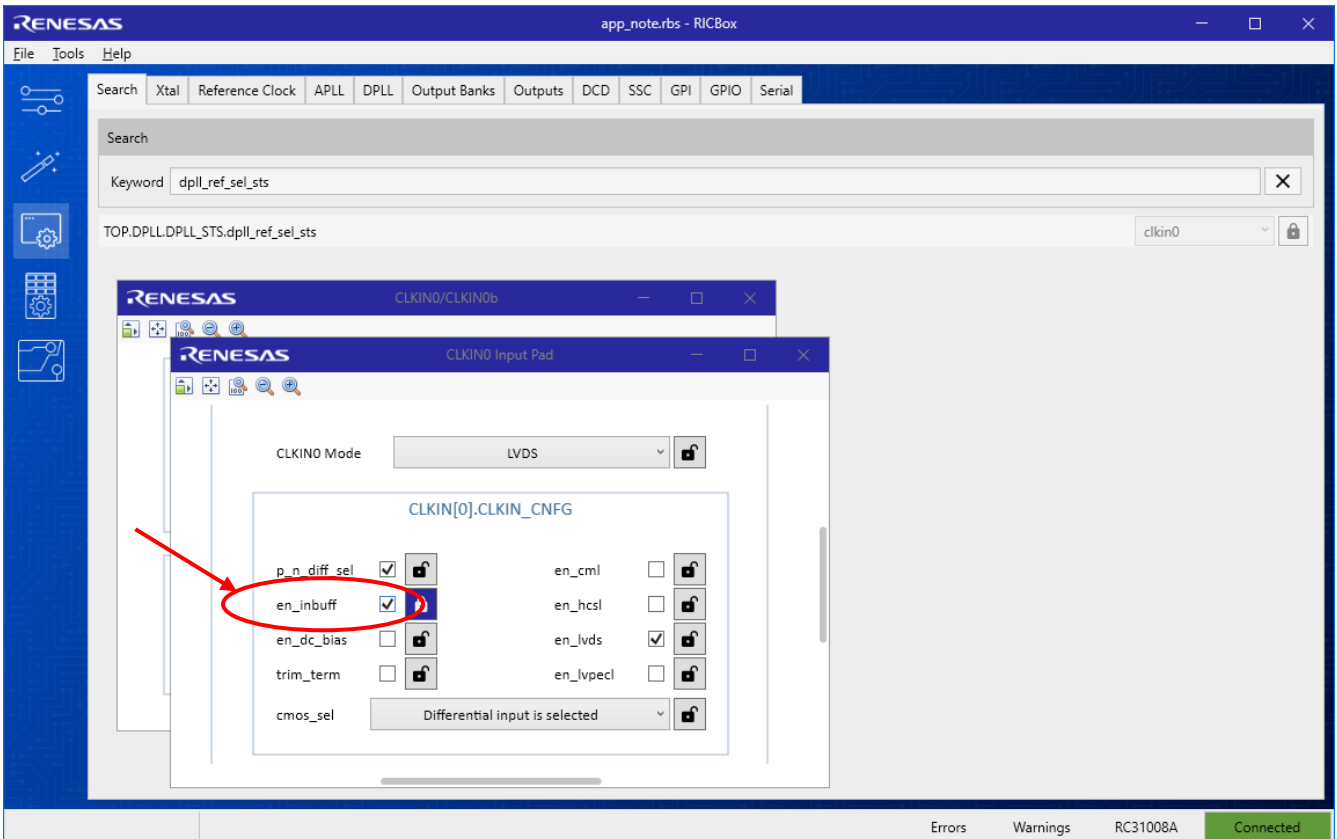


VersaClock 7 RC21/RC31 Series – Measurement of Hitless Switching

After clicking **Read**, the status field will be updated.



To cause a revertive switch back, simply check the 'en_inbuff' control and click **Read**.



IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.