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SH7263/SH7203 Group

Sample Application for the CAN Module (Data Frame Reception)

Introduction

This application note describes the controller area network module (RCAN-TL1) and provides an example of its application to data frame reception.

Target Devices

SH7263 and SH7203 Groups

Contents

1. Introduction

1.1 Specifications

- Transfer rate: 500 kbps
- Mailbox for transmission: Mailbox 0
- Received data frame is as follows.
  IDE: 0 (standard format), data length code (DLC): 2, and data: H'C1C2

1.2 Module Used

- Controller area network (RCAN-TL1): 1

1.3 Applicable Conditions

• MCU	SH7263/SH7203 (R5S72630/R5S72030)
• Clock operating mode	3 (the input from the USB_X1 pin is in use as the clock source)
• Operating frequency	Internal clock: 192 MHz Bus clock: 48 MHz Peripheral clock: 24 MHz
• C compiler:	SuperH RISC engine family C/C++ compiler package Ver.9.01Release01 from Renesas Technology
• Compiler options:	Default settings of the High-performance Embedded Workshop -cpu=sh2a -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1

1.4 Related Application Note

None

2. Description of the Sample Application

This sample program employs the RCAN-TL1 module to receive a data frame in standard format (IDE: 0).

2.1 Overview of Operations by the Module Used

The SH7203 CPU has two internal RCAN-TL1 modules that support CAN2.0B and comply with ISO-11898.

The RCAN-TL1 module has 32 programmable mailboxes, each supporting a reception filter mask, and a 16-bit timer function, providing for highly flexible communications. Figure 1 shows the structure of the RCAN-TL1 module. For details on the module, refer to the section on the controller area network in the *SH7203 Group Hardware Manual*.

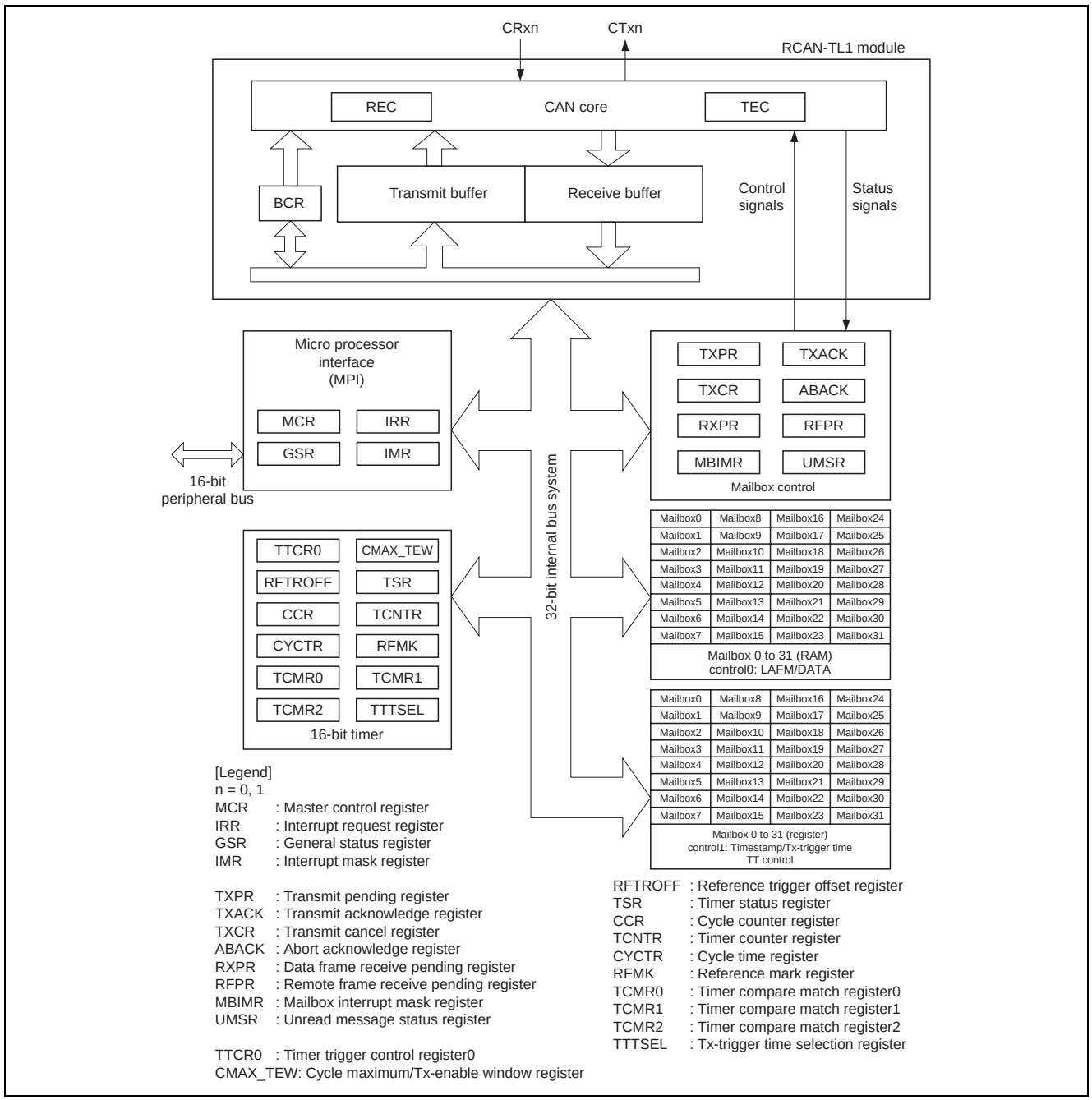


Figure 1 Structure of the RCAN-TL1 Module

2.2 Procedure for Setting the Module Used

This section describes initial settings for the reception of data frames by the RCAN-TL1 module.

Initial settings of the module are made in reset mode (configuration mode). On subsequent release from reset mode, the RCAN-TL1 module participates in CAN-bus activity. In initial settings in this sample program, one mailbox is set for transmission and reception respectively. Figures 2 and 3 show examples of the flow of initialization for the RCAN-TL1 module. For details on settings made to individual registers, refer to the *SH7203 Group Hardware Manual*.

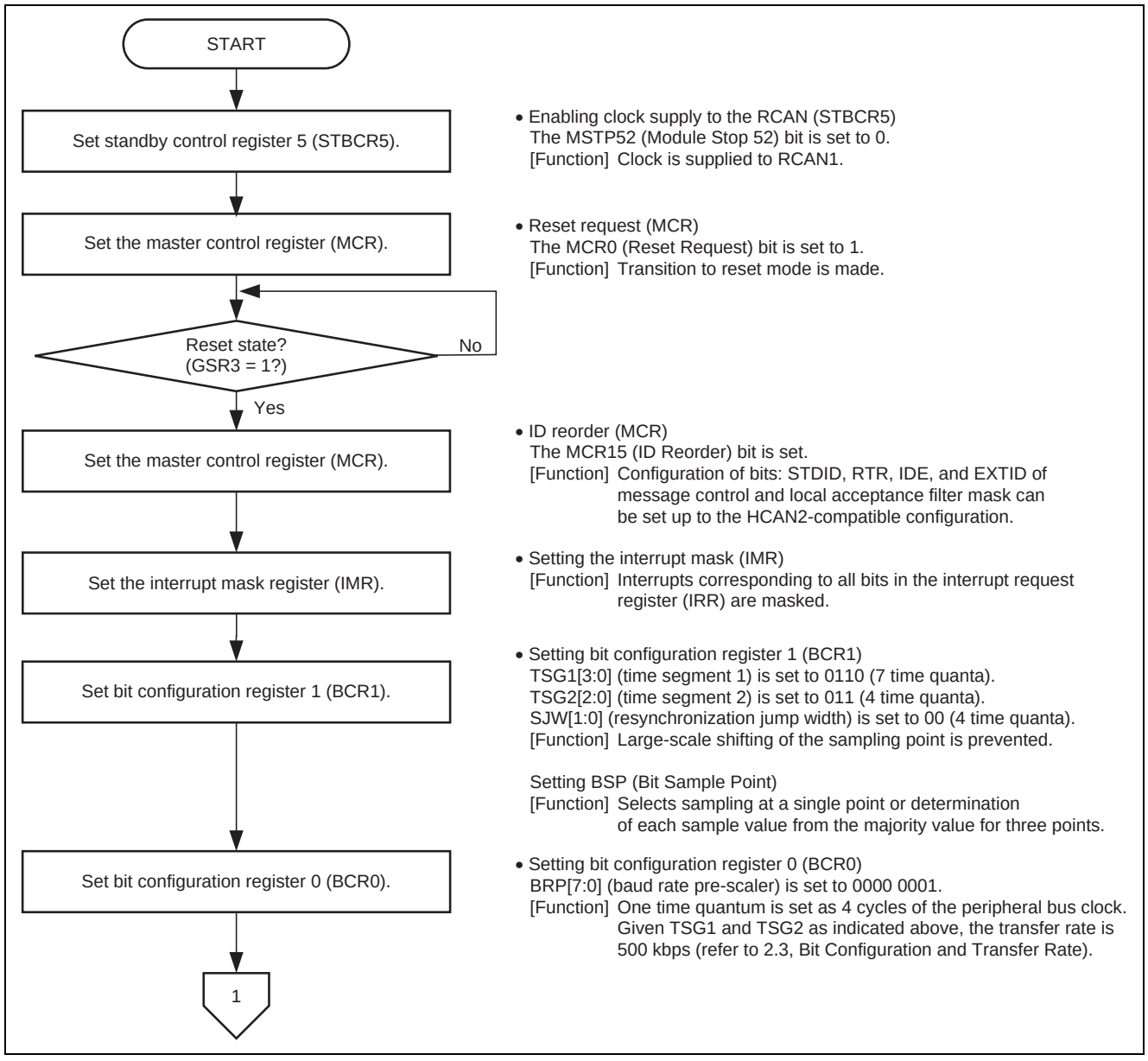
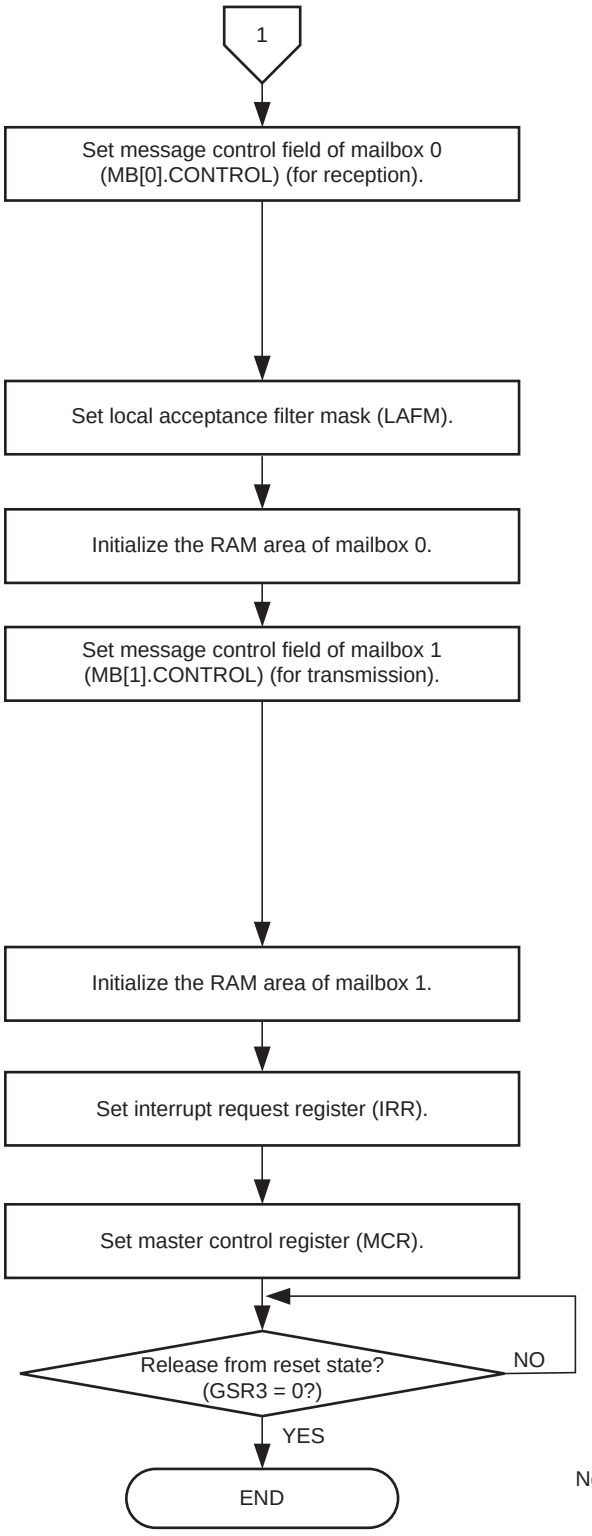


Figure 2 Example of Initialization Flow for the RCAN-TL1 Module (1)



- Setting message control (MB[0].CONTROL)
  MBC[2:0] (mailbox configuration) is set to 010.
  [Function] Reception of remote/data frame is enabled.
  IDE (identifier extension bit) is set to 0.
  [Function] Standard format
  RTR (remote transmission request bit) is set to 0.
  [Function] Data frame
  STDID[10:0] (standard identifier) is set to 0.
  [Function] ID = 0

- Setting local acceptance filter mask (LAFM)
  LAFM is set to H'0000 0000.
  [Function] Mask is not set.

- Clearing the RAM area of mailbox 0

- Setting message control (MB[1].CONTROL)*1
  MBC[2:0] (mailbox configuration) is set to 000.
  [Function] Transmission of remote/data frame is enabled.
  DLC[3:0] (data length code) is set to 0010.
  [Function] Data length = 2 bytes
  IDE (identifier extension bit) is set to 0.
  [Function] Standard format
  RTR (remote transmission request bit) is set to 0.
  [Function] Data frame
  STDID[10:0] (standard identifier) is set to 0.
  [Function] ID = 0

- Clearing the RAM area of mailbox 1*1

- Clearing interrupt request register (IRR)
  IRR0 to IRR15 are cleared.
  [Function] All interrupt flags are cleared, including the flag for the soft reset.

- Setting master control register (MCR)
  MCR0 (reset request) is cleared.
  [Function] Reset mode request is cleared.
  MCR1 (halt request) is cleared.
  [Function] Halt mode request is cleared.

Note: 1. This processing is not required for reception alone, but descriptions in this sample program are on the assumption that both transmission and reception are performed.

Figure 3 Example of Initialization Flow for the RCAN-TL1 Module (2)

2.3 Bit Configuration and Transfer Rate

One-bit time for the CAN module has the four segments indicated below.

(1) Synchronization segment (SS)
(2) Propagation time segment (PRSEG)
(3) Phase buffer segment 1 (PHSEG1)
(4) Phase buffer segment 2 (PHSEG2)

Furthermore, the individual segments are structured in units of a base time called the time quantum (Tq). Figure 4 shows an example of the configuration of a bit in the case where SS = Tq, PRSEG = 3Tq, PHSEG1 = 4Tq, and PHSEG2 = 4Tq.

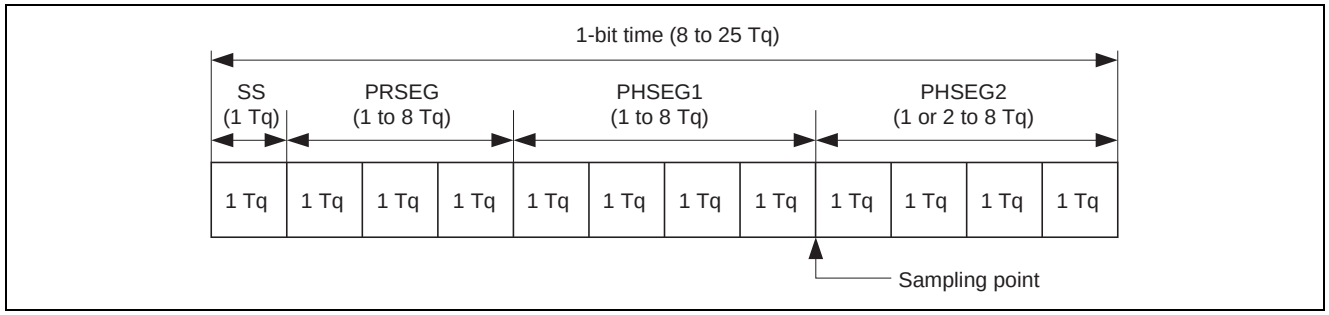


Figure 4 Configuration of One-Bit Time

In the RCAN-TL1, the Tq of PRSEG + PHSEG1 is set to TSG1[3:0] in bit configuration register 1 (BCR1) and the Tq of PHSEG2 is set to TSG2[2:0] (Tq = set value + 1). Additionally, the number of cycles of the peripheral-bus clock corresponding to 1Tq is set in BRP[7:0] of bit configuration register 0 (BCR0).

In the following description, BRP[7:0], TSG1[3:0] and TSG2[2:0] indicate the register settings, and BRP, TSEG1, TSEG2, and SJW indicate the values that correspond to these register settings. For the values corresponding to the values set in registers, refer to the section on the controller area network in the *SH7203 Group Hardware Manual*.

By definition, Tq for the RCAN-TL1 module is 1Tq = 2 × (BRP[7:0] + 1)/peripheral bus clock, and the transfer rate is calculated as follows.

Transfer rate = peripheral bus clock/(2 × (BRP[7:0] + 1) × the number of Tq in 1-bit time) =
peripheral bus clock/(2 × (BRP[7:0] + 1) × ((TSG1[3:0] + 1) + (TSG2[2:0] + 1) + 1)

The following restrictions apply to settings of the bit-configuration registers.

TSEG1 (Min) > TSEG2 ≥ SJW (Max) (SJW = 1 to 4)

SJW: Jump width for resynchronization. This segment is used to correct phase errors by extending phase buffer segment 1 or shortening phase buffer segment 2.

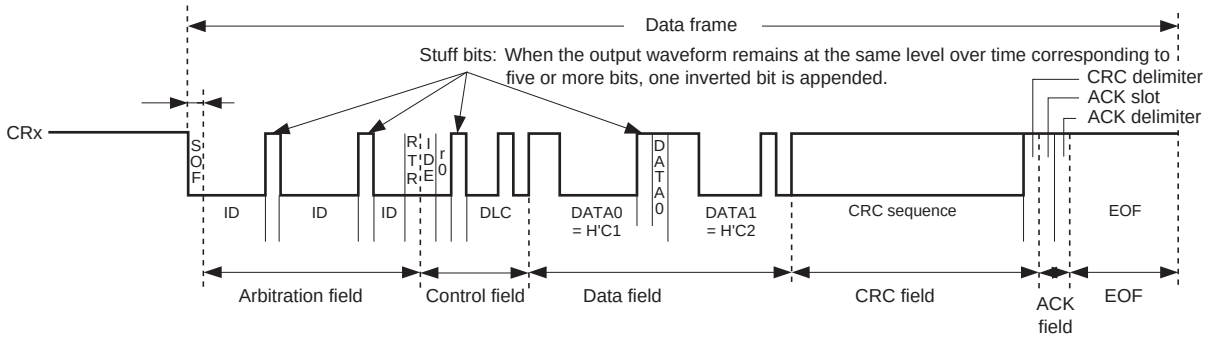
8 ≤ TSEG1 + TSEG2 + 1 ≤ 25 time quanta
TSEG2 ≥ 2

Since the settings in this sample program are as follows: peripheral bus clock = 24 MHz, BRP[7:0] = 1, TSG1[3:0] = 6, TSG2[2:0] = 3, the transfer rate is calculated with the following formula.

Transfer rate (bps) = 24 M (2 × (1+1) × ((6 + 1) + (3 + 1) + 1) = 500 k

2.4 Operation of the Sample Program

In this sample program, a data frame in standard format (IDE: 0) is received in mailbox 0 at a transfer rate of 500 kbps. Figure 5 shows waveforms for data frame reception.



SOF (Start of frame)	: Indicates start of data frame and remote frame.
ID (Identifier)	: Indicates priority of data.
RTR (Request for remote transmission)	: Indicates distinction between data frame and remote frame.
IDE (Identifier extension)	: Indicates distinction between standard format and extended format.
r0	: Reserved bit
DLC (Data length code)	: Indicates the number of bytes in the data field. Setting range: 0 to 8 bytes
DATA	: Data for transfer. The number of bytes transferred is the number set in the DLC field.
CRC sequence	: This value is used to check frames.
CRC delimiter	: This bit is used to delimit the CRC field and ACK field.
ACK slot	: The receiving unit is dominant, and overwrites this when no errors are detected in a transmitted message.
ACK delimiter	: This bit is used to delimit the ACK field and EOF.
EOF (End of frame):	: Indicates the end of the frame.

Figure 5 Waveform for Data Frame Reception by the RCAN-TL1

2.5 Procedure of Processing by the Sample Program

Tables 1 and 2 give an example of the settings for the controller area network (RCAN-TL1). Figure 6 shows an example of the flow of processing by this sample program.

Table 1 Register Settings for Controller Area Network (RCAN-TL1) (1)

Register Name	Address	Setting Value	Description
Standby control register (STBCR5)	H'FFFE 0410	H'FB	• MSTP52 = 0: RCAN1 runs
Master control register_1 (MCR_1)	H'FFFF 0800	H'0001	• MCR0 = 1: Reset mode transition request
		H'8001	• MCR15 = 1: RCAN-TL1 is not the same as HCAN2
		H'8000	• MCR0 = 0: Release from reset mode
Interrupt mask register_1 (IMR_1)	H'FFFF 080A	H'FFFF	• Disables all interrupts of RCAN1
Bit configuration register 1_1 (BCR1_1)	H'FFFF 0804	H'6300	• TSG1[3:0] = 0110: PRSEG + PHSEG1 = 6 Tq • TSG2[2:0] = 011: PHSEG2 = 4 Tq • SJW = 0: SJW = 2 Tq • BSP = 0: Bit sampling at one point
Bit configuration register 0_1 (BCR0_1)	H'FFFF 0806	H'0001	• BRP[7:0] = 1: 1 Tq = 4 × Pϕ
Message control field (MB[0].CONTROL1_1)	H'FFFF 0910	H'0200	• MBC[2:0] = 010: Enables reception of data frames and remote frames

Table 2 Register Settings for Controller Area Network (RCAN-TL1) (2)

Register Name	Address	Setting Value	Description
Message control field (MB[1].CONTROL1_1)	H'FFFF 0942	H'0002	• MBC[2:0] = 000: Enables transmission of data frames and remote frames • DLC[3:0] = 0010: 2-byte data length
Message control field (MB[1].CONTROL0_1)	H'FFFF 0932	H'0000 0000	• IDE = 0: Standard format • RTR = 0: Data frame • STDID[10:0] = 0: Standard ID = 0
Local acceptance filter mask_1 (MB[0].LAFM_1)	H'FFFF 0904	H'0000 0000	• Clear: MASK is not set
Local acceptance filter mask_1 (MB[1].LAFM_1)	H'FFFF 0936	H'0000 0000	
Message data field_1 (MB[0].MSG_DATA01 to 67)	H'FFFF 0908 to H'FFFF 090F	H'0000	• Data field clear (RAM area is cleared)
Message data field_1 (MB[1].MSG_DATA01 to 67)	H'FFFF 093A to H'FFFF 0941	H'0000	
Data frame receive pending register_1 (RXPR0_1)	H'FFFF 0842	H'0001	• RXPR[31:0] = H'0001: Clears the reception-completed flag

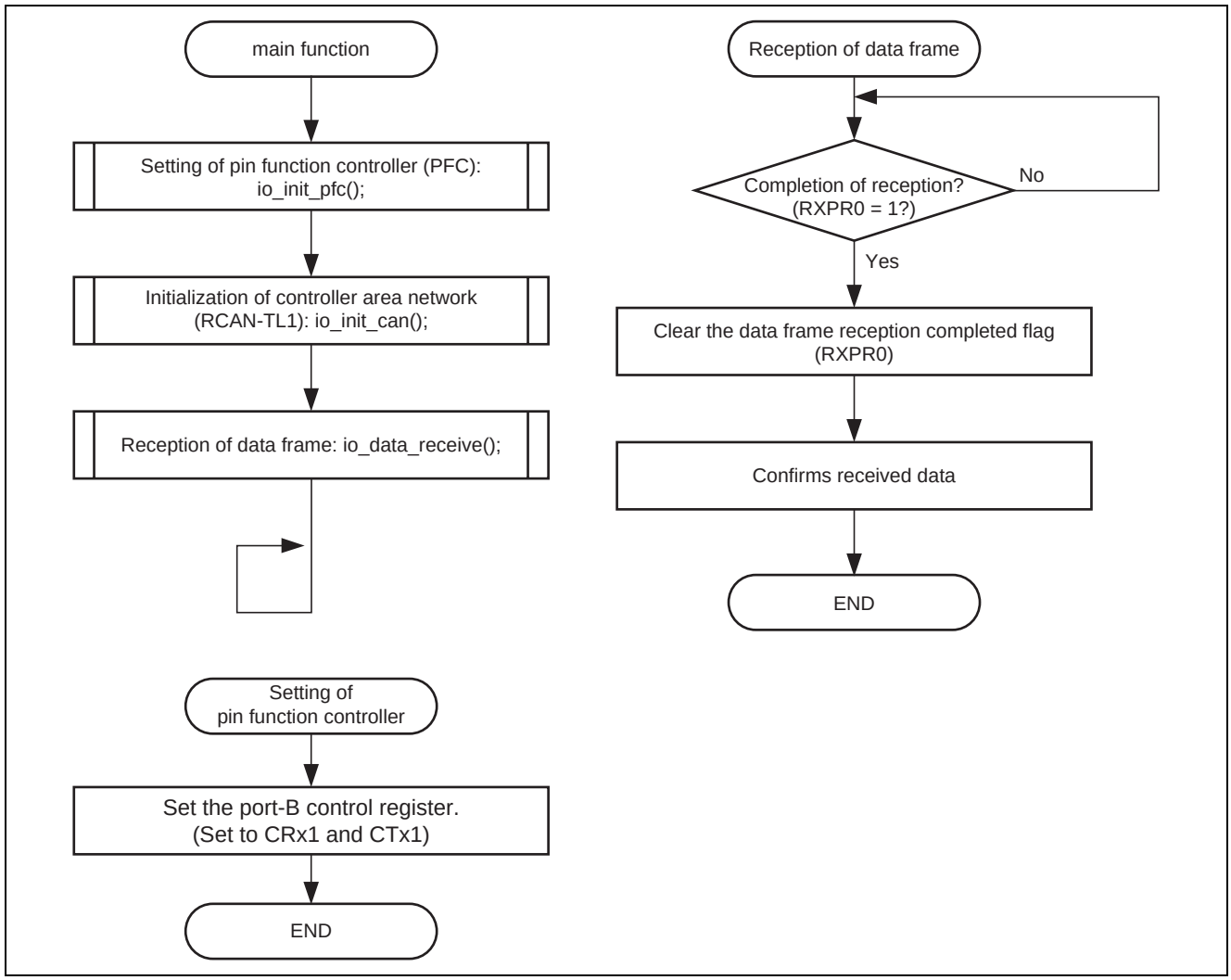


Figure 6 Example of Flow of Processing by the Sample Program

3. Sample Program

```
/*""FILE.COMMENT""*****************************************************************
*
*       System Name : SH7203 Sample Program
*       File Name   : main.c
*       Contents    : Application of CAN Module (Data Frame Reception)
*       Version     : 1.00.00
*       Model       : M3A-HS30
*       CPU         : SH7203
*       Compiler    : SHC9.0.3.0
*       Note        : The module receives a data frame in standard format (IDE:0) from
*                     mailbox 1 of CAN1 at a 500-kbps transfer rate over the CAN bus,
*                     and writes the received frame to RAM.
*
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*
*       history   : 2007.06.26 ver.1.00.00
*""FILE COMMENT END""*************************************************************/
#include <machine.h>
#include "iodefine.h"       /* SH7203 iodefine  */

/* ---- prototype declaration ---- */
void main(void);
void io_init_pfc(void);
void io_init_can(void);
void io_data_receive(void);

/* ---- symbol definition ---- */
#define CAN_GSR3 0x0008
#define CAN_MB0  0x0001

/* ---- RAM allocation variable declaration ---- */
unsigned char   nIDE = 0;           /* ide */
unsigned char   nRTR = 0;           /* rtr */
unsigned char   nDLC = 0;           /* dlc */
unsigned int    nSID = 0;           /* sid */
unsigned int    nEID = 0;           /* eid */
unsigned char   gRcv_data[8];       /* data of message */
```

Figure 7 Sample Program Listing: "main.c" (1)

```
44    /*""FUNC COMMENT""*****************************************************
45     * Outline     : Sample Program main
46     *-------------------------------------------------------------------------
47     * Include     : none
48     *-------------------------------------------------------------------------
49     * Declaration : void main(void);
50     *-------------------------------------------------------------------------
51     * Function    : Sample Program main
52     *-------------------------------------------------------------------------
53     * Argument    : none
54     *-------------------------------------------------------------------------
55     * Return Value: none
56     *-------------------------------------------------------------------------
57     * Notice      : none
58     *""FUNC COMMENT END""*************************************************/
59    void main(void)
60    {
61
62        /* ==== Setting of PFC ==== */
63        io_init_pfc();
64
65        /* ==== Initializing CAN module ==== */
66        io_init_can();
67
68        /* ==== CAN data frame reception ==== */
69        io_data_receive();
70
71        while(1){
72            /* loop */
73        }
74
75    }
76
77    /*""FUNC COMMENT""*****************************************************
78     * Outline     : Setting of PFC
79     *-------------------------------------------------------------------------
80     * Include     : #include "iodefine.h"
81     *-------------------------------------------------------------------------
82     * Declaration : void io_init_pfc(void);
83     *-------------------------------------------------------------------------
84     * Function    : Setting of Pin Function Controller(PFC)
85     *-------------------------------------------------------------------------
86     * Argument    : none
87     *-------------------------------------------------------------------------
88     * Return Value: none
89     *-------------------------------------------------------------------------
90     * Notice      : none
91     *""FUNC COMMENT END""*************************************************/
92    void io_init_pfc(void)
93    {
94        /* ==== Setting of PFC ==== */
95        /* ---- Port B control register L3 ---- */
96        PORT.PBCRL3.BIT.PB10MD = 0x1;   /* Set CRx1 */
97        PORT.PBCRL3.BIT.PB11MD = 0x1;   /* Set CTx1 */
98
99    }
```

Figure 8 Sample Program Listing: "main.c" (2)

```
100    /*""FUNC COMMENT""*****************************************************
101     * Outline     : Setting of RCAN
102     *-------------------------------------------------------------------------
103     * Include     : #include "iodefine.h"
104     *-------------------------------------------------------------------------
105     * Declaration : void io_init_can(void);
106     *-------------------------------------------------------------------------
107     * Function    : Setting of Controller Area Network(RCAN)
108     *-------------------------------------------------------------------------
109     * Argument    : none
110     *-------------------------------------------------------------------------
111     * Return Value: none
112     *-------------------------------------------------------------------------
113     * Notice      : none
114     *""FUNC COMMENT END""*************************************************/
115    void io_init_can(void)
116    {
117        int i;
118
119        /* ==== Setting of power down mode(RCAN1) ==== */
120        CPG.STBCR5.BIT.MSTP52 = 0;
121
122        /* ==== Initializing CAN module ==== */
123        RCAN1.MCR.WORD |= 0x0001;       /* CAN Interface reset mode */
124        while((RCAN1.GSR.WORD & CAN_GSR3) != CAN_GSR3){
125            /* Reset state waiting */
126        }
127
128        /* ---- RCAN mode selection ---- */
129        RCAN1.MCR.WORD |= 0x8000;       /* RCAN-TL1 is not same as HCAN2 */
130
131        /* ---- Disable all can interrupt ---- */
132        RCAN1.IMR.WORD  = 0xFFFF;
133
134    /* ---- Config baudrate ---- */
135        RCAN1.BCR1.WORD = 0x6300;       /* tsg1=6(7bit),tsg2=3(4bit),sjw=0(1bit),bsp=0 */
136        RCAN1.BCR0.WORD = 0x0001;       /* 500K bps */
137    //  RCAN1.BCR0.WORD = 0x0003;       /* 250K bps */
138    //  RCAN1.BCR0.WORD = 0x0007;       /* 125K bps */
139
140        /* ---- Config mailbox0 as reception slot ---- */
141        RCAN1.MB[0].CONTROL1.WORD = 0x0200;     /* can receive data and remote frame */
142        RCAN1.MB[0].CONTROL0.LONG = 0x00000000; /* Initialize the Message Control Field */
143        RCAN1.MB[0].LAFM.LONG = 0x00000000;
144        for(i = 0; i < 8; i++){                 /* data clear */
145            RCAN1.MB[0].MSG_DATA[i] =  0x00;
146        }
147        /* ---- Config mailbox1 as transmission slot ---- */
148        RCAN1.MB[1].CONTROL1.WORD = 0x0002;     /* Can send data or remote frame, dlc=2 */
149        RCAN1.MB[1].CONTROL0.LONG = 0x00000000; /* standard data frame, id=0x000 */
150        RCAN1.MB[1].LAFM.LONG = 0x00000000;
151        for(i = 0; i < 8; i++){                 /* data clear */
152            RCAN1.MB[1].MSG_DATA[i] =  0x00;
153        }
154
155        /* ---- Clear interrupt flags ---- */
156        RCAN1.IRR.WORD = 0xffff;
157
158        /* ---- Clear reset and halt ---- */
159        RCAN1.MCR.WORD &= 0xfffc;
160        while( (RCAN1.GSR.WORD & CAN_GSR3) != 0x0000 ){
161            /* reset state is end */
162        }
163    }
```

Figure 9 Sample Program Listing: "main.c" (3)

```
164    /*""FUNC COMMENT""************************************************
165     * Outline     : Reception of Data Frame
166     *-----------------------------------------------------------------
167     * Include     : #include "iodefine.h"
168     *-----------------------------------------------------------------
169     * Declaration : void io_data_receive(void);
170     *-----------------------------------------------------------------
171     * Function    : RCAN1 is used to receive a data frame.
172     *-----------------------------------------------------------------
173     * Argument    : none
174     *-----------------------------------------------------------------
175     * Return Value: none
176     *-----------------------------------------------------------------
177     * Notice      : none
178     *""FUNC COMMENT END""*******************************************/
179    void io_data_receive(void)
180    {
181        int i;
182
183        /* ---- Reception completion waiting ---- */
184        while((RCAN1.RXPR0.WORD & CAN_MB0) != CAN_MB0){
185        }
186
187        /* ---- Receive data storage ---- */
188        nIDE = RCAN1.MB[0].CONTROL0.BIT.IDE;
189        nRTR = RCAN1.MB[0].CONTROL0.BIT.RTR;
190        nDLC = RCAN1.MB[0].CONTROL1.BIT.DLC;
191        nSID = RCAN1.MB[0].CONTROL0.BIT.STDID;
192        nEID = RCAN1.MB[0].CONTROL0.BIT.EXDID;
193        if(nDLC > 8){
194            nDLC = 8;
195        }
196        for(i = 0; i < nDLC; i++){
197            gRcv_data[i] = RCAN1.MB[0].MSG_DATA[i];
198        }
199
200        /* ---- Reception completion flag clear ---- */
201        RCAN1.RXPR0.WORD = CAN_MB0;
202
203    }
204
205    /* End of File */
```

Figure 10 Sample Program Listing: "main.c" (4)

4. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manuals
  SH7263 Group Hardware Manual
  SH7203 Group Hardware Manual
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