RX62N Group, RX63N Group

Differences between RX62N Group and RX63N Group

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Abstract

This application note provides reference information on the differences between RX62N Group and RX63N Group microcontrollers.

Products

RX62N Group, RX63N Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Switching from the RX62N Group to the RX63N Group

The RX62N Group and RX63N Group are not interchangeable devices. Therefore, care must be exercised when switching to the RX63N Group. For details, see section 2., Description of Differences, as well as RX62N Group—User's Manual: Hardware and RX63N Group—User's Manual: Hardware.

1.1 Newly Added Functions

1. Option-setting memory
2. Low-speed on-chip oscillator (LOCO), high-speed on-chip oscillator (HOCO)
3. Frequency measurement circuit (MCK)
4. Battery backup function
5. Register write protection function
6. Multi pin function controller (MPC)
7. 16-bit timer pulse unit (TPUa)
8. IEBus™ controller (IEB)
9. Temperature sensor

1.2 Eliminated Functions

1. MD1 pin (mode 1 pin), MDE pin (endian selection pin)
2. Startup external bus width flags (MDSR.BSW[1:0])
3. Reset control/status register (RSTCSR)
4. Low-voltage detection control register key code register (LVDKEYR)
5. OSTDCR key code (OSTDCR.KEY[7:0])
6. Standby timer select bits (STS4 to STS0 in SBYCR)
7. Deep standby wait control register (DPSWCR)
8. Internal peripheral bus 5 (peripheral function, ICLK)
9. Watchdog timer: Interval timer mode
10. WDTOVF# signal output (External)
11. USB1 host controller function
12. Support for USB1 OTG (On The Go)
13. Serial peripheral interface: CMOS/open-drain output switching function

1.3 Modified Functions

1.3.1 Modification Type 1: Items Requiring Reconsideration Due to Specification Changes or Elimination of Functions

1. MCU operation mode entry methods: MD pin eliminated, UB codes A and B added.
2. Endian determination method: Bits MDE2 to MDE0 in MDEB and MDES
3. Voltage detection circuit (LVDA): Falling under Vdet → Passing through Vdet, other changes
4. Clock oscillator circuit: Low-speed on-chip oscillator (LOCO) startup, PLL frequency division, and oscillation stop detection modified, etc.
5. Low power consumption functions: Oscillation settling time modified, etc.
6. Interrupt controller (ICUb): Group interrupts, unit selection, digital filter function added.
7. Buses: Multiplex bus, peripheral bus update, bus priority added, etc.
8. I/O ports: Modifications to multi-function pin controller, etc.
9. Multi-function timer pulse unit 2 (MTU2a): 2 units → 1 unit, noise filter added.
10 Port output enable 2 (POE2a): Changes associated with elimination of the MTU unit
11. Realtime clock (RTCa): EXTAL operation, clock error connector function, 12 hour/24 hour modes added, other changes
12. Watchdog timer (WDTA): 8-bit → 14-bit
13. Ethernet controller (ETHERC): PAUSE frame transmission bit function modified.
14. USB 2.0 host/function module 1 (USB1): Suspend/resume function eliminated, other changes
15. Serial communications interfaces: 6 channels → 13 channels, status flag eliminated, functions added, etc.
16. 12-bit A/D converter (S12ADa): Trigger sources modified, 8 channels → 21 channels, registers added.
17. 10-bit A/D converter (ADA): Trigger sources modified, 4 channels × 2 units → 8 channels × 1 unit
18. ROM (flash memory for code storage): Write units modified.
19. E2 data flash: Block and write units modified, PCLK3 cycle during word or byte access → FCLK6 cycle

1.3.2 Modification Type 2: Items Requiring Reconsideration of Error Handling Due to Changes to the Interrupt Controller

1. CAN module: 1 channel → 3 channels, EXTAL operation added
2. Serial peripheral interface (RSPI): 2 channels → 3 channels, status flag eliminated, CMOS/open-drain output switching function eliminated
3. Multi-function timer pulse unit 2 (MTU2a): (See section 3.3.1 above.)

1.3.3 Modification Type 3: Items Requiring Reconsideration of Software Due to Partial Changes to Functions

1. DMA controller (DMACA): Maximum transfer count modified, other changes
2. EXDMA controller (EXDMAC): Maximum transfer count modified, other changes
3. Data transfer controller (DTCa): Maximum transfer count modified, other changes
4. Programmable pulse generator (PPG): Trigger sources modified.

1.4 Compatible Functions

1.4.1 Compatible Functions

1. Memory-protection unit (MPU)
2. 8-bit timer (TMR)
3. Compare match timer (CMT)
4. Ethernet controller DMA controller (EDMAC)
5. USB 2.0 host/function module 0 (USB0)
6. I^2C bus interface (RIIC)
7. CRC calculator (CRC)

1.4.2 Backward-Compatible Function

1. Independent watchdog timer (IWDTa): Window function added, other changes
2. D/A converter: Registers added.

2. Description of Differences

2.1 Differences in Functions and Specifications

Tables 2.1 to 2.31 list the differences in functions and specifications.

Table 2.1 Differences in Functions and Specifications (1)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td>Memory</td><td>ROM/RAM</td><td>• Memory configurations
ROM/RAM capacity: —
256 KB / 64 KB
—
384 KB / 64 KB
—
—
512 KB / 96 KB
—
—
—
—
—</td><td>• Memory configurations
ROM/RAM capacity: 0B /128 KB
256 KB / 64 KB
256 KB /128 KB
384 KB / 64 KB
384 KB /128 KB
512 KB / 64 KB
—
512 KB /128 KB
768 KB /128 KB
1.0 MB /128 KB
1.5 MB /128 KB
2.0 MB /128 KB</td></tr>
<tr><td>MCU operating modes</td><td>Operating mode</td><td>• Mode entry
MD1 / MD0 / Operating mode
0 / 1 / Boot mode
1 / 0 / USB boot mode
(User boot mode)
1 / 1 / Single-chip mode</td><td>• Mode entry
PC7 / MD / UB code A / Operating mode
Low / Low / — / Boot mode
High / Low / — / USB boot mode
Up to 426F6F74h / User boot mode
— / High / — / Single-chip mode</td></tr>
<tr><td></td><td></td><td>• Endian selection
• MDE pins
MDE pin = Low: Little-endian
MDE pin = High: Big-endian</td><td>• Endian selection
• MDEB.MDE[2:0] or MDES.MDE[2:0]
MDE[2:0] = 111b: Little-endian
MDE[2:0] = 000b: Big-endian</td></tr>
<tr><td></td><td>Registers/ bits</td><td>• Mode monitor register (MDMONR)
b0 / MD0 / MD0 pin status flag
b1 / MD1 / MD1 pin status flag
b7 / MDE / MDE pin status flag</td><td>• Mode monitor register (MDMONR)
b0 / MD / MD pin status flag
b1 / — / (Reserved bit)
b7 / — / (Reserved bit)</td></tr>
<tr><td></td><td></td><td>• Mode status register (MDSR)
b0 / IROM / On-chip ROM startup status flag
b1 / EXB / External bus startup status flag
b2 b3 / BSW[1:0] / External bus width flags
b4 / BOTS / Boot mode startup flag
b5 / — / (Reserved bit)
b6 / UBTS / USB boot mode startup flag</td><td>• Mode status register (MDSR)
b0 / — / (Reserved bit)
b1 / — / (Reserved bit)
b2 b3 / — / (Reserved bits)
b4 / — / (Reserved bit)
b5 / UBTS / User boot mode startup flag
b6 / — / (Reserved bit)</td></tr>
<tr><td>Resets</td><td>Functions</td><td>• Specification overview
Reset types: Pin reset
Power-on reset
Voltage monitoring reset
—
—
Deep software standby reset
Independent watchdog timer reset
Watchdog timer reset
—
— / —</td><td>• Specification overview
Reset types: RES# Pin reset
Power-on reset
Voltage monitoring 0 reset
Voltage monitoring 1 reset
Voltage monitoring 2 reset
Deep software standby reset
Independent watchdog timer reset
Watchdog timer reset
Software reset
Extended function: Cold start/warm start determination function</td></tr>
<tr><td></td><td>Registers/ bits</td><td>• Reset status register (RSTSR)
b0 / PORF / Power-on reset flag
b1 / LVD1F / LVD1 detect flag
b2 / LVD2F / LVD2 detect flag
b3 / — / (Reserved bit)
b7 / DPSRSTF / Deep software standby reset flag
—
• ‘
—</td><td>• Reset status register 0 (RSTSR0)
b0 / PORF / Power-on reset detect flag
b1 / LVD0RF / Voltage-monitoring 0 reset detect flag
b2 / LVD1RF / Voltage-monitoring 1 reset detect flag
b3 / LVD2RF / Voltage-monitoring 2 reset detect flag
b7 / DPSRSTF / Deep software standby reset flag
• Reset status register 1 (RSTSR1)
• Reset status register 2 (RSTSR2)
—
• Software reset register (SWRR)</td></tr>
</table>

Table 2.2 Differences in Functions and Specifications (2)

Item		RX62N Group	RX63N Group
Option-setting memory	Registers/ bits	—	• Option function select register 0 (OFS0) • Option function select register 1 (OFS1) • Endian select register B (MDEB) • Endian select register S (MDES)
Voltage detection circuit	Functions	—	• Voltage detection circuit 0 Monitored voltage: Vdet0 Detection object: Passing through Vdet0 Detection voltage: Fixed Interrupt: None
		• Voltage detection circuit 1 Monitored voltage: Vdet1 Detection object: Falling under Vdet 1 Detection voltage: Fixed Interrupt: Voltage monitor interrupt	• Voltage detection circuit 1 Monitored voltage: Vdet1 Detection object: Passing through Vdet1 Detection voltage: Selected with the LVDLVLR.LVD1LVL[3:0] bits Interrupt: Voltage monitor 1 interrupt Nonmaskable interrupt
		• Voltage detection circuit 2 Monitored voltage: Vdet2 Detection object: Falling under Vdet2 Detection voltage: Fixed Interrupt: Voltage monitor interrupt	• Voltage detection circuit 2 Monitored voltage: Vdet2 Detection object: Passing through Vdet2 Detection voltage: Selected with the LVDLVLR.LVD2LVL[3:0] bits Interrupt: Voltage monitor 2 interrupt Nonmaskable interrupt
	Registers/ bits	• Key code register for low-voltage detection control register (LVDKEYR) • Low-voltage detection control register (LVDCR)	—
		—	• Voltage monitoring circuit control register (LVCMPCR) • Voltage detection level select register (LVDLVLR) • Voltage monitoring 1 circuit control register 0 (LVD1CR0) • Voltage monitoring 2 circuit control register 0 (LVD2CR0) • Voltage monitoring 1 circuit control register 1 (LVD1CR1) • Voltage monitoring 2 circuit control register 1 (LVD2CR1) • Voltage monitoring 1 circuit status register (LVD1SR) • Voltage monitoring 2 circuit status register (LVD2SR)
Clock oscillator	Functions	• Specification overview Clock types: ICLK: 100.0 MHz (max.) — PCLK: 50.0 MHz (max.) — BCLK: 100.0 MHz (max.)*1 BCLK output pin: 50.0 MHz (max.)*1 SDCLK: 50.0 MHz (max.) SDCLK output pin: 50.0 MHz (max.) UCLK: 48.0 MHz (max.) — — — SUBCLK: 32.768 KHz IWDTCLK: 125.000 KHz (typ.) —	• Specification overview Clock types: ICLK: 100.0 MHz (max.) PCLKA: 100.0 MHz (max.) PCLKB: 50.0 MHz (max.) FCLK: 4 MHz to 50.0 MHz (During ROM or E2 data flash P/E) 50.0 MHz (max.) (During E2 data flash write) BCLK: 100.0MHz (max.) BCLK output pin: 50.0 MHz (max.) SDCLK: 50.0 MHz (max.) SDCLK output pin: 50.0 MHz (max.) UCLK: 48.0 MHz (max.) CANMCLK: 20.0 MHz (max.) IECLK: 50.0 MHz (max.) RTCMCLK: 4.0 MHz to 16.0 MHz RTCSCLK: 32.768 KHz IWDTCLK: 125.000 KHz JTAGTCK [generated]: 10.0MHz (max.) JTAGTCK [input]: 10.0 MHz (max.)
	Main clock oscillator	• Specification overview Resonator: Crystal oscillator — Frequency: 8.0 MHz to 14.0 MHz External clock: 14.0 MHz (max.)	• Specification overview Resonator: Crystal oscillator Ceramic oscillator Frequency: 4.0 MHz to 16.0 MHz External clock: 20.0 MHz (max.)
	Low-speed on-chip oscillator	—	• Oscillation frequency: 125.0 KHz

Note: 1. In the 100-pin LQFP version and the 85-pin TFLGA version: 8 to 50 MHz, BCLK output pin: 8 to 25 MHz

Table 2.3 Differences in Functions and Specifications (3)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="10">Clock oscillator</td><td rowspan="2">High-speed on-chip oscillator</td><td rowspan="2">—</td><td>• Oscillation frequency: 50.0 MHz</td></tr>
<tr><td>• HOCO power supply control</td></tr>
<tr><td>IWDT operating clock</td><td>• On-chip oscillator: 125.0KHz</td><td>• IWDT-dedicated on-chip oscillator: 125.0 KHz</td></tr>
<tr><td>JTAG external clock</td><td>—</td><td>• Input clock frequency: 10 MHz (max.)</td></tr>
<tr><td rowspan="6">Registers/ bits</td><td>• System clock control register (SCKCR)
<table>
<tr><td>b8
b11</td><td>PCK[3:0]</td><td>Peripheral module clock select bits</td></tr>
<tr><td>b12
b15</td><td>—</td><td>(Reserved bits)</td></tr>
<tr><td>b16
b19</td><td>BCK[3:0]</td><td>External bus clock and SDRAM clock selection bits</td></tr>
<tr><td>b22</td><td>PSTOP0</td><td>SDCLK pin output control bit</td></tr>
<tr><td>b23</td><td>PSTOP1</td><td>BCLK pin output control bit</td></tr>
<tr><td>b24
b27</td><td>ICK[3:0]</td><td>System clock select bits</td></tr>
<tr><td>b28
b31</td><td>—</td><td>(Reserved bits)</td></tr>
</table>
• PCK[3:0], BCK[3:0], ICK[3:0]
0000b: ×8
0001b: ×4
0010b: ×2
0011b: ×1</td><td>• System clock control register (SCKCR)
<table>
<tr><td>b8
b11</td><td>PCKB[3:0]</td><td>Peripheral module clock B select bits</td></tr>
<tr><td>b12
b15</td><td>PCKA[3:0]</td><td>Peripheral module clock A select bits</td></tr>
<tr><td>b16
b19</td><td>BCK[3:0]</td><td>Timer module clock select bits</td></tr>
<tr><td>b22</td><td>PSTOP0</td><td>SDCLK pin output control bit</td></tr>
<tr><td>b23</td><td>PSTOP1</td><td>BCLK pin output control bit</td></tr>
<tr><td>b24
b27</td><td>ICK[3:0]</td><td>System clock select bits</td></tr>
<tr><td>b28
b31</td><td>FCK[3:0]</td><td>FlashIF clock select bits</td></tr>
</table>
• PCKB[3:0], PCKA[3:0], BCK[3:0], ICK[3:0], FCK[3:0]
0000b: ×1/1
0001b: ×1/2
0010b: ×1/4
0011b: ×1/8
0100b: ×1/16
0101b: ×1/32
0110b: ×1/64</td></tr>
<tr><td rowspan="5">—</td><td>• System clock control register 2 (SCKCR2)</td></tr>
<tr><td>• System clock control register 3 (SCKCR3)</td></tr>
<tr><td>• PLL control register (PLLCR)</td></tr>
<tr><td>• PLL control register 2 (PLLCR2)</td></tr>
<tr><td>• Main clock oscillator control register (MOSCCR)</td></tr>
<tr><td>• Oscillation stop detection control register (OSTDCR)
<table>
<tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b6</td><td>OSTDF</td><td>Oscillation stop detection flag</td></tr>
<tr><td>B7</td><td>OSTDE</td><td>Oscillation stop detection function enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>OSTDCR Key code</td></tr>
</table></td><td>• Oscillation stop detection control register (OSTDCR)
<table>
<tr><td>b0</td><td>OSTDIE</td><td>Oscillation stop detection interrupt enable bit</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>OSTDE</td><td>Oscillation stop detection function enable bit</td></tr>
<tr><td>—</td><td>—</td><td>—</td></tr>
</table>
• Oscillation stop detection status register (OSTDSR)
<table>
<tr><td>b0</td><td>OSTDF</td><td>Oscillation stop detection flag</td></tr>
</table></td></tr>
<tr><td>• Sub-clock oscillator control register (SUBOSCCR)
<table>
<tr><td>b0</td><td>SUBSTOP</td><td>Sub-clock oscillator stop bit</td></tr>
</table></td><td>• Sub-clock oscillator control register (SOSCCR)
<table>
<tr><td>b0</td><td>SOSTP</td><td>Sub-clock oscillator stop bit</td></tr>
</table></td></tr>
<tr><td rowspan="5">—</td><td>• Main clock oscillator forced oscillation control register (MOFCR)</td></tr>
<tr><td>• IWDT-dedicated on-chip oscillator control register (ILOCOCR)</td></tr>
<tr><td>• Low-speed on-chip oscillator control register (LOCOCR)</td></tr>
<tr><td>• High-speed on-chip oscillator control register (HOCOCR)</td></tr>
<tr><td>• High-speed on-chip oscillator power supply control register (HOCOPCR)</td></tr>
</table>

Table 2.4 Differences in Functions and Specifications (4)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td>Clock oscillator</td><td>Functions</td><td>• Specification overview
<table><tr><td>Usage notes</td><td>—
—
—
—</td></tr></table></td><td>• Specification overview
<table><tr><td>Usage notes</td><td>Notes on oscillator connection pins
Notes on the subclock oscillator
Notes on low-CL crystal oscillator usage
Notes on 48-pin package products</td></tr></table></td></tr>
<tr><td>Frequency measurement circuit</td><td>Registers/ bits</td><td>—</td><td>• Counter-clock extension register 1 (SCK1)
• Counter-clock extension register 2 (SCK2)</td></tr>
<tr><td>Low power consumption functions</td><td>Registers/ bits</td><td>• Standby control register (SBYCR)
<table><tr><td>b8
b12</td><td>STS[4:0]</td><td>Standby timer select bits</td></tr><tr><td>b14</td><td>OPE</td><td>Output port enable bit</td></tr><tr><td>b15</td><td>SSBY</td><td>Software standby bit</td></tr></table>• SBYCR.STS[4:0]
00000b: (Setting prohibited)
00001b: (Setting prohibited)
00010b: (Setting prohibited)
00011b: (Setting prohibited)
00100b: (Setting prohibited)
00101b: Waiting time = 64 cycles
00110b: Waiting time = 512 cycles
00111b: Waiting time = 1024 cycles
01000b: Waiting time = 2048 cycles
01001b: Waiting time = 4096 cycles
01010b: Waiting time = 16384 cycles
01011b: Waiting time = 32768 cycles
01100b: Waiting time = 65536 cycles
01101b: Waiting time = 131072 cycles
01110b: Waiting time = 262144 cycles
01111b: Waiting time = 524288 cycles</td><td>• Standby control register (SBYCR)
<table><tr><td>b8
b12</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b14</td><td>OPE</td><td>Output port enable bit</td></tr><tr><td>b15</td><td>SSBY</td><td>Software standby bit</td></tr></table>• Main clock oscillator wait control register (MOSCWTCR)
<table><tr><td>b0
b4</td><td>MSTS[4:0]</td><td>Main clock oscillator waiting time bits</td></tr></table>• MOSCWTCR. MSTS[4:0]
00000b: Waiting time = 2 cycles
00001b: Waiting time = 4 cycles
00010b: Waiting time = 8 cycles
00011b: Waiting time = 16 cycles
00100b: Waiting time = 32 cycles
00101b: Waiting time = 64 cycles
00110b: Waiting time = 512 cycles
00111b: Waiting time = 1024 cycles
01000b: Waiting time = 2048 cycles
01001b: Waiting time = 4096 cycles
01010b: Waiting time = 16384 cycles
01011b: Waiting time = 32768 cycles
01100b: Waiting time = 65536 cycles
01101b: Waiting time = 131072 cycles
01110b: Waiting time = 262144 cycles
01111b: Waiting time = 524288 cycles
• PLL wait control register (PLLWTCR)
<table><tr><td>b0
b4</td><td>PSTS[4:0]</td><td>PLL waiting time bits</td></tr></table>• PLLWTCR.PSTS[4:0]
00000b: Waiting time = 16 cycles
... ...
01111b: Waiting time = 4194304 cycles
• Sub-clock oscillator wait control register (SOSCWTCR)
<table><tr><td>b0
b4</td><td>SSTS[4:0]</td><td>Subclock oscillator wait time setting bits</td></tr></table>• SOSCWTCR.SSTS[4:0]
00000b: Waiting time = 2 cycles
... ...
01111b: Waiting time = 524288 cycles</td></tr>
</table>

Table 2.5 Differences in Functions and Specifications (5)

Item		RX62N Group			RX63N Group		
Low power consumption functions	Registers/ bits	• Module stop control register A (MSTPCRA)			• Module stop control register A (MSTPCRA)		
		b4	MSTPA 4	8-bit timer 3/2 (unit 1) module stop setting bit	b4	MSTPA 4	8-bit timer 3/2 (unit 1) module stop setting bit
		b5	MSTPA 5	8-bit timer 1/0 (unit 0) module stop setting bit	b5	MSTPA 5	8-bit timer 1/0 (unit 0) module stop setting bit
		b8	MSTPA 8	Multifunction timer pulse unit (unit 1) module stop setting bit	b8	—	(Reserved bit)
		b9	MSTPA 9	Multifunction timer pulse unit (unit 0) module stop setting bit	b9	MSTPA 9	Multifunction timer pulse unit (unit 2) module stop setting bit
		b10	MSTPA10	Programmable pulse generator (unit 1) module stop setting bit	b10	MSTPA10	Programmable pulse generator (unit 1) module stop setting bit
		b11	MSTPA11	Programmable pulse generator (unit 0) module stop setting bit	b11	MSTPA11	Programmable pulse generator (unit 0) module stop setting bit
		b12	—	(Reserved bit)	b12	MSTPA12	16-bit timer pulse unit 1 (unit 1) module stop setting bit
		b13	—	(Reserved bit)	b13	MSTPA13	16-bit timer pulse unit 0 (unit 0) module stop setting bit
		b14	MSTPA14	Compare match timer (unit 1) module stop setting bit	b14	MSTPA14	Compare match timer (unit 1) module stop setting bit
		b15	MSTPA15	Compare match timer (unit 0) module stop setting bit	b15	MSTPA15	Compare match timer (unit 0) module stop setting bit
		b17	MSTPA17	12-bit A/D converter module stop setting bit	b17	MSTPA17	12-bit A/D converter module stop setting bit
		b19	MSTPA19	D/A converter module stop setting bit	b19	MSTPA19	D/A converter module stop setting bit
		b22	MSTPA22	10-bit A/D converter (unit 1) module stop setting bit	b22	—	(Reserved bit)
		b23	MSTPA23	10-bit A/D converter (unit 0) module stop setting bit	b23	MSTPA23	10-bit A/D converter module stop setting bit
		b24	—	(Reserved bit)	b24	MSTPA24	Module stop A24 setting bit
		b27	—	(Reserved bit)	b27	MSTPA27	Module stop A27 setting bit
		b28	MSTPA28	DMA controller/ Data transfer controller module stop setting bit	b28	MSTPA28	DMA controller/ Data transfer controller module stop setting bit
		b29	MSTPA29	EXDMA controller module stop setting bit	b29	MSTPA29	EXDMA controller module stop setting bit
		b31	ACSE	All-module clock stop mode enable bit	b31	ACSE	All-module clock stop mode enable bit

Table 2.6 Differences in Functions and Specifications (6)

Item		RX62N Group	RX63N Group
Low power consumption functions	Registers/ bits	• Module stop control register B (MSTPCRB)	• Module stop control register B (MSTPCRB)

b0	MSTPB 0	CAN module stop setting bit	b0	MSTPB 0	CAN module 0 module stop setting bit
b1	—	(Reserved bit)	b1	MSTPB 1	CAN module 1 module stop setting bit
b2	—	(Reserved bit)	b2	MSTPB 2	CAN module 2 module stop setting bit
b4	—	(Reserved bit)	b4	MSTPB 4	Serial communications interface SCId module stop setting bit
b8	—	(Reserved bit)	b8	MSTPB 8	Temperature sensor module stop setting bit
b15	MSTPB15	Ethernet controller DMA controller module stop setting bit	b15	MSTPB15	Ethernet controller DMA controller module stop setting bit
b16	MSTPB16	Serial peripheral interface 1 module stop setting bit	b16	MSTPB16	Serial peripheral interface 1 module stop setting bit
b17	MSTPB17	Serial peripheral interface 0 module stop setting bit	b17	MSTPB17	Serial peripheral interface 0 module stop setting bit
b18	MSTPB18	Universal serial bus interface (port 1) module stop setting bit	b18	MSTPB18	Universal serial bus interface (port 1) module stop setting bit
b19	MSTPB19	Universal serial bus interface (port 0) module stop setting bit	b19	MSTPB19	Universal serial bus interface (port 0) module stop setting bit
b20	MSTPB20	I^2C bus interface 1 module stop setting bit	b20	MSTPB20	I^2C bus interface 1 module stop setting bit
b21	MSTPB21	I^2C bus interface 0 module stop setting bit	b21	MSTPB21	I^2C bus interface 0 module stop setting bit
b23	MSTPB23	CRC calculator module stop setting bit	b23	MSTPB23	CRC calculator module stop setting bit
b24	—	(Reserved bit)	b24	MSTPB24	Serial communications interface 7 module stop setting bit
b25	MSTPB25	Serial communications interface 6 module stop setting bit	b25	MSTPB25	Serial communications interface 6 module stop setting bit
b26	MSTPB26	Serial communications interface 5 module stop setting bit	b26	MSTPB26	Serial communications interface 5 module stop setting bit
b27	—	(Reserved bit)	b27	MSTPB27	Serial communications interface 4 module stop setting bit
b28	MSTPB28	Serial communications interface 3 module stop setting bit	b28	MSTPB28	Serial communications interface 3 module stop setting bit
b29	MSTPB29	Serial communications interface 2 module stop setting bit	b29	MSTPB29	Serial communications interface 2 module stop setting bit
b30	MSTPB30	Serial communications interface 1 module stop setting bit	b30	MSTPB30	Serial communications interface 1 module stop setting bit
b31	MSTPB31	Serial communications interface 0 module stop setting bit	b31	MSTPB31	Serial communications interface 0 module stop setting bit

Table 2.7 Differences in Functions and Specifications (7)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="4">Low power consumption functions</td><td rowspan="4">Registers/ bits</td><td>• Module stop control register C (MSTPCRC)
<table>
<tr><td>b0</td><td>MSTPC 0</td><td>RAM0 module stop setting bit</td></tr>
<tr><td>b1</td><td>MSTPC 1</td><td>RAM1 module stop setting bit</td></tr>
<tr><td>b16</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b17</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b18</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b19</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b22</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b24</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b25</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b26</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b27</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• Module stop control register C (MSTPCRC)
<table>
<tr><td>b0</td><td>MSTPC 0</td><td>RAM0 module stop setting bit</td></tr>
<tr><td>b1</td><td>MSTPC 1</td><td>RAM1 module stop setting bit</td></tr>
<tr><td>b16</td><td>MSTPC16</td><td>I²C bus interface 3 module stop setting bit</td></tr>
<tr><td>b17</td><td>MSTPC17</td><td>I²C bus interface 2 module stop setting bit</td></tr>
<tr><td>b18</td><td>MSTPC18</td><td>IEBUS module stop setting bit</td></tr>
<tr><td>b19</td><td>MSTPC19</td><td>Clock frequency accuracy measurement circuit module stop setting bit</td></tr>
<tr><td>b22</td><td>MSTPC22</td><td>Serial peripheral interface 2 module stop setting bit</td></tr>
<tr><td>b24</td><td>MSTPC24</td><td>Serial communications interface 11 module stop setting bit</td></tr>
<tr><td>b25</td><td>MSTPC25</td><td>Serial communications interface 10 module stop setting bit</td></tr>
<tr><td>b26</td><td>MSTPC26</td><td>Serial communications interface 9 module stop setting bit</td></tr>
<tr><td>b27</td><td>MSTPC27</td><td>Serial communications interface 8 module stop setting bit</td></tr>
</table></td></tr>
<tr><td>—</td><td>• Operating power control register (OPCCR)
• Sleep mode return clock source switching register (RSTCKCR)</td></tr>
<tr><td>• Deep standby control register (DPSBYCR)
<table>
<tr><td>b0</td><td>RAMCUT0</td><td>On-chip RAM off 0 bit</td></tr>
<tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b4</td><td>RAMCUT1</td><td>On-chip RAM off 1 bit</td></tr>
<tr><td>b5</td><td>RAMCUT2</td><td>On-chip RAM off 2 bit</td></tr>
<tr><td>b6</td><td>IOKEEP</td><td>I/O port retention bit</td></tr>
<tr><td>b7</td><td>DPSBY</td><td>Deep software standby bit</td></tr>
</table>
• RAMCUT2 to RAMCUT0
000b: Power is supplied to the on-chip RAM (RAM0) and USB resume detecting unit in deep software standby mode.
111b: The above power supply levels are not provided
Setting prohibited other than above</td><td>• Deep standby control register (DPSBYCR)
<table>
<tr><td>b0
b1</td><td>DEEPCUT [1:0]</td><td>Deep cut bits</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b6</td><td>IOKEEP</td><td>I/O port retention bit</td></tr>
<tr><td>b7</td><td>DPSBY</td><td>Deep software standby bit</td></tr>
</table>
• DEEPCUT[1:0]
00b: Power is supplied to the RAM (RAM0) and USB resume detecting unit in deep software standby mode.
01b: The above power supply levels are not provided
10b: (Setting prohibited)
11b: Power is not supplied to the RAM (RAM0) and USB resume detecting unit in deep software standby mode. In addition, the LVD is stopped and the low power consumption function of the power-on reset circuit is enabled.</td></tr>
<tr><td>• Deep standby wait control register (DPSWCR)
• DPSWCR.WTSTS[5:0]
00101b: Waiting time = 64 cycles
00110b: Waiting time = 512 cycles
00111b: Waiting time = 1024 cycles
01000b: Waiting time = 2048 cycles
01001b: Waiting time = 4096 cycles
01010b: Waiting time = 16384 cycles
01011b: Waiting time = 32768 cycles
01100b: Waiting time = 65536 cycles
01101b: Waiting time = 131072 cycles
01110b: Waiting time = 262144 cycles
01111b: Waiting time = 524288 cycles</td><td>—
(LOCO return)</td></tr>
</table>

Table 2.8 Differences in Functions and Specifications (8)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="5">Low power consumption functions</td><td rowspan="5">Registers/ bits</td><td>• Deep standby interrupt enable register (DPSIER)
<table><tr><td>b0</td><td>DIRQ0E</td><td>IRQ0 pin enable bit</td></tr><tr><td>b1</td><td>DIRQ1E</td><td>IRQ1 pin enable bit</td></tr><tr><td>b2</td><td>DIRQ2E</td><td>IRQ2 pin enable bit</td></tr><tr><td>b3</td><td>DIRQ3E</td><td>IRQ3 pin enable bit</td></tr><tr><td>b4</td><td>DLVDE</td><td>LVD deep standby cancel signal enable bit</td></tr><tr><td>b5</td><td>DRTCE</td><td>RTC deep standby cancel signal enable bit</td></tr><tr><td>b6</td><td>DUSBE</td><td>USB suspend/resume deep standby cancel signal enable bit</td></tr><tr><td>b7</td><td>DNMIE</td><td>NMI pin enable bit</td></tr></table></td><td>• Deep standby interrupt enable register (DPSIER)
<table><tr><td>b0</td><td>DIRQ0E</td><td>IRQ0-DS pin enable bit</td></tr><tr><td>b1</td><td>DIRQ1E</td><td>IRQ1-DS pin enable bit</td></tr><tr><td>b2</td><td>DIRQ2E</td><td>IRQ2-DS pin enable bit</td></tr><tr><td>b3</td><td>DIRQ3E</td><td>IRQ3-DS pin enable bit</td></tr><tr><td>b4</td><td>DIRQ4E</td><td>IRQ4-DS pin enable bit</td></tr><tr><td>b5</td><td>DIRQ5E</td><td>IRQ5-DS pin enable bit</td></tr><tr><td>b6</td><td>DIRQ6E</td><td>IRQ6-DS pin enable bit</td></tr><tr><td>b7</td><td>DIRQ7E</td><td>IRQ7-DS pin enable bit</td></tr></table>• Deep standby interrupt enable register 2 (DPSIER2)
<table><tr><td>b0</td><td>DLVD1IE</td><td>LVD1 deep standby cancel signal enable bit</td></tr><tr><td>b1</td><td>DLVD2IE</td><td>LVD2 deep standby cancel signal enable bit</td></tr><tr><td>b2</td><td>DRTCIIE</td><td>RTC interval interrupt deep standby cancel signal enable bit</td></tr><tr><td>b3</td><td>DRTCAIE</td><td>RTC alarm interrupt deep standby cancel signal enable bit</td></tr><tr><td>b4</td><td>DNMIE</td><td>NMI pin enable bit</td></tr><tr><td>b5</td><td>DRIICDIE</td><td>SDA2-DS deep standby cancel signal enable bit</td></tr><tr><td>b6</td><td>DRIICCIE</td><td>SCL2-DS deep standby cancel signal enable bit</td></tr><tr><td>b7</td><td>DUSBIE</td><td>USB suspend/resume deep standby cancel signal enable bit</td></tr></table></td></tr>
<tr><td>—</td><td>• Deep standby interrupt enable register 1 (DPSIER1)
• Deep standby interrupt enable register 3 (DPSIER3)</td></tr>
<tr><td>• Deep standby interrupt flag register (DPSIFR)
<table><tr><td>b0</td><td>DIRQ0F</td><td>IRQ0 deep standby cancel flag</td></tr><tr><td>b1</td><td>DIRQ1F</td><td>IRQ1 deep standby cancel flag</td></tr><tr><td>b2</td><td>DIRQ2F</td><td>IRQ2 deep standby cancel flag</td></tr><tr><td>b3</td><td>DIRQ3F</td><td>IRQ3 deep standby cancel flag</td></tr><tr><td>b4</td><td>DLVDF</td><td>LVD deep standby cancel flag</td></tr><tr><td>b5</td><td>DRTCF</td><td>RTC deep standby cancel flag</td></tr><tr><td>b6</td><td>DUSBF</td><td>USB suspend/resume deep standby cancel flag</td></tr><tr><td>b7</td><td>DNMIF</td><td>NMI deep standby cancel flag</td></tr></table></td><td>• Deep standby interrupt flag register 0 (DPSIFR0)
<table><tr><td>b0</td><td>DIRQ0F</td><td>IRQ0-DS pin deep standby cancel flag</td></tr><tr><td>b1</td><td>DIRQ1F</td><td>IRQ1-DS pin deep standby cancel flag</td></tr><tr><td>b2</td><td>DIRQ2F</td><td>IRQ2-DS pin deep standby cancel flag</td></tr><tr><td>b3</td><td>DIRQ3F</td><td>IRQ3-DS pin deep standby cancel flag</td></tr><tr><td>b4</td><td>DIRQ4F</td><td>IRQ4-DS pin deep standby cancel flag</td></tr><tr><td>b5</td><td>DIRQ5F</td><td>IRQ5-DS pin deep standby cancel flag</td></tr><tr><td>b6</td><td>DIRQ6F</td><td>IRQ6-DS pin deep standby cancel flag</td></tr><tr><td>b7</td><td>DIRQ7F</td><td>IRQ7-DS pin deep standby cancel flag</td></tr></table>• Deep standby interrupt flag register 2 (DPSIFR2)
<table><tr><td>b0</td><td>DLVD1IF</td><td>LVD1 deep standby cancel flag</td></tr><tr><td>b1</td><td>DLVD2IF</td><td>LVD2 deep standby cancel flag</td></tr><tr><td>b2</td><td>DRTCIIF</td><td>RTC interval interrupt deep standby cancel flag</td></tr><tr><td>b3</td><td>DRTCAIF</td><td>RTC alarm interrupt deep standby cancel flag</td></tr><tr><td>b4</td><td>DNMIF</td><td>NMI deep standby cancel flag</td></tr><tr><td>b5</td><td>DRIICDIF</td><td>SDA2-DS deep standby cancel flag</td></tr><tr><td>b6</td><td>DRIICCIF</td><td>SCL2-DS deep standby cancel flag</td></tr><tr><td>b7</td><td>DUSBIF</td><td>USB suspend/resume deep standby cancel flag</td></tr></table></td></tr>
</table>

Table 2.9 Differences in Functions and Specifications (9)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="4">Low power consumption functions</td><td rowspan="4">Registers/ bits</td><td>—</td><td>• Deep standby interrupt flag register 1 (DPSIFR1)
• Deep standby interrupt flag register 3 (DPSIFR3)</td></tr>
<tr><td>• Deep standby interrupt edge register (DPSIEGR)
<table><tr><td>b0</td><td>DIRQ0EG</td><td>IRQ0 edge select bit</td></tr><tr><td>b1</td><td>DIRQ1EG</td><td>IRQ1 edge select bit</td></tr><tr><td>b2</td><td>DIRQ2EG</td><td>IRQ2 edge select bit</td></tr><tr><td>b3</td><td>DIRQ3EG</td><td>IRQ3 edge select bit</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>DNMIEG</td><td>NMI edge select bit</td></tr></table></td><td>• Deep standby interrupt edge register 0 (DPSIEGR0)
<table><tr><td>b0</td><td>DIRQ0EG</td><td>IRQ0-DS edge select bit</td></tr><tr><td>b1</td><td>DIRQ1EG</td><td>IRQ1-DS edge select bit</td></tr><tr><td>b2</td><td>DIRQ2EG</td><td>IRQ2-DS edge select bit</td></tr><tr><td>b3</td><td>DIRQ3EG</td><td>IRQ3-DS edge select bit</td></tr><tr><td>b4</td><td>DIRQ4EG</td><td>IRQ4-DS edge select bit</td></tr><tr><td>b5</td><td>DIRQ5EG</td><td>IRQ5-DS edge select bit</td></tr><tr><td>b6</td><td>DIRQ6EG</td><td>IRQ6-DS edge select bit</td></tr><tr><td>b7</td><td>DIRQ7EG</td><td>IRQ7-DS edge select bit</td></tr></table>• Deep standby interrupt edge register 2 (DPSIEGR2)
<table><tr><td>b0</td><td>DLVD1EG</td><td>LVD1 edge select bit</td></tr><tr><td>b1</td><td>DLVD2EG</td><td>LVD2 edge select bit</td></tr><tr><td>b4</td><td>DNMIEG</td><td>NMI edge select bit</td></tr><tr><td>b5</td><td>DRIICDEG</td><td>SDA2-DS edge select bit</td></tr><tr><td>b6</td><td>DRIICCEG</td><td>SCL2-DS edge select bit</td></tr></table></td></tr>
<tr><td>—</td><td>• Deep standby interrupt edge register 1 (DPSIEGR1)
• Deep standby interrupt edge register 3 (DPSIEGR3)</td></tr>
<tr><td>Battery backup function</td><td>Functions</td><td>—</td><td>• Specification overview
<table><tr><td>Battery backup power supplied to</td><td>Sub-clock oscillator
Realtime clock</td></tr></table></td></tr>
<tr><td>Register write protection function</td><td>Registers/ bits</td><td>—</td><td>• Protect register (PRCR)</td></tr>
<tr><td rowspan="4">Interrupt controller</td><td rowspan="4">Functions</td><td>• Peripheral function interrupts
<table><tr><td>Interrupts</td><td>Interrupts from peripheral modules</td></tr><tr><td>Sources</td><td>146</td></tr><tr><td>Interrupt detection</td><td>Edge detection/level detection</td></tr></table></td><td>• Peripheral function interrupts
<table><tr><td>Interrupts</td><td>Interrupts from peripheral modules</td></tr><tr><td>Sources</td><td>187</td></tr><tr><td>Interrupt detection</td><td>Edge detection/level detection</td></tr></table></td></tr>
<tr><td>—</td><td>• Group function interrupts
<table><tr><td>Edge detection</td><td>7 (groups 0 to 6)</td></tr><tr><td>Level detection</td><td>1 (group 12)</td></tr></table>• Unit selection function
<table><tr><td>Units</td><td>6</td></tr></table></td></tr>
<tr><td>• Non-maskable interrupts
<table><tr><td>Interrupt types</td><td>NMI pin interrupt
Digital filter function: Not Supported</td></tr><tr><td></td><td>Oscillation stop detection interrupt</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>Voltage-monitoring interrupt</td></tr><tr><td></td><td>—</td></tr></table></td><td>• Non-maskable interrupts
<table><tr><td>Interrupt types</td><td>NMI pin interrupt
Digital filter function: Supported</td></tr><tr><td></td><td>Oscillation stop detection interrupt</td></tr><tr><td></td><td>WDT underflow/ refresh error</td></tr><tr><td></td><td>IWDT underflow/ refresh error</td></tr><tr><td></td><td>Voltage-monitoring 1 interrupt</td></tr><tr><td></td><td>Voltage-monitoring 2 interrupt</td></tr></table></td></tr>
<tr><td>• Return from power-down modes
<table><tr><td>Sleep mode</td><td>Non-maskable interrupts
All interrupt sources</td></tr><tr><td>All-module clock stop mode</td><td>Non-maskable interrupts
IRQ0 to IRQ15 interrupts
WDT interrupts
TMR interrupts
USB resume interrupts
RTC alarm interrupts</td></tr><tr><td>Software standby mode</td><td>Non-maskable interrupts
IRQ0 to IRQ15 interrupts
USB interrupts (USBR)
RTC interrupts</td></tr></table></td><td>• Return from power-down modes
<table><tr><td>Sleep mode</td><td>Non-maskable interrupts
All interrupt sources</td></tr><tr><td>All-module clock stop mode</td><td>Non-maskable interrupts
IRQ0 to IRQ15 interrupts
— (WDT: Non-maskable interrupts)
TMR interrupts
USB resume interrupts
RTC alarm/periodic interrupts</td></tr><tr><td>Software standby mode</td><td>Non-maskable interrupts
IRQ0 to IRQ15 interrupts
USB resume interrupts
RTC alarm/periodic interrupts</td></tr></table></td></tr>
</table>

Table 2.10 Differences in Functions and Specifications (10)

Item		RX62N Group	RX63N Group
Interrupt controller	Vector table	• Vector table (1/4)	• Vector table (1/4)

No	Interrupts	Name	DTCER	IPR
0	—	(Reserved)	—	—
1	—	(Reserved)	—	—
2	—	(Reserved)	—	—
3	—	(Reserved)	—	—
4	—	(Reserved)	—	—
5	—	(Reserved)	—	—
6	—	(Reserved)	—	—
7	—	(Reserved)	—	—
8	—	(Reserved)	—	—
9	—	(Reserved)	—	—
10	—	(Reserved)	—	—
11	—	(Reserved)	—	—
12	—	(Reserved)	—	—
13	—	(Reserved)	—	—
14	—	(Reserved)	—	—
15	—	(Reserved)	—	—
16	Bus error	BUSERR	—	00
21	FCU	FIFERR	—	01
23		FRDYI		02
27	ICU	SWINT	027	03
28	CMT0	CMI0	028	04
29	CMT1	CMI1	029	05
30	CMT2	CMI2	030	06
31	CMT3	CMI3	031	07
32	ETHER	EINT	—	08
33	—	(Reserved)	—	09
34	—	(Reserved)	—	0A
35	—	(Reserved)	—	0B
36	USB0	D0FIFO0	036	0C
37		D1FIFO0	037	0D
38		USBI0	—	0E
39	—	(Reserved)	—	0F
40	USB1	D0FIFO1	040	10
41		D1FIFO1	041	11
42		USBI1	—	12
43	—	(Reserved)	—	13
44	RSPI0	SPEI0	—	14
45		SPRI0	045	
46		SPTI0	046	
47		SPII0	—	
48	RSPI1	SPEI1	—	15
49		SPRI1	049	
50		SPTI1	050	
51		SPII1	—	
52	—	(Reserved)	—	—
53	—	(Reserved)	—	—
54	—	(Reserved)	—	—
55	—	(Reserved)	—	—
56	CAN0	ERS0	—	18
57		RXF0		
58		TXF0		
59		RXM0		
60		TXM0		
61	—	(Reserved)	—	1D
62	RTC	PRD	—	1E
63		CUP		1F

No	Interrupts	Name	DTCER	IPR
0	—	Unconditional trap dedicated	—	—
1	—	Unconditional trap dedicated	—	—
2	—	Unconditional trap dedicated	—	—
3	—	Unconditional trap dedicated	—	—
4	—	Unconditional trap dedicated	—	—
5	—	Unconditional trap dedicated	—	—
6	—	Unconditional trap dedicated	—	—
7	—	Unconditional trap dedicated	—	—
8	—	Unconditional trap dedicated	—	—
9	—	Unconditional trap dedicated	—	—
10	—	Unconditional trap dedicated	—	—
11	—	Unconditional trap dedicated	—	—
12	—	Unconditional trap dedicated	—	—
13	—	Unconditional trap dedicated	—	—
14	—	Unconditional trap dedicated	—	—
15	—	Unconditional trap dedicated	—	—
16	Bus error	BUSERR	—	000
21	FCU	FIFERR	—	001
23		FRDYI		002
27	ICU	SWINT	027	003
28	CMT0	CMI0	028	004
29	CMT1	CMI1	029	005
30	CMT2	CMI2	030	006
31	CMT3	CMI3	031	007
32	Ehter	EINT	—	032
33	USB0	D0FIFO0	033	033
34		D1FIFO0	034	034
35		USBI0	—	035
36	USB1	D0FIFO1	036	036
37		D1FIFO1	037	037
38		USBI1	—	038
39	RSPI0	SPRI0	039	039
40		SPTI0	040	
41		SPII0	—	
42	RSPI1	SPRI1	042	042
43		SPTI1	043	
44		SPII1	—	
45	RSPI2	SPRI2	045	045
46		SPTI2	046	
47		SPII2	—	
48	CAN0	RXF0	—	048
49		TXF0		
50		RXM0		
51		TXM0		
52	CAN1	RXF1	—	052
53		TXF1		
54		RXM1		
55		TXM1		
56	CAN2	RXF2	—	056
57		TXF2		
58		RXM2		
59		TXM2		
60	—	(Reserved)	—	—
61	—	(Reserved)	—	—
62	RTC	CUP	—	062
63	—	(Reserved)	—	—

Table 2.11 Differences in Functions and Specifications (11)

Item		RX62N Group	RX63N Group
Interrupt controller	Vector table	• Vector table (2/4)	• Vector table (2/4)

No	Interrupts	Name	DTCER	IPR
64	External pin	IRQ0	064	20
65		IRQ1	065	21
66		IRQ2	066	22
67		IRQ3	067	23
68		IRQ4	068	24
69		IRQ5	069	25
70		IRQ6	070	26
71		IRQ7	071	27
72		IRQ8	072	28
73		IRQ9	073	29
74		IRQ10	074	2A
75		IRQ11	075	2B
76		IRQ12	076	2C
77		IRQ13	077	2D
78		IRQ14	078	2E
79		IRQ15	079	2F
90	USB	USBR0	—	3A
91		USBR1		3B
92	RTC	ALM	—	3C
93	—	(Reserved)	—	—
96	WDT	WOVI	—	40
98	AD0	ADI0	098	44
99	AD1	ADI1	099	45
102	S12AD	S12ADI0	102	48
106	—	(Reserved)	—	—
107	—	(Reserved)	—	—
108	—	(Reserved)	—	—
109	—	(Reserved)	—	—
110	—	(Reserved)	—	—
111	—	(Reserved)	—	—
112	—	(Reserved)	—	—
114	MTU0	TGIA0	114	51
115		TGIB0	115	
116		TGIC0	116	
117		TGID0	117	
118		TCIV0	—	52
119		TGIE0		
120		TGIF0		
121	MTU1	TGIA1	121	53
122		TGIB1	122	
123		TCIV1	—	54
124		TCIU1		
125	MTU2	TGIA2	125	55
126		TGIB2	126	
127		TCIV2	—	56
128		TCIU2		
129	MTU3	TGIA3	129	57
130		TGIB3	130	
131		TGIC3	131	
132		TGID3	132	
133		TCIV3	—	58
134	MTU4	TGIA4	134	59
135		TGIB4	135	
136		TGIC4	136	
137		TGID4	137	
138		TCIV4	138	5A
139	MTU5	TGIU5	139	5B
140		TGIV5	140	
141		TGIW5	141	

No	Interrupts	Name	DTCER	IPR
64	ICU	IRQ0	064	064
65		IRQ1	065	065
66		IRQ2	066	066
67		IRQ3	067	067
68		IRQ4	068	068
69		IRQ5	069	069
70		IRQ6	070	070
71		IRQ7	071	071
72		IRQ8	072	072
73		IRQ9	073	073
74		IRQ10	074	074
75		IRQ11	075	075
76		IRQ12	076	076
77		IRQ13	077	077
78		IRQ14	078	078
79		IRQ15	079	079
90	USB	USBR0	—	090
91		USBR1		091
92	RTC	ALM	—	092
93		PRD		093
96	—	(Reserved)	—	—
98	AD	ADI0	098	098
99	—	(Reserved)	—	—
102	S12AD	S12ADI0	102	102
106	ICU	GROUP0	—	106
107		GROUP1	—	107
108		GROUP2	—	108
109		GROUP3	—	109
110		GROUP4	—	110
111		GROUP5	—	111
112		GROUP6	—	112
114		GROUP12	—	114
115	—	(Reserved)	—	—
116	—	(Reserved)	—	—
117	—	(Reserved)	—	—
118	—	(Reserved)	—	—
119	—	(Reserved)	—	—
120	—	(Reserved)	—	—
121	—	(Reserved)	—	—
122	SCI12	SCIX0	—	122
123		SCIX1		
124		SCIX2		
125		SCIX3		
126	TPU0	TGI0A	126	126
127		TGI0B	127	
128		TGI0C	128	
129		TGI0D	129	
130	TPU1	TGI1A	130	130
131		TGI1B	131	
132	TPU2	TGI2A	132	132
133		TGI2B	133	
134	TPU3	TGI3A	134	134
135		TGI3B	135	
136		TGI3C	136	
137		TGI3D	137	
138	TPU4	TGI4A	138	138
139		TGI4B	139	
140	TPU5	TGI5A	140	140
141		TGI5B	141	

Table 2.12 Differences in Functions and Specifications (12)

Item		RX62N Group	RX63N Group
Interrupt controller	Vector table	• Vector table (3/4)	• Vector table (3/4)

No	Interrupts	Name	DTCER	IPR
142	MTU6	TGIA6	142	5C
143		TGIB6	143	
144		TGIC6	144	
145		TGID6	145	
146		TCIV6	—	5D
147		TGIE6		
148		TGIF6		
149	MTU7	TGIA7	149	5E
150		TGIB7	150	
151		TCIV7	—	5F
152		TCIU7		
153	MTU8	TGIA8	153	60
154		TGIB8	154	
155		TCIV8	—	61
156		TCIU8		
157	MTU9	TGIA9	157	62
158		TGIB9	158	
159		TGIC9	159	
160		TGID9	160	
161		TCIV9	—	63
162	MTU10	TGIA10	162	64
163		TGIB10	163	
164		TGIC10	164	
165		TGID10	165	
166		TCIV10	166	65
167	MTU11	TGIU11	167	66
168		TGIV11	168	
169		TGIW11	169	
170	POE	OEI1	—	67
171		OEI2		
172		OEI3		
173		OEI4		
174	TMR0	CMIA0	174	68
175		CMIB0	175	
176		OVI0	—	
177	TMR1	CMIA1	177	69
178		CMIB1	178	
179		OVI1	—	
180	TMR2	CMIA2	180	6A
181		CMIB2	181	
182		OVI2	—	
183	TMR3	CMIA3	183	6B
184		CMIB3	184	
185		OVI3	—	
186	—	(Reserved)	—	—
187	—	(Reserved)	—	—
188	—	(Reserved)	—	—
189	—	(Reserved)	—	—
190	—	(Reserved)	—	—
191	—	(Reserved)	—	—
192	—	(Reserved)	—	—
193	—	(Reserved)	—	—
194	—	(Reserved)	—	—
195	—	(Reserved)	—	—
196	—	(Reserved)	—	—
197	—	(Reserved)	—	—
198	DMACA	DMACI0	198	70
199		DMACI1	199	71
200		DMACI2	200	72
201		DMACI3	201	73
202	EXDMAC	EXDMACI0	202	74
203		EXDMACI1	203	75

No	Interrupts	Name	DTCER	IPR
142	TPU6/MTU0	TGI6A/TGIA0	142	142
143		TGI6B/TGIB0	143	
144		TGI6C/TGIC0	144	
145		TGI6D/TGID0	145	
146		—/TGIE0	—	146
147		—/TGIF0		
148	TPU7/MTU1	TGI7A/TGIA1	148	148
149		TGI7B/TGIB1	149	
150	TPU8/MTU2	TGI8A/TGIA2	150	150
151		TGI8B/TGIB2	151	
152	TPU9/MTU3	TGI9A/TGIA3	152	152
153		TGI9B/TGIB3	153	
154		TGI9C/TGIC3	154	
155		TGI9D/TGID3	155	
156	TPU10/MTU4	TGI10A/TGIA4	156	156
157		TGI10B/TGIB4	157	
158		—/TGIC4	158	
159		—/TGID4	159	
160		—/TGIV4	160	160
161	TPU11/MTU5	—/TGIU5	161	161
162		—/TGIV5	162	
163		—/TGIW5	163	
164		TGI11A/—	164	164
165		TGI11B/—	165	
166	POE	OEI1	—	166
167		OEI2		
168	—	(Reserved)	—	—
169	—	(Reserved)	—	—
170	TMR0	CMIA0	170	170
171		CMIB0	171	
172		OVI0	—	
173	TMR1	CMIA1	173	173
174		CMIB1	174	
175		OVI1	—	
176	TMR2	CMIA2	176	176
177		CMIB2	177	
178		OVI2	—	
179	TMR3	CMIA3	179	179
180		CMIB3	180	
181		OVI3	—	
182	RIIC0	EEI0	—	182
183		RXI0	183	183
184		TXI0	184	184
185		TEI0	—	185
186	RIIC1	EEI1	—	186
187		RXI1	187	187
188		TXI1	188	188
189		TEI1	—	189
190	RIIC2	EEI2	—	190
191		RXI2	191	191
192		TXI2	192	192
193		TEI2	—	193
194	RIIC3	EEI3	—	194
195		RXI3	195	195
196		TXI3	196	196
197		TEI3	—	197
198	DMAC	DMAC0I	198	198
199		DMAC1I	199	199
200		DMAC2I	200	200
201		DMAC3I	201	201
202	EXDMAC	EXDMAC0I	202	202
203		EXDMAC1I	203	203

Table 2.13 Differences in Functions and Specifications (13)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="3">Interrupt controller</td><td>Vector table</td><td>• Vector table (4/4)
<table>
<tr><th>No</th><th>Interrupts</th><th>Name</th><th>DTCER</th><th>IPR</th></tr>
<tr><td>214</td><td>SCI0</td><td>ERI0</td><td>—</td><td>80</td></tr>
<tr><td>215</td><td></td><td>RXI0</td><td>215</td><td></td></tr>
<tr><td>216</td><td></td><td>TXI0</td><td>216</td><td></td></tr>
<tr><td>217</td><td></td><td>TEI0</td><td>—</td><td></td></tr>
<tr><td>218</td><td>SCI1</td><td>ERI1</td><td>—</td><td>81</td></tr>
<tr><td>219</td><td></td><td>RXI1</td><td>219</td><td></td></tr>
<tr><td>220</td><td></td><td>TXI1</td><td>220</td><td></td></tr>
<tr><td>221</td><td></td><td>TEI1</td><td>—</td><td></td></tr>
<tr><td>222</td><td>SCI2</td><td>ERI2</td><td>—</td><td>82</td></tr>
<tr><td>223</td><td></td><td>RXI2</td><td>223</td><td></td></tr>
<tr><td>224</td><td></td><td>TXI2</td><td>224</td><td></td></tr>
<tr><td>225</td><td></td><td>TEI2</td><td>—</td><td></td></tr>
<tr><td>226</td><td>SCI3</td><td>ERI3</td><td>—</td><td>83</td></tr>
<tr><td>227</td><td></td><td>RXI3</td><td>227</td><td></td></tr>
<tr><td>228</td><td></td><td>TXI3</td><td>228</td><td></td></tr>
<tr><td>229</td><td></td><td>TEI3</td><td>—</td><td></td></tr>
<tr><td>230</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>231</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>232</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>233</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>234</td><td>SCI5</td><td>ERI5</td><td>—</td><td>85</td></tr>
<tr><td>235</td><td></td><td>RXI5</td><td>235</td><td></td></tr>
<tr><td>236</td><td></td><td>TXI5</td><td>236</td><td></td></tr>
<tr><td>237</td><td></td><td>TEI5</td><td>—</td><td></td></tr>
<tr><td>238</td><td>SCI6</td><td>ERI6</td><td>—</td><td>86</td></tr>
<tr><td>239</td><td></td><td>RXI6</td><td>239</td><td></td></tr>
<tr><td>240</td><td></td><td>TXI6</td><td>240</td><td></td></tr>
<tr><td>241</td><td></td><td>TEI6</td><td>—</td><td></td></tr>
<tr><td>242</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>243</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>244</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>245</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>246</td><td>RIIC0</td><td>ICEEI0</td><td>—</td><td>88</td></tr>
<tr><td>247</td><td></td><td>ICRXI0</td><td>247</td><td>89</td></tr>
<tr><td>248</td><td></td><td>ICTXI0</td><td>248</td><td>8A</td></tr>
<tr><td>249</td><td></td><td>ICTEI0</td><td>—</td><td>8B</td></tr>
<tr><td>250</td><td>RIIC1</td><td>ICEEI1</td><td>—</td><td>8C</td></tr>
<tr><td>251</td><td></td><td>ICRXI1</td><td>251</td><td>8D</td></tr>
<tr><td>252</td><td></td><td>ICTXI1</td><td>252</td><td>8E</td></tr>
<tr><td>253</td><td></td><td>ICTEI1</td><td>—</td><td>8F</td></tr>
<tr><td>254</td><td>—</td><td>(Reserved)</td><td>—</td><td>90</td></tr>
<tr><td>255</td><td>—</td><td>(Reserved)</td><td>—</td><td>91</td></tr>
</table></td><td>• Vector table (4/4)
<table>
<tr><th>No</th><th>Interrupts</th><th>Name</th><th>DTCER</th><th>IPR</th></tr>
<tr><td>214</td><td>SCI0</td><td>RXI0</td><td>214</td><td>214</td></tr>
<tr><td>215</td><td></td><td>TXI0</td><td>215</td><td></td></tr>
<tr><td>216</td><td></td><td>TEI0</td><td>—</td><td></td></tr>
<tr><td>217</td><td>SCI1</td><td>RXI1</td><td>217</td><td>217</td></tr>
<tr><td>218</td><td></td><td>TXI1</td><td>218</td><td></td></tr>
<tr><td>219</td><td></td><td>TEI1</td><td>—</td><td></td></tr>
<tr><td>220</td><td>SCI2</td><td>RXI2</td><td>220</td><td>220</td></tr>
<tr><td>221</td><td></td><td>TXI2</td><td>221</td><td></td></tr>
<tr><td>222</td><td></td><td>TEI2</td><td>—</td><td></td></tr>
<tr><td>223</td><td>SCI3</td><td>RXI3</td><td>223</td><td>223</td></tr>
<tr><td>224</td><td></td><td>TXI3</td><td>224</td><td></td></tr>
<tr><td>225</td><td></td><td>TEI3</td><td>—</td><td></td></tr>
<tr><td>226</td><td>SCI4</td><td>RXI4</td><td>226</td><td>226</td></tr>
<tr><td>227</td><td></td><td>TXI4</td><td>227</td><td></td></tr>
<tr><td>228</td><td></td><td>TEI4</td><td>—</td><td></td></tr>
<tr><td>229</td><td>SCI5</td><td>RXI5</td><td>229</td><td>229</td></tr>
<tr><td>230</td><td></td><td>TXI5</td><td>230</td><td></td></tr>
<tr><td>231</td><td></td><td>TEI5</td><td>—</td><td></td></tr>
<tr><td>232</td><td>SCI6</td><td>RXI6</td><td>232</td><td>232</td></tr>
<tr><td>233</td><td></td><td>TXI6</td><td>233</td><td></td></tr>
<tr><td>234</td><td></td><td>TEI6</td><td>—</td><td></td></tr>
<tr><td>235</td><td>SCI7</td><td>RXI7</td><td>235</td><td>235</td></tr>
<tr><td>236</td><td></td><td>TXI7</td><td>236</td><td></td></tr>
<tr><td>237</td><td></td><td>TEI7</td><td>—</td><td></td></tr>
<tr><td>238</td><td>SCI8</td><td>RXI8</td><td>238</td><td>238</td></tr>
<tr><td>239</td><td></td><td>TXI8</td><td>239</td><td></td></tr>
<tr><td>240</td><td></td><td>TEI8</td><td>—</td><td></td></tr>
<tr><td>241</td><td>SCI9</td><td>RXI9</td><td>241</td><td>241</td></tr>
<tr><td>242</td><td></td><td>TXI9</td><td>242</td><td></td></tr>
<tr><td>243</td><td></td><td>TEI9</td><td>—</td><td></td></tr>
<tr><td>244</td><td>SCI10</td><td>RXI10</td><td>244</td><td>244</td></tr>
<tr><td>245</td><td></td><td>TXI10</td><td>245</td><td></td></tr>
<tr><td>246</td><td></td><td>TEI10</td><td>—</td><td></td></tr>
<tr><td>247</td><td>SCI11</td><td>RXI11</td><td>247</td><td>247</td></tr>
<tr><td>248</td><td></td><td>TXI11</td><td>248</td><td></td></tr>
<tr><td>249</td><td></td><td>TEI11</td><td>—</td><td></td></tr>
<tr><td>250</td><td>SCI12</td><td>RXI12</td><td>250</td><td>250</td></tr>
<tr><td>251</td><td></td><td>TXI12</td><td>251</td><td></td></tr>
<tr><td>252</td><td></td><td>TEI12</td><td>—</td><td></td></tr>
<tr><td>253</td><td>IEB</td><td>IEBINT</td><td>—</td><td>253</td></tr>
<tr><td>254</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
<tr><td>255</td><td>—</td><td>(Reserved)</td><td>—</td><td>—</td></tr>
</table></td></tr>
<tr><td>Registers/ bits</td><td>• Non-maskable interrupt status register (NMISR)
<table>
<tr><td>b0</td><td>NMIST</td><td>NMI status flag</td></tr>
<tr><td>b1</td><td>LVDST</td><td>Voltage monitoring interrupt status flag</td></tr>
<tr><td>b2</td><td>OSTST</td><td>Oscillation stop detection interrupt status flag</td></tr>
<tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
</table>
• Non-maskable interrupt enable register (NMIER)
<table>
<tr><td>b0</td><td>NMIEN</td><td>NMI pin interrupt enable bit</td></tr>
<tr><td>b1</td><td>LVDEN</td><td>Voltage monitoring interrupt enable bit</td></tr>
<tr><td>b2</td><td>OSTEN</td><td>Oscillation stop detection interrupt enable bit</td></tr>
<tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• Non-maskable interrupt status register (NMISR)
<table>
<tr><td>b0</td><td>NMIST</td><td>NMI status flag</td></tr>
<tr><td>b1</td><td>OSTST</td><td>Oscillation stop detection interrupt status flag</td></tr>
<tr><td>b2</td><td>WDTST</td><td>WDT underflow/refresh error status flag</td></tr>
<tr><td>b3</td><td>IWDTST</td><td>IWDT underflow/refresh error status flag</td></tr>
<tr><td>b4</td><td>LVD1ST</td><td>Voltage monitoring 1 interrupt status flag</td></tr>
<tr><td>b5</td><td>LVD2ST</td><td>Voltage monitoring 2 interrupt status flag</td></tr>
</table>
• Non-maskable interrupt enable register (NMIER)
<table>
<tr><td>b0</td><td>NMIEN</td><td>NMI pin interrupt enable bit</td></tr>
<tr><td>b1</td><td>OSTEN</td><td>Oscillation stop detection interrupt enable bit</td></tr>
<tr><td>b2</td><td>WDTEN</td><td>WDT underflow/refresh error enable bit</td></tr>
<tr><td>b3</td><td>IWDTEN</td><td>IWDT underflow/refresh error enable bit</td></tr>
<tr><td>b4</td><td>LVD1EN</td><td>Voltage monitoring 1 interrupt enable bit</td></tr>
<tr><td>b5</td><td>LVD2EN</td><td>Voltage monitoring 2 interrupt enable bit</td></tr>
</table></td></tr>
</table>

Table 2.14 Differences in Functions and Specifications (14)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="3">Interrupt controller</td><td rowspan="3">Registers/ bits</td><td>• Non-maskable interrupt clear register (NMICLR)
<table><tr><td>b0</td><td>NMICLR</td><td>NMI clear bit</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2</td><td>OSTCLR</td><td>OST clear bit</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• Non-maskable interrupt clear register (NMICLR)
<table><tr><td>b0</td><td>NMICLR</td><td>NMI clear bit</td></tr><tr><td>b1</td><td>OSTCLR</td><td>OST clear bit</td></tr><tr><td>b2</td><td>WDTCLR</td><td>WDT clear bit</td></tr><tr><td>b3</td><td>IWDTCLR</td><td>IWDT clear bit</td></tr><tr><td>b4</td><td>LVD1CLR</td><td>LVD1 clear bit</td></tr><tr><td>b5</td><td>LVD2CLR</td><td>LVD2 clear bit</td></tr></table></td></tr>
<tr><td>—</td><td>• NMI pin digital filter enable register (NMIFLTE)
• NMI pin digital filter setting register (NMIFLTC)
• IRQ pin digital filter enable register 0 (IRQFLTE0)
• IRQ pin digital filter enable register 1 (IRQFLTE1)
• IRQ pin digital filter setting register 0 (IRQFLTC0)
• IRQ pin digital filter setting register 1 (IRQFLTC1)
• Group m interrupt source register (GRPm)
• Group m interrupt enable register (GENm)
• Group m interrupt clear register (GCRm)
• Unit selecting register (SEL)</td></tr>
<tr><td colspan="2"></td><td></td><td></td></tr>
<tr><td rowspan="3">Bus</td><td rowspan="3">Functions</td><td>• Bus configuration (on-chip peripheral buses)
<table><tr><td>On-chip peripheral bus 1</td><td>DMACA, peripheral function</td><td>ICLK</td></tr><tr><td>On-chip peripheral bus 2</td><td>Peripheral function</td><td>PCLK</td></tr><tr><td>On-chip peripheral bus 3</td><td>USB</td><td>PCLK</td></tr><tr><td>On-chip peripheral bus 4</td><td>EDMAC, ETHERC</td><td>ICLK</td></tr><tr><td>On-chip peripheral bus 5</td><td>Peripheral function</td><td>ICLK</td></tr><tr><td>On-chip peripheral bus 6</td><td>On-chip ROM, data flash</td><td>PCLK</td></tr></table></td><td>• Bus configuration (on-chip peripheral buses)
<table><tr><td>On-chip peripheral bus 1</td><td>DTC, DMAC, EXDMAC, interrupt controller, bus error monitoring section</td><td>ICLK</td></tr><tr><td>On-chip peripheral bus 2</td><td>Peripheral buses other than on-chip peripheral buses 1, 3, 4, and 5</td><td>PCLKB</td></tr><tr><td>On-chip peripheral bus 3</td><td>USB</td><td>PCLKB</td></tr><tr><td>On-chip peripheral bus 4</td><td>EDMAC, ETHERC</td><td>PCLKA</td></tr><tr><td>On-chip peripheral bus 5</td><td>—</td><td>—</td></tr><tr><td>On-chip peripheral bus 6</td><td>ROM, E2 data flash</td><td>FCLK</td></tr></table></td></tr>
<tr><td>• Bus error (illegal address access)
<table><tr><td rowspan="2">Address</td><td colspan="2">On-chip ROM mode</td></tr><tr><td>Enabled</td><td>Disabled</td></tr><tr><td>0000 0000h to 0007 FFFFh</td><td colspan="2">—</td></tr><tr><td>0008 0000h to 0009 0FFFh</td><td colspan="2">—</td></tr><tr><td>0009 1000h to 0009 FFFFh</td><td colspan="2">○</td></tr><tr><td>000A 0000h to 000A 00FFh</td><td colspan="2">—</td></tr><tr><td>000A 0100h to 000A 01FFh</td><td colspan="2">○</td></tr><tr><td>000A 0200h to 000A 02FFh</td><td colspan="2">—</td></tr><tr><td>000A 0300h to 000A 03FFh</td><td colspan="2">○</td></tr><tr><td>000A 0400h to 000A 041Fh</td><td colspan="2">—</td></tr><tr><td>000A 0420h to 000B FFFFh</td><td colspan="2">○</td></tr><tr><td>000C 0000h to 000C 043Fh</td><td colspan="2">—</td></tr><tr><td>000C 0440h to 000D FFFFh</td><td colspan="2">○</td></tr><tr><td>000E 0000h to 000F FFFFh</td><td colspan="2">○</td></tr><tr><td>0010 0000h to 0011 FFFFh</td><td>—</td><td rowspan="12">○</td></tr><tr><td>0012 0000h to 007F 7FFFh</td><td>○</td></tr><tr><td>007F 8000h to 007F 9FFFh</td><td>—</td></tr><tr><td>007F A000h to 007F BFFFh</td><td>○</td></tr><tr><td>007F C000h to 007F C4FFh</td><td>—</td></tr><tr><td>007F C500h to 007F FBFFh</td><td>○</td></tr><tr><td>007F FC00h to 007F FFFFh</td><td>—</td></tr><tr><td>0080 0000h to 00DF FFFFh</td><td>—</td></tr><tr><td>00E0 0000h to 00FF FFFFh</td><td>—</td></tr><tr><td>0100 0000h to 07FF FFFFh</td><td colspan="2">[IA]</td></tr><tr><td>0800 0000h to 0FFF FFFFh</td><td colspan="2">[IA]</td></tr><tr><td>1000 0000h to 7FFF FFFFh</td><td colspan="2">○</td></tr><tr><td>8000 0000h to FEFF FFFFh</td><td>—</td><td>○</td></tr><tr><td>FF00 0000h to FFFF FFFFh</td><td>—</td><td>[IA]</td></tr></table></td><td>• Bus error (illegal address access)
<table><tr><td rowspan="2">Address</td><td colspan="2">On-chip ROM mode</td></tr><tr><td>Enabled</td><td>Disabled</td></tr><tr><td>0000 0000h to 0007 FFFFh</td><td colspan="2">—</td></tr><tr><td>0008 0000h to 0008 7FFFh</td><td colspan="2">—</td></tr><tr><td>0008 8000h to 0009 FFFFh</td><td colspan="2">Δ</td></tr><tr><td>000A 0000h to 000B FFFFh</td><td colspan="2">Δ</td></tr><tr><td>000C 0000h to 000D FFFFh</td><td colspan="2">Δ</td></tr><tr><td>000E 0000h to 000F FFFFh</td><td colspan="2">—</td></tr><tr><td>0010 0000h to 00FF FFFFh</td><td>Δ</td><td>○</td></tr><tr><td>0100 0000h to 07FF FFFFh</td><td colspan="2">[IA]</td></tr><tr><td>0800 0000h to 0FFF FFFFh</td><td colspan="2">[IA]</td></tr><tr><td>1000 0000h to 7FFF FFFFh</td><td colspan="2">○</td></tr><tr><td>8000 0000h to FEFF FFFFh</td><td>—</td><td>○</td></tr><tr><td>FF00 0000h to FFFF FFFFh</td><td>—</td><td>[IA]</td></tr></table></td></tr>
<tr><td>—</td><td>• Multiplexed bus function</td></tr>
</table>

Table 2.15 Differences in Functions and Specifications (15)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="4">Bus</td><td rowspan="4">Registers/ bits</td><td>• CSn control register (CSnCR)<table><tr><td>b0</td><td>EXENB</td><td>Operation enable bit</td></tr><tr><td>b4
b5</td><td>BSIZE[1:0]</td><td>External bus width select bits</td></tr><tr><td>b8</td><td>EMODE</td><td>Endian mode bit</td></tr><tr><td>b12</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• CSn control register (CSnCR)<table><tr><td>b0</td><td>EXENB</td><td>Operation enable bit</td></tr><tr><td>b4
b5</td><td>BSIZE[1:0]</td><td>External bus width select bits</td></tr><tr><td>b8</td><td>EMODE</td><td>Endian mode bit</td></tr><tr><td>b12</td><td>MPXEN</td><td>Address/data multiplexed I/O interface select bit</td></tr></table></td></tr>
<tr><td>—</td><td>• CS recovery cycle insertion enable register (CSRECEN)</td></tr>
<tr><td>• CSn wait control register 2 (CSnWCR2)<table><tr><td>b0
b2</td><td>CSROFF [2:0]</td><td>Read-access CS extension cycle select bits</td></tr><tr><td>b4
b5</td><td>CSWOFF [2:0]</td><td>Write-access CS extension cycle select bits</td></tr><tr><td>b8
b10</td><td>WDOFF [2:0]</td><td>Write data output extension cycle select bits</td></tr><tr><td>b12
b13</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b16
b18</td><td>RDON[2:0]</td><td>RD assert wait select bits</td></tr><tr><td>b20
b22</td><td>WRON[2:0]</td><td>WR assert wait select bits</td></tr><tr><td>b24
b26</td><td>WDON[2:0]</td><td>Write data output wait select bits</td></tr><tr><td>b28
b30</td><td>CSON[2:0]</td><td>CS assert wait select bits</td></tr></table></td><td>• CSn wait control register 2 (CSnWCR2)<table><tr><td>b0
b2</td><td>CSROFF [2:0]</td><td>Read-access CS extension cycle select bits</td></tr><tr><td>b4
b5</td><td>CSWOFF [2:0]</td><td>Write-access CS extension cycle select bits</td></tr><tr><td>b8
b10</td><td>WDOFF [2:0]</td><td>Write data output extension cycle select bits</td></tr><tr><td>b12
b13</td><td>AWAIT[1:0]</td><td>Address cycle wait select bits</td></tr><tr><td>b16
b18</td><td>RDON[2:0]</td><td>RD assert wait select bits</td></tr><tr><td>b20
b22</td><td>WRON[2:0]</td><td>WR assert wait select bits</td></tr><tr><td>b24
b26</td><td>WDON[2:0]</td><td>Write data output wait select bits</td></tr><tr><td>b28
b30</td><td>CSON[2:0]</td><td>CS assert wait select bits</td></tr></table></td></tr>
<tr><td>—</td><td>• Bus priority control register (BUSPRI)</td></tr>
<tr><td rowspan="5">DMA controller</td><td rowspan="5">Registers/ bits</td><td>• DMA control register A (DMCRA)<table><tr><td>Block transfer mode</td><td>Transfer count</td><td>1 to 1023</td></tr></table>• 000h setting prohibited</td><td>• DMA control register A (DMCRA)<table><tr><td>Block transfer mode</td><td>Transfer count</td><td>1 to 1024</td></tr></table>• No limitations</td></tr>
<tr><td>• DMA control register B (DMCRB)
• Set to 3FFh for normal transfer mode.</td><td>• DMA control register B (DMCRB)
• The DMCRB register is not used in normal transfer mode. The set value is invalid.</td></tr>
<tr><td>• Transfer source address extension repeat area overflow interrupt enable bit (DMINT/SARIE)
• None listed</td><td>• Transfer source address extension repeat area overflow interrupt enable bit (DMINT/SARIE)
• When the DMACm.DMCNT.DTE bit for the channel whose transfer was completed by an interrupt is set to 1, it becomes possible to start the transfer again from the transfer complete state.</td></tr>
<tr><td>• DMACA module activation register (DMAST)
• To perform DMA transfers, the application should set the DMST bit to 1 and then set the DMCNT.DTE bit for each channel used to 1.</td><td>• DMACA module activation register (DMAST)
• It is possible to set multiple channels to the transfer request acceptance enabled state by setting the DMST bit is set to 1 after the DMACm.DMCNT.DTE bits for multiple channels have been set to 1 (DMAC start enabled).
Also, if the DMST bit is set to 0 during DMAC operation, DMA operation will be temporarily stopped after the data transfer for the one transfer request that is executing has completed. In this state, it is possible to perform DMA transfers consecutively by setting the DMST bit to 1 again.</td></tr>
<tr><td colspan="2"></td></tr>
<tr><td rowspan="5">EXDMA controller</td><td rowspan="5">Registers/ bits</td><td>• EXDMA transfer count register (EDMCRA)<table><tr><td>Repeated transfer mode</td><td>Transfer count</td><td>1 to 1023</td></tr><tr><td>Block transfer mode</td><td>Transfer count</td><td>1 to 1023</td></tr><tr><td>Cluster transfer mode</td><td>Cluster size</td><td>1 to 7</td></tr></table>• 000h setting prohibited</td><td>• EXDMA transfer count register (EDMCRA)<table><tr><td>Repeated transfer mode</td><td>Transfer count</td><td>1 to 1024</td><td>1024</td></tr><tr><td>Block transfer mode</td><td>Transfer count</td><td>1 to 1024</td><td>1024</td></tr><tr><td>Cluster transfer mode</td><td>Cluster size</td><td>1 to 8</td><td>1024</td></tr></table>• No limitations</td></tr>
<tr><td>• EXDMA block transfer count register (EDMCRB)
• Set to 3FFh for normal transfer mode.</td><td>• EXDMA block transfer count register (EDMCRB)
• The EDMCRB register is not used in normal transfer mode. The set value is invalid.</td></tr>
<tr><td>• Transfer request selection bits (EDMTMD.DCTG[1:0])
• 11b: DMA transfer request from a peripheral module (MTU1 compare match)</td><td>• Transfer request selection bits (EDMTMD.DCTG[1:0])
• 11b: DMA transfer request from a peripheral module (MTU1 or TPU7 compare match)</td></tr>
<tr><td>• EXDAM output settings register (EDMOMD)<table><tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b1</td><td>DACKW</td><td>EDCAKn pin negate wait bit</td></tr><tr><td>b2</td><td>DACKE</td><td>EDACKn pin output enable bit</td></tr><tr><td>b3</td><td>DACKS</td><td>EDACKn pin polarity setting bit</td></tr></table></td><td>• EXDAM output settings register (EDMOMD)<table><tr><td>b0</td><td>DACKSEL</td><td>EDACKn pin toggle selection bit</td></tr><tr><td>b1</td><td>DACKW</td><td>EDACKn pin negate wait bit</td></tr><tr><td>b2</td><td>DACKE</td><td>EDACKn pin output enable bit</td></tr><tr><td>b3</td><td>DACKS</td><td>EDACKn pin polarity setting bit</td></tr></table></td></tr>
</table>

Table 2.16 Differences in Functions and Specifications (16)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="4">DTC controller</td><td rowspan="4">Registers/ bits</td><td>• DTC transfer count register A (CRA)
<table><tr><td>Block transfer mode</td><td>Transfer count</td><td>1 to 255</td></tr></table>• 00h setting prohibited</td><td>• DTC transfer count register A (CRA)
<table><tr><td>Block transfer mode</td><td>Transfer count</td><td>1 to 256</td></tr></table>• No limitations.</td></tr>
<tr><td>• DTC transfer count register B (CRB)
• This register must be set to FFFFh in normal transfer mode and in repeat transfer mode.</td><td>• DTC transfer count register B (CRB)
• The CRB register is not used in normal transfer mode and in repeat transfer mode. The set value is invalid.</td></tr>
<tr><td>• 16.3 Sources of Activation
• None listed</td><td>• 20.3 Sources of Activation
• Once the DTC acknowledges a startup request, (omitted) the highest priority request is acknowledged.</td></tr>
<tr><td>• The setting from section 16.9.3, Interrupt controller DTC startup enable register (ICU.DTCERi)
• The DTC startup enable registers (ICU.DTCERi registers, where i = interrupt vector number) may only be set when the DTCST.DTCST bit is 0 (DTC module stopped).</td><td>• The setting from section 20.9.3, Interrupt controller DTC startup enable register (ICU.DTCERn)
• None listed</td></tr>
<tr><td rowspan="4">I/O port</td><td rowspan="3">Functions</td><td>—</td><td>• Overview
• The 64-pin and 48-pin products each provide port switching register A (PSRA) and port switching register B (PRSB), which allow PORTC to be used as an 8-bit port by switching the general-purpose I/O functions of certain pins.</td></tr>
<tr><td>• Handling of unused pins
<table><tr><td>Pin Name</td><td>Handling</td></tr><tr><td>Ports 0 to 9
Ports A to E</td><td>• Each such pin must be connected through a resistor to either VCC (pulled up) or VSS (pulled down).
• Pins may also be left open in the state where the corresponding PORTn.ICR register is set to its initial value (input buffer disabled).*1</td></tr></table>Note: 1. Do not change the corresponding PORTn.ICR register from its initial value. Through currents may flow if the register's value is changed.</td><td>• Handling of unused pins
<table><tr><td>Pin Name</td><td>Handling</td></tr><tr><td>Ports 0 to 9
Ports A to G
Port J</td><td>• Each such pin must be set to input (the corresponding PORTn.PDR bit set to 0) and must be connected through a resistor to either VCC (pulled up) or VSS (pulled down).*1
• Pins may also be set to output (the corresponding PORTn.PDR bit set to 1) and left open.*1*2</td></tr></table>Notes: 1. Set the corresponding PORTn.PMR bit to 0 and set the corresponding PmnPFS.ISEL and ASEL bits to 0.
2. When an unused pin is set to output and left open, the port will be in the input state from the point when a reset is cleared until the port goes to the input state. As a result the pin voltage level will be unstable during the period it is in the input state and power supply current drain may increase during this period.</td></tr>
<tr><td>—</td><td>• Notes on products with less than 176 pins
In products with less than 176 pins, the port direction register (PDR) bits for port m pins that do not exist for the 176 pins are reserved bits. The value 1 (output) must be written to these bits.</td></tr>
<tr><td rowspan="8">Registers/ bits</td><td>• Data direction register (DDR)</td><td>• Port direction register (PDR)</td></tr>
<tr><td>• Data register (DR)</td><td>• Port output data register (PODR)</td></tr>
<tr><td>• Port register (PORT)</td><td>• Port input data register (PIDR)</td></tr>
<tr><td>• Input buffer control register (ICR)</td><td>• Port mode register (PMR)</td></tr>
<tr><td>• Open drain control register (ODR)
<table><tr><td>b0</td><td>B0</td><td>Pn0 output type select bit</td></tr><tr><td>b1</td><td>B1</td><td>Pn1 output type select bit</td></tr><tr><td>b2</td><td>B2</td><td>Pn2 output type select bit</td></tr><tr><td>b3</td><td>B3</td><td>Pn3 output type select bit</td></tr><tr><td>b4</td><td>B4</td><td>Pn4 output type select bit</td></tr><tr><td>b5</td><td>B5</td><td>Pn5 output type select bit</td></tr><tr><td>b6</td><td>B6</td><td>Pn6 output type select bit</td></tr><tr><td>b7</td><td>B7</td><td>Pn7 output type select bit</td></tr></table></td><td>• Open drain control register 0 (ODR0)
<table><tr><td>b0</td><td>B0</td><td>Pm0 output type select bit</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2</td><td>B2</td><td>Pm1 output type select bit</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>B4</td><td>Pm2 output type select bit</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>B6</td><td>Pm3 output type select bit</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr></table>• Open drain control register 1 (ODR1)
<table><tr><td>b0</td><td>B0</td><td>Pm4 output type select bit</td></tr><tr><td>b2</td><td>B2</td><td>Pm5 output type select bit</td></tr><tr><td>b4</td><td>B4</td><td>Pm6 output type select bit</td></tr><tr><td>b6</td><td>B6</td><td>Pm7 output type select bit</td></tr></table></td></tr>
<tr><td>• Pull-up resistor control register (PCR)</td><td>• Pull-up control register (PCR)</td></tr>
<tr><td>—</td><td>• Driving ability control register (DSCR)</td></tr>
<tr><td>—</td><td>• Port switching register A (PSRA)</td></tr>
<tr><td>—</td><td>• Port switching register B (PSRB)</td></tr>
</table>

Table 2.17 Differences in Functions and Specifications (17)

Item		RX62N Group	RX63N Group
I/O port	Registers/ bits	• Port function control register 0 (PF0CSE) • Port function control register 1 (PF1CSS) • Port function control register 2 (PF2CSS) • Port function control register 3 (PF3BUS) • Port function control register 4 (PF4BUS) • Port function control register 5 (PF5BUS) • Port function control register 6 (PF6BUS) • Port function control register 7 (PF7DMA) • Port function control register 8 (PF8IRQ) • Port function control register 9 (PF9IRQ) • Port function control register A (PFAADC) • Port function control register B (PFBTMR) • Port function control register C (PFCMTU) • Port function control register D (PFDMTU) • Port function control register E (PFENET) • Port function control register F (PFFSCI) • Port function control register G (PFGSPI) • Port function control register H (PFHSPI) • Port function control register J (PFJCAN) • Port function control register K (PFKUSB) • Port function control register L (PFLUSB) • Port function control register M (PFMPOE) • Port function control register N (PFNPOE)	—
Multi-function pin controller	Registers/ bits	—	• Write-protect register (PWPR) • P0n pin function control register (P0nPFS) • P1n pin function control register (P1nPFS) • P2n pin function control register (P2nPFS) • P3n pin function control register (P3nPFS) • P4n pin function control register (P4nPFS) • P5n pin function control register (P5nPFS) • P6n pin function control register (P6nPFS) • P7n pin function control register (P7nPFS) • P8n pin function control register (P8nPFS) • P9n pin function control register (P9nPFS) • PAn pin function control register (PAnPFS) • PBn pin function control register (PBnPFS) • PCn pin function control register (PCnPFS) • PDn pin function control register (PDnPFS) • PEn pin function control register (PEnPFS) • PFn pin function control register (PFnPFS) • PJ3 pin function control register (PJ3PFS) • CS output enable register (PFCSE) • CS output pin select register 0 (PFCSS0) • CS output pin select register 1 (PFCSS1) • Address output enable register 0 (PFAOE0) • Address output enable register 1 (PFAOE1) • External bus control register 0 (PFBCR0) • External bus control register 1 (PFBCR1) • Ethernet control register (PFENET) • USB0 control register (PFUSB0) • USB1 control register (PFUSB1)

Table 2.18 Differences in Functions and Specifications (18)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="3">Multi-function timer pulse unit 2</td><td>Units</td><td>• Two units [MTU0 to MTU5, MTU6 to MTU11]</td><td>• One unit [MTU0 to MTU5]</td></tr>
<tr><td>Registers/ bits</td><td>—</td><td>• Noise filter control register (NFCR)</td></tr>
<tr><td>Functions</td><td></td><td>• Usage Notes<table><tr><td>Usage notes</td><td>Notes on MTU5.TCNT and MTU5.TGR
Interrupt signals due to compare match events are output continuously.</td></tr></table></td></tr>
<tr><td rowspan="11">Port output enable 2</td><td rowspan="11">Registers/ bits</td><td>• Input level control/status register 2 (ICSR2)
• Output level control/status register 2 (OCSR2)</td><td>—</td></tr>
<tr><td>• Input level control/status register 3 (ICSR3)<table><tr><td>b0
b1</td><td>POE8M [1:0]</td><td>POE8 mode select bits</td></tr><tr><td>b8</td><td>PIE3</td><td>Port interrupt enable 3 bit</td></tr><tr><td>b9</td><td>POE8E</td><td>POE8 high-impedance enable bit</td></tr><tr><td>b12</td><td>POE8F</td><td>POE8 flag</td></tr></table></td><td>• Input level control/status register 2 (ICSR2)<table><tr><td>b0
b1</td><td>POE8M [1:0]</td><td>POE8 mode select bits</td></tr><tr><td>b8</td><td>PIE2</td><td>Port interrupt enable 2 bit</td></tr><tr><td>b9</td><td>POE8E</td><td>POE8 high-impedance enable bit</td></tr><tr><td>b12</td><td>POE8F</td><td>POE8 flag</td></tr></table></td></tr>
<tr><td>• Input level control/status register 4 (ICSR4)</td><td>—</td></tr>
<tr><td>• Software port output enable register (SPOER)<table><tr><td>b0</td><td>CH34HIZ</td><td>MTU3 and MTU4 output high-impedance enable bit</td></tr><tr><td>b1</td><td>CH0HIZ</td><td>MTU0 output high-impedance enable bit</td></tr><tr><td>b2</td><td>CH910HIZ</td><td>MTU9 and MTU10 output high-impedance enable bit</td></tr><tr><td>b3</td><td>CH6HIZ</td><td>MTU6 output high-impedance enable bit</td></tr></table></td><td>• Software port output enable register (SPOER)<table><tr><td>b0</td><td>CH34HIZ</td><td>MTU3 and MTU4 output high-impedance enable bit</td></tr><tr><td>b1</td><td>CH0HIZ</td><td>MTU0 output high-impedance enable bit</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr></table></td></tr>
<tr><td>• Port output enable control register 1 (POECR1)<table><tr><td>b0</td><td>PE0ZE</td><td>MTIOC0A high-impedance enable bit</td></tr><tr><td>b1</td><td>PE1ZE</td><td>MTIOC0B high-impedance enable bit</td></tr><tr><td>b2</td><td>PE2ZE</td><td>MTIOC0C high-impedance enable bit</td></tr><tr><td>b3</td><td>PE3ZE</td><td>MTIOC0D high-impedance enable bit</td></tr><tr><td>b4</td><td>PE4ZE</td><td>MTIOC6A high-impedance enable bit</td></tr><tr><td>b5</td><td>PE5ZE</td><td>MTIOC6B high-impedance enable bit</td></tr><tr><td>b6</td><td>PE6ZE</td><td>MTIOC6C high-impedance enable bit</td></tr><tr><td>b7</td><td>PE7ZE</td><td>MTIOC6D high-impedance enable bit</td></tr></table></td><td>• Port output enable control register 1 (POECR1)<table><tr><td>b0</td><td>PE0ZE</td><td>MTIOC0A high-impedance enable bit</td></tr><tr><td>b1</td><td>PE1ZE</td><td>MTIOC0B high-impedance enable bit</td></tr><tr><td>b2</td><td>PE2ZE</td><td>MTIOC0C high-impedance enable bit</td></tr><tr><td>b3</td><td>PE3ZE</td><td>MTIOC0D high-impedance enable bit</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr></table></td></tr>
<tr><td>• Port output enable control register 2 (POECR2)<table><tr><td>b4</td><td>P6CZE</td><td>MTU port 6 high-impedance enable bit</td></tr><tr><td>b5</td><td>P5CZE</td><td>MTU port 5 high-impedance enable bit</td></tr><tr><td>b6</td><td>P4CZE</td><td>MTU port 4 high-impedance enable bit</td></tr><tr><td>b8</td><td>P3CZEB</td><td>MTU port 3 high-impedance enable B bit</td></tr><tr><td>b9</td><td>P2CZEB</td><td>MTU port 2 high-impedance enable B bit</td></tr><tr><td>b10</td><td>P1CZEB</td><td>MTU port 1 high-impedance enable B bit</td></tr><tr><td>b12</td><td>P3CZEA</td><td>MTU port 3 high-impedance enable A bit</td></tr><tr><td>b13</td><td>P2CZEA</td><td>MTU port 2 high-impedance enable A bit</td></tr><tr><td>b14</td><td>P1CZEA</td><td>MTU port 1 high-impedance enable A bit</td></tr></table></td><td>• Port output enable control register 2 (POECR2)<table><tr><td>b4</td><td>P3CZEA</td><td>MTU port 3 high-impedance enable bit</td></tr><tr><td>b5</td><td>P2CZEA</td><td>MTU port 2 high-impedance enable bit</td></tr><tr><td>b6</td><td>P1CZEA</td><td>MTU port 1 high-impedance enable bit</td></tr></table></td></tr>
<tr><td>—</td><td>• Input level control/status register 3 (ICSR3)</td></tr>
</table>

Table 2.19 Differences in Functions and Specifications (19)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td>16-bit timer pulse unit</td><td>Registers/ bits</td><td>—</td><td>• Timer control register (TCR)
• Timer mode register (TMDR)
• Timer I/O control registers (TIORH, TIORL, TIOR)
• Timer interrupt enable register (TIER)
• Timer status register (TSR)
• Timer counter (TCNT)
• Timer general registers A to D (TGRA to TGRD)
• Timer start register (TSTR)
• Timer synchronous register (TSYR)
• Noise filter control register (NFCR)</td></tr>
<tr><td rowspan="3">Programmable pulse generator</td><td rowspan="3">Registers/ bits</td><td>• PPG trigger select register (PTRSLR)
b0 PTRSL PPG trigger select bit
• PTRSL
0: The PPG1 trigger is selected for MTU0 to MTU3
1: The PPG1 trigger is selected for MTU6 to MTU9</td><td>• PPG trigger select register (PTRSLR)
b0 PTRSL PPG trigger select bit
• PTRSL
0: The PPG1 trigger is selected for MTU0 to MTU3
1: The PPG1 trigger is selected for TPU0 to TPU3</td></tr>
<tr><td>• PPG output control register (PCR)
b0 b1 G0CMS [1:0] Group 4 compare match selection bits
b2 b3 G1CMS [1:0] Group 5 compare match selection bits
b4 b5 G2CMS [1:0] Group 6 compare match selection bits
b6 b7 G3CMS [1:0] Group 7 compare match selection bits
• PPG1.PCR.G0CMS[1:0] to G3CMS[1:0]
Value of PTRSL bit in PPG1.PTRSLR is 0.
00b: Compare match in MTU6
01b: Compare match in MTU7
10b: Compare match in MTU8
11b: Compare match in MTU9</td><td>• PPG output control register (PCR)
b0 b1 G0CMS [1:0] Group 4 compare match selection bits
b2 b3 G1CMS [1:0] Group 5 compare match selection bits
b4 b5 G2CMS [1:0] Group 6 compare match selection bits
b6 b7 G3CMS [1:0] Group 7 compare match selection bits
• PPG1.PCR.G0CMS[1:0] to G3CMS[1:0]
Value of PTRSL bit in PPG1.PTRSLR is 0.
00b: Compare match in TPU0
01b: Compare match in TPU1
10b: Compare match in TPU2
11b: Compare match in TPU3</td></tr>
<tr><td>• PPG output mode register (PMR)
b0 G0NOV Group 4 non-overlap bit
b1 G1NOV Group 5 non-overlap bit
b2 G2NOV Group 6 non-overlap bit
b3 G3NOV Group 7 non-overlap bit
b4 G0INV Group 4 output polarity inversion bit
b5 G1INV Group 5 output polarity inversion bit
b6 G2INV Group 6 output polarity inversion bit
b7 G3INV Group 7 output polarity inversion bit
• PPG1.PMR.G0NOV to G3NOV
0: Normal operation
(Output values updated on compare match A in the selected MTUn)
1: Non-overlapping operation
(Output values updated on compare match A or B in the selected MTUn)</td><td>• PPG output mode register (PMR)
b0 G0NOV Group 4 non-overlap bit
b1 G1NOV Group 5 non-overlap bit
b2 G2NOV Group 6 non-overlap bit
b3 G3NOV Group 7 non-overlap bit
b4 G0INV Group 4 output polarity inversion bit
b5 G1INV Group 5 output polarity inversion bit
b6 G2INV Group 6 output polarity inversion bit
b7 G3INV Group 7 output polarity inversion bit
• PPG1.PMR.G0NOV to G3NOV
Value of PTRSL bit in PPG1.PTRSLR is 1.
0: Normal operation
(Output values updated on compare match A in the selected TPUn)
1: Non-overlapping operation
(Output values updated on compare match A or B in the selected TPUn)</td></tr>
</table>

Table 2.20 Differences in Functions and Specifications (20)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="2">Realtime clock</td><td>Functions</td><td>• Specification overview
<table>
<tr><td>Count source</td><td>Dedicated RTC clock (32.768 kHz)</td></tr>
<tr><td></td><td>—</td></tr>
<tr><td>Clock/calendar function</td><td>Counts the year, month, day, day of week, hour, minute, and seconds and displays them in BCD.</td></tr>
<tr><td></td><td>Displays the 1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, and 64 Hz states in binary.</td></tr>
<tr><td></td><td>—</td></tr>
<tr><td></td><td>Start/stop function</td></tr>
<tr><td></td><td>30-second adjustment function</td></tr>
<tr><td></td><td>Automatic leap year correction function</td></tr>
<tr><td></td><td>1 HZ clock output</td></tr>
<tr><td></td><td>—</td></tr>
<tr><td>Interrupts</td><td>Alarm interrupt (ALM)</td></tr>
<tr><td></td><td>Periodic interrupt (PRD)</td></tr>
<tr><td></td><td>Carry interrupt (CUP)</td></tr>
<tr><td></td><td>Software standby mode and deep software standby mode can be cleared by an alarm.</td></tr>
<tr><td>—</td><td>—</td></tr>
</table></td><td>• Specification overview
<table>
<tr><td>Count source*1</td><td>Dedicated RTC clock (32.768 kHz)</td></tr>
<tr><td></td><td>Main clock (EXTAL)</td></tr>
<tr><td>Clock/calendar function</td><td>Counts the year, month, day, day of week, hour, minute, and seconds and displays them in BCD.</td></tr>
<tr><td></td><td>Displays the 1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, and 64 Hz states in binary.</td></tr>
<tr><td></td><td>12/24 hour mode switching function</td></tr>
<tr><td></td><td>Start/stop function</td></tr>
<tr><td></td><td>30-second adjustment function</td></tr>
<tr><td></td><td>Automatic leap year correction function</td></tr>
<tr><td></td><td>1 HZ clock output</td></tr>
<tr><td></td><td>Clock error correction function</td></tr>
<tr><td>Interrupts</td><td>Alarm interrupt (ALM)</td></tr>
<tr><td></td><td>Periodic interrupt (PRD)</td></tr>
<tr><td></td><td>Carry interrupt (CUP)</td></tr>
<tr><td></td><td>Software standby mode and deep software standby mode can be cleared by an alarm or periodic interrupt.</td></tr>
<tr><td>Time capture function</td><td>The time can be captured by three event inputs.</td></tr>
</table>
Note: 1. The count source must be set so that (peripheral module clock frequency) ≥ (count source clock frequency).</td></tr>
<tr><td>Registers/ bits</td><td>• Hour counter (RHRCNT)
<table>
<tr><td>b0 b3</td><td>HOUR1 [3:0]</td><td>Hour ones position count bits</td></tr>
<tr><td>b4 b5</td><td>HOUR10 [1:0]</td><td>Hour tens position count bits</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
</table>
• Day-of-week counter (RWKCNT)
<table>
<tr><td>b0 b2</td><td>DAY[2:0]</td><td>Day of the week count bits</td></tr>
</table>
• Date counter (RDAYCNT)
<table>
<tr><td>b0 b3</td><td>DAY1[3:0]</td><td>Day ones position count bits</td></tr>
<tr><td>b5 b4</td><td>DAY10[1:0]</td><td>Day tens position count bits</td></tr>
</table>
• Year counter (RYRCNT)
<table>
<tr><td>b0 b3</td><td>YEAR1 [3:0]</td><td>Year ones position count bits</td></tr>
<tr><td>b4 b7</td><td>YEAR10 [3:0]</td><td>Year tens position count bits</td></tr>
<tr><td>b8 b11</td><td>YEAR100 [3:0]</td><td>Year one-hundred position count bits</td></tr>
<tr><td>b12 b15</td><td>YEAR1000 [3:0]</td><td>Year one-thousand position count bits</td></tr>
</table>
• Hour alarm register (RHRAR)
<table>
<tr><td>b0 b3</td><td>HOUR1 [3:0]</td><td>One-hour bits</td></tr>
<tr><td>b4 b5</td><td>HOUR10 [1:0]</td><td>Ten-hour bits</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>ENB</td><td>ENB bit</td></tr>
</table>
• Day-of-week alarm register (RWKAR)
<table>
<tr><td>b0 b2</td><td>DAY[2:0]</td><td>Day of the week setting value bits</td></tr>
<tr><td>b7</td><td>ENB</td><td>ENB bit</td></tr>
</table>
• Date alarm register (RDAYAR)
<table>
<tr><td>b0 b3</td><td>DAY1[3:0]</td><td>One-day bits</td></tr>
<tr><td>b4 b5</td><td>DAY10[1:0]</td><td>Ten-day bits</td></tr>
<tr><td>b7</td><td>ENB</td><td>ENB bit</td></tr>
</table></td><td>• Hour counter (RHRCNT)
<table>
<tr><td>b0 b3</td><td>HR1[3:0]</td><td>Hour ones position count bits</td></tr>
<tr><td>b4 b5</td><td>HR10[1:0]</td><td>Hour tens position count bits</td></tr>
<tr><td>b6</td><td>PM</td><td>PM bit</td></tr>
</table>
• Day-of-week counter (RWKCNT)
<table>
<tr><td>b0 b2</td><td>DAYW[2:0]</td><td>Day of the week count bits</td></tr>
</table>
• Date counter (RDAYCNT)
<table>
<tr><td>b0 b3</td><td>DATE1[3:0]</td><td>Day ones position count bits</td></tr>
<tr><td>b5 b4</td><td>DATE10 [1:0]</td><td>Day tens position count bits</td></tr>
</table>
• Year counter (RYRCNT)
<table>
<tr><td>b0 b3</td><td>YR1[3:0]</td><td>Year ones position count bits</td></tr>
<tr><td>b4 b7</td><td>YR10[3:0]</td><td>Year tens position count bits</td></tr>
<tr><td>b8 b11</td><td>—</td><td>(Reserved bits)</td></tr>
<tr><td>b12 b15</td><td>—</td><td>(Reserved bits)</td></tr>
</table>
• Hour alarm register (RHRAR)
<table>
<tr><td>b0 b3</td><td>HR1[3:0]</td><td>One-hour bits</td></tr>
<tr><td>b4 b5</td><td>HR10[1:0]</td><td>Ten-hour bits</td></tr>
<tr><td>b6</td><td>PM</td><td>PM bit</td></tr>
<tr><td>b7</td><td>ENB</td><td>ENB bit</td></tr>
</table>
• Day-of-week alarm register (RWKAR)
<table>
<tr><td>b0 b2</td><td>DAYW[2:0]</td><td>Day of the week setting value bits</td></tr>
<tr><td>b7</td><td>ENB</td><td>ENB bit</td></tr>
</table>
• Date alarm register (RDAYAR)
<table>
<tr><td>b0 b3</td><td>DATE1[3:0]</td><td>One-day bits</td></tr>
<tr><td>b4 b5</td><td>DATE10 [1:0]</td><td>Ten-day bits</td></tr>
<tr><td>b7</td><td>ENB</td><td>ENB bit</td></tr>
</table></td></tr>
</table>

Table 2.21 Differences in Functions and Specifications (21)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="5">Realtime clock</td><td rowspan="5">Registers/ bits</td><td>• Year alarm register (RYRAR)
<table><tr><td>b0
b3</td><td>YEAR1
[3:0]</td><td>One-year bits</td></tr><tr><td>b4
b7</td><td>YEAR10
[3:0]</td><td>Ten-year bits</td></tr><tr><td>b8
b11</td><td>YEAR100
[3:0]</td><td>One-hundred-year bits</td></tr><tr><td>b12
b15</td><td>YEAR1000
[3:0]</td><td>One-thousand-year bits</td></tr></table></td><td>• Year alarm register (RYRAR)
<table><tr><td>b0
b3</td><td>YR1[3:0]</td><td>One-year bits</td></tr><tr><td>b4
b7</td><td>YR10[3:0]</td><td>Ten-year bits</td></tr><tr><td>b8
b11</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b12
b15</td><td>—</td><td>(Reserved bits)</td></tr></table></td></tr>
<tr><td>• RTC control register 1 (RCR1)
<table><tr><td>b0</td><td>AIE</td><td>Alarm interrupt enable bit</td></tr><tr><td>b1</td><td>CIE</td><td>Carry interrupt enable bit</td></tr><tr><td>b2</td><td>PIE</td><td>Periodic interrupt enable bit</td></tr><tr><td>b4
b6</td><td>PES[2:0]</td><td>Periodic interrupt selection bits</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr></table>• PES[2:0]
000b: Periodic interrupt not generated
001b: Periodic interrupt set to 1/256 of a second
010b: Periodic interrupt set to 1/64 of a second
011b: Periodic interrupt set to 1/16 of a second
100b: Periodic interrupt set to 1/4 of a second
101b: Periodic interrupt set to 1/2 of a second
110b: Periodic interrupt set to 1 of a second
111b: Periodic interrupt set to 2 of a seconds</td><td>• RTC control register 1 (RCR1)
<table><tr><td>b0</td><td>AIE</td><td>Alarm interrupt enable bit</td></tr><tr><td>b1</td><td>CIE</td><td>Carry interrupt enable bit</td></tr><tr><td>b2</td><td>PIE</td><td>Periodic interrupt enable bit</td></tr><tr><td>b4

b7</td><td>PES[3:0]</td><td>Periodic interrupt selection bits</td></tr></table>• PES[3:0]
0000b: Periodic interrupt not generated
0001b: Periodic interrupt not generated
0010b: Periodic interrupt not generated
0011b: Periodic interrupt not generated
0100b: Periodic interrupt not generated
0101b: Periodic interrupt not generated
0110b: Periodic interrupt set to 1/256 of a second
0111b: Periodic interrupt set to 1/128 of a second
1000b: Periodic interrupt set to 1/64 of a second
1001b: Periodic interrupt set to 1/32 of a second
1010b: Periodic interrupt set to 1/16 of a second
1011b: Periodic interrupt set to 1/8 of a second
1100b: Periodic interrupt set to 1/4 of a second
1101b: Periodic interrupt set to 1/2 of a second
1110b: Periodic interrupt set to 1 of a second
1111b: Periodic interrupt set to 2 of a seconds</td></tr>
<tr><td>• RTC control register 2 (RCR2)
<table><tr><td>b0</td><td>START</td><td>Start bit</td></tr><tr><td>b1</td><td>RESET</td><td>Reset bit</td></tr><tr><td>b2</td><td>ADJ</td><td>30 second adjustment bit</td></tr><tr><td>b3</td><td>RTCOE</td><td>RTCOUT output control bit</td></tr><tr><td>b4</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• RTC control register 2 (RCR2)
<table><tr><td>b0</td><td>START</td><td>Start bit</td></tr><tr><td>b1</td><td>RESET</td><td>RTC software reset bit</td></tr><tr><td>b2</td><td>ADJ30</td><td>30 second adjustment bit</td></tr><tr><td>b3</td><td>RTCOE</td><td>RTCOUT output enable bit</td></tr><tr><td>b4</td><td>AADJE</td><td>Automatic correction function enable bit</td></tr><tr><td>b5</td><td>AADJP</td><td>Automatic correction period selection bit</td></tr><tr><td>b6</td><td>HR24</td><td>Time mode bit</td></tr></table></td></tr>
<tr><td>—</td><td>• RTC control register 3 (RCR3)
• RTC control register 4 (RCR4)
• Frequency register H/L (RFRH/L)
• Time error adjustment register (RADJ)
• Time capture control registers 0 to 2 (RTCCR0 to 2)
• Second capture registers 0 to 2 (RSECCP0 to 2)
• Minute capture registers 0 to 2 (RMINCP0 to 2)
• Hour capture registers 0 to 2 (RHRCP0 to 2)
• Date capture registers 0 to 2 (RDAYCP0 to 2)
• Month capture registers 0 to 2 (RMONCP0 to 2)</td></tr>
<tr><td>Watchdog timer</td><td>Functions</td><td>• Specification overview
<table><tr><td>Counter clock</td><td>PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192, PCLK/32768, PCLK/131072</td></tr><tr><td>Number of bits</td><td>8</td></tr><tr><td>Operating modes</td><td>Watchdog timer mode
Interval timer mode</td></tr><tr><td>Operation start mode</td><td>—
Register start mode</td></tr><tr><td>—</td><td>—</td></tr><tr><td>Output signals</td><td>WDTOVF# signal output (external)
Reset signal (internal)
Interval timer interrupt (WOVI)</td></tr></table></td><td>• Specification overview
<table><tr><td>Counter clock</td><td>PCLK/4, PCLK/64, PCLK/128, PCLK/512, PCLK/2048, PCLK/8192</td></tr><tr><td>Number of bits</td><td>14</td></tr><tr><td>Operating modes</td><td>Watchdog timer mode
—</td></tr><tr><td>Operation start mode</td><td>Auto-start mode
Register start mode</td></tr><tr><td>Window function</td><td>Support for setting window start and end positions</td></tr><tr><td>Output signals</td><td>—
Reset signal (internal)
Interrupt request signal (WUNI)</td></tr></table></td></tr>
</table>

Table 2.22 Differences in Functions and Specifications (22)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="2">Watchdog timer</td><td rowspan="2">Registers/ bits</td><td>• Timer counter (TCNT)
• Timer control/status register (TCSR)
• Reset control/status register (RSTCSR)
• Write window A register (WINA)
• Write window B register (WINB)</td><td>—</td></tr>
<tr><td>—</td><td>• WDT refresh register (WDTRR)
• WDT control register (WDTCR)
• WDT status register (WDTSR)
• WDT reset control register (WDTRCR)</td></tr>
<tr><td rowspan="4">Independent watchdog timer</td><td>Functions</td><td>• Specification overview
<table>
<tr><td>Counter clock</td><td>IWDTCLK, IWDTCLK/16, IWDTCLK/32, IWDTCLK/64, IWDTCLK/128, IWDTCLK/256</td></tr>
<tr><td>Number of bits</td><td>14</td></tr>
<tr><td>Operating mode</td><td>—</td></tr>
<tr><td></td><td>Register start mode</td></tr>
<tr><td>—</td><td>—</td></tr>
<tr><td>Reset sources</td><td>When an underflow occurs</td></tr>
<tr><td></td><td>—</td></tr>
</table></td><td>• Specification overview
<table>
<tr><td>Clock division ratio *1</td><td>Divide by 1, 16, 32, 64, 128, or 256</td></tr>
<tr><td>Number of bits</td><td>14</td></tr>
<tr><td>Operating mode</td><td>Auto-start mode</td></tr>
<tr><td></td><td>Register start mode</td></tr>
<tr><td>Window function</td><td>Support for setting window start and end positions</td></tr>
<tr><td>Reset sources</td><td>When an underflow occurs</td></tr>
<tr><td></td><td>When a refresh error occurs</td></tr>
</table>
Note: 1. This value must be set so that (peripheral module clock frequency ≥ 4 × (post-division count source frequency).</td></tr>
<tr><td>Registers/ bits</td><td>• IWDT control register (IWDTCR)
<table>
<tr><td>b0
b1</td><td>TOPS[1:0]</td><td>Time-out selection bits</td></tr>
<tr><td>b4
b7</td><td>CKS[3:0]</td><td>Clock selection bits</td></tr>
<tr><td>b8
b9</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b12
b13</td><td>—</td><td>(Reserved bit)</td></tr>
</table>
• CKS[3:0]
00--b: IWDTCLK
0100b: IWDTCLK/16
0101b: IWDTCLK/32
0110b: IWDTCLK/64
0111b: IWDTCLK/128
1---b: IWDTCLK/256
• IWDT status register (IWDTSR)
<table>
<tr><td>b0
b13</td><td>CNTVAL [13:0]</td><td>Down-counter value bits</td></tr>
<tr><td>b14</td><td>UNDFF</td><td>Underflow flag</td></tr>
<tr><td>b15</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td><td>• IWDT control register (IWDTCR)
<table>
<tr><td>b0
b1</td><td>TOPS[1:0]</td><td>Time-out period selection bits</td></tr>
<tr><td>b4
b7</td><td>CKS[3:0]</td><td>Clock division ratio selection bits</td></tr>
<tr><td>b8
b9</td><td>RPES[1:0]</td><td>Window end position selection bits</td></tr>
<tr><td>b12
b13</td><td>RPSS[1:0]</td><td>Window start position selection bits</td></tr>
</table>
• CKS[3:0]
0000b: IWDTCLK
0010b: IWDTCLK/16
0011b: IWDTCLK/32
0100b: IWDTCLK/64
1111b: IWDTCLK/128
0101b: IWDTCLK/256
Setting prohibited other than above
• IWDT status register (IWDTSR)
<table>
<tr><td>b0
b13</td><td>CNTVAL [13:0]</td><td>Down-counter value bits</td></tr>
<tr><td>b14</td><td>UNDFF</td><td>Underflow flag</td></tr>
<tr><td>b15</td><td>REFEF</td><td>Refresh error flag</td></tr>
</table></td></tr>
<tr><td>—</td><td>• IWDT reset control register (IWDTRCR)
• IWDT count stop control register (IWDTCSTPR)</td></tr>
<tr><td>Ethernet controller</td><td>Registers/ bits</td><td>• ETHERC mode register (ECMR)
<table>
<tr><td>b20</td><td>TPC</td><td>PAUSE frame transmission bit</td></tr>
</table>
• TPC
0: PAUSE frame not transmitted during the PAUSE period
1: PAUSE frame transmitted during the PAUSE period</td><td>• ETHERC mode register (ECMR)
<table>
<tr><td>b20</td><td>TPC</td><td>PAUSE frame transmission bit</td></tr>
</table>
• TPC
0: PAUSE frame transmitted during the PAUSE period
1: PAUSE frame not transmitted during the PAUSE period</td></tr>
<tr><td>USB2.0 host/function module</td><td>Functions</td><td>• Specification overview
<table>
<tr><td>USB0</td><td>Host controller function</td></tr>
<tr><td></td><td>Function controller function</td></tr>
<tr><td></td><td>Support for OTG (On The Go)</td></tr>
<tr><td>USB1</td><td>Host controller function</td></tr>
<tr><td></td><td>Function controller function</td></tr>
<tr><td></td><td>Support for OTG (On The Go)</td></tr>
</table></td><td>• Specification overview
<table>
<tr><td>USB0</td><td>Host controller function</td></tr>
<tr><td></td><td>Function controller function</td></tr>
<tr><td></td><td>Support for OTG (On The Go)</td></tr>
<tr><td>USB1</td><td>—</td></tr>
<tr><td></td><td>Function controller function</td></tr>
<tr><td></td><td>—</td></tr>
</table></td></tr>
</table>

Table 2.23 Differences in Functions and Specifications (23)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td>USB2.0 host/function module</td><td>Registers/ bits</td><td>
• CFIFO port register (CFIFO)
<table>
<tr><td>b0
b7</td><td>H[7:0]</td><td rowspan="2">FIFO port bits</td></tr>
<tr><td>b8
b15</td><td>L[7:0]</td></tr>
</table>
• D0FIFO port register (D0FIFO)
<table>
<tr><td>b0
b7</td><td>H[7:0]</td><td rowspan="2">FIFO port bits</td></tr>
<tr><td>b8
b15</td><td>L[7:0]</td></tr>
</table>
• D1FIFO port register (D1FIFO)
<table>
<tr><td>b0
b7</td><td>H[7:0]</td><td rowspan="2">FIFO port bits</td></tr>
<tr><td>b8
b15</td><td>L[7:0]</td></tr>
</table>
• SOF output configuration register (SOFCFG)
<table>
<tr><td>b8</td><td>TRNENSEL</td><td>Transaction enabled period switching bit</td></tr>
</table>
• TRNENSEL
0: Low speed not supported
1: Do not use this setting
• USB request value register (USBVAL)
<table>
<tr><td>b0
b15</td><td>—</td><td>—</td></tr>
</table>
• USB request index register (USBINDX)
<table>
<tr><td>b0
b15</td><td>—</td><td>—</td></tr>
</table>
• USB request length register (USBLENG)
<table>
<tr><td>b0
b15</td><td>—</td><td>—</td></tr>
</table>
• PIPEn transaction counter registers (PIPEnTRN)
<table>
<tr><td>b0
b15</td><td>—</td><td>—</td></tr>
</table>
• Device address n configuration registers (DEVADDn)
<table>
<tr><td>b6
b7</td><td>USBSPD
[1:0]</td><td>Transmission target device transfer speed bits</td></tr>
</table>
• USBSPD[1:0]
00b: DEVADDn register unused
01b: Do not use this setting
10b: Full-speed
11b: Do not use this setting
• Deep standby USB transceiver control/pin monitor register (DPUSR0R)
<table>
<tr><td>b0</td><td>SRPC0</td><td>USB0 single end receiver control</td></tr>
<tr><td>b4</td><td>FIXPHY0</td><td>USB0 transceiver output fixed</td></tr>
<tr><td>b8</td><td>SRPC1</td><td>USB1 single end receiver control</td></tr>
<tr><td>b12</td><td>FIXPHY1</td><td>USB1 transceiver output fixed</td></tr>
<tr><td>b16</td><td>DP0</td><td>USB0 DP input</td></tr>
<tr><td>b17</td><td>DM0</td><td>USB0 DM input</td></tr>
<tr><td>b20</td><td>DOVCA0</td><td>USB0 OVRCURA input</td></tr>
<tr><td>b21</td><td>DOVCB0</td><td>USB0 OVRCURB input</td></tr>
<tr><td>b23</td><td>DVBSTS0</td><td>USB0 VBUS input</td></tr>
<tr><td>b24</td><td>DP1</td><td>USB1 DP input</td></tr>
<tr><td>b25</td><td>DM1</td><td>USB1 DM input</td></tr>
<tr><td>b28</td><td>DOVCA1</td><td>USB1 OVRCURA input</td></tr>
<tr><td>b29</td><td>DOVCB1</td><td>USB1 OVRCURB input</td></tr>
<tr><td>b31</td><td>DVBSTS1</td><td>USB1 VBUS input</td></tr>
</table>
</td><td>
• CFIFO port register (CFIFO)
<table>
<tr><td>b0

b15</td><td>FIFOPORT
[15:0]</td><td>FIFO port bits</td></tr>
</table>
• D0FIFO port register (D0FIFO)
<table>
<tr><td>b0

b15</td><td>FIFOPORT
[15:0]</td><td>FIFO port bits</td></tr>
</table>
• D1FIFO port register (D1FIFO)
<table>
<tr><td>b0

b15</td><td>FIFOPORT
[15:0]</td><td>FIFO port bits</td></tr>
</table>
• SOF output configuration register (SOFCFG)
<table>
<tr><td>b8</td><td>TRNENSEL</td><td>Transaction enabled period switching bit</td></tr>
</table>
• TRNENSEL
0: Low speed not supported
1: Low speed supported
• Bit 8 in the USB1.SOFCFG register is a reserved bit.
• USB request value register (USBVAL)
<table>
<tr><td>b0
b15</td><td>WVALUE
[15:0]</td><td>Value bits</td></tr>
</table>
• USB request index register (USBINDX)
<table>
<tr><td>b0
b15</td><td>WINDEX
[15:0]</td><td>Index bits</td></tr>
</table>
• USB request length register (USBLENG)
<table>
<tr><td>b0
b15</td><td>WLENGTH
[15:0]</td><td>Length bits</td></tr>
</table>
• PIPEn transaction counter registers (PIPEnTRN)
<table>
<tr><td>b0
b15</td><td>TRNCNT
[15:0]</td><td>Transaction count bits</td></tr>
</table>
• Device address n configuration registers (DEVADDn)
<table>
<tr><td>b6
b7</td><td>USBSPD
[1:0]</td><td>Transmission target device transfer speed bits</td></tr>
</table>
• USBSPD[1:0]
00b: DEVADDn register unused
01b: Low-speed
10b: Full-speed
11b: Do not use this setting
• Deep standby USB transceiver control/pin monitor register (DPUSR0R)
<table>
<tr><td>b0</td><td>SRPC0</td><td>USB0 single end receiver control</td></tr>
<tr><td>b4</td><td>FIXPHY0</td><td>USB0 transceiver output fixed</td></tr>
<tr><td>b8</td><td>SRPC1</td><td>USB1 single end receiver control</td></tr>
<tr><td>b12</td><td>FIXPHY1</td><td>USB1 transceiver output fixed</td></tr>
<tr><td>b16</td><td>DP0</td><td>USB0 DP input</td></tr>
<tr><td>b17</td><td>DM0</td><td>USB0 DM input</td></tr>
<tr><td>b20</td><td>DOVCA0</td><td>USB0 OVRCURA input</td></tr>
<tr><td>b21</td><td>DOVCB0</td><td>USB0 OVRCURB input</td></tr>
<tr><td>b23</td><td>DVBSTS0</td><td>USB0 VBUS input</td></tr>
<tr><td>b24</td><td>DP1</td><td>USB1 DP input</td></tr>
<tr><td>b25</td><td>DM1</td><td>USB1 DM input</td></tr>
<tr><td>b28</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b29</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b31</td><td>DVBSTS1</td><td>USB1 VBUS input</td></tr>
</table>
</td></tr>
</table>

Table 2.24 Differences in Functions and Specifications (24)

<table>
<tr><th>Item</th><th></th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td>USB2.0 host/function module</td><td>Registers/ bits</td><td>• Deep standby USB suspend/resume interrupt register (DPUSR1R)
<table>
<tr><td>b0</td><td>DPINTE0</td><td>USB0 DP interrupt enable/clear bit</td></tr>
<tr><td>b1</td><td>DMINTE0</td><td>USB0 DM interrupt enable/clear bit</td></tr>
<tr><td>b4</td><td>DOVRCRAE0</td><td>USB0 OVRCURA interrupt enable/clear bit</td></tr>
<tr><td>b5</td><td>DOVRCRBE0</td><td>USB0 OVRCURB interrupt enable/clear bit</td></tr>
<tr><td>b7</td><td>DVBSE0</td><td>USB0 VBUS interrupt enable/clear bit</td></tr>
<tr><td>b8</td><td>DPINTE1</td><td>USB1 DP interrupt enable/clear bit</td></tr>
<tr><td>b9</td><td>DMINTE1</td><td>USB1 DM interrupt enable/clear bit</td></tr>
<tr><td>b12</td><td>DOVRCRAE1</td><td>USB1 OVRCURA interrupt enable/clear bit</td></tr>
<tr><td>b13</td><td>DOVRCRBE1</td><td>USB1 OVRCURB interrupt enable/clear bit</td></tr>
<tr><td>b15</td><td>DVBSE1</td><td>USB1 VBUS interrupt enable/clear bit</td></tr>
<tr><td>b16</td><td>DPINT0</td><td>Recovery due to USB0 DP interrupt factor indicator bit</td></tr>
<tr><td>b17</td><td>DMINT0</td><td>Recovery due to USB0 DM interrupt factor indicator bit</td></tr>
<tr><td>b20</td><td>OVRCURAINT0</td><td>Recovery due to USB0 OVRCURA interrupt factor indicator bit</td></tr>
<tr><td>b21</td><td>OVRCURBINT0</td><td>Recovery due to USB0 OVRCURB interrupt factor indicator bit</td></tr>
<tr><td>b23</td><td>DVBINT0</td><td>Recovery due to USB0 VBUS interrupt factor indicator bit</td></tr>
<tr><td>b24</td><td>DPINT1</td><td>Recovery due to USB1 DP interrupt factor indicator bit</td></tr>
<tr><td>b25</td><td>DMINT1</td><td>Recovery due to USB1 DM interrupt factor indicator bit</td></tr>
<tr><td>b28</td><td>DOVRCRA1</td><td>Recovery due to USB1 OVRCURA interrupt factor indicator bit</td></tr>
<tr><td>b29</td><td>DOVRCRB1</td><td>Recovery due to USB1 OVRCURB interrupt factor indicator bit</td></tr>
<tr><td>b31</td><td>DVBINT1</td><td>Recovery due to USB1 VBUS interrupt factor indicator bit</td></tr>
</table></td><td>• Deep standby USB suspend/resume interrupt register (DPUSR1R)
<table>
<tr><td>b0</td><td>DPINTE0</td><td>USB0 DP interrupt enable/clear bit</td></tr>
<tr><td>b1</td><td>DMINTE0</td><td>USB0 DM interrupt enable/clear bit</td></tr>
<tr><td>b4</td><td>DOVRCRAE0</td><td>USB0 OVRCURA interrupt enable/clear bit</td></tr>
<tr><td>b5</td><td>DOVRCRBE0</td><td>USB0 OVRCURB interrupt enable/clear bit</td></tr>
<tr><td>b7</td><td>DVBSE0</td><td>USB0 VBUS interrupt enable/clear bit</td></tr>
<tr><td>b8</td><td>DPINTE1</td><td>USB1 DP interrupt enable/clear bit</td></tr>
<tr><td>b9</td><td>DMINTE1</td><td>USB1 DM interrupt enable/clear bit</td></tr>
<tr><td>b12</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b13</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b15</td><td>DVBSE1</td><td>USB1 VBUS interrupt enable/clear bit</td></tr>
<tr><td>b16</td><td>DPINT0</td><td>Recovery due to USB0 DP interrupt factor indicator bit</td></tr>
<tr><td>b17</td><td>DMINT0</td><td>Recovery due to USB0 DM interrupt factor indicator bit</td></tr>
<tr><td>b20</td><td>DOVRCRA0</td><td>Recovery due to USB0 OVRCURA interrupt factor indicator bit</td></tr>
<tr><td>b21</td><td>DOVRCRB0</td><td>Recovery due to USB0 OVRCURB interrupt factor indicator bit</td></tr>
<tr><td>b23</td><td>DVBINT0</td><td>Recovery due to USB0 VBUS interrupt factor indicator bit</td></tr>
<tr><td>b24</td><td>DPINT1</td><td>Recovery due to USB1 DP interrupt factor indicator bit</td></tr>
<tr><td>b25</td><td>DMINT1</td><td>Recovery due to USB1 DM interrupt factor indicator bit</td></tr>
<tr><td>b28</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b29</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b31</td><td>DVBINT1</td><td>Recovery due to USB1 VBUS interrupt factor indicator bit</td></tr>
</table></td></tr>
<tr><td>Serial communications interface</td><td>Functions</td><td>• SCIa
<table>
<tr><td>Serial communication modes</td><td>Asynchronous</td></tr>
<tr><td></td><td>Clock synchronous</td></tr>
<tr><td></td><td>Smart card interface</td></tr>
<tr><td></td><td>—</td></tr>
<tr><td></td><td>—</td></tr>
<tr><td></td><td>TMR clock input</td></tr>
</table></td><td>• SCIc
<table>
<tr><td>Serial communication modes</td><td>Asynchronous</td></tr>
<tr><td></td><td>Clock synchronous</td></tr>
<tr><td></td><td>Smart card interface</td></tr>
<tr><td></td><td>Simple I2C bus (MSB-first only)</td></tr>
<tr><td></td><td>Simple SPI bus</td></tr>
<tr><td></td><td>TMR clock input</td></tr>
<tr><td>Hardware flow control</td><td>Asynchronous</td></tr>
<tr><td></td><td>Clock synchronous</td></tr>
</table>
• SCId
<table>
<tr><td>Serial communication modes</td><td>Asynchronous</td></tr>
<tr><td></td><td>Clock synchronous</td></tr>
<tr><td></td><td>Smart card interface</td></tr>
<tr><td></td><td>Simple I2C bus (MSB-first only)</td></tr>
<tr><td></td><td>Simple SPI bus</td></tr>
<tr><td></td><td>TMR clock input</td></tr>
<tr><td>Hardware flow control</td><td>Asynchronous</td></tr>
<tr><td></td><td>Clock synchronous</td></tr>
<tr><td>Extended serial mode</td><td>Start Frame transmission/reception function</td></tr>
</table></td></tr>
<tr><td></td><td>Registers/ bits</td><td>• Serial status register (SSR)
<table>
<tr><td>b0</td><td>MPBT</td><td>Multi-processor bit transfer bit</td></tr>
<tr><td>b1</td><td>MPB</td><td>Multi-processor bit</td></tr>
<tr><td>b2</td><td>TEND</td><td>Transmit end flag</td></tr>
<tr><td>b3</td><td>PER</td><td>Parity error flag</td></tr>
<tr><td>b4</td><td>FER</td><td>Framing error flag</td></tr>
<tr><td>b5</td><td>ORER</td><td>Overrun error flag</td></tr>
<tr><td>b6</td><td>RDRF</td><td>Receive data full flag</td></tr>
<tr><td>b7</td><td>TDRE</td><td>Transmit data empty flag</td></tr>
</table></td><td>• Serial status register (SSR)
<table>
<tr><td>b0</td><td>MPBT</td><td>Multi-processor bit transfer bit</td></tr>
<tr><td>b1</td><td>MPB</td><td>Multi-processor bit</td></tr>
<tr><td>b2</td><td>TEND</td><td>Transmit end flag</td></tr>
<tr><td>b3</td><td>PER</td><td>Parity error flag</td></tr>
<tr><td>b4</td><td>FER</td><td>Framing error flag</td></tr>
<tr><td>b5</td><td>ORER</td><td>Overrun error flag</td></tr>
<tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr>
</table></td></tr>
</table>

Table 2.25 Differences in Functions and Specifications (25)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="28">Serial communications interface</td><td rowspan="28">Registers/ bits</td><td>• Serial extended mode register (SEMR)
<table><tr><td>b0</td><td>ACS0</td><td>Asynchronous mode clock source select bit</td></tr><tr><td>b4</td><td>ABCS</td><td>Asynchronous mode base clock select bit</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr></table></td><td>• Serial extended mode register (SEMR)
<table><tr><td>b0</td><td>ACS0</td><td>Asynchronous mode clock source select bit</td></tr><tr><td>b4</td><td>ABCS</td><td>Asynchronous mode base clock select bit</td></tr><tr><td>b5</td><td>NFEN</td><td>Digital noise filter function enable bit</td></tr></table></td></tr>
<tr><td rowspan="27">—</td><td>• Noise filter setting register (SNFR)</td></tr>
<tr><td>• I²C mode register 1 (SIMR1)</td></tr>
<tr><td>• I²C mode register 2 (SIMR2)</td></tr>
<tr><td>• I²C mode register 3 (SIMR3)</td></tr>
<tr><td>• I²C status register (SISR)</td></tr>
<tr><td>• SPI mode register (SPMR)</td></tr>
<tr><td>• Extended serial module enable register (ESMER)</td></tr>
<tr><td>• Control register 0 (CR0)</td></tr>
<tr><td>• Control register 1 (CR1)</td></tr>
<tr><td>• Control register 2 (CR2)</td></tr>
<tr><td>• Control register 3 (CR3)</td></tr>
<tr><td>• Port control register (PCR)</td></tr>
<tr><td>• Interrupt control register (ICR)</td></tr>
<tr><td>• Status register (STR)</td></tr>
<tr><td>• Status clear register (STCR)</td></tr>
<tr><td>• Control field 0 data register (CF0DR)</td></tr>
<tr><td>• Control field 0 compare enable register (CF0CR)</td></tr>
<tr><td>• Control field 0 receive data register (CF0RR)</td></tr>
<tr><td>• Primary Control field 1 data register (PCF1DR)</td></tr>
<tr><td>• Secondary Control field 1 data register (SCF1DR)</td></tr>
<tr><td>• Control Field 1 compare enable register (CF1CR)</td></tr>
<tr><td>• Control field 1 receive data register (CF1RR)</td></tr>
<tr><td>• Timer control register (TCR)</td></tr>
<tr><td>• Timer mode register (TMR)</td></tr>
<tr><td>• Timer prescaler register (TPRE)</td></tr>
<tr><td>• Timer count register (TCNT)</td></tr>
<tr><td>I²C bus interface</td><td>Functions</td><td>• Specification overview
<table><tr><td>Usage notes</td><td>Setting input buffer control register
—</td></tr></table></td><td>• Specification overview
<table><tr><td>Usage notes</td><td>—
Points to note on starting transfer</td></tr></table></td></tr>
<tr><td rowspan="3">CAN module</td><td>Functions</td><td>• CAN module Specification
<table><tr><td>CAN clock source</td><td>Peripheral module clock (PCLK)
—</td></tr></table></td><td>• CAN module Specification
<table><tr><td>CAN clock source</td><td>Peripheral module clock (PCLK)
CANMCLK</td></tr></table></td></tr>
<tr><td>Units</td><td>• One unit [CAN0]</td><td>• Three units [CAN0 to CAN2]</td></tr>
<tr><td>Registers/ bits</td><td>• Bit configuration register (BCR)
<table><tr><td>b0</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b8 b10</td><td>TSEG2[2:0]</td><td>Time segment 2 control bits</td></tr><tr><td>b12 b13</td><td>SJW[1:0]</td><td>Resynchronization jump width control bits</td></tr><tr><td>b16 b25</td><td>BRP[9:0]</td><td>Prescaler division ratio select bits</td></tr><tr><td>b28 b31</td><td>TSEG1[3:0]</td><td>Time segment 1 control bits</td></tr></table>• Mask invalid register (MKIVLR)
<table><tr><td>b0 b31</td><td>—</td><td>—</td></tr></table></td><td>• Bit configuration register (BCR)
<table><tr><td>b0</td><td>CCLKS0</td><td>CAN clock source selection bit</td></tr><tr><td>b8 b10</td><td>TSEG2[2:0]</td><td>Time segment 2 control bits</td></tr><tr><td>b12 b13</td><td>SJW[1:0]</td><td>Resynchronization jump width control bits</td></tr><tr><td>b16 b25</td><td>BRP[9:0]</td><td>Prescaler division ratio select bits</td></tr><tr><td>b28 b31</td><td>TSEG1[3:0]</td><td>Time segment 1 control bits</td></tr></table>• Mask invalid register (MKIVLR)
<table><tr><td>b0 b31</td><td>MB0 MB31</td><td>Mask invalid bits</td></tr></table></td></tr>
</table>

Table 2.26 Differences in Functions and Specifications (26)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td>CAN module</td><td>Registers/ bits</td><td>• Mailbox interrupt enable register (MIER)
[Normal mailbox mode]<table><tr><td>b0
b31</td><td>—</td><td>Interrupt enable bits</td></tr></table>[FIFO mailbox mode]<table><tr><td>b0
b23</td><td>—</td><td>Interrupt enable bits</td></tr><tr><td>b24</td><td>—</td><td>Transmit FIFO interrupt enable bit</td></tr><tr><td>b25</td><td>—</td><td>Transmit FIFO interrupt generation timing control bit</td></tr><tr><td>b28</td><td>—</td><td>Receive FIFO interrupt enable bit</td></tr><tr><td>b29</td><td>—</td><td>Receive FIFO interrupt generation timing control bit</td></tr></table></td><td>• Mailbox interrupt enable register (MIER)
[Normal mailbox mode]<table><tr><td>b0
b31</td><td>MB0
MB31</td><td>Interrupt enable bits</td></tr></table>[FIFO mailbox mode]<table><tr><td>b0
b23</td><td>MB0
MB23</td><td>Interrupt enable bits</td></tr><tr><td>b24</td><td>MB24</td><td>Transmit FIFO interrupt enable bit</td></tr><tr><td>b25</td><td>MB25</td><td>Transmit FIFO interrupt generation timing control bit</td></tr><tr><td>b28</td><td>MB28</td><td>Receive FIFO interrupt enable bit</td></tr><tr><td>b29</td><td>MB29</td><td>Receive FIFO interrupt generation timing control bit</td></tr></table></td></tr>
<tr><td>Serial peripheral interface</td><td>Functions</td><td>• RSPI specification<table><tr><td>Bit rate</td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td>Other functions</td><td>CMOS/open-drain output switching function possible</td></tr><tr><td></td><td>RSPI disable function (initialization)</td></tr><tr><td></td><td>Loopback mode function</td></tr></table></td><td>• RSPI specification<table><tr><td>Bit rate</td><td>In master mode, PCLK is divided by the internal baud rate generator to generate RSPCK (the divisor is a value from 2 to 4096)</td></tr><tr><td></td><td>In slave mode, an externally input clock is used as the serial clock (the maximum frequency is PCLK divided by 8)
High-level width: 4 cycles of PCLK, low-level width: 4 cycles of PCLK</td></tr><tr><td>Other functions</td><td>—</td></tr><tr><td></td><td>RSPI disable function (initialization)</td></tr><tr><td></td><td>Loopback mode function</td></tr></table></td></tr>
<tr><td></td><td>Channels</td><td>• 2 channels [RSPI0, RSPI1]</td><td>• 3 channels [RSPI0 to RSPI2]</td></tr>
<tr><td></td><td>Registers/ bits</td><td>• RSPI pin control register<table><tr><td>b0</td><td>SPLP</td><td>RSPI loopback bit</td></tr><tr><td>b1</td><td>SPLP2</td><td>RSPI loopback 2 bit</td></tr><tr><td>b2</td><td>SPOM</td><td>RSPI output pin mode bit</td></tr><tr><td>b4</td><td>MOIFV</td><td>MOSI idle fixed value bit</td></tr><tr><td>b5</td><td>MOIFE</td><td>MOSI idle fixed value enabled bit</td></tr></table>• RSPI status register (SPSR)<table><tr><td>b0</td><td>OVRF</td><td>Overrun error flag</td></tr><tr><td>b1</td><td>IDLNF</td><td>RSPI idle flag</td></tr><tr><td>b2</td><td>MODF</td><td>Mode fault error flag</td></tr><tr><td>b3</td><td>PERF</td><td>Parity error flag</td></tr><tr><td>b5</td><td>SPTEF</td><td>Transmit buffer empty flag</td></tr><tr><td>b7</td><td>SPRF</td><td>Receive buffer full flag</td></tr></table>• RSPI data register (SPDR)<table><tr><td>b0
b15</td><td>L[15:0]</td><td>—</td></tr><tr><td>b16
b31</td><td>H[15:0]</td><td>—</td></tr></table>• RSPI data control register (SPDCR)<table><tr><td>b0
b1</td><td>SPFC[1:0]</td><td>Number of frames specification bits</td></tr><tr><td>b2
b3</td><td>SLSEL[1:0]</td><td>SSL pin output selection bits</td></tr><tr><td>b4</td><td>SPRDTD</td><td>RSPI receive/transmit data selection bit</td></tr><tr><td>b5</td><td>SPLW</td><td>RSPI longword access/word access specification bit</td></tr></table></td><td>• RSPI pin control register<table><tr><td>b0</td><td>SPLP</td><td>RSPI loopback bit</td></tr><tr><td>b1</td><td>SPLP2</td><td>RSPI loopback 2 bit</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>MOIFV</td><td>MOSI idle fixed value bit</td></tr><tr><td>b5</td><td>MOIFE</td><td>MOSI idle fixed value enabled bit</td></tr></table>• RSPI status register (SPSR)<table><tr><td>b0</td><td>OVRF</td><td>Overrun error flag</td></tr><tr><td>b1</td><td>IDLNF</td><td>RSPI idle flag</td></tr><tr><td>b2</td><td>MODF</td><td>Mode fault error flag</td></tr><tr><td>b3</td><td>PERF</td><td>Parity error flag</td></tr><tr><td>b5</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>—</td><td>(Reserved bit)</td></tr></table>• RSPI data register (SPDR)<table><tr><td>b0

b31</td><td>SPD0

SPD31</td><td>—</td></tr></table>• RSPIdata control register (SPDCR)<table><tr><td>b0
b1</td><td>SPFC[1:0]</td><td>Number of frames specification bits</td></tr><tr><td>b2
b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b4</td><td>SPRDTD</td><td>RSPI receive/transmit data selection bit</td></tr><tr><td>b5</td><td>SPLW</td><td>RSPI longword access/word access specification bit</td></tr></table></td></tr>
<tr><td>IEBus™ controller</td><td>Registers/ bits</td><td>—</td><td>• IEBus control register (IECTR)
• IEBus command register (IECMR)
• IEBus master control register (IEMCR)
• IEBus master unit address register 1 (IEAR1)
• IEBus master unit address register 2 (IEAR2)
• IEBus slave address setting register 1 (IESA1)
• IEBus slave address setting register 2 (IESA2)
• IEBus transmit message length register (IETBFL)
• IEBus reception master address register 1 (IEMA1)
• IEBus reception master address register 2 (IEMA2)</td></tr>
</table>

Table 2.27 Differences in Functions and Specifications (27)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td>IEBus™ controller</td><td>Registers/ bits</td><td>—</td><td>• IEBus receive control field register (IERCTL)
• IEBus receive message length register (IERBFL)
• IEBus lock address register 1 (IELA1)
• IEBus lock address register 2 (IELA2)
• IEBus general flag register (IEFLG)
• IEBus transmit status register (IETSR)
• IEBus transmit interrupt enable register (IEIET)
• IEBus receive status register (IERSR)
• IEBus receive interrupt enable register (IEIER)
• IEBus clock selection register (IECKSR)
• IEBus transmit data buffer registers 001 to 032 (IETB001 to IETB032)
• IEBus receive data buffer registers 001 to 032 (IERB001 to IERB032)</td></tr>
<tr><td>12-bit A/D converter</td><td>Functions</td><td>• Specification overview
<table><tr><td>Input channels</td><td>8 channels</td></tr><tr><td>Start triggers</td><td>Software trigger</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>MTU</td></tr><tr><td></td><td>TMR</td></tr><tr><td></td><td>External trigger (ADTRG0# pin)</td></tr><tr><td>—</td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td>Data register</td><td>For analog inputs: 8</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>A/D conversion results are saved in 12-bit A/D registers.</td></tr><tr><td></td><td>In addition mode, A/D conversion results are saved in 14-bit A/D data registers.</td></tr><tr><td>Functions</td><td>Sample-and-hold function</td></tr><tr><td></td><td>—</td></tr><tr><td></td><td>A/D conversion addition mode</td></tr></table></td><td>• Specification overview
<table><tr><td>Input channels</td><td>21 channels</td></tr><tr><td>Start triggers</td><td>Software trigger</td></tr><tr><td></td><td>TPU</td></tr><tr><td></td><td>MTU</td></tr><tr><td></td><td>TMR</td></tr><tr><td></td><td>External trigger (ADTRG0# pin)</td></tr><tr><td>Extended analog input</td><td>Temperature sensor output</td></tr><tr><td></td><td>A/D conversion of internal reference voltage</td></tr><tr><td>Data register</td><td>For analog inputs: 21</td></tr><tr><td></td><td>For temperature sensors: 1</td></tr><tr><td></td><td>For internal reference voltage: 1</td></tr><tr><td></td><td>A/D conversion results are saved in 12-bit A/D registers.</td></tr><tr><td></td><td>In addition mode, A/D conversion results are saved in 14-bit A/D data registers.</td></tr><tr><td>Functions</td><td>Sample-and-hold function</td></tr><tr><td></td><td>Variable number of sampling states function</td></tr><tr><td></td><td>A/D conversion addition mode</td></tr></table></td></tr>
<tr><td></td><td>Registers/ bits</td><td>• A/D channel select register (ADANS)
<table><tr><td>b0
b7</td><td>ANS[7:0]</td><td>A/D channel select bits</td></tr><tr><td>b8
b15</td><td>—</td><td>(Reserved bits)</td></tr></table></td><td>• A/D channel select register 0 (ADANS0)
<table><tr><td>b0

b15</td><td>ANS0[15:0]</td><td>A/D channel select bits</td></tr></table></td></tr>
<tr><td></td><td></td><td>—</td><td>• A/D channel select register 1 (ADANS1)</td></tr>
<tr><td></td><td></td><td>• A/D-converted value addition mode select register (ADADS)
<table><tr><td>b0
b7</td><td>ADS[7:0]</td><td>A/D-converted value addition channel select bits</td></tr><tr><td>b8
b15</td><td>—</td><td>(Reserved bits)</td></tr></table></td><td>• A/D-converted value addition mode select register 0 (ADADS0)
<table><tr><td>b0

b15</td><td>ADS0[15:0]</td><td>A/D-converted value addition channel select bits</td></tr></table></td></tr>
<tr><td></td><td></td><td>—</td><td>• A/D-converted value addition mode select register 1 (ADADS1)</td></tr>
<tr><td></td><td></td><td>• A/D start trigger select register (ADSTRGR)
<table><tr><td>b0
b3</td><td>ADSTRS [3:0]</td><td>A/D start trigger select bits</td></tr></table>• ADSTRGR.ADSTRS[3:0]
----b: Software trigger
0000b: A/D conversion start trigger pin (ADTRG0# pin)
0001b: MTU0 compare-match/input-capture A
0010b: MTU0 compare-match/input-capture B
0011b: MTU0 to 4 compare-match/input-capture A
0100b: MTU6 to 10 compare-match/input-capture A
0101b: MTU0 compare-match E
0110b: MTU0 compare-match F
0111b: MTU4 compare-match
1000b: MTU10 compare-match
1001b: TMR0 compare-match A
1010b: TMR2 compare-match A</td><td>• A/D start trigger select register (ADSTRGR)
<table><tr><td>b0
b3</td><td>ADSTRS [3:0]</td><td>A/D start trigger select bits</td></tr></table>• ADSTRGR.ADSTRS[3:0]
----b: Software trigger
0000b: A/D conversion start trigger pin (ADTRG0# pin)
0001b: MTU0 compare-match/input-capture A
0010b: MTU0 compare-match/input-capture B
0011b: MTU0 to 4 compare-match/input-capture A
0100b: TPU0 to 4 compare-match/input-capture A
0101b: MTU0 compare-match E
0110b: MTU0 compare-match F
0111b: MTU4 compare-match
1000b: TPU0 compare-match/input-capture A
1001b: TMR0 compare-match A
1010b: TMR2 compare-match A</td></tr>
</table>

Table 2.28 Differences in Functions and Specifications (28)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="5">12-bit A/D converter</td><td rowspan="5">Registers/ bits</td><td rowspan="3">—</td><td>• A/D-converted extended input control register (ADEXICR)</td></tr>
<tr><td>• A/D temperature sensor data register (ADTSDR)</td></tr>
<tr><td>• A/D internal reference voltage data register (ADOCDR)</td></tr>
<tr><td>• A/D data registers 0 to 7 (ADDR0 to ADDR7)</td><td>• A/D data registers 0 to 20 (ADDR0 to ADDR20)</td></tr>
<tr><td>—</td><td>• A/D sampling state register 01 (ADSSTR01)
• A/D sampling state register 23 (ADSSTR23)</td></tr>
<tr><td rowspan="4">10-bit A/D converter</td><td>Functions</td><td>• Specification overview
<table>
<tr><td>Input channels</td><td>(1 unit × 4 channels) × 2</td></tr>
<tr><td>Start triggers</td><td>Software trigger</td></tr>
<tr><td></td><td>—</td></tr>
<tr><td></td><td>MTU</td></tr>
<tr><td></td><td>TMR</td></tr>
<tr><td></td><td>External trigger (ADTRG0# pin)</td></tr>
<tr><td></td><td>External trigger (ADTRG1# pin)</td></tr>
</table></td><td>• Specification overview
<table>
<tr><td>Input channels</td><td>1 unit × 8 channels + 1 extended channel</td></tr>
<tr><td>Start triggers</td><td>Software trigger</td></tr>
<tr><td></td><td>TPU</td></tr>
<tr><td></td><td>MTU</td></tr>
<tr><td></td><td>TMR</td></tr>
<tr><td></td><td>External trigger (ADTRG# pin)</td></tr>
<tr><td></td><td>—</td></tr>
</table></td></tr>
<tr><td rowspan="3">Registers/ bits</td><td>• A/D data registers A to D (ADDRA to D)</td><td>• A/D data registers A to D (ADDRA to D)</td></tr>
<tr><td>—</td><td>• A/D data registers E to H (ADDRA to H)</td></tr>
<tr><td>• A/D control/status register (ADCSR)
<table>
<tr><td>b0
b3</td><td>CH[3:0]</td><td>Channel select bits</td></tr>
<tr><td>b5</td><td>ADST</td><td>A/D start bit</td></tr>
<tr><td>b6</td><td>ADIE</td><td>A/D interrupt enable bit</td></tr>
</table>
• AD0.ADCSR.CH[3: 0]
0000b: AN0 (single mode)/AN0 (scan mode)
0001b: AN1 (single mode)/AN0 and AN1 (scan mode)
0010b: AN2 (single mode)/AN0 to AN2 (scan mode)
0011b: AN3 (single mode)/AN0 to AN3 (scan mode)
Setting prohibited other than above
• AD1.ADCSR.CH[3:0]
0000b: AN4 (single mode)/AN4 (scan mode)
0001b: AN5 (single mode)/AN4, 5 (scan mode)
0010b: AN6 (single mode)/AN4 to 6 (scan mode)
0011b: AN7 (single mode)/AN4 to 7 (scan mode)
Setting prohibited other than above</td><td>• A/D control/status register (ADCSR)
<table>
<tr><td>b0
b2</td><td>CH[2:0]</td><td>Channel select bits</td></tr>
<tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr>
<tr><td>b5</td><td>ADST</td><td>A/D start bit</td></tr>
<tr><td>b6</td><td>ADIE</td><td>A/D interrupt enable bit</td></tr>
</table>
• ADCSR.CH[2:0]
000b: AN0 (single mode)/AN0 (scan mode)
001b: AN1 (single mode)/AN0 and AN1 (scan mode)
010b: AN2 (single mode)/AN0 to AN2 (scan mode)
011b: AN3 (single mode)/AN0 to AN3 (scan mode)
100b: AN4 (single mode)/AN0 to AN4 (scan mode)
101b: AN5 (single mode)/AN0 to AN5 (scan mode)
110b: AN6 (single mode)/AN0 to AN6 (scan mode)
111b: AN7 (single mode)/AN0 to AN7 (scan mode)</td></tr>
<tr><td>• A/D control register (ADCR)
<table>
<tr><td>b0
b1</td><td>MODE[1:0]</td><td>Operation mode select bits</td></tr>
<tr><td>b2
b3</td><td>CKS[1:0]</td><td>Clock select bits</td></tr>
<tr><td>b5
b7</td><td>TRGS[2:0]</td><td>Trigger select bits</td></tr>
</table>
• AD0.ADCR.TGRS[2:0]
000b: Software trigger
001b: MTU0 to MTU4 compare-match/input-capture A
010b: TMR0 compare-match
011b: A/D conversion start trigger pin (ADTRG0# pin)
100b: MTU0 compare-match/input-capture A
101b: MTU6 to MTU10 compare-match/input-capture A
110b: MTU4 compare-match
111b: MTU10 compare-match
• AD1.ADCR.TGRS[2:0]
000b: Software trigger
001b: MTU0 to MTU4 compare-match/input-capture A
010b: TMR0 compare-match
011b: A/D conversion start trigger pin (ADTRG1# pin)
100b: MTU0 compare-match/input-capture B
101b: MTU6 to MTU10 compare-match/input-capture A
110b: MTU4 compare-match
111b: MTU10 compare-match</td><td>• A/D control register (ADCR)
<table>
<tr><td>b0
b1</td><td>MODE[1:0]</td><td>Operation mode select bits</td></tr>
<tr><td>b2
b3</td><td>CKS[1:0]</td><td>Clock select bits</td></tr>
<tr><td>b5
b7</td><td>TRGS[2:0]</td><td>Trigger select bits</td></tr>
</table>
• ADCR.TRGS[2:0]
000b: Software trigger
001b: MTU0 to MTU4 compare-match/input-capture A
010b: TMR0 compare-match
011b: A/D conversion start trigger pin (ADTRG# pin)
100b: MTU0 compare-match/input-capture A
101b: TPU0 to MTU4 compare-match/input-capture A
110b: MTU4 compare-match
111b: TPU0 compare-match/input-capture A</td></tr>
</table>

Table 2.29 Differences in Functions and Specifications (29)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td>10-bit A/D converter</td><td>Registers/ bits</td><td>• ADDRn format select register (ADDPR)
<table><tr><td>b4
b5</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b6</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>DPSEL</td><td>ADDRn format select bit</td></tr></table></td><td>• A/D control register2 (ADCR2)
<table><tr><td>b4
b5</td><td>EXSEL[1:0]</td><td>Extended analog input select bits</td></tr><tr><td>b6</td><td>EXOEN</td><td>Extended analog output control bit</td></tr><tr><td>b7</td><td>DPSEL</td><td>ADDRy format select bit</td></tr></table></td></tr>
<tr><td>D/A converter</td><td>Functions</td><td>• Specification overview
<table><tr><td>—</td><td>—</td></tr></table></td><td>• Specification overview
<table><tr><td>Countermeasure against interference from analog modules</td><td>Countermeasure against interference between D/A and A/D converters</td></tr></table></td></tr>
<tr><td></td><td>Registers/ bits</td><td>—</td><td>• D/A A/D synchronous start control register (DAADSCR)</td></tr>
<tr><td>Temperature sensor</td><td>Registers/ bits</td><td>—</td><td>• Temperature sensor control register (TSCR)</td></tr>
<tr><td>Flash memory for code storage</td><td>Functions</td><td>• Specification overview
<table><tr><td>Memory space</td><td>User area: up to 512 KB
User boot area: 16 KB</td></tr><tr><td>Write unit</td><td>256-byte units</td></tr><tr><td>Block structure</td><td>4 KB × 8 blocks
16 KB × 30 blocks
—
—</td></tr><tr><td>BG0 (background operation) function</td><td>• Programs located in the ROM area can be executed during data flash program or erase operations.
• The CPU can execute programs located in areas other than the ROM or data flash areas during ROM program or erase operations.</td></tr><tr><td>On-board programming</td><td>Boot mode
USB boot mode
—
User program mode</td></tr><tr><td>Off-board programming</td><td>The user MAT and user boot MAT areas can be programmed using a PROM writer</td></tr><tr><td>Protection functions</td><td>Error protection</td></tr></table></td><td>• Specification overview
<table><tr><td>Memory space</td><td>User area: up to 2 MB
User boot area: 16 KB</td></tr><tr><td>Write unit</td><td>128-byte units</td></tr><tr><td>Block structure</td><td>4 KB × 8 blocks
16 KB × 30 blocks
32 KB × 16 blocks
64 KB × 16 blocks</td></tr><tr><td>BG0 (background operation) function</td><td>The CPU can execute programs in the ROM area during E2 data flash P/E operations.</td></tr><tr><td>On-board programming</td><td>Boot mode
USB boot mode
User boot mode
User program mode</td></tr><tr><td>Off-board programming</td><td>The user area and the user boot area can be programmed using a Flash programmer.</td></tr><tr><td>Protection functions</td><td>FCU command-locked state</td></tr></table></td></tr>
<tr><td></td><td>Registers/ bits</td><td>• Flash status register 1 (FSTATR1)
<table><tr><td>b0
b1</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b7</td><td>FCUERR</td><td>FCU error bit</td></tr></table>• b1 and b0: Reserved bits
The read value is undefined. Writing to these bits has no effect.
• Flash P/E mode entry register (FENTRYR)
<table><tr><td>b0</td><td>FENTRY0</td><td>ROM P/E mode entry bit 0</td></tr><tr><td>b1</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b2</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b3</td><td>—</td><td>(Reserved bit)</td></tr><tr><td>b7</td><td>FENTRYD</td><td>Data flash P/E mode entry bit</td></tr><tr><td>b8
b15</td><td>FEKEY[7:0]</td><td>Key code</td></tr></table>• FENTRYR.FENTRY0
FENTRY0: 512 KB/384 KB/256 KB
• Peripheral clock notification register (PCKAR)
<table><tr><td>b0
b7</td><td>PCKA[7:0]</td><td>Peripheral clock notification bits</td></tr></table>Bits used to set the peripheral clock (PCLK) during write or erase of ROM or data flash.</td><td>• Flash status register 1 (FSTATR1)
<table><tr><td>b0
b1</td><td>—</td><td>(Reserved bits)</td></tr><tr><td>b7</td><td>FCUERR</td><td>FCU error flag</td></tr></table>• b1 and b0: Reserved bits
These bits are read as 0. Writing to them has no effect.
• Flash P/E mode entry register (FENTRYR)
<table><tr><td>b0</td><td>FENTRY0</td><td>ROM P/E mode entry bit 0</td></tr><tr><td>b1</td><td>FENTRY1</td><td>ROM P/E mode entry bit 1</td></tr><tr><td>b2</td><td>FENTRY2</td><td>ROM P/E mode entry bit 2</td></tr><tr><td>b3</td><td>FENTRY3</td><td>ROM P/E mode entry bit 3</td></tr><tr><td>b7</td><td>FENTRYD</td><td>E2 data flash P/E mode entry bit</td></tr><tr><td>b8
b15</td><td>FEKEY[7:0]</td><td>Key code</td></tr></table>• FENTRYR.FENTRY0 to 3
FENTRY0: 2 MB/1.5 MB/1.0 MB/768 KB/512 KB/256 KB
FENTRY1: 2 MB/1.5 MB/1.0 MB/768 KB
FENTRY2: 2 MB/1.5 MB
FENTRY3: 2 MB
• Peripheral clock notification register (PCKAR)
<table><tr><td>b0
b7</td><td>PCKA[7:0]</td><td>Peripheral clock notification bits</td></tr></table>Bits used to set the FlashIF clock (FCLK) during P/E of ROM or E2 data flash.</td></tr>
</table>

Table 2.30 Differences in Functions and Specifications (30)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td rowspan="2">Flash memory for data storage</td><td>Functions</td><td>
• Specification overview
<table>
<tr><td>Reading via the peripheral bus</td><td>A read operation takes three cycles of PCLK3 in words or bytes.</td></tr>
<tr><td>Write unit</td><td>8-byte or 128-byte units</td></tr>
<tr><td>BG0 (background operation) function</td><td>• Programs located in the ROM area can be executed during data flash program or erase operations.
• The CPU can execute programs located in areas other than the ROM or data flash areas during ROM program or erase operations.</td></tr>
<tr><td>Programming command</td><td>2nd cycle data: 04h (8 bytes)
40h (128 bytes)</td></tr>
<tr><td>Block structure</td><td>2 KB × 16 blocks</td></tr>
<tr><td>Blank check unit</td><td>2 KB/8-byte units</td></tr>
<tr><td rowspan="3">On-board programming</td><td>Boot mode</td></tr>
<tr><td>USB (user) boot mode</td></tr>
<tr><td>—</td></tr>
<tr><td></td><td>User program mode</td></tr>
<tr><td>Protect function</td><td>Error protect function</td></tr>
</table>
</td><td>
• Specification overview
<table>
<tr><td>Reading via the peripheral bus</td><td>A read operation takes three cycles of FCLK6 in words or bytes.</td></tr>
<tr><td>Write unit</td><td>2-byte units</td></tr>
<tr><td>BG0 (background operation) function</td><td>The CPU can execute programs in the ROM area during E2 data flash P/E operations.</td></tr>
<tr><td>Programming command</td><td>2nd cycle data: 01h (2 bytes)</td></tr>
<tr><td>Block structure</td><td>32 byte × 1024 blocks</td></tr>
<tr><td>Blank check unit</td><td>2 KB/2-byte units</td></tr>
<tr><td rowspan="4">On-board programming</td><td>Boot mode</td></tr>
<tr><td>USB boot mode</td></tr>
<tr><td>User boot mode</td></tr>
<tr><td>User program mode</td></tr>
<tr><td>Protect function</td><td>FCU command clock function</td></tr>
</table>
</td></tr>
<tr><td>Registers/ bits</td><td>
• Data flash read enable register 0 (DFLRE0)
<table>
<tr><td>b0</td><td>DBRE00</td><td>DB00 block read enable bit</td></tr>
<tr><td>b1</td><td>DBRE01</td><td>DB01 block read enable bit</td></tr>
<tr><td>b2</td><td>DBRE02</td><td>DB02 block read enable bit</td></tr>
<tr><td>b3</td><td>DBRE03</td><td>DB03 block read enable bit</td></tr>
<tr><td>b4</td><td>DBRE04</td><td>DB04 block read enable bit</td></tr>
<tr><td>b5</td><td>DBRE05</td><td>DB05 block read enable bit</td></tr>
<tr><td>b6</td><td>DBRE06</td><td>DB06 block read enable bit</td></tr>
<tr><td>b7</td><td>DBRE07</td><td>DB07 block read enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
• Data flash read enable register 1 (DFLRE1)
<table>
<tr><td>b0</td><td>DBRE08</td><td>DB08 block read enable bit</td></tr>
<tr><td>b1</td><td>DBRE09</td><td>DB09 block read enable bit</td></tr>
<tr><td>b2</td><td>DBRE10</td><td>DB10 block read enable bit</td></tr>
<tr><td>b3</td><td>DBRE11</td><td>DB11 block read enable bit</td></tr>
<tr><td>b4</td><td>DBRE12</td><td>DB12 block read enable bit</td></tr>
<tr><td>b5</td><td>DBRE13</td><td>DB13 block read enable bit</td></tr>
<tr><td>b6</td><td>DBRE14</td><td>DB14 block read enable bit</td></tr>
<tr><td>b7</td><td>DBRE15</td><td>DB15 block read enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
</td><td>
• E2 data flash read enable register 0 (DFLRE0)
<table>
<tr><td>b0</td><td>DBRE00</td><td>0000-0063 block read enable bit</td></tr>
<tr><td>b1</td><td>DBRE01</td><td>0064-0127 block read enable bit</td></tr>
<tr><td>b2</td><td>DBRE02</td><td>0128-0191 block read enable bit</td></tr>
<tr><td>b3</td><td>DBRE03</td><td>0192-0255 block read enable bit</td></tr>
<tr><td>b4</td><td>DBRE04</td><td>0256-0319 block read enable bit</td></tr>
<tr><td>b5</td><td>DBRE05</td><td>0320-0383 block read enable bit</td></tr>
<tr><td>b6</td><td>DBRE06</td><td>0384-0447 block read enable bit</td></tr>
<tr><td>b7</td><td>DBRE07</td><td>0448-0511 block read enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
• E2 data flash read enable register 1 (DFLRE1)
<table>
<tr><td>b0</td><td>DBRE08</td><td>0512-0575 block read enable bit</td></tr>
<tr><td>b1</td><td>DBRE09</td><td>0576-0639 block read enable bit</td></tr>
<tr><td>b2</td><td>DBRE10</td><td>0640-0703 block read enable bit</td></tr>
<tr><td>b3</td><td>DBRE11</td><td>0704-0767 block read enable bit</td></tr>
<tr><td>b4</td><td>DBRE12</td><td>0768-0831 block read enable bit</td></tr>
<tr><td>b5</td><td>DBRE13</td><td>0832-0895 block read enable bit</td></tr>
<tr><td>b6</td><td>DBRE14</td><td>0896-0959 block read enable bit</td></tr>
<tr><td>b7</td><td>DBRE15</td><td>0960-1023 block read enable bit</td></tr>
<tr><td>b8
b15</td><td>KEY[7:0]</td><td>Key code</td></tr>
</table>
</td></tr>
</table>

Table 2.31 Differences in Functions and Specifications (31)

<table>
<tr><th colspan="2">Item</th><th>RX62N Group</th><th>RX63N Group</th></tr>
<tr><td>Flash memory for data storage</td><td>Registers/ bits</td><td>

• Data flash programming/erasure enable register 0 (DFLWE0)

b0	DBWE00	DB00 block programming/erasure enable bit
b1	DBWE01	DB01 block programming/erasure enable bit
b2	DBWE02	DB02 block programming/erasure enable bit
b3	DBWE03	DB03 block programming/erasure enable bit
b4	DBWE04	DB04 block programming/erasure enable bit
b5	DBWE05	DB05 block programming/erasure enable bit
b6	DBWE06	DB06 block programming/erasure enable bit
b7	DBWE07	DB07 block programming/erasure enable bit
b8 b15	KEY[7:0]	Key code

• Data flash programming/erasure enable register 1 (DFLWE1)

b0	DBWE08	DB08 block programming/erasure enable bit
b1	DBWE09	DB09 block programming/erasure enable bit
b2	DBWE10	DB10 block programming/erasure enable bit
b3	DBWE11	DB11 block programming/erasure enable bit
b4	DBWE12	DB12 block programming/erasure enable bit
b5	DBWE13	DB13 block programming/erasure enable bit
b6	DBWE14	DB14 block programming/erasure enable bit
b7	DBWE15	DB15 block programming/erasure enable bit
b8 b15	KEY[7:0]	Key code

• Flash P/E mode entry register (FENTRYR)

b0	FENTRY0	ROM P/E mode entry bit 0
b1	—	(Reserved bit)
b2	—	(Reserved bit)
b3	—	(Reserved bit)
b7	FENTRYD	Data flash P/E mode entry bit
b8 b15	FEKEY[7:0]	Key code

• FENTRYR.FENTRY0
FENTRY0: 512 KB/384 KB/256 KB

• Data flash blank check control register (DFLBCCNT)

b0	BCSIZE	Blank check size setting bit
b1	—	(Reserved bit)
b2	—	(Reserved bit)
b3 b10	BCADR [7:0]	Blank check address setting bits
b15	—	(Reserved bit)

</td><td>

• E2 data flash programming/erasure enable register 0 (DFLWE0)

b0	DBWE00	0000-0063 block P/E enable bit
b1	DBWE01	0064-0127 block P/E enable bit
b2	DBWE02	0128-0191 block P/E enable bit
b3	DBWE03	0192-0255 block P/E enable bit
b4	DBWE04	0256-0319 block P/E enable bit
b5	DBWE05	0320-0383 block P/E enable bit
b6	DBWE06	0384-0447 block P/E enable bit
b7	DBWE07	0448-0511 block P/E enable bit
b8 b15	KEY[7:0]	Key code

• E2 data flash P/E enable register 1 (DFLWE1)

b0	DBWE08	0512-0575 block P/E enable bit
b1	DBWE09	0576-0639 block P/E enable bit
b2	DBWE10	0640-0703 block P/E enable bit
b3	DBWE11	0704-0767 block P/E enable bit
b4	DBWE12	0768-0831 block P/E enable bit
b5	DBWE13	0832-0895 block P/E enable bit
b6	DBWE14	0896-0959 block P/E enable bit
b7	DBWE15	0960-1023 block P/E enable bit
b8 b15	KEY[7:0]	Key code

• Flash P/E mode entry register (FENTRYR)

b0	FENTRY0	ROM P/E mode entry bit 0
b1	FENTRY1	ROM P/E mode entry bit 1
b2	FENTRY2	ROM P/E mode entry bit 2
b3	FENTRY3	ROM P/E mode entry bit 3
b7	FENTRYD	E2 data flash P/E mode entry bit
b8 b15	FEKEY[7:0]	Key code

• FENTRYR.FENTRY0 to 3
FENTRY0: 2 MB/1.5 MB/1.0 MB/768 KB/512 KB/256 KB
FENTRY1: 2 MB/1.5 MB/1.0 MB/768 KB
FENTRY2: 2 MB/1.5 MB
FENTRY3: 2 MB

• E2 data flash blank check control register (DFLBCCNT)

b0 b10	BCADR [10:0]	Blank check address setting bits
b15	BCSIZE	Blank check size setting bit

</td></tr>
</table>

3. Reference Documents

RX62N Group, RX621 Group User's Manual: Hardware Rev.1.30
RX63N Group, RX631 Group User's Manual: Hardware Rev.1.50
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest information can be downloaded from the Renesas Electronics website.)

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REVISION HISTORY	RX62N Group, RX63N Group Application Note Differences between RX62N Group and RX63N Group

Rev.	Date	Description	
		Page	Summary
1.00	Sep. 26, 2013	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different type numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different type numbers, implement a system-evaluation test for each of the products.

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