RX23W Group

Guidelines for Bluetooth Board Design

Introduction

This document describes RF board design guidelines for RX23W *Bluetooth*® 5.0 (Core Specification v5.0) RF transceiver. Please refer "RX Family Hardware Design Guide for board design" (R01AN1411) except Bluetooth 5.0 RF transceiver part.

Target Device

RX23W Group

Note: The contents of this document are provided as a reference and do not guarantee the signal quality in the system. When designing the actual system, thoroughly evaluate the product in the overall system and apply these contents on your own responsibility.

Contents

1. Overview

Sections 2, 3, and 4 of this document describe board design guidelines for RX23W QFN package, RX23W BGA package, and RX23W LGA package, respectively. This document briefly describes the Bluetooth 5.0 RF transceiver unit pins used in the RX23W.

1.1 Related documents

The following documents are related to this application note. Also refer to these documents when using this application note.

- RX23W group User's Manual: Hardware (R01UH0823)
- RX Family Hardware Design Guide (R01AN1411)
- RX23W group Tuning procedure of Bluetooth dedicated clock frequency (R01AN4762)

2. Board design guidelines for RX23W QFN

2.1 RX23W QFN Pin list

Table 2-1 is the description of Bluetooth 5.0 RF transceiver unit pins in RX23W QFN.

Table 2-1 Description of Bluetooth 5.0 RF transceiver unit pins in RX23W QFN

Pin Number	Pin Name	I/O	Functions
48	CLKOUT_RF	Output	Bluetooth-Dedicated clock output pin, whose frequency can be set to 4, 2, or 1MHz. The default output setting is off. Connecting the clock output pin to the external clock input pin of MCU, the RF clock can be used as the MCU system clock.
32	ANT	In/Out	RF single I/O pin for RF transceiver. Adjust the characteristic impedance of the signal line to 50ohm.
38	XTAL1_RF	Input	Pins for connecting the Bluetooth-dedicated clock oscillator. 32-MHz oscillator connection pin
37	XTAL2_RF	Output	Pins for connecting the Bluetooth-dedicated clock oscillator. 32-MHz oscillator connection pin
40	DCLOUT	Output	RF transceiver power-supply (DC-DC converter or linear regulator) output pin
46	DCLIN_A	Input	RF transceiver power-supply output connection pin. This pin should be connected to an external inductor and capacitor when the DC-DC converter mode is selected. When the linear regulator mode is selected, this pin should be connected to an external capacitor.
45	DCLIN_D	Input	RF transceiver power-supply output connection pin. This pin should be connected to an external inductor and capacitor when the DC-DC converter mode is selected. When the linear regulator mode is selected, this pin should be connected to an external capacitor.
44	VCC_RF	Input	RF transceiver power supply pin
39	AVCC_RF	Input	RF transceiver power supply pin
28	ICGND (VSS_RF)	Input	RF transceiver ground pin. In this document, this pin is called “ICGND”.
Exposed Die Pad	VSS_RF	Input	RF transceiver ground pin

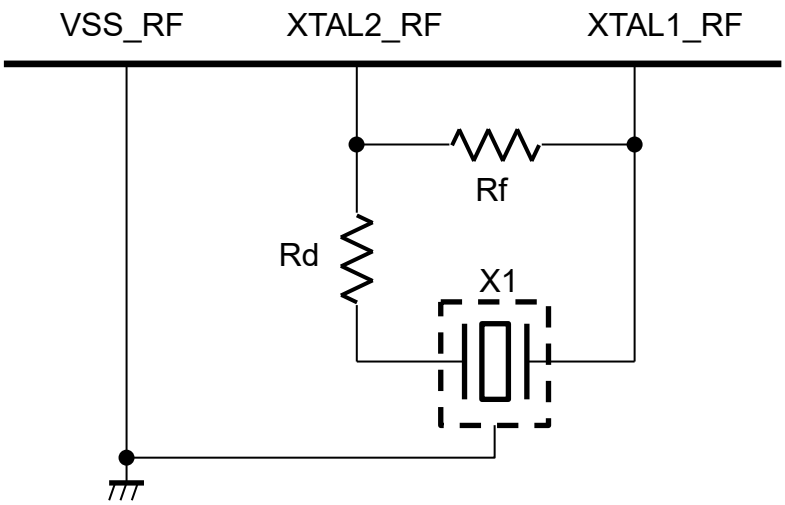
2.2 Oscillator circuit for Bluetooth-dedicated clock

Note the following when designing an oscillator circuit for Bluetooth-dedicated clock.

- Place the crystal resonator close to the “XTAL1_RF” and “XTAL2_RF” pins. We recommend the wiring length between the RX23W and the crystal resonator of approximately 6 mm, as shown in "Figure 2-2 Example of the pattern around the crystal resonator".
- Shield the pattern for the “XTAL1_RF” and “XTAL2_RF” pins with the ground pattern. Do not place the pattern for these signals in parallel with or across other patterns where a large current flows or the level changes frequently.
- Not place any signal, power, and ground lines except the oscillator circuit’s on and below the oscillator circuit area. We recommend that the ground pattern is placed in the layers under the oscillator circuit, as shown in "Figure 2-2 Example of the pattern around the crystal resonator".
- Separate the oscillator circuit and the signal line from an antenna to “ANT” pin by placing slit patterns on all layers.
- Ensure a return path in layer2 (additional layer3 if possible) from ground of the crystal resonator to "Exposed Die Pad (VSS_RF)”, as shown in "Figure 2-2 Example of the pattern around the crystal resonator".
- External load capacitors (CL) for frequency tuning are unnecessary, because the capacitors are built in IC. For Tuning procedure of Bluetooth dedicated clock frequency, see the descriptions of the application note, the Hardware Design Guide(R01AN4762). The latest version can be downloaded from the Renesas Electronics website.
- Insert a damping resistor (Rd) as required. Set the resistance to the value recommended by the oscillator manufacturer as the value depends on the oscillator and its driving capability. If the oscillator manufacturer states that the addition of a feedback resistor (Rf) to the oscillator is required, insert Rf between XTAL1_RF and XTAL2_RF according to the instructions.
- When the frequency-divided clock for the Bluetooth-dedicated clock is output, note designing board pattern. The wiring length should be as short as possible. In addition, must not branch the wiring. And avoid using vias on the transmission line. A maximum of 2 is recommended.
- Shield the transmission line of CLKOUT_RF with the "VSS" pattern to avoid noise couplings to “VSS_RF”.

Note: Bluetooth 5.0 RF transceiver clock frequency accuracy which includes initial error, temperature drift, and ageing effect should be less than or equal to +/-50ppm in the Bluetooth specification. Therefore, the frequency error should be as less as possible.

Figure 2-1 shows an example of the crystal resonator connection. Figure 2-2 shows an example of the pattern around the crystal resonator.



Note: The resistance of Rd and Rf should be determined thorough oscillation characteristics evaluation with a crystal resonator to be mounted. These resistors might not be required, depending on the oscillation characteristics.

Figure 2-1 Example of the crystal resonator connection.

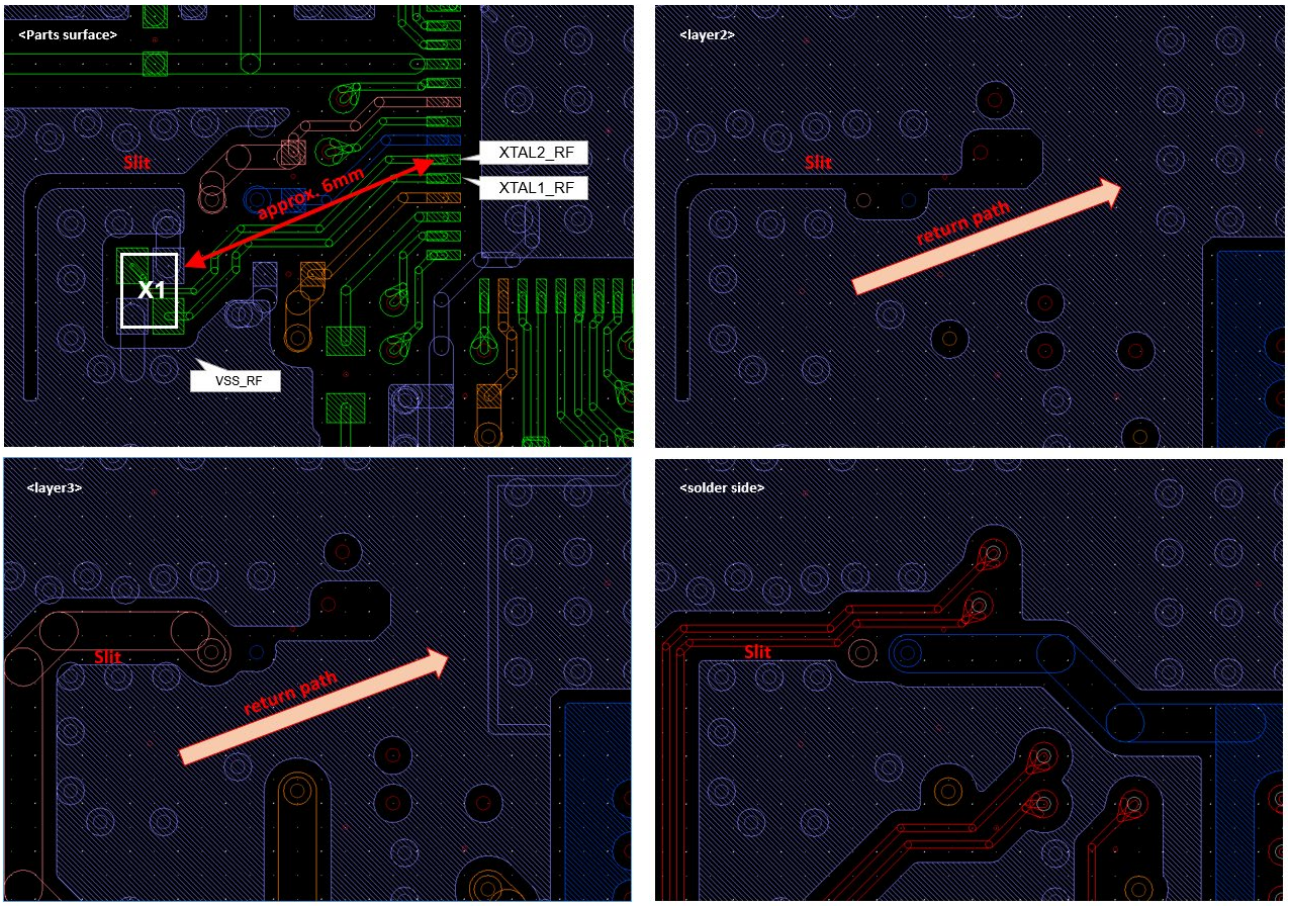


Figure 2-2 Example of the pattern around the crystal resonator

Table 2-2 shows confirmed operation crystal resonator list (reference).

Table 2-2 Tested crystal resonator list (reference)

Manufacturer	Parts number	SMD/Lead size code (in mm)	Frequency (MHz)	Frequency Tolerance (ppm)	Frequency Stability (ppm)	Equivalent Series Resistance (ohm)	Load Capacitance (pF)
NDK	NX1612SA-32.000MHZ-CHP-CIS-3	1612	32.00	+/-10	+/-20	Max 100	6
NDK	NX1210AB- 32.000MHZ-CHP-CIX-3	1210	32.00	Total +/-30		Max 100	6
Kyocera	CX1612DB32000 A0WPNC1	1612	32.00	Total +/-25		Max 100	5
Kyocera	CX1210SB32000 B0GPJC1	1210	32.00	Total +/-30		Max 80	6
Murata	XRCMD32M000FZQ52R0	1612	32.00	Total +/-30		Max 60	6
Murata	XRCTD32M000N1P00R0	1210	32.00	Total +/-30		Max 120	6

2.3 Antenna connection pin

Note the followings for antenna connection pin design.

- Adjust the characteristic impedance of 50ohm for the signal line from an antenna to “ANT” pin. Optimize the width of signal line and the gap between signal line and ground pattern, considering the PCB permittivity and layer thickness. Depending on the antenna used, additional parts such as inductors or capacitors may be required. In "Figure 2-3 Example of the pattern around “ANT” pin", the coplanar waveguide is used.
- When mounting a connector, keep the characteristic impedance of 50ohm including the connector.
- The directly under layer of the coplanar waveguide should be solid ground, having no crossing with any signal, power, and other ground lines.
- Place vias as many as possible between the coplanar waveguide ground pattern and the solid ground. We recommend that the via spacing should be approximately 0.9mm, as shown in "Figure 2-3 Example of the pattern around “ANT” pin".

Figure 2-3 shows an example of the pattern around “ANT” pin.

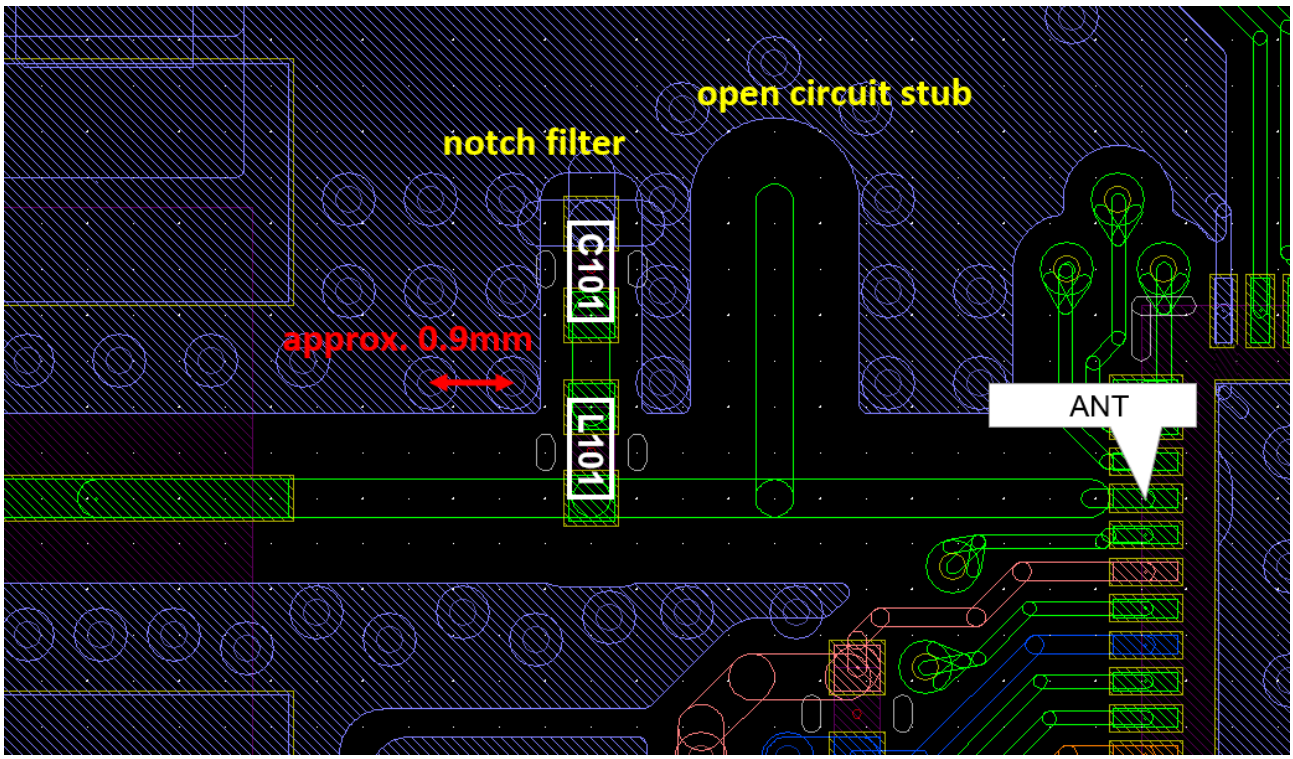


Figure 2-3 Example of the pattern around “ANT” pin

- Pay attention to an emission level of 5th order harmonics, when selecting 4 dBm transmitted output mode and evaluating of US(FCC) regulatory with a coaxial cable. The emission should be suppressed with an RF filter implementation.

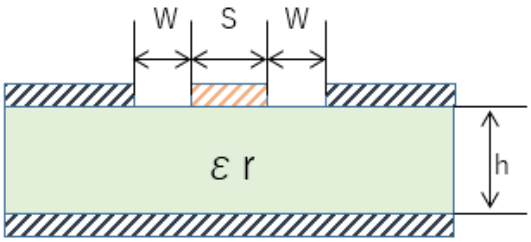
  RF filter requirements
  Frequency band to be suppressed: 12.01 to 12.4 GHz
  Minimum attenuation: 8dB

- Pay attention to an emission level of 3rd order harmonics, when selecting 0 dBm transmitted output mode and evaluating of US(FCC) regulatory with a coaxial cable. The emission should be suppressed with an RF filter implementation.

  RF filter requirements
  Frequency band to be suppressed: 7250 to 7440 MHz
  Minimum attenuation: 2dB

This document describes an example of an open circuit stub and an example of LPF using SMD parts. Both of these circuits can suppress 5th order harmonics of 4 dBm transmitted output mode and the 3rd order harmonics of 0 dBm transmitted output mode.

Figure 2-4 shows an example of the open circuit stub.



Permittivity(ε_r)=4.45
S=0.41mm
W=0.72mm
h=0.2mm
Frequency=12400MHz (2480MHz x 5)

Obtain an effective permittivity $\varepsilon_{r,eff}$ from the above board composition.
effective permittivity $\varepsilon_{r,eff} \fallingdotseq 3.515$

The wavelength of 12400MHz is approximately 24.18 mm. Then calculate the length of a stub by using the formula below.
the length of a stub $L = 0.25*\lambda / (\varepsilon_{r,eff})^{0.5} = 3.224$mm

Note: Place the open circuit stub as close to “ANT” pin as possible. We recommend that it should place approximately 3.5mm, as shown in example pattern on the right figure.

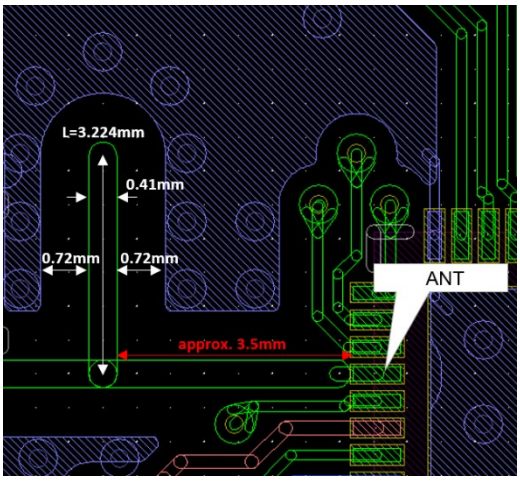


Figure 2-4 Example of the open circuit stub

Note: The pattern width and pattern pitch for impedance control vary depending on board thickness, material, and layer configuration. Contact the board manufacturer for more information.

Figure 2-5 shows an example of LPF using SMD parts

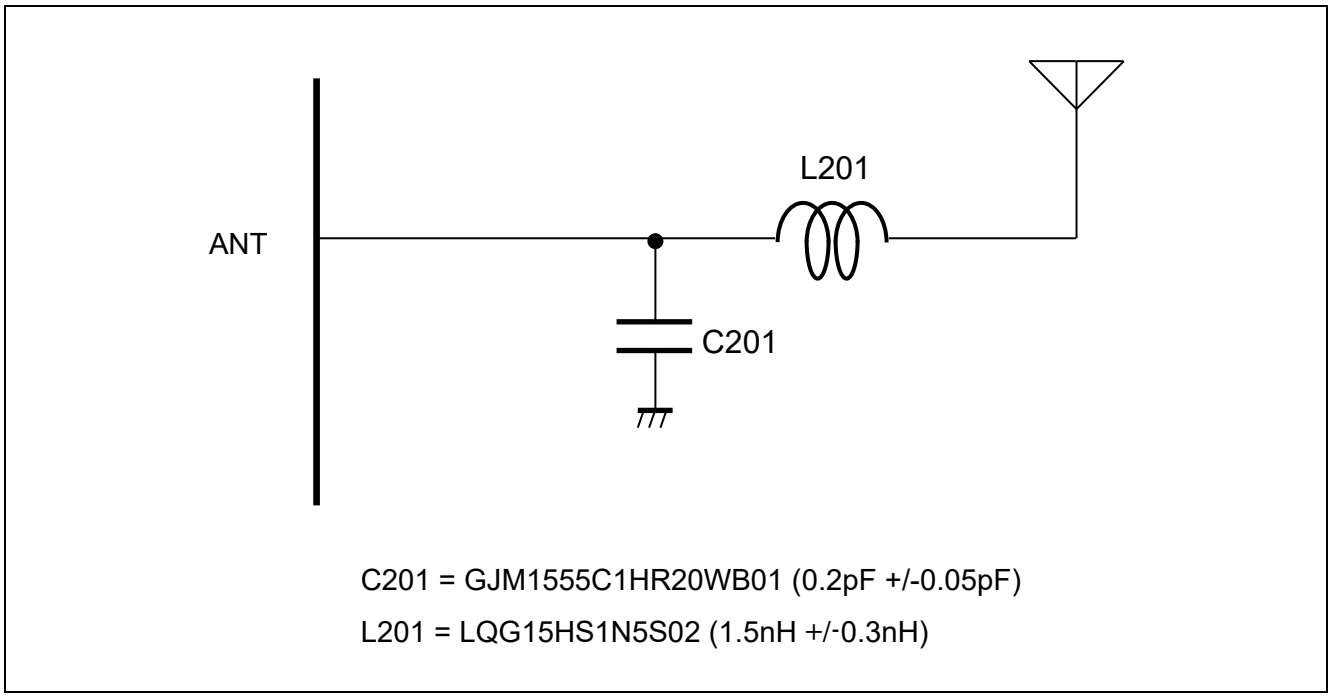


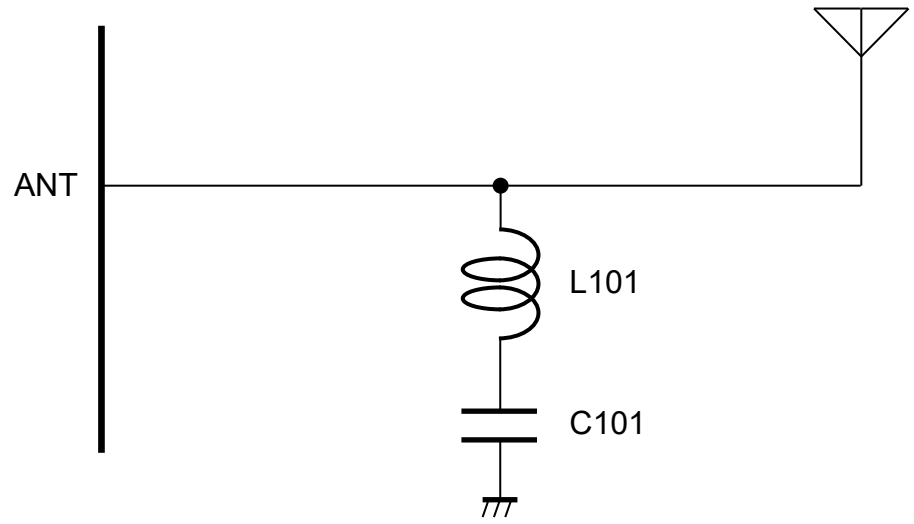
Figure 2-5 Example of LPF using SMD parts

Note: Depending on the PCB design, the value may differ. Adjust the value, if necessary.

- When certifying of Korea (KCC) regulatory, an emission of 1.9GHz frequency band should be suppressed with an RF filter implementation.

  RF filter requirements
  Frequency band to be suppressed: 1921 to 1984 MHz
  Minimum attenuation: 7dB

This document describes an example of a notch filter. Figure 2-6 shows an example of the notch filter.



L101 = LQG15HS7N5J02 (7.5nH +/-5%)
C101 = GCM1555C1HR50BA16 (0.5pF +/-0.1pF)

RF filter requirements
Frequency band to be suppressed : 1921 to 1984 MHz
Minimum attenuation : 7dB

Note: Depending on the PCB design, the value of capacitor C101 may differ.
Adjust the value of capacitor C101, if necessary.

Figure 2-6 Example of the notch filter

2.4 Power supply mode for Bluetooth 5.0 RF transceiver

Note the followings for external circuit design in each power supply mode of the Bluetooth 5.0 RF transceiver. User should select the power mode for Bluetooth 5.0 RF transceiver which DC-DC converter mode or Linear regulator mode.

When the DC-DC converter mode is selected, inductors on PCB are required. However, the BLE operating current reduction is conferred. On the other hand, When the Linear regulator mode is selected, BLE operating current increases more than DC-DC converter mode. However, the BoM cost and Board area can be reduced because mounting inductors for DC-DC converter mode is unnecessary.

2.4.1 DC-DC converter mode

Note the followings in external circuit design for the DC-DC converter mode.

- Design the signal pattern from “DCLOUT” pin to “VSS_RF” through an inductor “L1” and a capacitor “C1” shorter and wider for low impedance connection. Place ground pattern in area which is enclosed with line connecting “DCLOUT” and “DCLIN_A”, as shown in "Figure 2-8 Example of the PCB pattern for DC-DC converter mode". In addition, connect a capacitor “C1” and “VSS_RF” to this ground pattern.
- Connect the line connecting “DCLOUT” and “DCLIN_A” on parts surface of the board through no the via.
- Reduce loop area which is enclosed with line connecting “DCLOUT” and “DCLIN_A” as small as possible.
- Placing the inductor “L1” and capacitor as close as possible to the “DCLOUT” pin is recommended.
- Not place other SMD parts except the external circuit for DC-DC converter mode, on the loop which is enclosed with line connecting “DCLOUT” and “DCLIN_A”.
- Ensure a return path in layer2 (additional layer3 if possible) from ground in the loop to "Exposed Die Pad (VSS_RF)”, as shown in "Figure 2-8 Example of the PCB pattern for DC-DC converter mode".
- Recommended electrical characteristics of “L1” is follows;
  - Inductance=10uH +/-20%
  - Rated current (min)=90mA
  - DC resistance(max)=1.0ohm
  - Self resonant frequency(min)= 30MHz.
  - Less power loss and good DC superimposing
- “C2” capacitance should be less than or equal to 2.2uF +/-20%.
- Not place any analog signal, power, and ground lines except the external circuit for DC-DC converter mode, on and below the circuit area.
- With mounting an inductor “L2”, noise caused by the DC-DC converter can be reduced. Therefore, it is recommended to prepare inductor L2 mount space on a board pattern.

Figure 2-7 shows an example of the external circuit for DC-DC converter mode, Figure 2-8 shows an example of the PCB pattern.

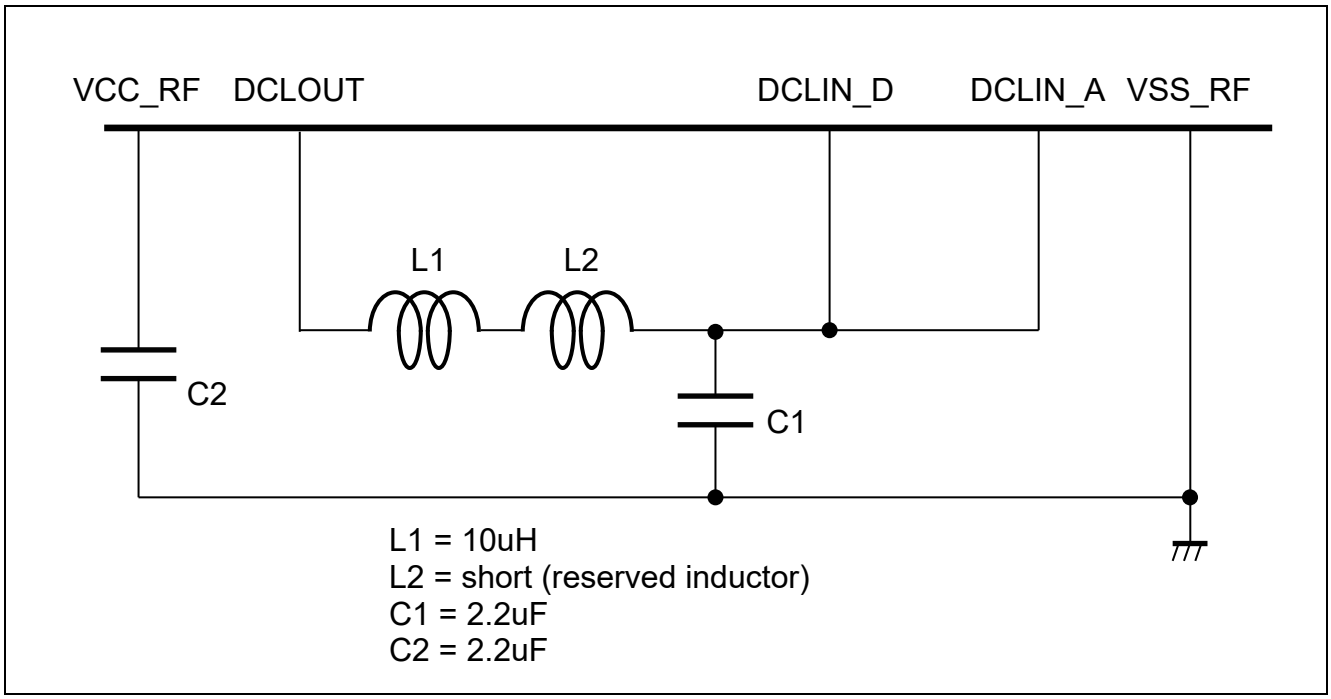


Figure 2-7 Example of the external circuit for DC-DC converter mode

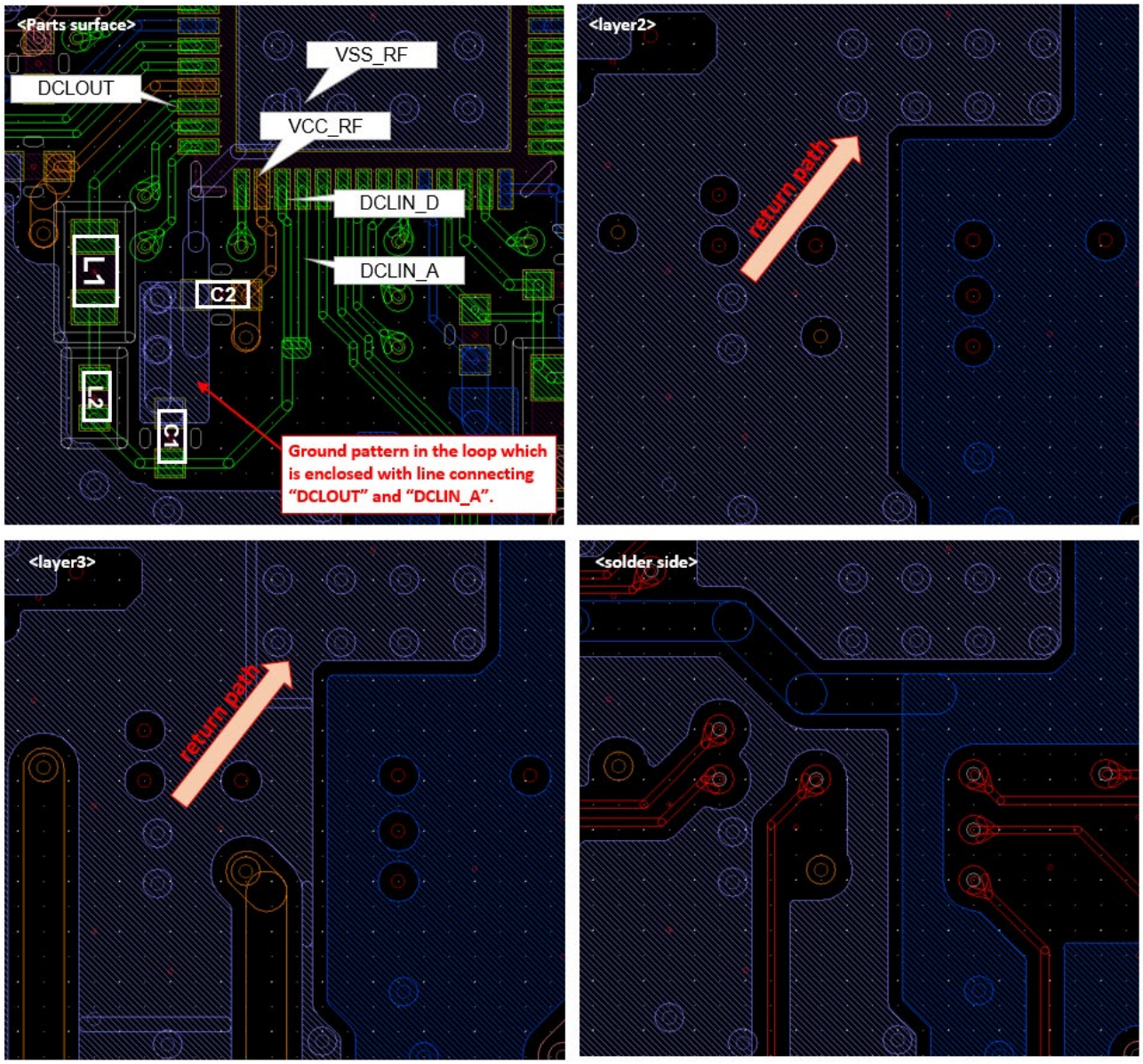


Figure 2-8 Example of the PCB pattern for DC-DC converter mode

2.4.2 Linear regulator mode

Note the followings in external circuit design for the Linear regulator mode.

- Make the signal pattern from “DCLOUT” pin to “VSS_RF” through “C1” shorter and wider for low impedance connection. Place ground pattern in area which is enclosed with line connecting “DCLOUT” and “DCLIN_A”, as shown in "Figure 2-10 Example of the PCB pattern for Linear regulator mode". In addition, connect a capacitor “C1” and “VSS_RF” to this ground pattern.
- Connect the line connecting “DCLOUT” and “DCLIN_A” on parts surface of the board through no the via.
- Reduce loop area which is enclosed with line connecting “DCLOUT” and “DCLIN_A” as small as possible.
- Not place other SMD parts except the external circuit for Linear regulator mode, on the loop which is enclosed with line connecting “DCLOUT” and “DCLIN_A”.
- Ensure a return path in layer2 (additional layer3 if possible) from ground in the loop to "Exposed Die Pad (VSS_RF)”, as shown in "Figure 2-10 Example of the PCB pattern for Linear regulator mode".
- Not place any analog signal, power, and ground lines except the external circuit for Linear regulator, on and below the circuit area.
- “C2” capacitance should be less than or equal to 0.47uF +/-20%.

Figure 2-9 shows an example of the external circuit for Linear regulator mode, Figure 2-10 shows an example of the PCB pattern.

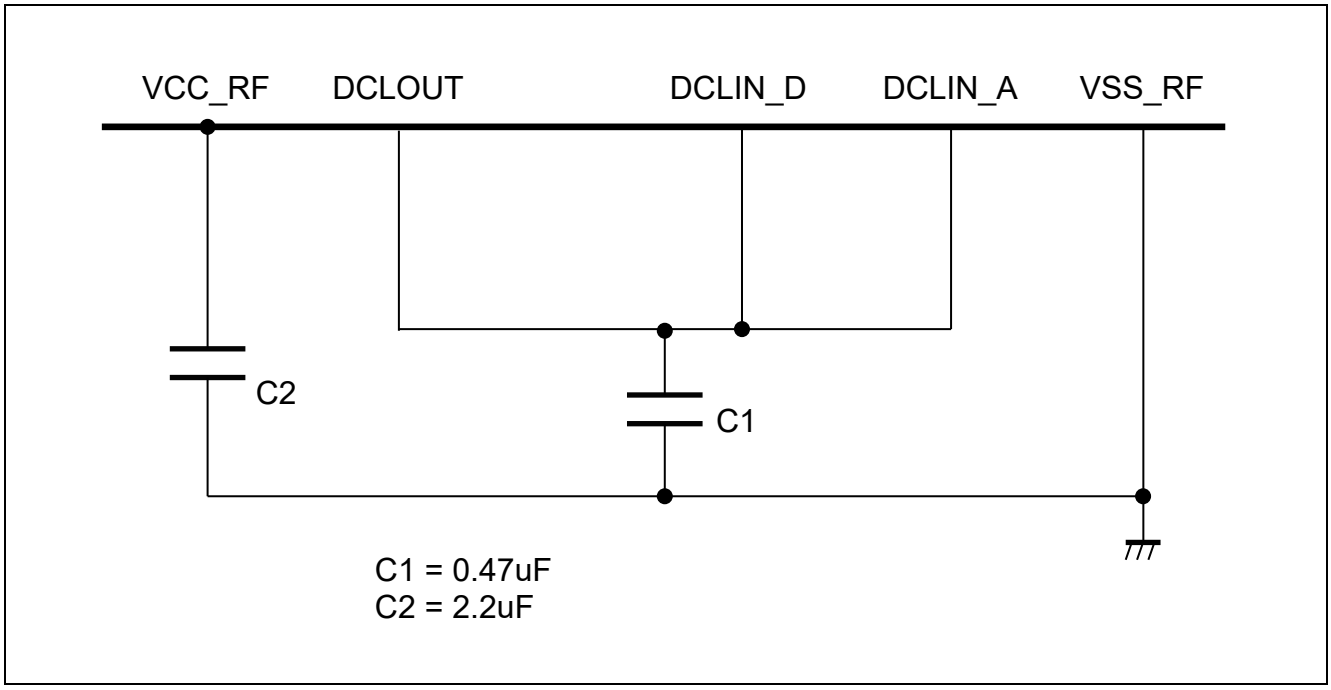


Figure 2-9 Example of the external circuit for Linear regulator mode

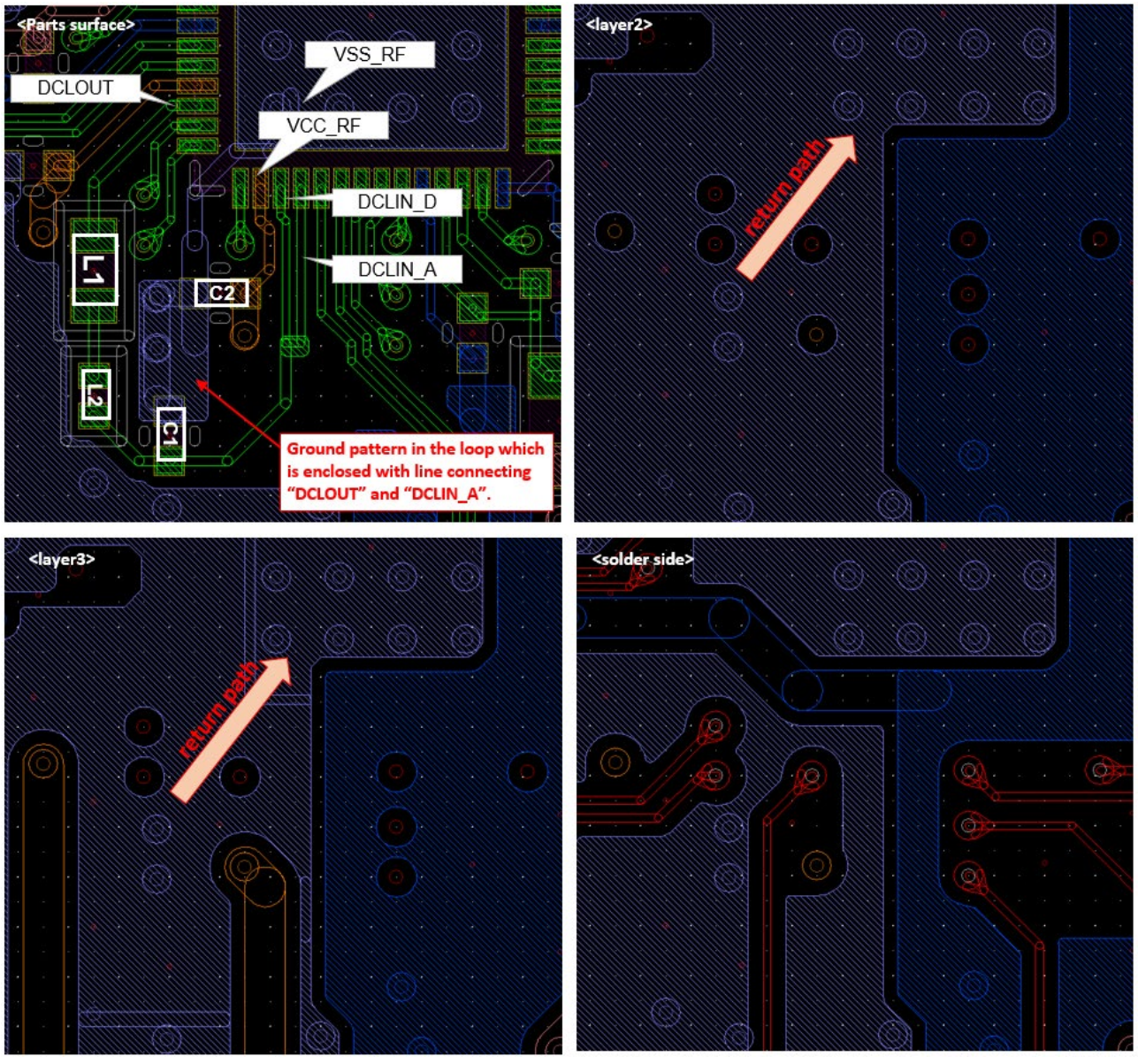


Figure 2-10 Example of the PCB pattern for Linear regulator mode

2.5 Power supply and ground patterns

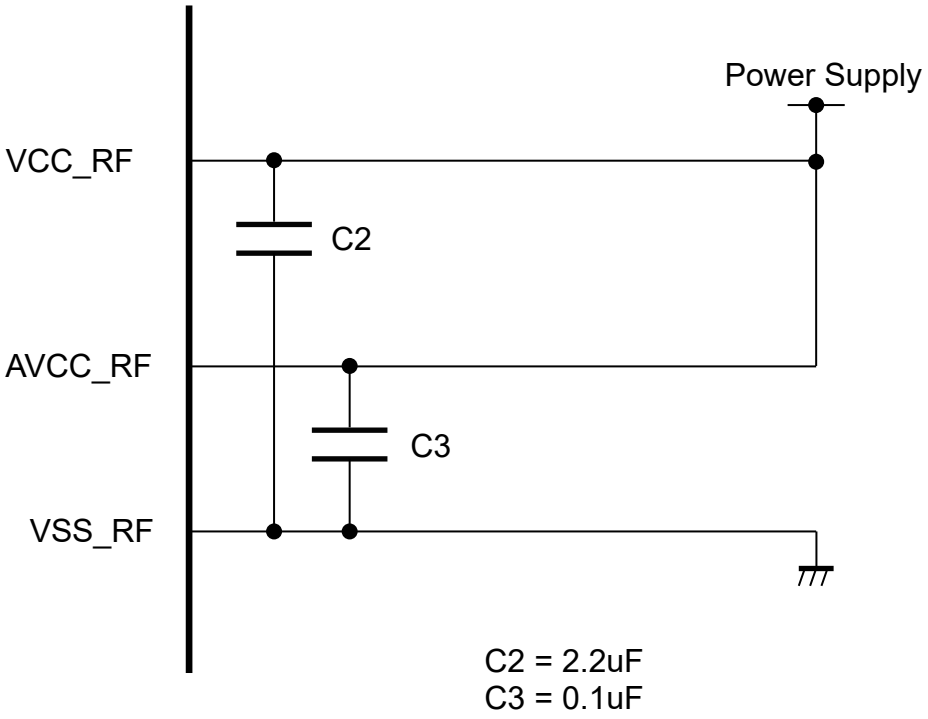
Note the followings for power supply patterns and ground patterns design.

2.5.1 Power supply

Note the followings for power supply patterns design.

- Not bring other power, and ground lines close up “AVCC_RF” and “VCC_RF” to avoid noise couplings.
- Connect power supply patterns “VCC_RF”, “AVCC_RF”, and other power supply “VCC” with single point short. And separate power supply patterns “VCC_RF”, “AVCC_RF”, and “VCC” each other.
- Make the power supply patterns of “VCC_RF” and “AVCC_RF” low impedance.
- Place bypass capacitors of “VCC_RF” and “AVCC_RF” nearby IC pin.
- Not place one or more vias on a connection between a bypass capacitor and “VCC_RF” or “AVCC_RF” pin.

Figure 2-11 shows an example of how to place the bypass capacitors.



Note: Noise varies depending on the board mounting. Add bypass capacitors as required.

Figure 2-11 Example of bypass capacitor connection

2.5.2 Ground

Note the followings for ground patterns design.

- Design a ground pattern to be as wide plane as possible.
- When using ground pattern as the shield line, place away from the oscillation circuit and the digital circuit as much as possible not to give noise the shield line.
- Back pad of IC Package (Exposed Die Pad) is a Bluetooth 5.0 RF transceiver reference ground. Not pass other power, and ground lines through the reference ground to avoid noise effects. And not separate the reference ground pattern.
- Under layer of IC Package should be “VSS_RF” solid ground. Make the ground patterns of “VSS_RF” low impedance. It is recommended to place vias as shown in "Figure 2-12 Example of the ground pattern".
- Not bring other power and ground lines close up “VSS_RF” to avoid noise couplings.
- When connecting the ground pattern to other layer of same potential, the connection should be low impedance with many vias.
- Connect “VSS_RF” and other grounds which are “VSS”, “AVSS0”, and “VSS_USB”, with single point short.
- Separate “ICGND” pin and "Exposed Die Pad (VSS_RF)” on the surface layer of the board.

Figure 2-12 shows an example of the ground pattern.

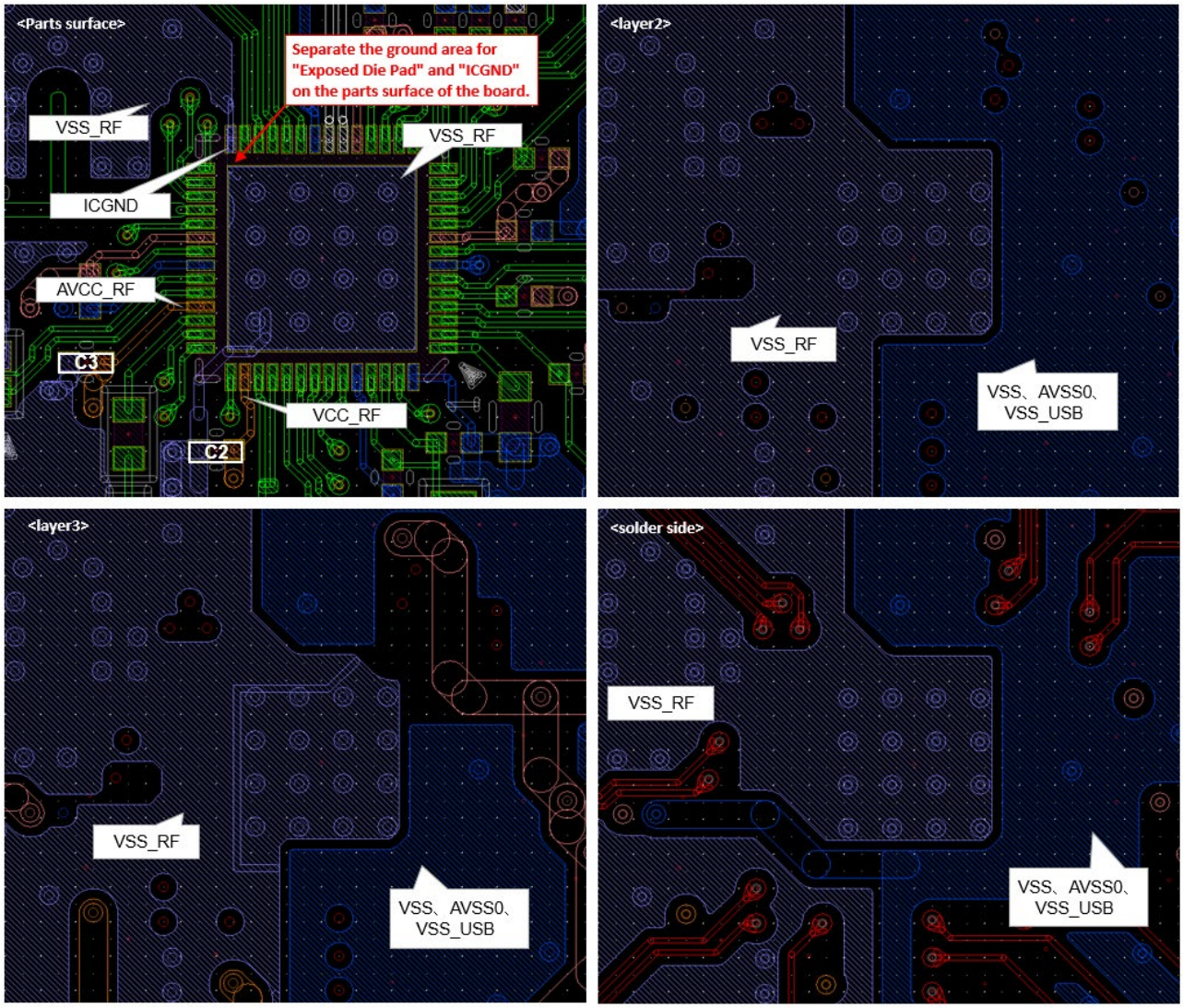


Figure 2-12 Example of the ground pattern

2.6 Circuit diagram for reference

Figure 2-13 shows a reference circuit diagram in which the Bluetooth 5.0 RF transceiver related part is only described.

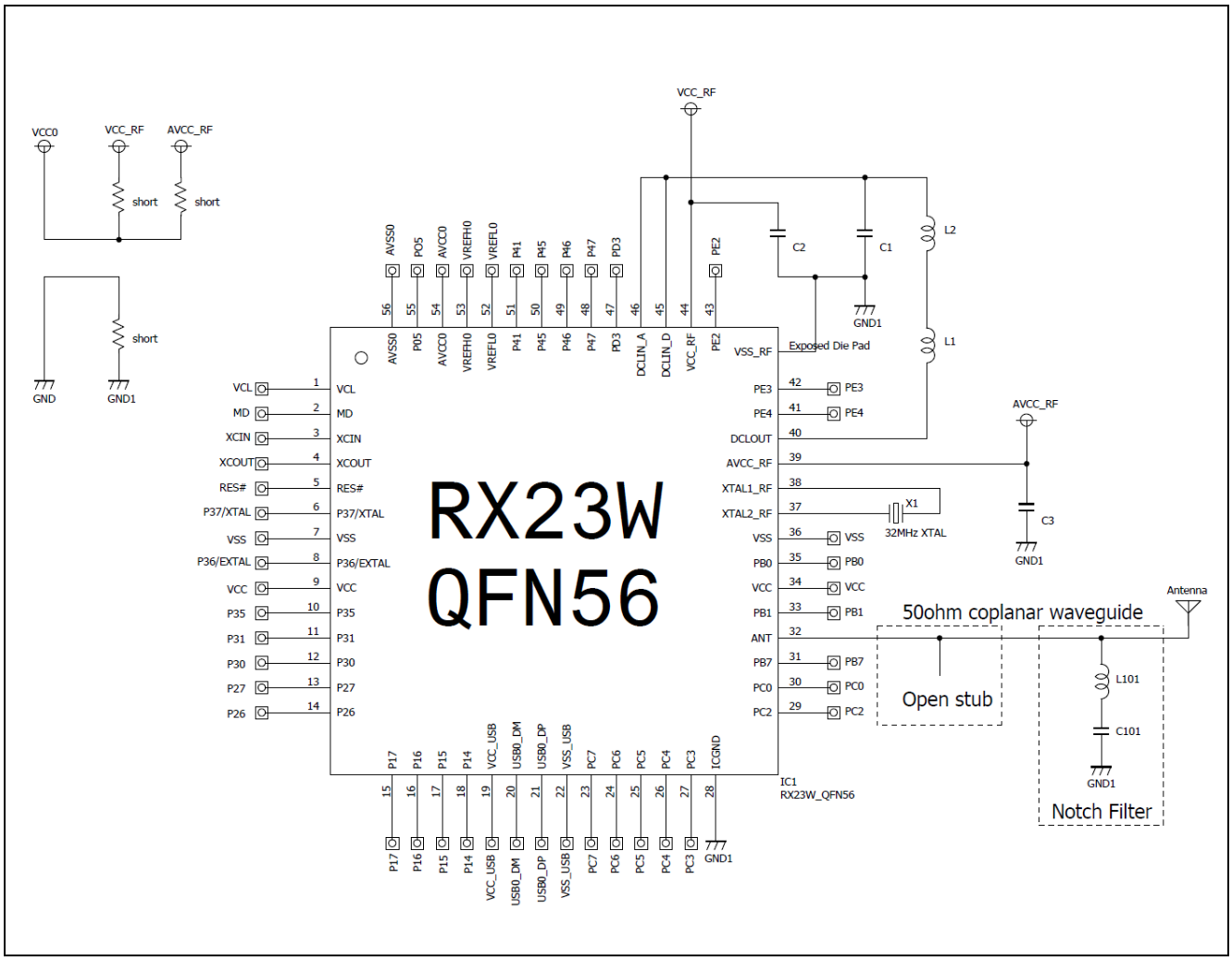


Figure 2-13 Circuit diagram (for reference)

2.7 Parts list for reference

Table 2-3 lists the parts.

Table 2-3 Parts list (for reference)

No.	Mount Parts Reference	Size code (mm)	Type	Value	Parts number	Manufacturer
1	IC1		RX23W QFN chip			Renesas
2	X1	1612	Crystal	32.00MHz	CX1612DB32000A0WPNC1	Kyocera
3	L1	1608	Inductor for decoupling circuits (*1)	10uH	MLZ1608M100WT000 (*1)	TDK
			Short pattern (*2)	–	–	–
4	L2	1005	Reserved inductor (*1)	–	–	–
			Short pattern (*2)	–	–	–
5	C1	1005	Chip ceramic capacitor	2.2uF (*1)	GRM155R61A225KE95 (*1)	Murata
				470nF (*2)	GRM155B30J474KE18(*2)	Murata
6	C2	1005	Chip ceramic capacitor	2.2uF	GRM155R61A225KE95	Murata
7	C3	1005	Chip ceramic capacitor	0.1uF	GRM155R61E104KA87D	Murata
8	L101	1005	Multilayer type RF inductor	7.5nH (*3)	LQG15HS7N5J02	Murata
9	C101	1005	Chip ceramic capacitor	0.5pF (*3)	GCM1555C1HR50BA16	Murata

Notes: *1. DC-DC converter mode
*2. Linear regulator mode
*3. notch filter used

3. Board design guidelines for RX23W BGA

3.1 RX23W BGA Pin list

Table 3-1 is the description of Bluetooth 5.0 RF transceiver unit pins in RX23W BGA.

Table 3-1 Description of Bluetooth 5.0 RF transceiver unit pins in RX23W BGA

Pin Number	Pin Name	I/O	Functions
F10	CLKOUT_RF	Output	Bluetooth-Dedicated clock output pin, whose frequency can be set to 4, 2, or 1MHz. The default output setting is off. Connecting the clock output pin to the external clock input pin of MCU, the RF clock can be used as the MCU system clock.
K2	ANT	In/Out	RF single I/O pin for RF transceiver. Adjust the characteristic impedance of the signal line to 50ohm.
K7	XTAL1_RF	Input	Pins for connecting the Bluetooth-dedicated clock oscillator. 32-MHz oscillator connection pin
K6	XTAL2_RF	Output	Pins for connecting the Bluetooth-dedicated clock oscillator. 32-MHz oscillator connection pin
K9	DCLOUT	Output	RF transceiver power-supply (DC-DC converter or linear regulator) output pin
G10	DCLIN_A	Input	RF transceiver power-supply output connection pin. This pin should be connected to an external inductor and capacitor when the DC-DC converter mode is selected. When the linear regulator mode is selected, this pin should be connected to an external capacitor.
H10	DCLIN_D	Input	RF transceiver power-supply output connection pin. This pin should be connected to an external inductor and capacitor when the DC-DC converter mode is selected. When the linear regulator mode is selected, this pin should be connected to an external capacitor.
J10	VCC_RF	Input	RF transceiver power supply pin
K8	AVCC_RF	Input	RF transceiver power supply pin
K1	ICGND (VSS_RF)	Input	RF transceiver ground pin In this document, this pin is called “ICGND”.
D4,E3,F3,F8, G3,G8,H3,H5, H6,H7,J2,J7,K 3 and K10	VSS_RF	Input	RF transceiver ground pin

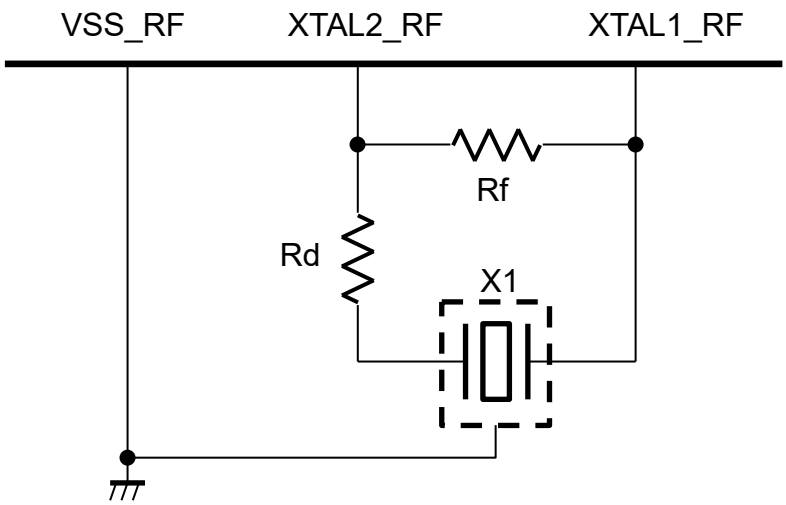
3.2 Oscillator circuit for Bluetooth-dedicated clock

Note the following when designing an oscillator circuit for Bluetooth-dedicated clock.

- Place the crystal resonator close to the “XTAL1_RF” and “XTAL2_RF” pins. We recommend the wiring length between the RX23W and the crystal resonator of approximately 7 mm, as shown in "Figure 3-2 Example of the pattern around the crystal resonator".
- Shield the pattern for the “XTAL1_RF” and “XTAL2_RF” pins with the ground pattern. Do not place the pattern for these signals in parallel with or across other patterns where a large current flows or the level changes frequently.
- Not place any signal, power, and ground lines except the oscillator circuit’s on and below the oscillator circuit area. We recommend that the ground pattern is placed in the layers under the oscillator circuit, as shown in "Figure 3-2 Example of the pattern around the crystal resonator".
- Separate the oscillator circuit and the signal line from an antenna to “ANT” pin by placing slit patterns on all layers.
- Ensure a return path in layer2 (additional layer3 if possible) from ground of the crystal resonator to "VSS_RF”, as shown in "Figure 3-2 Example of the pattern around the crystal resonator".
- External load capacitors (CL) for frequency tuning are unnecessary, because the capacitors are built in IC. For Tuning procedure of Bluetooth dedicated clock frequency, see the descriptions of the application note, the Hardware Design Guide(R01AN4762). The latest version can be downloaded from the Renesas Electronics website.
- Insert a damping resistor (Rd) as required. Set the resistance to the value recommended by the oscillator manufacturer as the value depends on the oscillator and its driving capability. If the oscillator manufacturer states that the addition of a feedback resistor (Rf) to the oscillator is required, insert Rf between XTAL1_RF and XTAL2_RF according to the instructions.
- When the frequency-divided clock for the Bluetooth-dedicated clock is output, note designing board pattern. The wiring length should be as short as possible. In addition, must not branch the wiring. And avoid using vias on the transmission line. A maximum of 2 is recommended.
- Shield the transmission line of CLKOUT_RF with the "VSS" pattern to avoid noise couplings to “VSS_RF”.

Note: Bluetooth 5.0 RF transceiver clock frequency accuracy which includes initial error, temperature drift, and ageing effect should be less than or equal to +/-50ppm in the Bluetooth specification. Therefore, the frequency error should be as less as possible.

Figure 3-1 shows an example of the crystal resonator connection. Figure 3-2 shows an example of the pattern around the crystal resonator.



Note: The resistance of Rd and Rf should be determined thorough oscillation characteristics evaluation with a crystal resonator to be mounted. These resistors might not be required, depending on the oscillation characteristics.

Figure 3-1 Example of the crystal resonator connection.

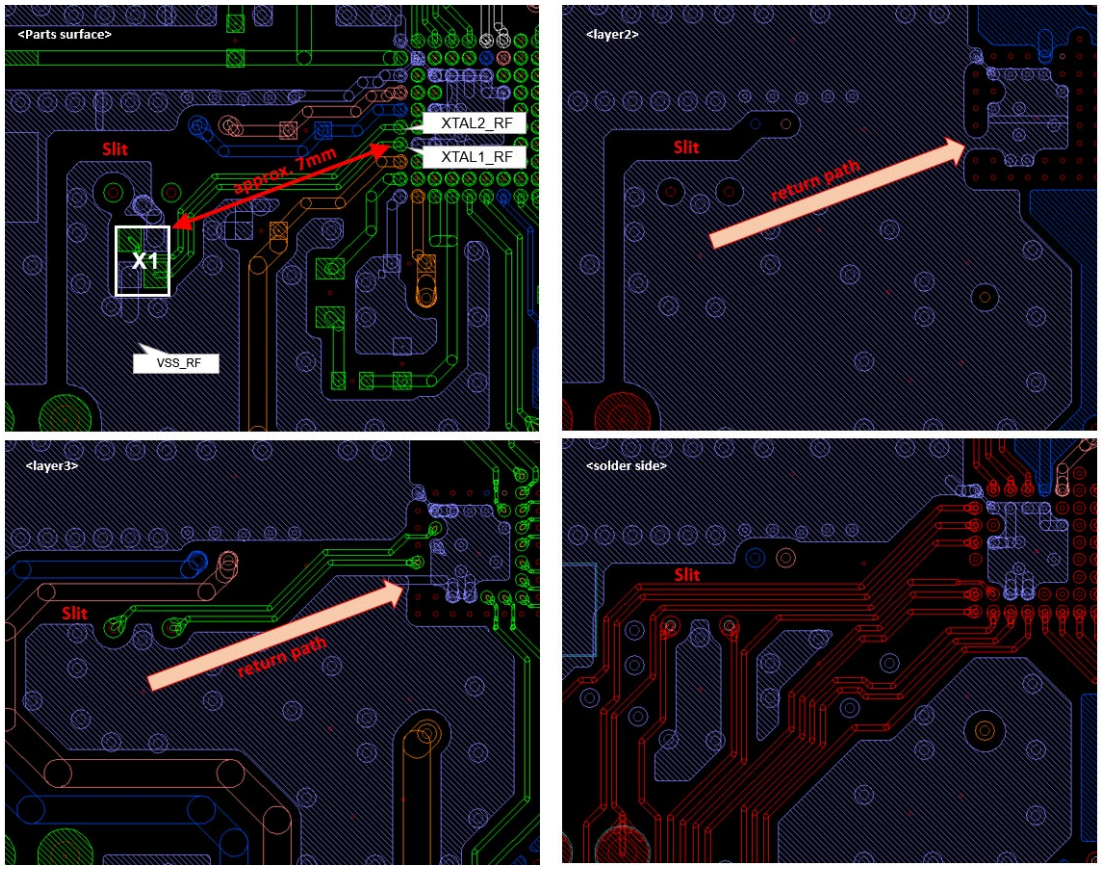


Figure 3-2 Example of the pattern around the crystal resonator

Table 3-2 shows confirmed operation crystal resonator list (reference).

Table 3-2 Tested crystal resonator list (reference)

Manufacturer	Parts number	SMD/Lead size code (in mm)	Frequency (MHz)	Frequency Tolerance (ppm)	Frequency Stability (ppm)	Equivalent Series Resistance (ohm)	Load Capacitance (pF)
NDK	NX1612SA-32.000MHZ-CHP-CIS-3	1612	32.00	+/-10	+/-20	Max 100	6
NDK	NX1210AB- 32.000MHZ-CHP-CIX-3	1210	32.00	Total +/-30		Max 100	6
Kyocera	CX1612DB32000 A0WPNC1	1612	32.00	Total +/-25		Max 100	5
Kyocera	CX1210SB32000 B0GPJC1	1210	32.00	Total +/-30		Max 80	6
Murata	XRCMD32M000FZQ52R0	1612	32.00	Total +/-30		Max 60	6
Murata	XRCTD32M000N1P00R0	1210	32.00	Total +/-30		Max 120	6

3.3 Antenna connection pin

Note the followings for antenna connection pin design.

- Adjust the characteristic impedance of 50ohm for the signal line from an antenna to “ANT” pin. Optimize the width of signal line and the gap between signal line and ground pattern, considering the PCB permittivity and layer thickness. Depending on the antenna used, additional parts such as inductors or capacitors may be required. In the "Figure 3-3 Example of the pattern around “ANT” pin", the coplanar waveguide is used.
- When mounting a connector, keep the characteristic impedance of 50ohm including the connector.
- The directly under layer of the coplanar waveguide should be solid ground, having no crossing with any signal, power, and other ground lines.
- Place vias as many as possible between the coplanar waveguide ground pattern and the solid ground. We recommend that the via spacing should be approximately 0.9mm, as shown in "Figure 3-3 Example of the pattern around “ANT” pin".

Figure 3-3 shows an example of the pattern around “ANT” pin.

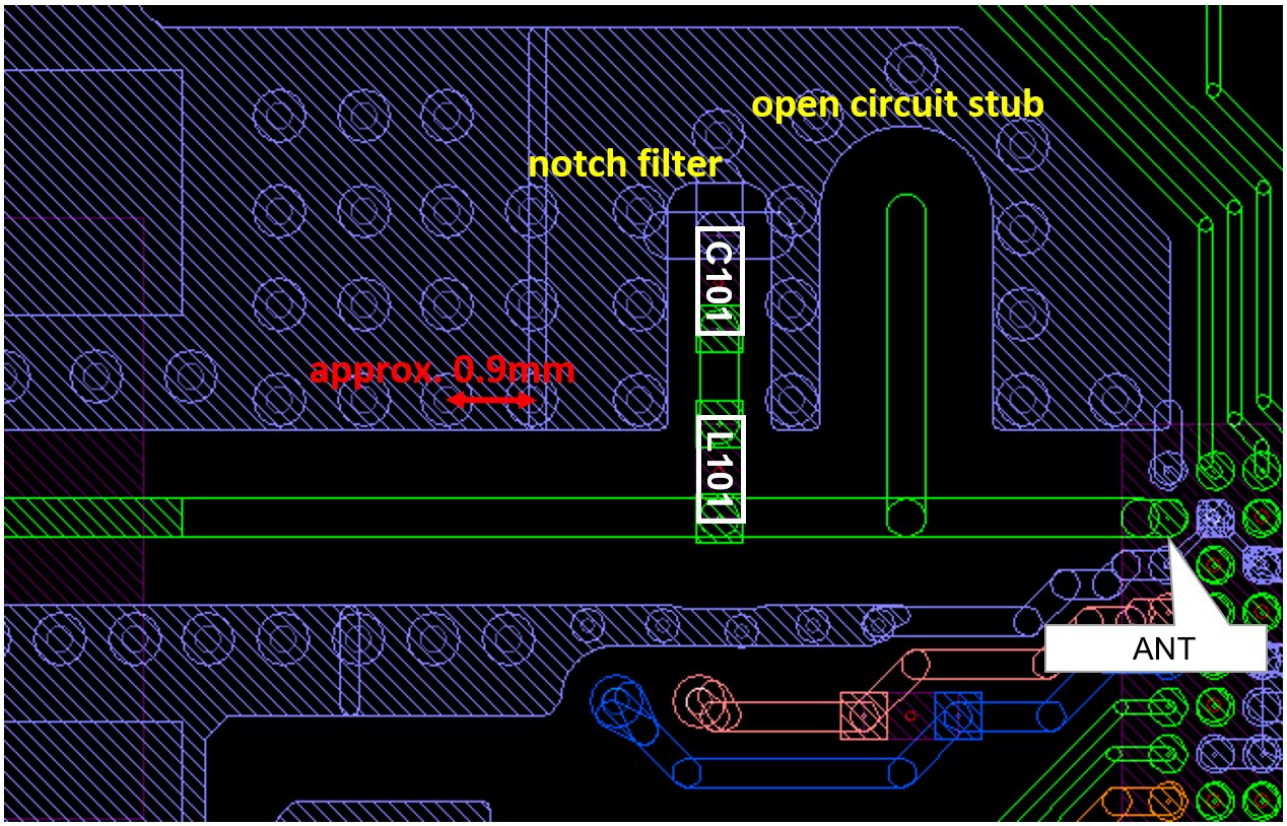


Figure 3-3 Example of the pattern around “ANT” pin

- Pay attention to an emission level of 5th order harmonics, when selecting 4 dBm transmitted output mode and evaluating of US(FCC) regulatory with a coaxial cable. The emission should be suppressed with an RF filter implementation.

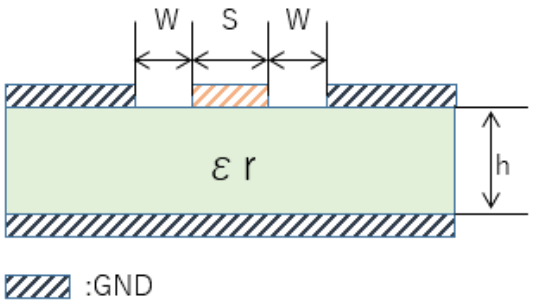
  RF filter requirements
  Frequency band to be suppressed: 12.01 to 12.4 GHz
  Minimum attenuation: 8dB

- Pay attention to an emission level of 3rd order harmonics, when selecting 0 dBm transmitted output mode and evaluating of US(FCC) regulatory with a coaxial cable. The emission should be suppressed with an RF filter implementation.

  RF filter requirements
  Frequency band to be suppressed: 7250 to 7440 MHz
  Minimum attenuation: 2dB

This document describes an example of an open circuit stub and an example of LPF using SMD parts. Both of these circuits can suppress 5th order harmonics of 4 dBm transmitted output mode and the 3rd order harmonics of 0 dBm transmitted output mode.

Figure 3-4 shows an example of the open circuit stub.



Permittivity(ε_r)=4.45
S=0.41mm
W=0.72mm
h=0.2mm
Frequency=12400MHz (2480MHz x 5)

Obtain an effective permittivity $\varepsilon_{r,eff}$ from the above board composition.
effective permittivity $\varepsilon_{r,eff} \fallingdotseq 3.515$

The wavelength of 12400MHz is approximately 24.18 mm. Then calculate the length of a stub by using the formula below.
the length of a stub $L = 0.25*\lambda / (\varepsilon_{r,eff})^{0.5} = 3.224$mm

Note: Place the open circuit stub as close to “ANT” pin as possible. We recommend that it should place approximately 2.5mm, as shown in example pattern on the right figure.

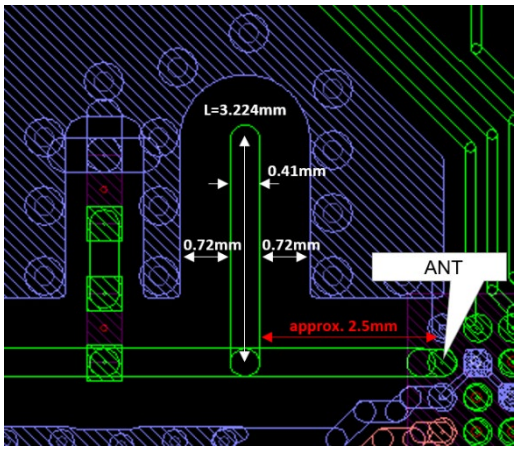


Figure 3-4 Example of the open circuit stub

Note: The pattern width and pattern pitch for impedance control vary depending on board thickness, material, and layer configuration. Contact the board manufacturer for more information.

Figure 3-5 shows an example of LPF using SMD parts

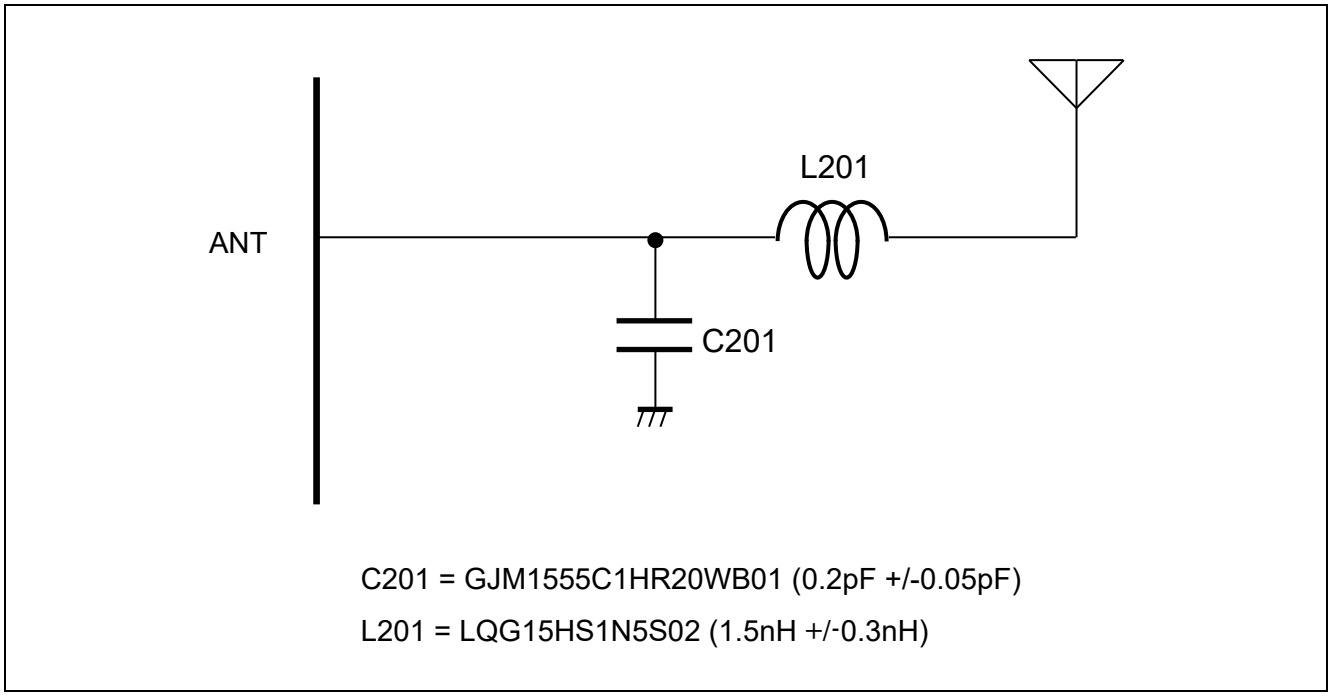


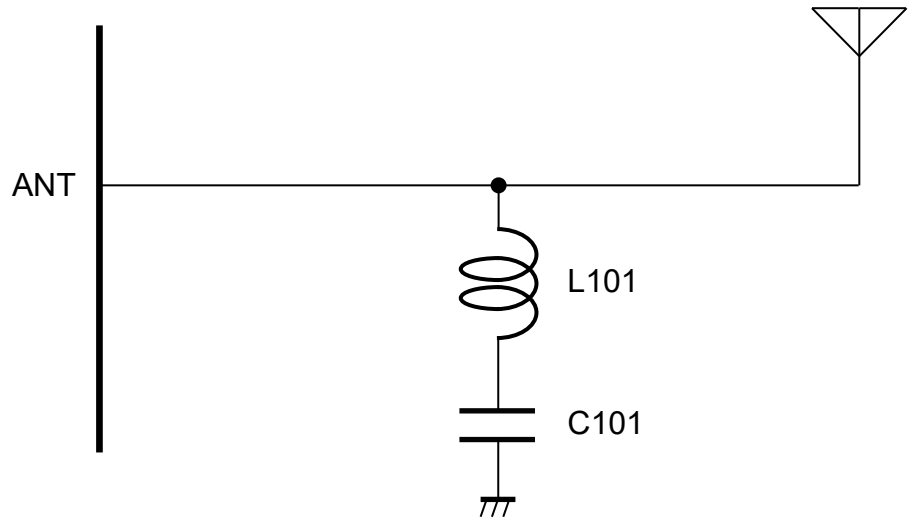
Figure 3-5 Example of LPF using SMD parts

Note: Depending on the PCB design, the value may differ. Adjust the value, if necessary.

- When certifying of Korea (KCC) regulatory, an emission of 1.9GHz frequency band should be suppressed with an RF filter implementation.

  RF filter requirements
  Frequency band to be suppressed: 1921 to 1984 MHz
  Minimum attenuation: 7dB

This document describes an example of a notch filter. Figure 3-6 shows an example of the notch filter.



L101 = LQG15HS7N5J02 (7.5nH +/-5%)
C101 = GCM1555C1HR50BA16 (0.5pF +/-0.1pF)

RF filter requirements
Frequency band to be suppressed : 1921 to 1984 MHz
Minimum attenuation : 7dB

Note: Depending on the PCB design, the value of capacitor C101 may differ.
Adjust the value of capacitor C101, if necessary.

Figure 3-6 Example of the notch filter

3.4 Power supply mode for Bluetooth 5.0 RF transceiver

Note the followings for external circuit design in each power supply mode of the Bluetooth 5.0 RF transceiver. User should select the power mode for Bluetooth 5.0 RF transceiver which DC-DC converter mode or Linear regulator mode.

When the DC-DC converter mode is selected, inductors on PCB are required. However, the BLE operating current reduction is conferred. On the other hand, When the Linear regulator mode is selected, BLE operating current increases more than DC-DC converter mode. However, the BoM cost and Board area can be reduced because mounting inductors for DC-DC converter mode is unnecessary.

3.4.1 DC-DC converter mode

Note the followings in external circuit design for the DC-DC converter mode.

- Design the signal pattern from “DCLOUT” pin to “VSS_RF” through an inductor “L1” and a capacitor “C1” shorter and wider for low impedance connection. Place ground pattern in area which is enclosed with line connecting “DCLOUT” and “DCLIN_A”, as shown in "Figure 3-8 Example of the PCB pattern for DC-DC converter mode". In addition, connect a capacitor “C1” and “VSS_RF” to this ground pattern.
- Connect the line connecting “DCLOUT” and “DCLIN_A” on parts surface of the board through no the via.
- Reduce loop area which is enclosed with line connecting “DCLOUT” and “DCLIN_A” as small as possible.
- Placing the inductor “L1” and capacitor as close as possible to the “DCLOUT” pin is recommended.
- Not place other SMD parts except the external circuit for DC-DC converter mode, on the loop which is enclosed with line connecting “DCLOUT” and “DCLIN_A”.
- Ensure a return path in layer2 (additional layer3 if possible) from ground in the loop to "VSS_RF”, as shown in "Figure 3-8 Example of the PCB pattern for DC-DC converter mode".
- Recommended electrical characteristics of “L1” is follows;
  - Inductance=10uH +/-20%
  - Rated current (min)=90mA
  - DC resistance(max)=1.0ohm
  - Self resonant frequency(min)= 30MHz.
  - Less power loss and good DC superimposing
- “C2” capacitance should be less than or equal to 2.2uF +/-20%.
- Not place any analog signal, power, and ground lines except the external circuit for DC-DC converter mode, on and below the circuit area.
- Recommended electrical characteristics of “L2” is follows;
  - Inductance=4.7nH +/-0.3nH
  - Rated current (min)=500mA
  - DC resistance(max)=0.2ohm
  - Self resonant frequency(min)= 6GHz

    With mounting an inductor “L2”, the noise level of higher harmonics due to switching can be reduced.

Figure 3-7 shows an example of the external circuit for DC-DC converter mode, Figure 3-8 shows an example of the PCB pattern.

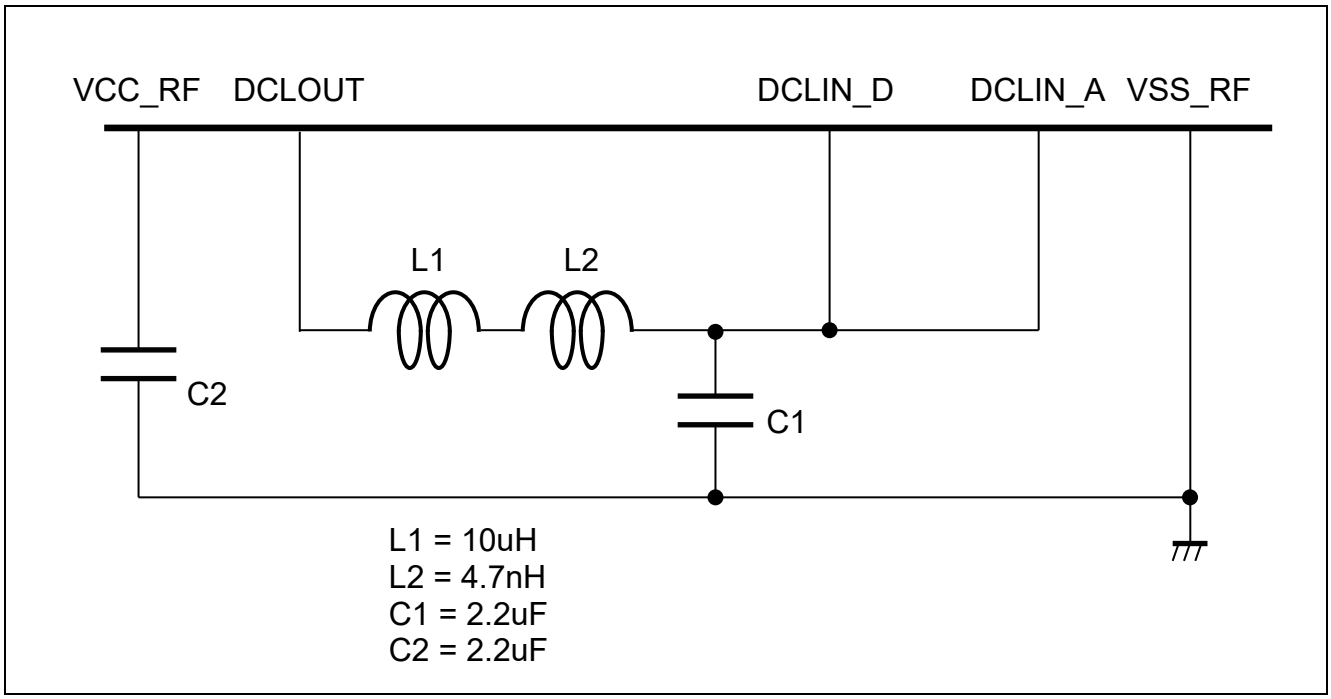


Figure 3-7 Example of the external circuit for DC-DC converter mode

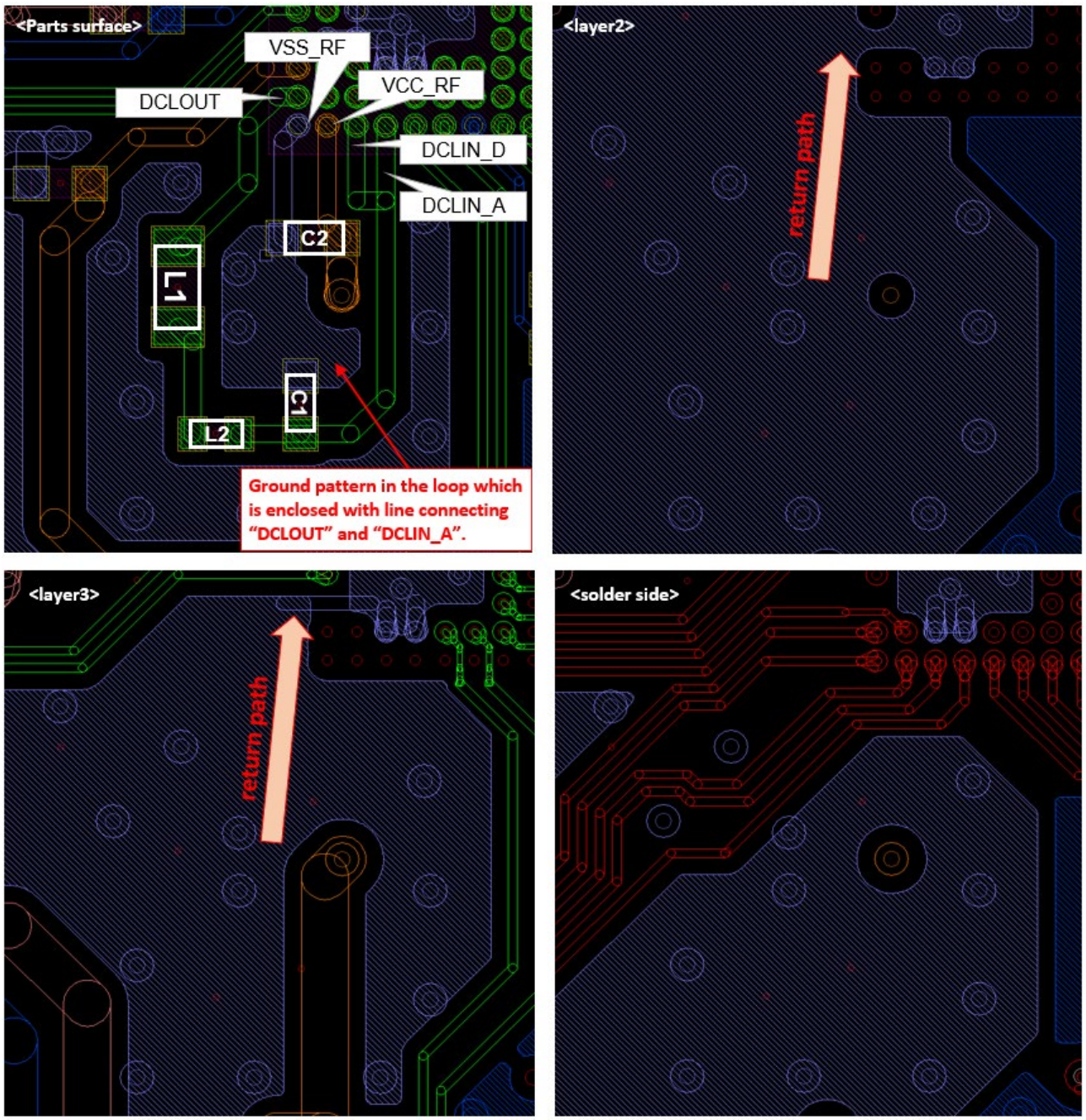


Figure 3-8 Example of the PCB pattern for DC-DC converter mode

3.4.2 Linear regulator mode

Note the followings in external circuit design for the Linear regulator mode.

- Make the signal pattern from “DCLOUT” pin to “VSS_RF” through “C1” shorter and wider for low impedance connection. Place ground pattern in area which is enclosed with line connecting “DCLOUT” and “DCLIN_A”, as shown in "Figure 3-10 Example of the PCB pattern for Linear regulator mode". In addition, connect a capacitor “C1” and “VSS_RF” to this ground pattern.
- Connect the line connecting “DCLOUT” and “DCLIN_A” on parts surface of the board through no the via.
- Reduce loop area which is enclosed with line connecting “DCLOUT” and “DCLIN_A” as small as possible.
- Not place other SMD parts except the external circuit for Linear regulator mode, on the loop which is enclosed with line connecting “DCLOUT” and “DCLIN_A”.
- Ensure a return path in layer2 (additional layer3 if possible) from ground in the loop to "VSS_RF”, as shown in "Figure 3-10 Example of the PCB pattern for Linear regulator mode".
- Not place any analog signal, power, and ground lines except the external circuit for Linear regulator, on and below the circuit area.
- “C2” capacitance should be less than or equal to 0.47uF +/-20%.

Figure 3-9 shows an example of the external circuit for Linear regulator mode, Figure 3-10 shows an example of the PCB pattern.

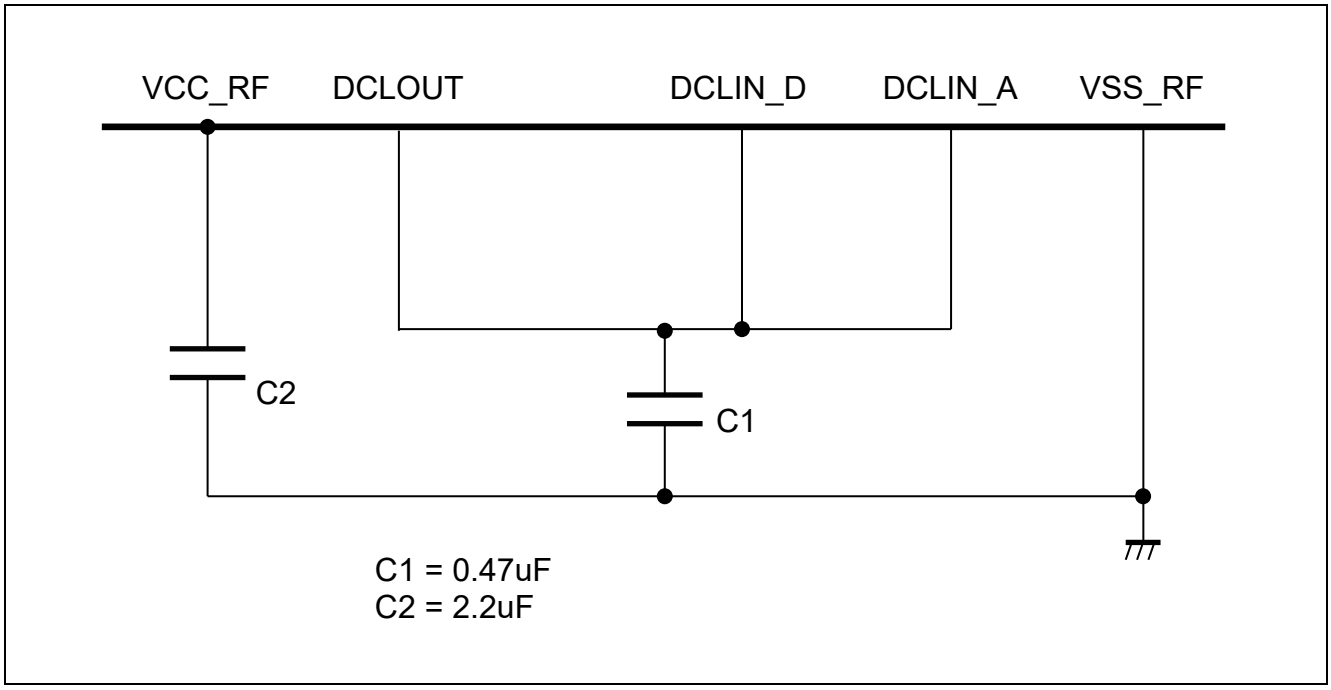


Figure 3-9 Example of the external circuit for Linear regulator mode

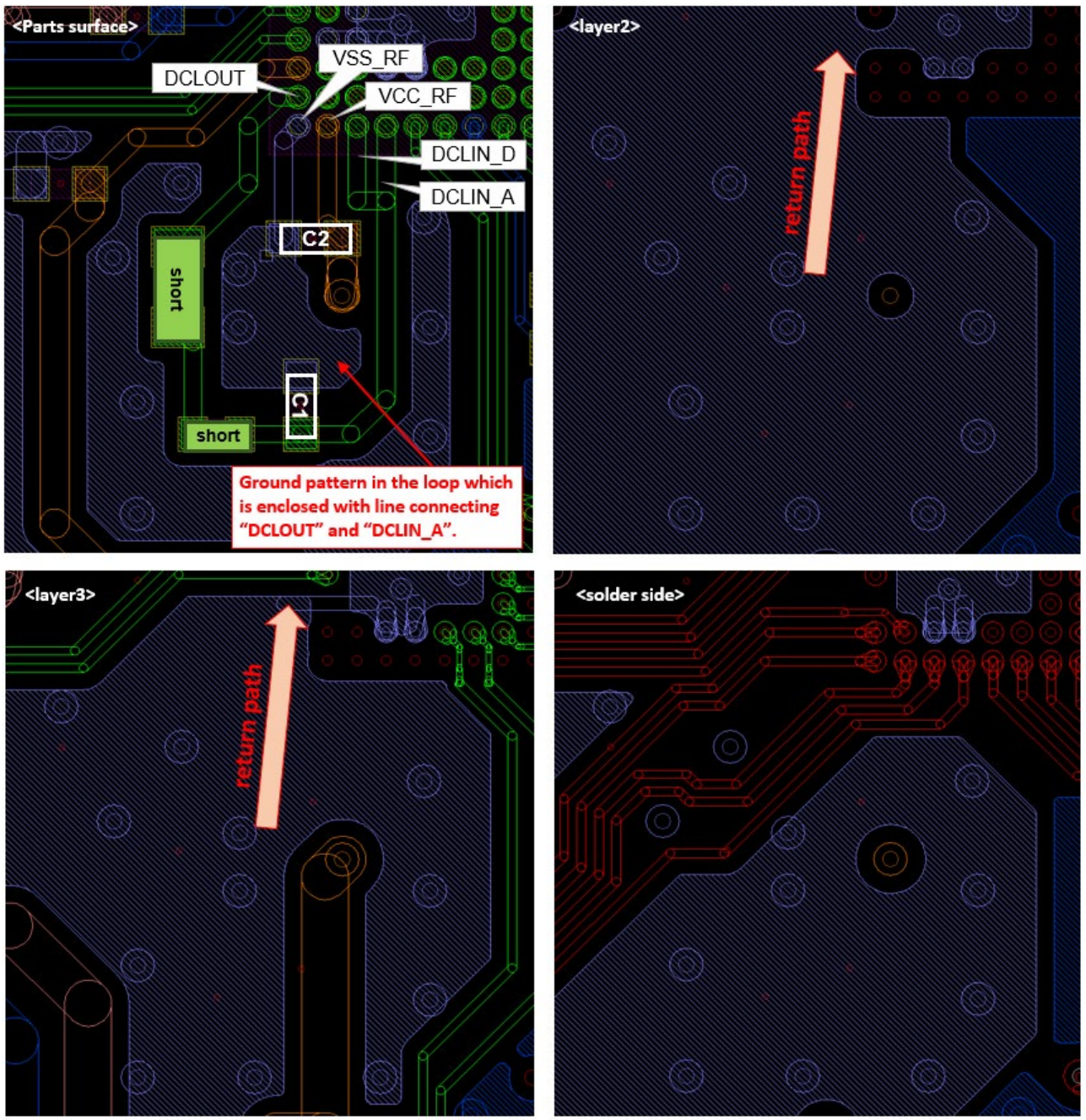


Figure 3-10 Example of the PCB pattern for Linear regulator mode

3.5 Power supply and ground patterns

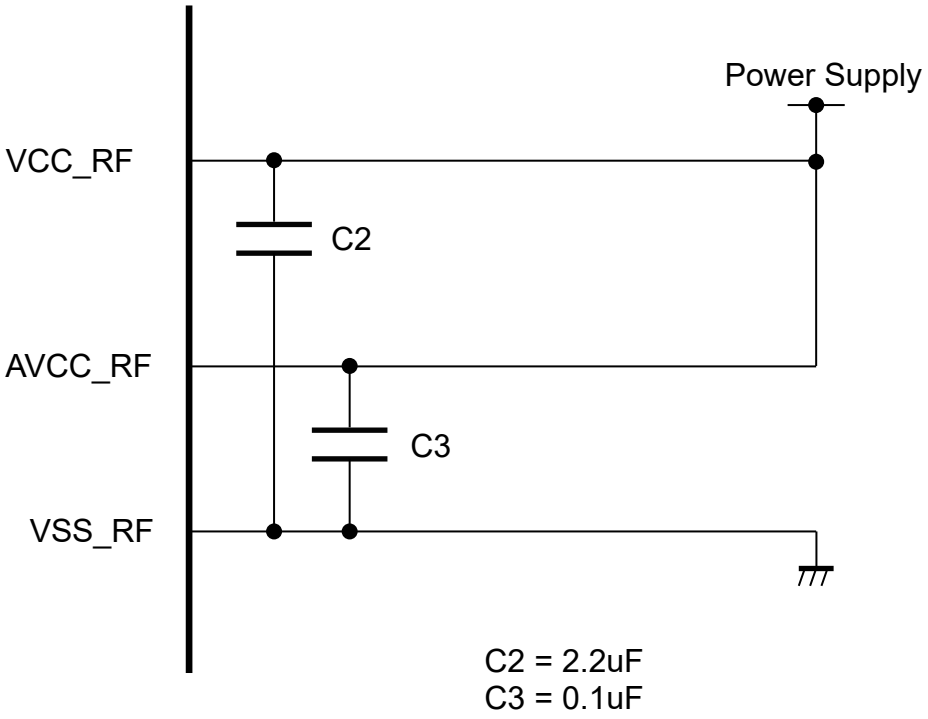
Note the followings for power supply patterns and ground patterns design.

3.5.1 Power supply

Note the followings for power supply patterns design.

- Not bring other power, and ground lines close up “AVCC_RF” and “VCC_RF” to avoid noise couplings.
- Connect power supply patterns “VCC_RF”, “AVCC_RF”, and other power supply “VCC” with single point short. And separate power supply patterns “VCC_RF”, “AVCC_RF”, and “VCC” each other.
- Make the power supply patterns of “VCC_RF” and “AVCC_RF” low impedance.
- Place bypass capacitors of “VCC_RF” and “AVCC_RF” nearby IC pin.
- Not place one or more vias on a connection between a bypass capacitor and “VCC_RF” or “AVCC_RF” pin.

Figure 3-11 shows an example of how to place the bypass capacitors.



Note: Noise varies depending on the board mounting. Add bypass capacitors as required.

Figure 3-11 Example of bypass capacitor connection

3.5.2 Ground

Note the followings for ground patterns design.

- Design a ground pattern to be as wide plane as possible.
- When using ground pattern as the shield line, place away from the oscillation circuit and the digital circuit as much as possible not to give noise the shield line.
- Under layer of IC Package should be “VSS_RF” solid ground. Make the ground patterns of “VSS_RF” low impedance. Not pass other power, and ground lines through the reference ground to avoid noise effects. And not separate the reference ground pattern. It is recommended to place vias as shown in "Figure 3-12 Example of the ground pattern".
- Not bring other power and ground lines close up “VSS_RF” to avoid noise couplings.
- When connecting the ground pattern to other layer of same potential, the connection should be low impedance with many vias.
- Connect “VSS_RF” and other grounds which are “VSS”, “AVSS0”, and “VSS_USB”, with single point short.
- Separate “ICGND” pin and " VSS_RF” on the surface layer of the board.

Figure 3-12 shows an example of the ground pattern.

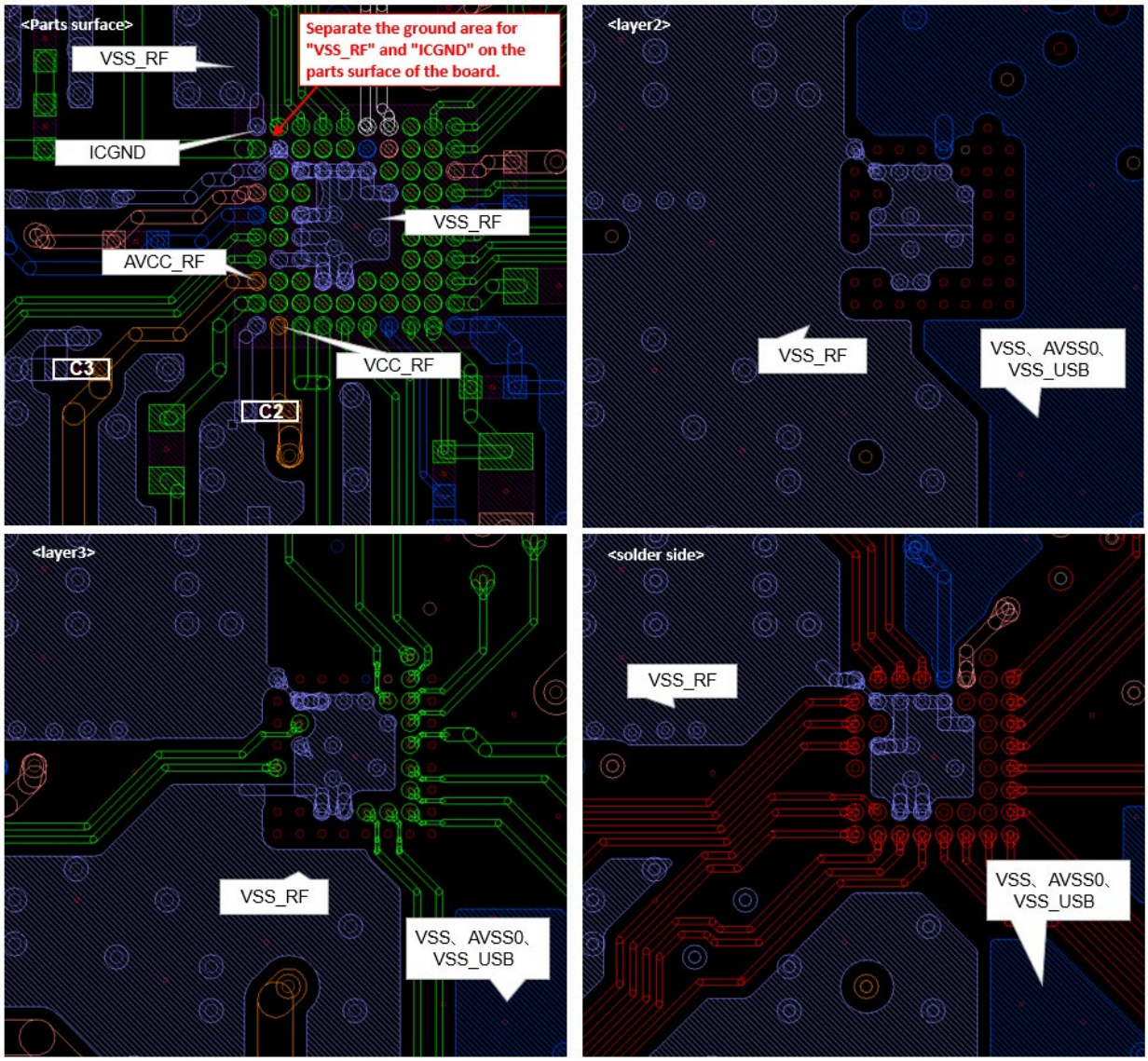


Figure 3-12 Example of the ground pattern

3.6 Circuit diagram for reference

Figure 3-13 shows a reference circuit diagram in which the Bluetooth 5.0 RF transceiver related part is only described.

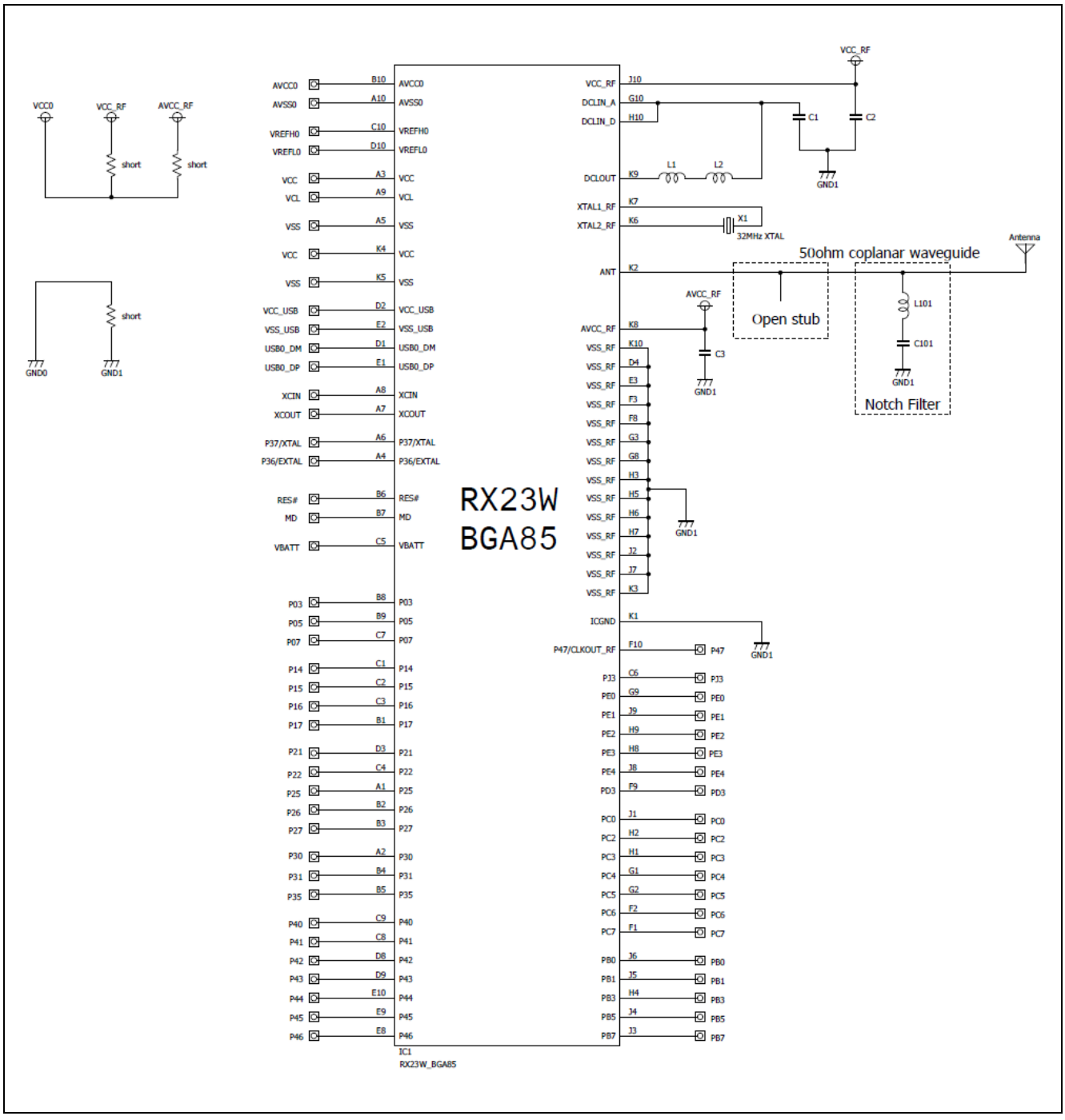


Figure 3-13 Circuit diagram (for reference)

3.7 Parts list for reference

Table 3-3 lists the parts.

Table 3-3 Parts list (for reference)

No.	Mount Parts Reference	Size code (mm)	Type	Value	Parts number	Manufacturer
1	IC1		RX23W BGA chip			Renesas
2	X1	1612	Crystal	32.00MHz	CX1612DB32000A0WPNC1	Kyocera
3	L1	1608	Inductor for decoupling circuits (*1)	10uH	MLZ1608M100WT000 (*1)	TDK
			Short pattern (*2)	–	–	–
4	L2	1005	Chip Inductor (*1)	4.7nH	LQG15HS4N7S02	Murata
			Short pattern (*2)	–	–	–
5	C1	1005	Chip ceramic capacitor	2.2uF (*1)	GRM155R61A225KE95 (*1)	Murata
				470nF (*2)	GRM155B30J474KE18(*2)	Murata
6	C2	1005	Chip ceramic capacitor	2.2uF	GRM155R61A225KE95	Murata
7	C3	1005	Chip ceramic capacitor	0.1uF	GRM155R61E104KA87D	Murata
8	L101	1005	Multilayer type RF inductor	7.5nH (*3)	LQG15HS7N5J02	Murata
9	C101	1005	Chip ceramic capacitor	0.5pF (*3)	GCM1555C1HR50BA16	Murata

Notes: *1. DC-DC converter mode
*2. Linear regulator mode
*3. notch filter used

4. Board design guidelines for RX23W LGA

The RX23W LGA is a module incorporating a crystal resonator for Bluetooth-dedicated clock and a small PCB trace antenna. We strongly recommend the use of four-layer or six-layer boards for the main board design.
The configuration examples of the actually manufactured board are shown below.

- Configuration example for four-layer boards

  Layer Configuration of the Board
  Parts surface:RX23W LGA, RF transceiver signals, bypass capacitors, and other signals
  Layer2:Ground plane
  Layer3:Power plane, signals except RF transceiver part
  Solder side: Signals except RF transceiver part

  Board material: FR4

  Dielectric constant εr: 4.3, dielectric loss tangent: 0.016

  Layer configuration of the board: 4 layers, total thickness of 1.6 mm

- Configuration example for six-layer boards

  Layer Configuration of the Board
  Parts surface:RX23W LGA, RF transceiver signals, bypass capacitors, and other signals
  Layer2:Ground plane
  Layer3:Power plane, signals except RF transceiver part
  Layer4:Signals except RF transceiver part
  Layer5:Ground plane, signals except RF transceiver part
  Solder side: Signals except RF transceiver part

  Board material: FR4

  Dielectric constant εr: 4.3, dielectric loss tangent: 0.018

  Layer configuration of the board: 6 layers, total thickness of 1.6 mm

In this section, the guidelines of the RF transceiver unit are shown based on the above layer configuration.

4.1 RX23W LGA Pin list

Table 4-1 is the description of Bluetooth 5.0 RF transceiver unit pins in RX23W LGA.
Figure 4-1 shows an example of connections for each pin.

Table 4-1 Description of Bluetooth 5.0 RF transceiver unit pins in RX23W LGA

Pin Number	Pin Name	I/O	Functions
24	CLKOUT_RF	Output	Bluetooth-Dedicated clock output pin, whose frequency can be set to 4, 2, or 1MHz. The default output setting is off. Connecting the clock output pin to the external clock input pin of MCU, the RF clock can be used as the MCU system clock.
10	ANT	In/Out	RF single I/O pin for RF transceiver. Adjust the characteristic impedance of the signal line to 50ohm.
11	INT_ANT	In/Out	This pin is used for input to and output from the internal antenna. It should be connected to "ANT" pin on the main board.
74	XTAL1_RF	Input	Pins for connecting the Bluetooth-dedicated clock oscillator. "XTAL1_RF" and "XTAL2_RF" pins should be connected on the main board.
75	XTAL2_RF	Output	
76	DCLOUT	Output	RF transceiver power-supply (linear regulator) output pin
77	DCLIN_D	Input	RF transceiver power-supply output connection pin. This pin should be connected to "DCLOUT" pin on the main board.
78	DCLIN_A	Input	
31	VCC	Input	Power supply pin. Connect it to the system power supply. RF transceiver power supply pin("VCC_RF", "AVCC_RF") share the same external pin with "VCC" pin.
73	ICGND (VSS_RF)	Input	RF transceiver ground pin. In this document, this pin is called “ICGND”.
9,12,13,14, 15,16,17,18, 19,20,79,80, 81,82,83	VSS_RF	Input	RF transceiver ground pin

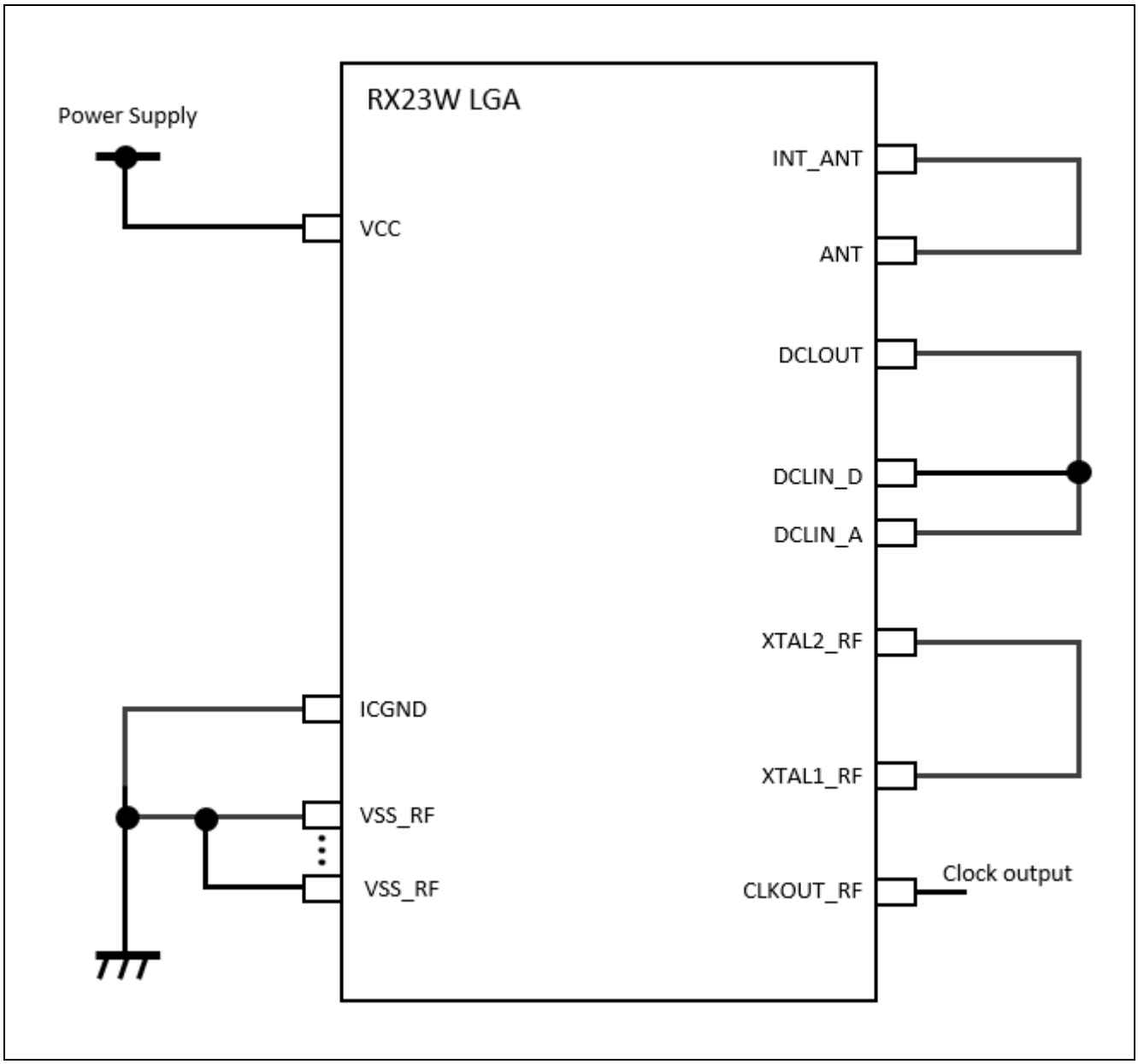


Figure 4-1 Example of connections for each pin

4.2 Oscillator circuit for Bluetooth-dedicated clock

Note the followings for "XTAL1_RF" and "XTAL2_RF" pins design.

2-1. The crystal resonator and external load capacitors (CL) for frequency tuning are unnecessary, because they are built in IC.

2-2. Connect the wiring between pins ”XTAL1_RF” and ”XTAL2_RF” on the solder side through the via holes shown in Figure 4-2. When this guideline is kept, the adjustment of the frequency of the Bluetooth-dedicated clock oscillator is not necessary.

The initial setting (CLVAL = 7) of Bluetooth middleware can be used without adjustment.
CLVAL : Capacitor setting for frequency tuning

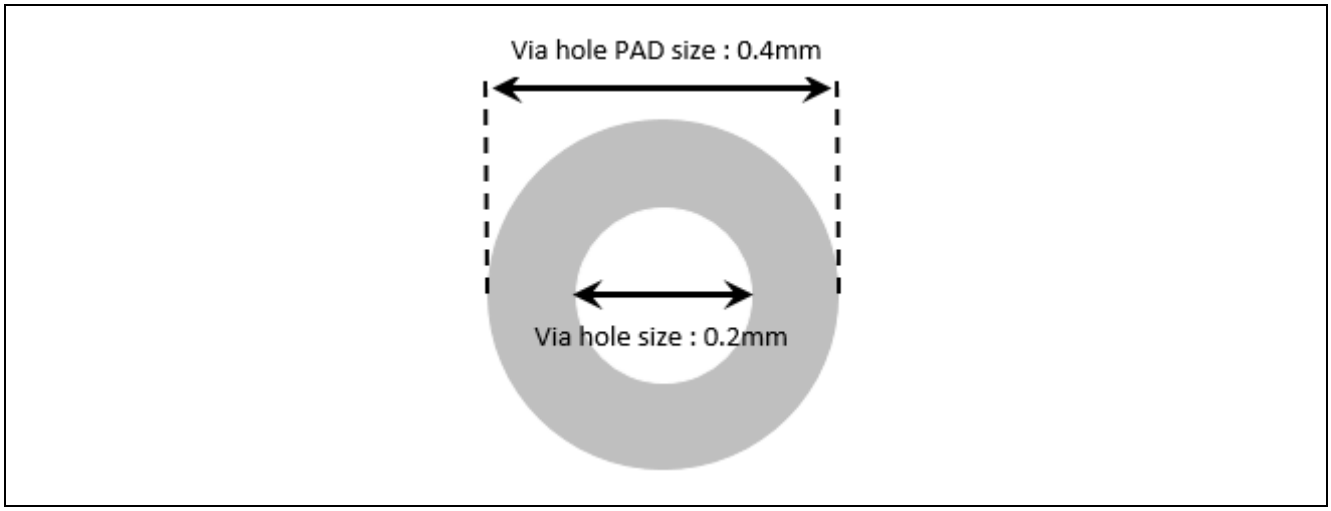


Figure 4-2 Via size for "XTAL1_RF" and "XTAL2_RF" pins (Common to both four-layer board and six-layer board)

2-3. When the frequency-divided clock for the Bluetooth-dedicated clock is output, note designing board pattern. The wiring length should be as short as possible. In addition, must not branch the wiring. And avoid using vias on the transmission line. A maximum of 2 is recommended.

2-4. Shield the transmission line of CLKOUT_RF with the "VSS" pattern to avoid noise couplings to “VSS_RF”.

4.3 Antenna connection pin

Note the followings for "ANT" and "INT_ANT" pins design.

3-1. When the internal antenna is used, the wiring length between "ANT" and "INT_ANT" pins should be as short as possible on the parts surface of the main board.

3-2. When the internal antenna is not used, "INT_ANT" pin should be open.

3-3. When evaluating RF characteristics directly from "ANT" pin, Adjust the characteristic impedance of 50ohm for the signal line.

4.4 Power supply mode for Bluetooth 5.0 RF transceiver

Note the followings for "DCLOUT", "DCLIN_A" and "DCLIN_D" pins design.

4-1. The capacitor for Linear regulator is unnecessary, because the capacitor is built in IC.

4-2. We recommend that the “DCLOUT”, “DCLIN_A”, and “DCLIN_D” pins be wired in two layers, the parts surface and the solder side.

4.5 Ground

Note the followings for ground patterns design.

5-1. Not separate the ground area with other signal lines so that the ground area is as wide plane as possible.

5-2. Not place power supply and signal lines on the layer 2 as it should be a solid ground.

5-3. Connect “VSS_RF” and other grounds which are “VSS”, “AVSS0”, and “VSS_USB”, with single point short. And separate the ground pattern directly under the IC package as shown in Figure 4-3.

5-4. When connecting the ground pattern to other layer of same potential, the connection should be low impedance with many vias.

5-5. Connect "ICGND" pin to “VSS_RF” only on the solder side through a via.
Note that the "VSS_RF" is separated on the parts surface side directly under the IC package.

Figure 4-3 shows an example of the pattern under the RX23W LGA package.

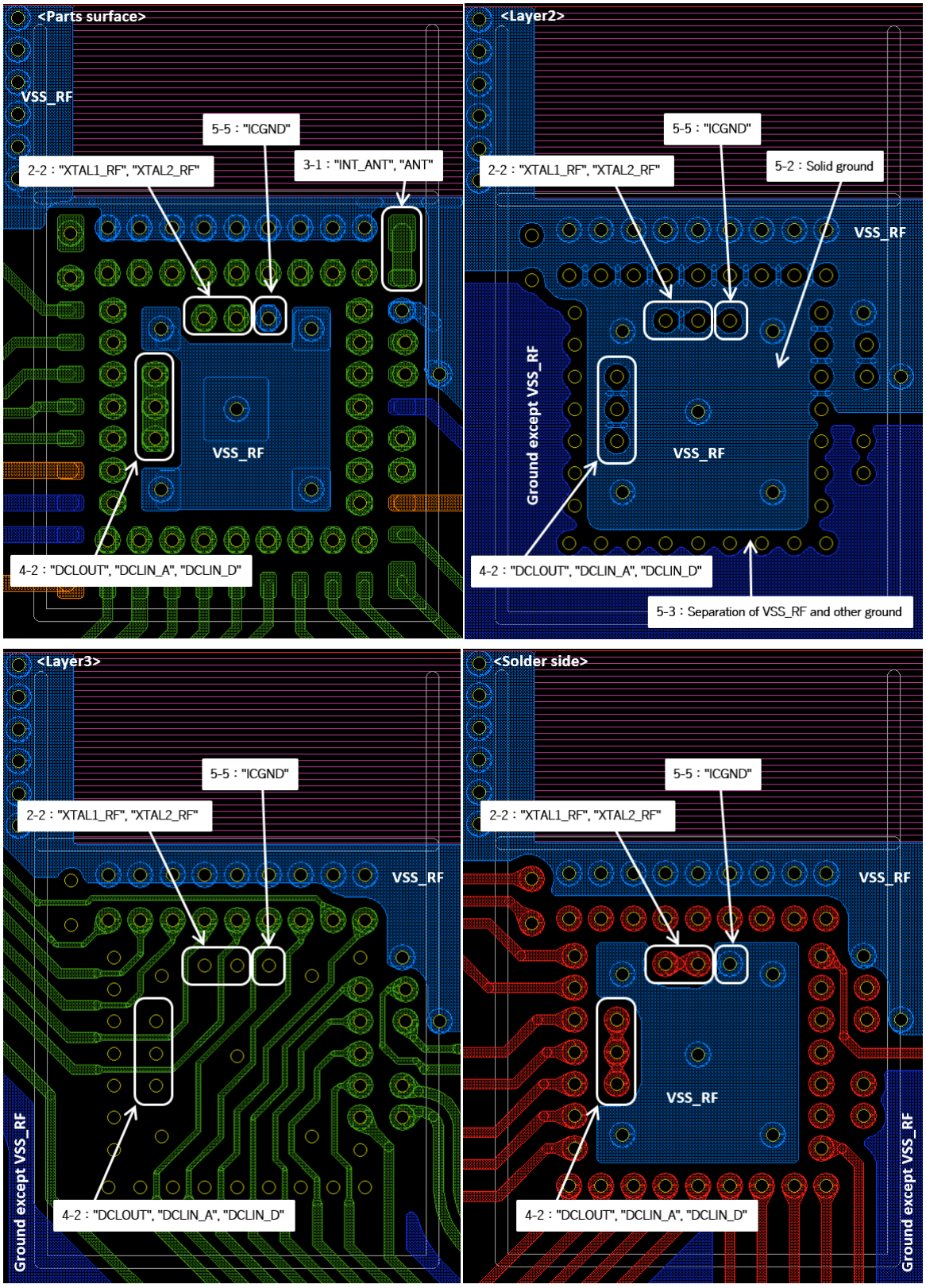


Figure 4-3 Example of the pattern under the RX23W LGA package

4.6 Antenna layout

Note the followings for the internal antenna patterns design.

The antenna is built in the unsputtered 6.1x3.0mm area, as shown in Figure 4-4.

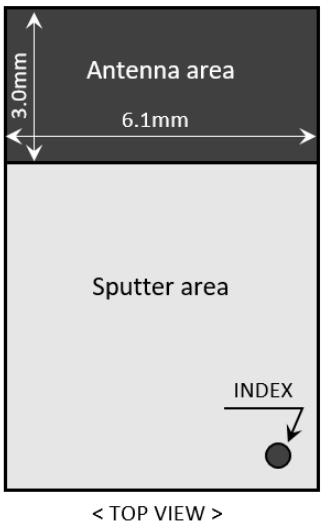


Figure 4-4 Antenna built in area

6-1. Place this MCU near the top right corner of the main board.

6-2. The area directly under and to the right of the antenna area is the pattern prohibiting area where the copper foil pattern cannot be placed. Do not place any signal, power, and ground lines on all layers of this area.

6-3. Place "VSS_RF" pattern on all layers in the area on the left side of the antenna area. And the “VSS_RF” pattern must not be separated and many vias should be placed.

6-4. Place "VSS_RF" on the main board with an overlap width of 0.5 mm on the lower layer of the left side of the antenna.

6-5. Place "VSS_RF" pattern in the left area and lower area so as to surround the pattern prohibiting area for antenna on the main board. And the “VSS_RF” pattern must not be separated and many vias should be placed.

6-6. This MCU must be mounted 20mm from the right end(Copper foil edge) of the main board. However, when the transmission power setting is 0 dBm mode, it can be mounted at a position 20 mm or less from the right end of the main board.

Figure 4-5 shows an example of the antenna layout.

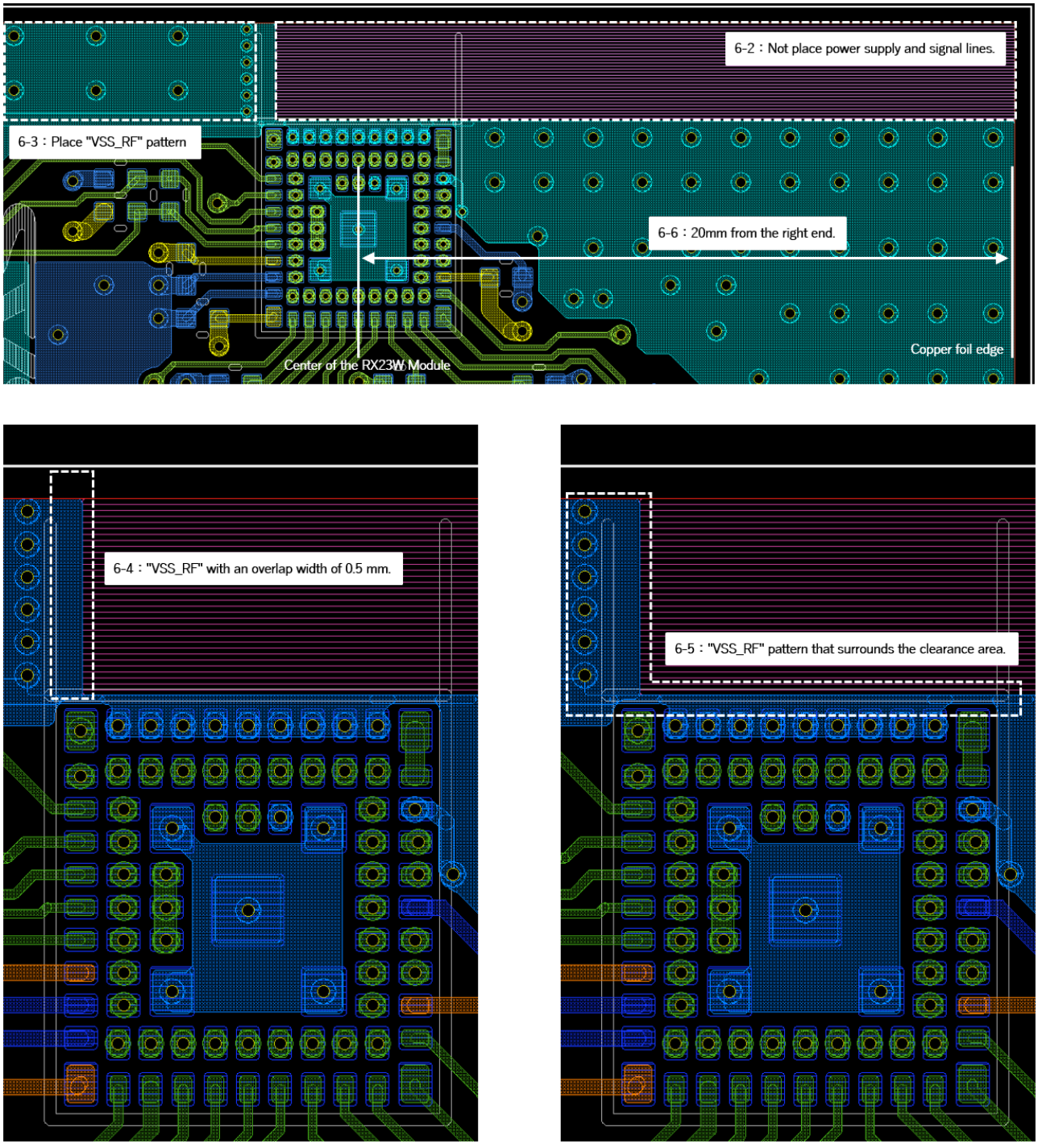


Figure 4-5 Example of the antenna layout

4.7 Main Board Design

To secure the antenna characteristics, take into account the following points to note in mounting this module on the main board.

7-1. It is recommended that the length of the main board is longer than 40 mm to get optimal antenna performance, because the image antenna including the ground is formed on the main board.

7-2. Make a solid ground to be included in the layer configuration of the main board as large as possible.

7-3. The outer periphery of the main board except for the pattern prohibiting area where the copper foil pattern cannot be placed directly under the antenna must be surrounded by “VSS_RF” patterns, and as many ground vias as possible must be placed.

7-4. It is recommended to mount at locations A, B, C and D as shown in Figure 4-6.
In the case of mounting at locations E, F, G, H, and I, good antenna characteristics cannot be obtained.

Figure 4-6 shows an example of the main board layout.

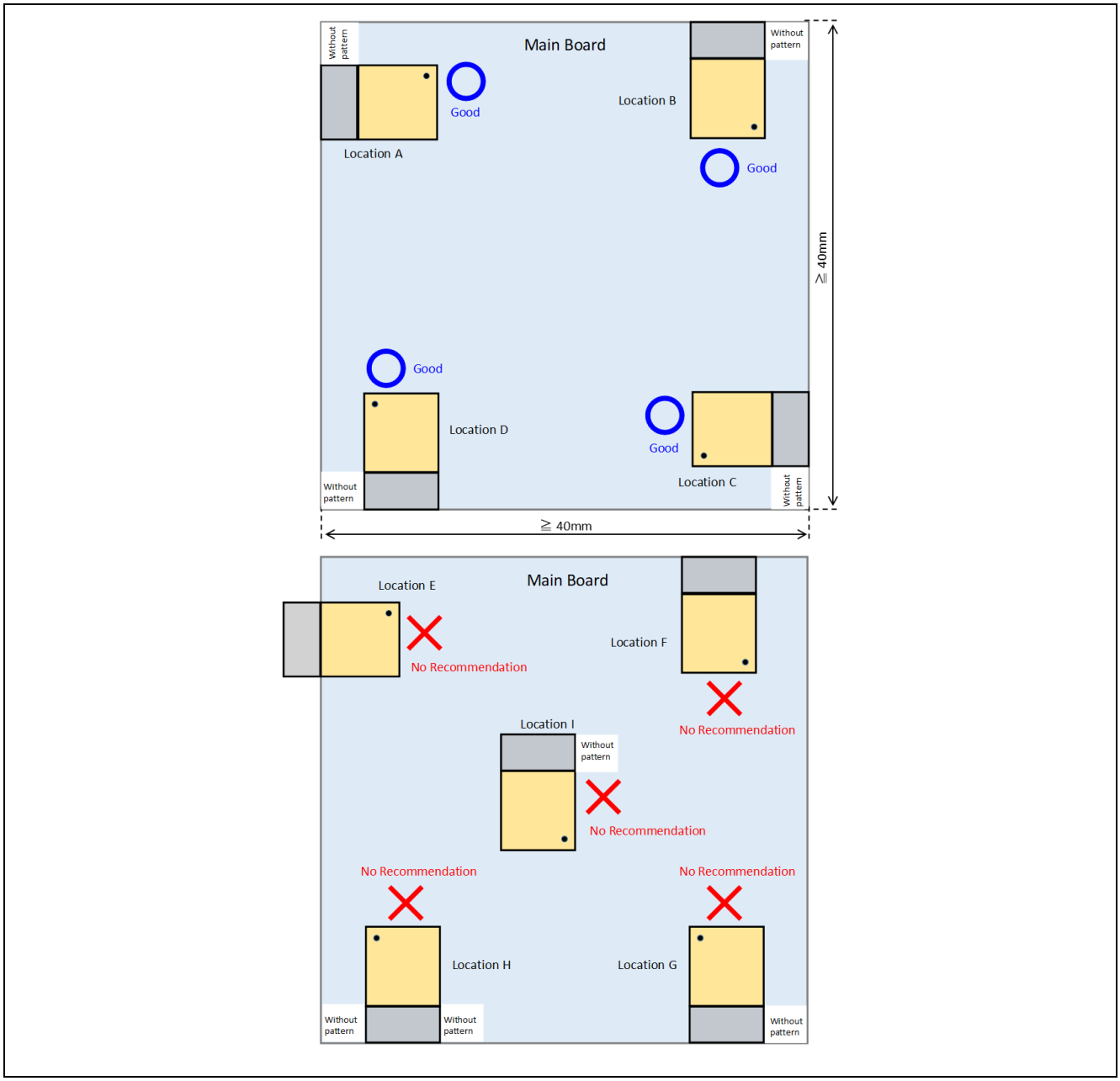
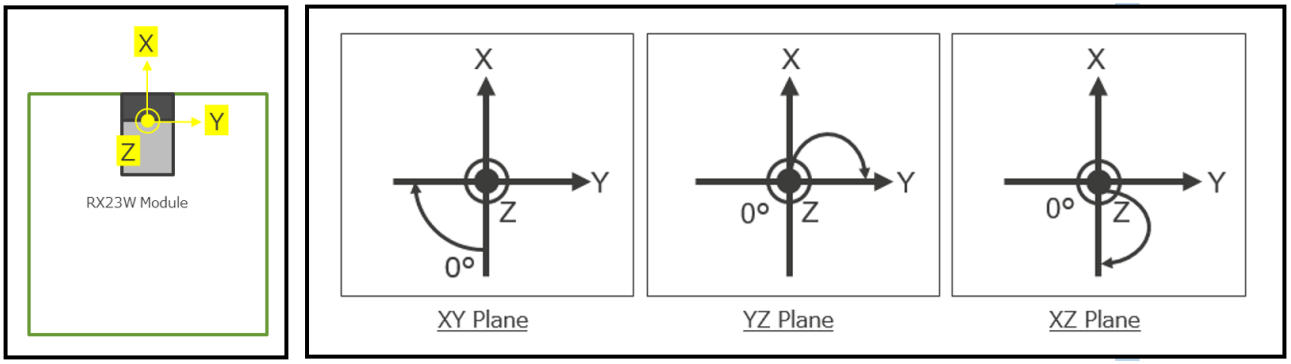


Figure 4-6 Example of the main board layout

4.8 Emission characteristics

Figure 4-7 shows the coordinate axes, the positions where rotation starts (0°), and the directions of rotation of the evaluation board. The coordinate axes are defined as shown in Figure 4-7(a). The positions where rotation starts (0°) and its directions in obtaining the emission patterns in each plane are defined as shown in Figure 4-7(b).



(a) Coordinate axes (b) Positions where rotation starts (0°) and its directions

Figure 4-7 Coordinates and Rotation of the main board

Figure 4-8 shows the measurement results of the internal antenna emission characteristics.

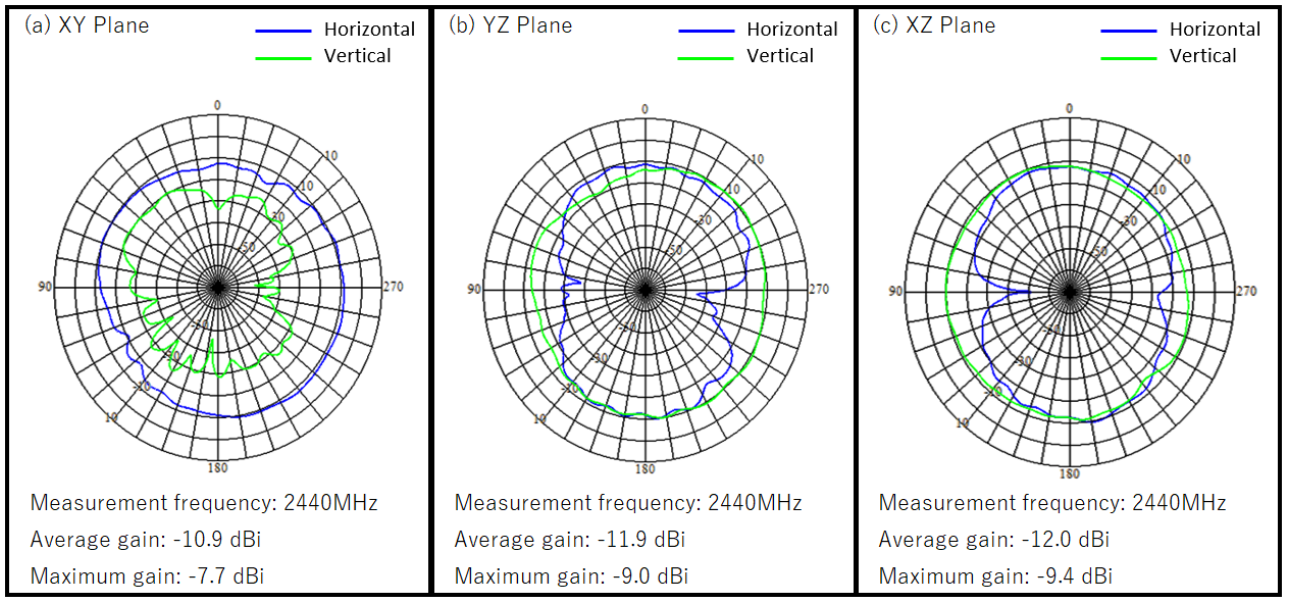


Figure 4-8 Measurement results of the internal antenna emission characteristics

4.9 Housing Design

When this MCU is housed in a plastic housing, it is recommended that the distance between the main board and the plastic housing keep at least 1 mm away in order to ensure the characteristics of the antenna. At this time, keep at least 1 mm away from the top of the package only on the mounting surface of this MCU.

Note: Since the constraints are based on the conditions shown in Figure 4-9, the antenna characteristics are affected by the actual designed housing structure.

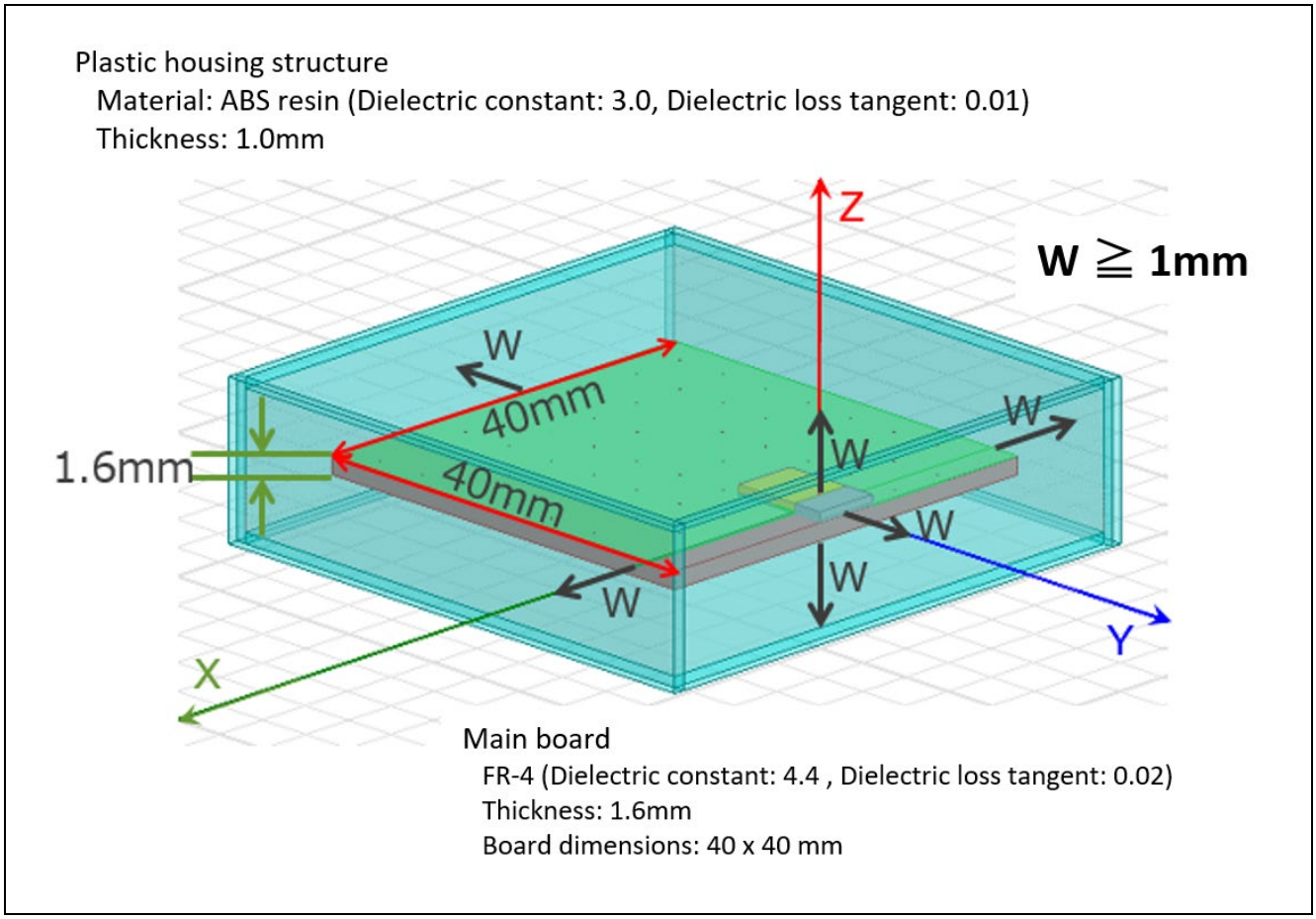
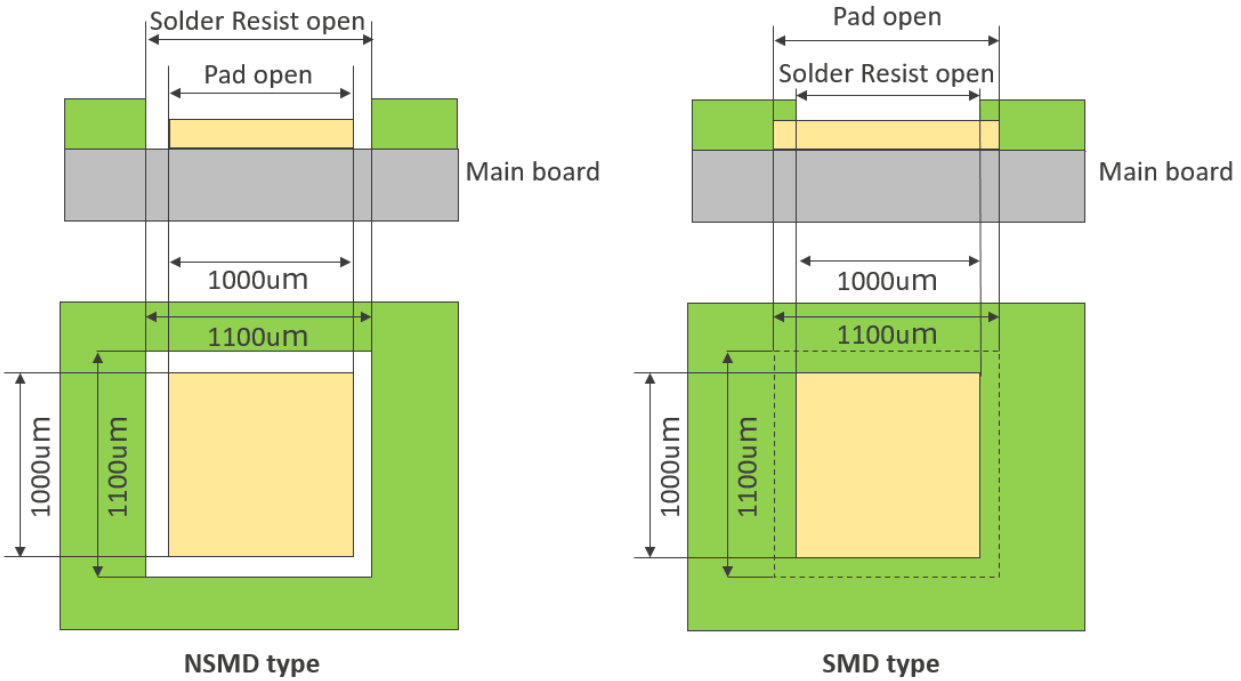


Figure 4-9 Plastic housing conditions

4.10 Foot pattern design example

There are two types of mounting pad; solder mask defined (SMD), in which the solder resist overlays the mounting pads, and non solder mask defined (NSMD), in which the solder resist does not overlay the pads. Figure 4-10 shows the foot pattern design example with pin number 83 (1000 x 1000um).



Since the stress after solder mounting is distributed evenly at the solder joint, it is said that it is acceptable to design the mounting pad dimensions to have the same as the dimension of the lands on the package.

Figure 4-10 Foot pattern design example

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Nov.01.19	—	First edition issued
2.00	Jan.31.21	40 to 50	4.Board design guidelines for RX23W LGA, added
2.01	Sep.30.21	51	4.10 Foot pattern design example, added

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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