RL78/I1B Group

Using the 24-bit ΔΣ (Delta-Sigma) A/D Converter

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Introduction

This application note describes usage of the 24-bit ΔΣ (Delta-Sigma) Analog-to-Digital Converter (ADC) peripheral featured in the RL78/I1B processor.

Target Device

RL78/I1B.

Development Environment

IDE: e[2] studio v4.0.1.007

Compiler: GNURL78 v15.01

Hardware: Renesas RL78/I1B Target Board (Part No. RTE510MPG0TGB00000R)

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1. Introduction

The RL78/I1B features an integrated and adjustable 24-bit ΔΣ A/D converter module (ADC), which is capable of measuring small analogue signals with wide dynamic ranges at high signal-to-noise ratios (SNRs). The ΔΣ conversion method is more precise and has better noise tolerance than the Successive Approximation method also used for ADCs, with the practical tradeoffs being a slower conversion speed and higher power consumption.

For a detailed overview of the ΔΣ technique, refer to Renesas application note R01AN1437EJ0100. This document also provides details of the Successive Approximation technique.

This application note focuses on the usage of the 24-bit ΔΣ ADC in the RL78/I1B.

2. Summary of the ΔΣ A/D Converter Peripheral

The 24-bit ΔΣ A/D converter has the following specification and functionality:

- SNDR (SINAD): 80 dB min. (when pre-amplifier gain of ×1 is selected)
- 24-bit resolution (conversion result register: 24 bits)
- 3 channels (2x current channels, 1x voltage channel) (80-pin products)
- 4 channels (2x current channels, 2x voltage channels) (100-pin products)
- All ΔΣ A/D channels have differential inputs
- PGA with selectable gain
  - ×1, ×2, ×4, ×8, ×16, or ×32 (channels 0 and 2: current channels)
  - ×1, ×2, ×4, ×8, or ×16 (channels 1 and 3: voltage channels)
- Operating voltage: AVDD = 2.4 to 5.5 V, AVSS = 0 V
- Analog input voltage range (differential voltage)
  - ±0.500 V (when PGA gain of ×1 is selected)
  - ±0.250 V (when PGA gain of ×2 is selected)
  - ±0.125 V (when PGA gain of ×4 is selected)
  - ±62.5 mV (when PGA gain of ×8 is selected)
  - ±31.25 mV (when PGA gain of ×16 is selected)
  - ±15.625 mV (when PGA gain of ×32 is selected)
- Internal reference voltage generator (0.8 V typ.) with 30ppm/°C typ. temperature coefficient
- Sampling frequency: 3906.25 Hz or 1953.125 Hz
- HPF cutoff frequency: 0.607 Hz, 1.214 Hz, 2.429 Hz, or 4.857 Hz can be selected. The HPF eliminates the DC component in the input signal and the DC offset generated by the analog circuit.
- Operating clock: High-speed system clock (f_{MX}) (only 12 MHz crystal resonator can be used) or High-speed on-chip oscillator (f_{IH})

This application note uses the 100-pin R5F10MPG device, which features four independent ΔΣ ADC channels.

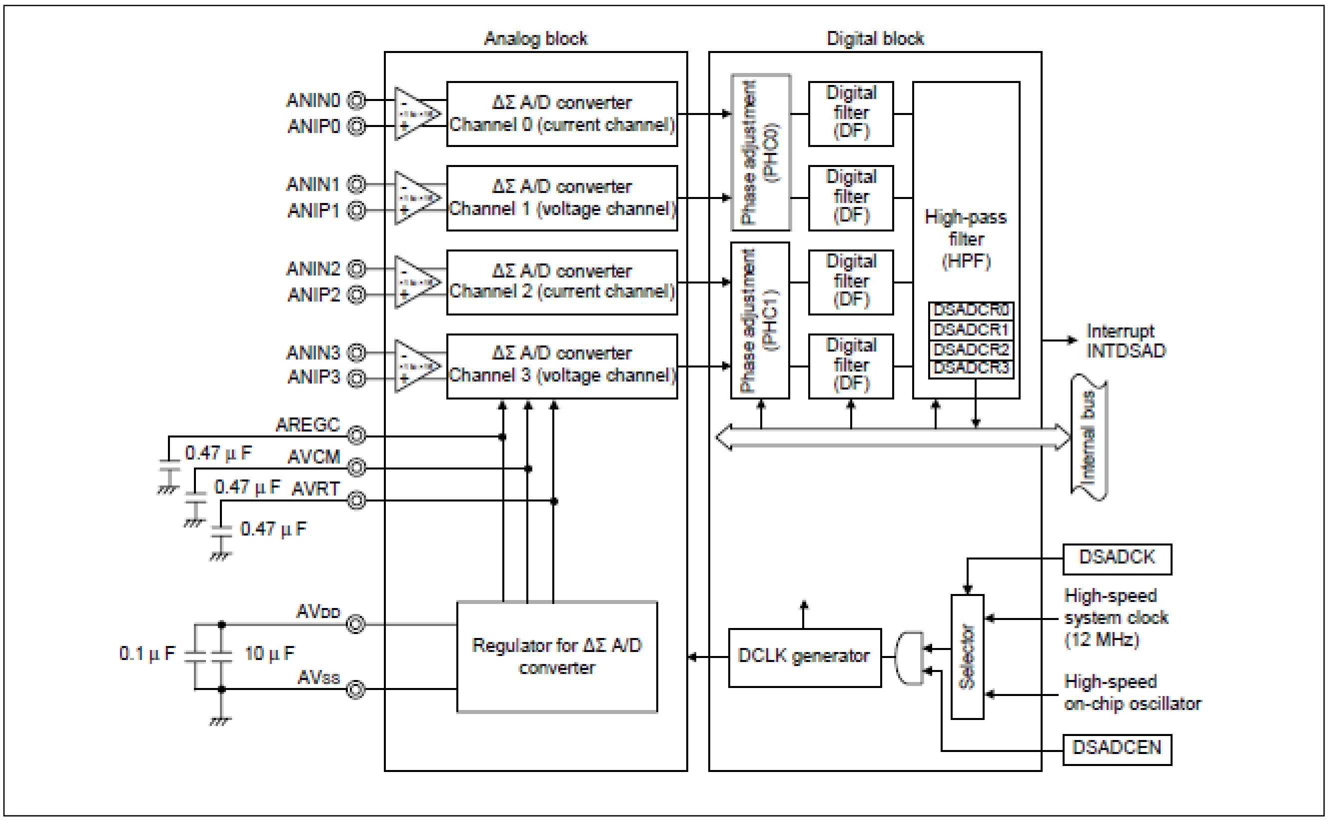


Figure 1 Block Diagram of 24-bit ΔΣ A/D Converter (100-Pin Products)

3. Operation

The 24-bit ΔΣ A/D converter (ADC) peripheral on the R5F100MPG has the signal input pins to facilitate four independent ΔΣ ADC conversion results. By passing 2-bit values obtained from these ΔΣ ADC conversion results through the digital filter, the value is converted into 24-bit digital values.

The mode setting of the ΔΣ ADC of the analog block depends on the values of the DSADMR, DSADGCR0, and DSADGCR1 register.

When running the ΔΣ ADC from the high-speed on-chip oscillator (HOCO) clock (fIH), be sure to run the HOCO clock frequency correction function according to the I1B Hardware Users' Manual before trusting results from the ΔΣ ADC.

When selecting the high-speed system clock (fMX), execute a NOP instruction twice after switching to the selected clock.

The 24-bit converter starts operating when the DSADPONn bit (n = 0 to 3) and the DSADCEn bit in the DSADMR register are set to 1. **A short stabilisation time is required after power-on of the peripheral and after the start of conversions, prior to conversions being valid**. Perform initialisation in accordance with the flowchart below in figure 2.

4. Flowchart of 24-bit ΔΣ A/D Converter Operation

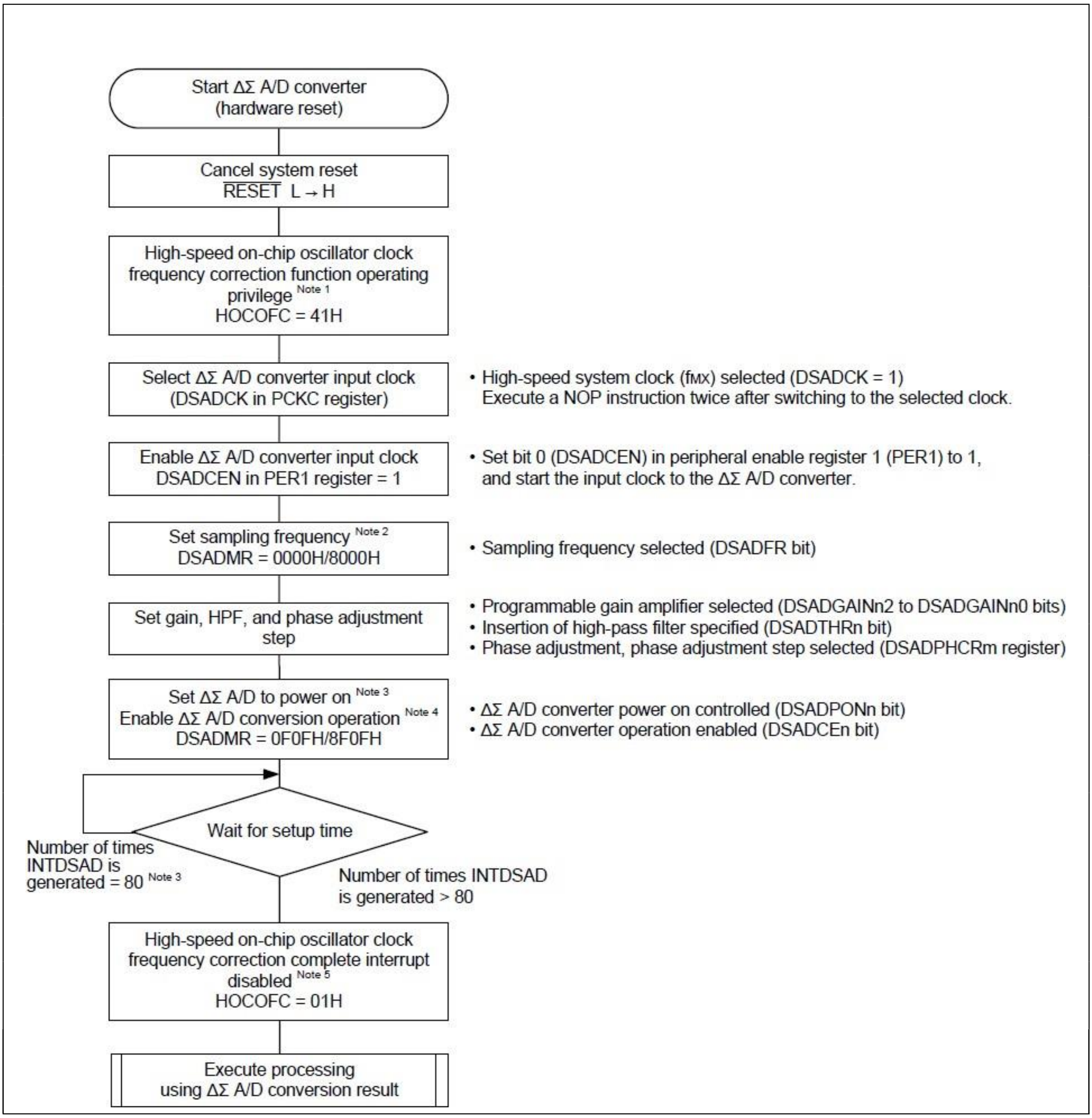


Figure 2 Initialisation flow for 24-bit ΔΣ A/D converter

Notes

1. When selecting the high-speed on-chip oscillator clock, be sure to run the high-speed on-chip oscillator clock frequency correction function before running the ΔΣ A/D converter.

2. Set the sampling frequency while the ΔΣ A/D converter is powered down.

3. The setup time (the number of times INTDSAD is to be generated) when DSADPONn is set to 0 and then 1 will be officially determined after evaluation.

4. If the ΔΣ A/D converter is temporarily stopped for initialisation (DSADCEn = 0 with DSADPONn = 1) and then restarted, it is necessary to wait for a certain setup time. In this case, since stabilization time is necessary for the converter, wait for one INTDSAD to be generated as the setup time.
To initialise the ΔΣ A/D converter, make sure that DSADCEn remains 0 for at least 1.4 μs.

5. Perform only when selecting the high-speed on-chip oscillator clock.

5. Sample Project

The sample C project provides a working example of the 24-bit ΔΣ A/D Converter peripheral running under the high-speed on-chip oscillator (HOCO). The project has been written to work with the RL78/I1B Target Board (Part No. RTE510MPG0TGB00000R) featuring the 100-pin R5F10MPG device. The project was developed using Renesas e^{2}studio v4.0.1.007 and the KPIT GNURL78 toolchain, v15.01.

The peripheral drivers for the sample program have been generated using Renesas Applilet AP4 (v1.04.02.01).

5.1 Scope

The sample C project is intended to simulate a single-phase metering application, where it is desirable to be able to measure both supply voltage and current. Of course, an ADC is only capable of measuring voltage, so to measure current a current probe (e.g., a CT), which produces a voltage proportional to the current being sensed, would be required. Current sensors and analogue filters generally introduce a phase-shift into the measurement, so the sample project arbitrarily uses the phase adjustment circuits available in the ΔΣ ADC peripheral to simulate the phase compensation that would be required in a real application.

The sample C project uses two signal generators to generate sine waves at 50Hz as the input signals for the ΔΣ ADC (for both the current and voltage channels), and the SW1 push-button on the RL78/I1B target board to toggle the settings of the ΔΣ ADC.

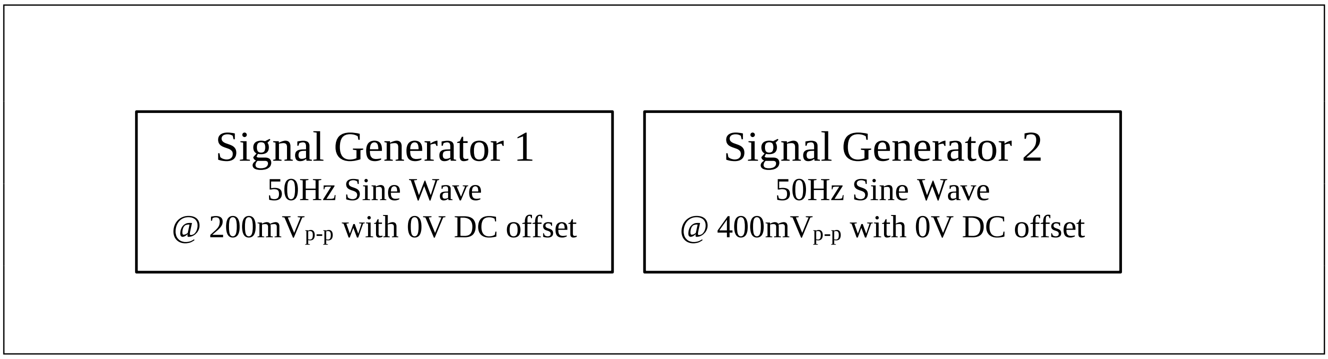
5.2 Hardware Setup

Before running the application, it is necessary to add signal wires to the RL78/I1B target board. Add a length of wire to pins:

- Connector CN7, pin 8: ANIN0: Current Channel (0), negative input
- Connector CN7, pin 7: ANIP0: Current Channel (0), positive input
- Connector CN7, pin 6: ANIN1: Voltage Channel (1) , negative input
- Connector CN7, pin 5: ANIP1: Voltage Channel (1), positive input

Connect the positive wires to the positive terminals of an each signal generator. Similarly, connect the negative wires to the negative terminals. To mitigate against common-mode voltages in the signal wires being transferred to the measurements, the pairs are twisted. For real designs, and certainly for higher frequencies, common-mode voltage elimination should be fully considered for analog input channels.

Note: Please refer to board schematic to locate CN7 & associated pins as this varies from board marking.



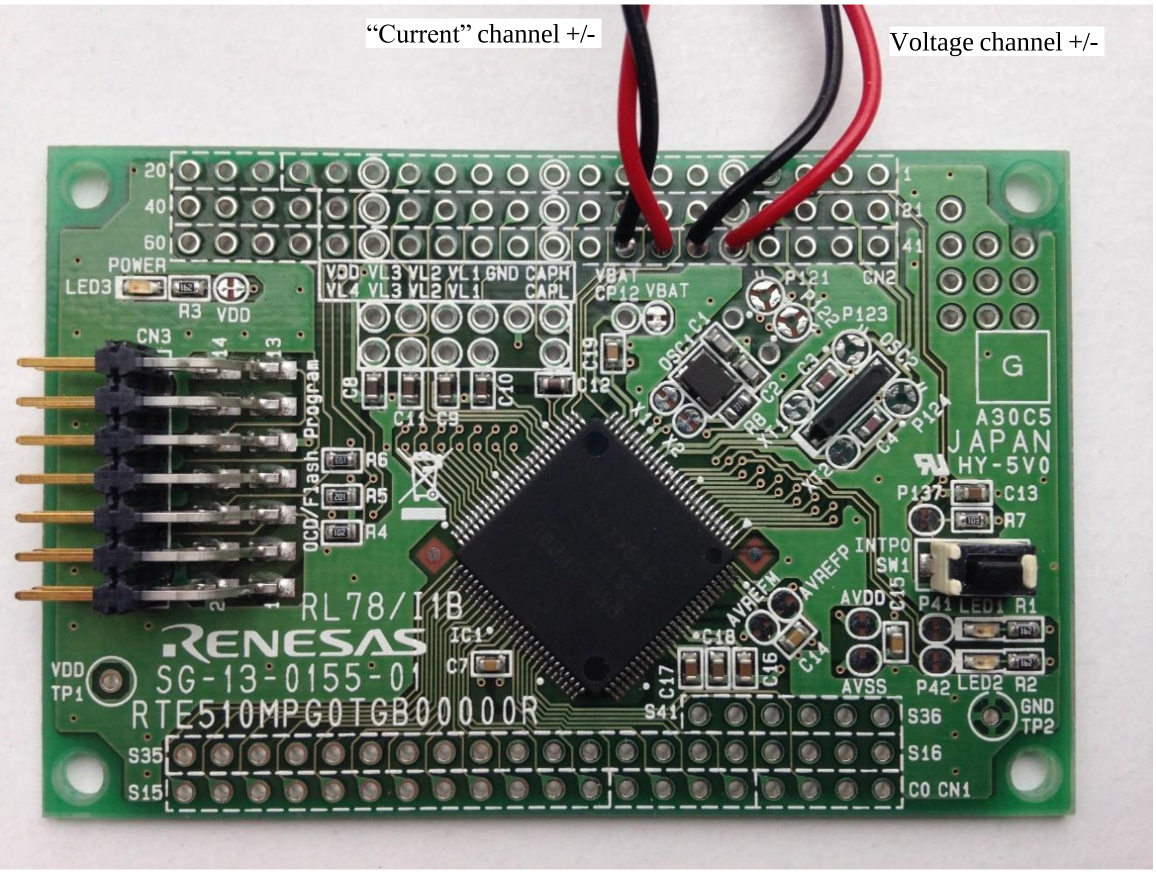


Figure 3 Diagram of hardware setup for 24-bit ΔΣ A/D sample project

Note: Please refer to board schematic to locate CN7 & associated pins as this varies from board marking.

5.3 Operation

With the RL78/I1B prepared and with the ΔΣ ADC signals connected to the signal generators that will provide the ADC inputs on channels 0 and 1, the sample program can be run. During program execution, pressing the SW1 push-button will toggle the settings of the ΔΣ ADC.

Note, the sample program toggles between gain settings of x1 and x2 on both channels 0 and 1. To avoid overdriving the ADC inputs for either gain setting, it is recommended that the signal generators are set to output a level below the maximum input level for the x2 gain setting. Attention should be paid to the conversion of differential to single-ended signal levels if single-ended signal sources are used.

The operation of the sample program is as follows:

1. Following a reset, the program first performs hardware initialisation. The GPIO ports, HOCO, HOCO frequency correction function, ΔΣ ADC and interrupt controller are configured in `R_Systeminit()`, before `main()` is entered. The HOCO frequency correction function is configured in continuous mode and the HOCO is set to run at 12MHz. The ΔΣ ADC is initially configured with a sampling frequency of 3906.25Hz, 24-bit resolution, x1 analog gain and an arbitrary phase shift on the 'current' channel (channel 0).The integrated digital high pass filter is configured with a cut-off frequency of 0.607Hz and is applied to both channels. **.**
2. After `main()` is entered, the interrupt for the SW1 push-button is enabled, after which the ΔΣ ADC is initialised. Since the ADC has been configured to run off the HOCO, it is first necessary to correct the HOCO's frequency so that the ADC conversion results can be fully trusted. This process is started after hardware initialisation, and the HOCO clock frequency correction interrupt is issued when it is completed.
3. During the HOCO clock frequency correction process, the ΔΣ ADC is started and conversions will start being made. The ADC requires a small stabilisation time after power-on, during which conversion results should not be trusted. At the time of writing, it is necessary to wait for a minimum of 80 conversions to be made before one can be sure that the ADC has stabilised. Program execution remains in `dsadc_init()` until both the HOCO clock frequency has been corrected and the 80 invalid conversions have been made.
4. The program is now continually making conversions using the ΔΣ ADC. After every conversion has been completed, the `r_dsadc_interrupt()` handler is called, wherein the conversion results for the current and voltage channels are retrieved immediately. Initially, the ADC is configured have 24-bit conversion resolution. The relationship between the ADC value and the analogue voltage being measured is shown below.
5. If the SW1 push-button is pressed, the settings of the ADC are toggled. Whilst the settings are being changed, the ADC is disabled (but not powered-down, so a stabilisation period is not required). The new settings turn the phase shift on the current channel off, decrease the sampling frequency to 1953.125Hz, double the gain to x2 and reduce the resolution to 16-bit. The ADC is then restarted and conversions continue, this time placing conversion results in a 16-bit buffer to account for the decrease in resolution.
6. Pressing SW1 again will revert the ΔΣ ADC back to its initial settings.

To view the measurements whilst the program is running, add a watch expression on any or all of the four variables used for storing results:

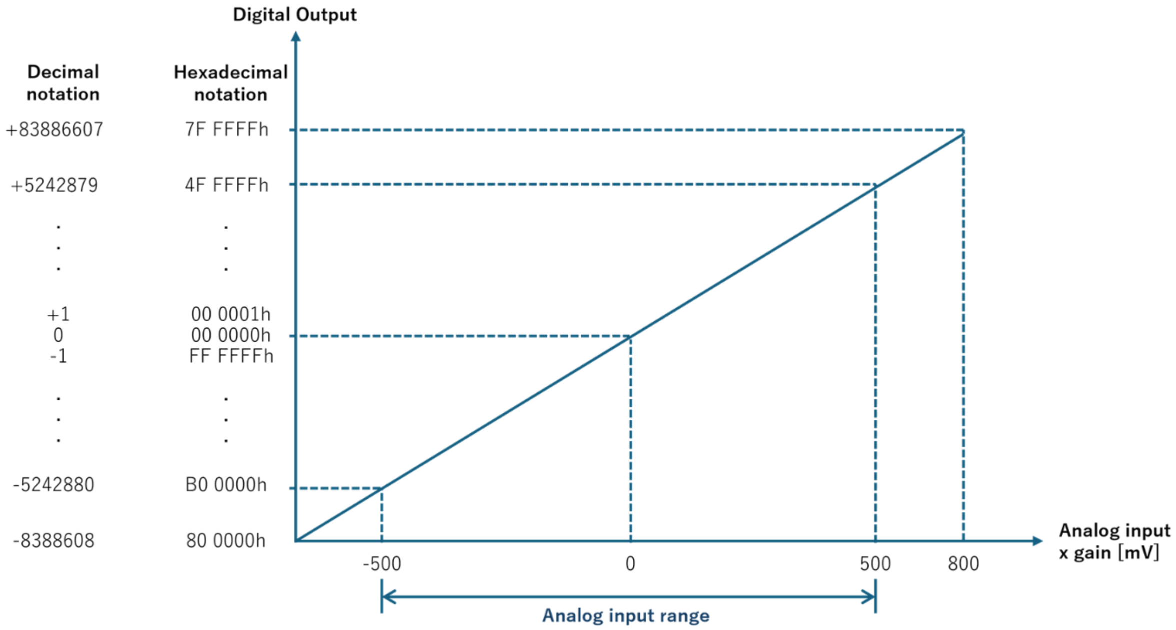
- `s_current_dsadc_val`
- `s_voltage_dsadc_val`
- `s_current_dsadc_val_16bit`
- `s_voltage_dsadc_val_16bit`

To do this in e²studio, whilst the program is running, highlight the variable definition (located in *r_cg_main*.c, from line 65) and, from the 'Debug' perspective, drag the variable into the 'Expressions' window. Then, right-click on the variable added to the 'Expressions' window and select 'Real-time Refresh'. The value of the variable being watched will now change periodically (defined by the 'real-time refresh interval', located in the same menu).

Note: It can be seen that there are two sets of variables for the results, one set is 32-bit and the other is 16-bit. These are necessary to store the results when the ΔΣ ADC resolution is 24-bit and 16-bit, respectively.

5.3.1 Output Format of the 24-bit ΔΣ A/D Converter

The ΔΣ ADC conversion data is the maximum value when the analog input voltage equals the reference voltage (0.8V). Generally, the digital value corresponding to the analog input voltage can be obtained by multiplying the full-scale (FS) value of the ADC by the ratio of the analog input voltage to the reference voltage, as shown in the following expression:



5.4 Sample Project Flow

Figure 5 shows the flow for ΔΣ ADC converter sample project, including switching operating modes.

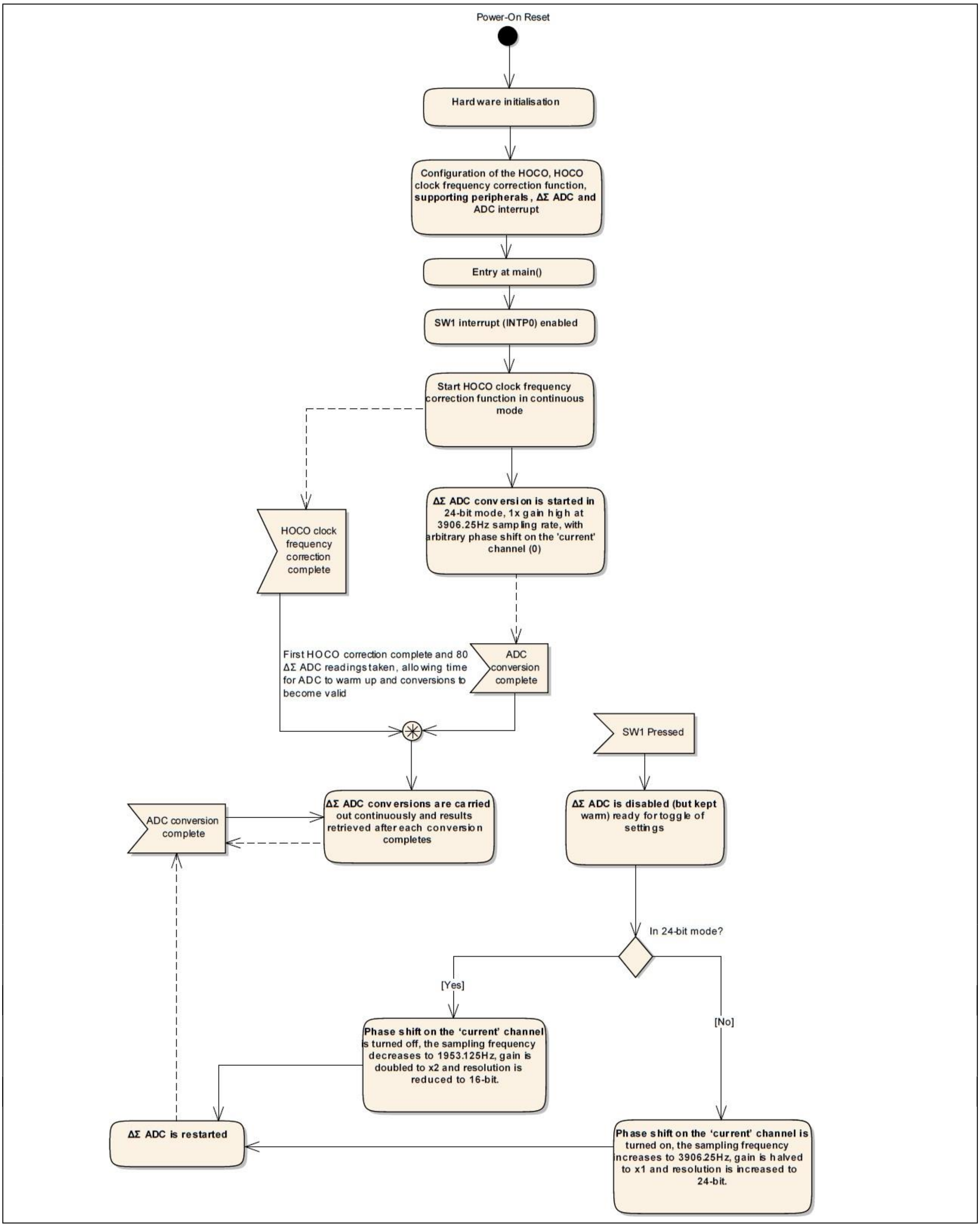


Figure 5 Sample Project Flow

Website and Support

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Revision History

Rev.	Date	Description	
		Page	Summary
1.0	Mar 17, 2016	All	First issue.
1.1	May 19, 2025	p.8	Change the figure 3 image
		p.10	Modification of values for Decimal notation and Hexadecimal notation

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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