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RL78/G1F

Current Measurement with Programmable Gain Amplifier (PGA) CC-RL

Outline

This application note explains how to measure current using the RL78/G1F built-in programmable gain amplifier (PGA) and A/D converter (ADC).

Target Device

RL78/G1F

When using the application for a microcomputer (MCU) other than RL78/G1F, please evaluate thoroughly based on your target MCU's specifications.

Contents

1. Specifications

This application note explains how to measure current using the RL78/G1F built-in programmable gain amplifier (PGA) and A/D converter (ADC).

RL78/G1F is equipped with a PGA-dedicated GND pin (PGAGND). When using the PGA, connect PGAGND to the GND pin of the measurement system. A/D conversion accuracy can be improved by using AV_{REFP} and AV_{REFM} as ADC reference voltages $AV_{REF}(+)$ and $AV_{REF}(-)$, correspondingly. This ensures the current will be measured accurately.

Caution: The same potential must be applied to both PGAGND and V_{SS}.

This application uses the PGA and ADC to measure the voltage of one end of a shunt resistor and convert the result into the current value. When there is no current, the A/D conversion value is stored in RAM as the offset correction value to eliminate the effect of the PGA input offset voltage. After the voltage is converted to a current value, the current is measured in 1 second intervals. The offset correction value stored in RAM is subtracted from the measurement result and the current value is calculated. The three most recently measurement current values are retained in RAM.

Detailed specifications are as follows:

- Select the optimal gain (x1, x4, x8, x16, or x32) and measure the voltage of one end of the shunt resistor at the highest gain possible. (When x1: PGA is not used.)
- Use PGAGND as PGA(-) input.
- The PGA input offset correction is only applied to the + side. Input offset voltage is measured 10 times for each gain x1 to x32. The resulting mean value is stored in RAM as the gain x1 to x32 offset correction value.
- The ADC reference voltage setting can be changed by the constant definition.

  Constant VREF_AVREF is defined as the default; ADC reference voltage $AV_{REF}(+)$ is set to AV_{REFP} and $AV_{REF}(-)$ to AV_{REFM}. If this definition is removed, $AV_{REF}(+)$ is set to V_{DD} and $AV_{REF}(-)$ to V_{SS}.

  The user can also choose whether to set the AV_{REF} value in a constant or calculate it in a program. Constant VREF_FIX is defined as the default, and AV_{REF} is set in constant VREF_VOLTAGE". If this definition is removed, AV_{REF} is calculated from the A/D conversion results of the internal reference voltage (1.45 V). We do not recommend using the internal reference voltage (1.45 V) for this application as it has an approximate -4.8% to +3.4% error which may affect the accuracy of the current measurement.

Note: AV_{REF} indicates the A/D converter reference voltage (potential difference of $AV_{REF(+)}$ and $AV_{REF(-)}$).

Table 1.1 lists the A/D converter reference voltage setting changes based on constant definitions

Table 1.1 A/D Converter Reference Voltage Setting Changes Based on Constant Definitions

VREF_FIX	VREF_AVREF	Description
Undefined	Undefined	Sets $AV_{REF}(+)$ to V_{DD} and $AV_{REF}(-)$ to V_{SS} Calculates AV_{REF} from A/D conversion result of internal reference voltage (1.4 V)
Undefined	Defined	Sets $AV_{REF}(+)$ to AV_{REFP} and $AV_{REF}(-)$ to AV_{REFM} Calculates AV_{REF} from A/D conversion result of internal reference voltage (1.4 V)
Defined	Undefined	Sets $AV_{REF}(+)$ to V_{DD} and $AV_{REF}(-)$ to V_{SS} Sets AV_{REF} value to the value of constant VREF_VOLTAGE
Defined	Defined	Set $AV_{REF}(+)$ to AV_{REFP} and $AV_{REF}(-)$ to AV_{REFM} Sets AV_{REF} value to the value of constant VREF_VOLTAGE

Table 1.2 lists the application's peripheral functions and their usage.

Table 1.2 Peripheral Functions And Their Usage

Peripheral Function	Usage
Programmable gain amplifier (PGA)	Amplifies analog input
A/D converter (ADC)	Converts analog input to digital value
Timer array unit (TAU)	Channel 0: Current measurement timer Channel 1: Operation stabilization wait timer

Figure 1.1 shows the state transition of the application.

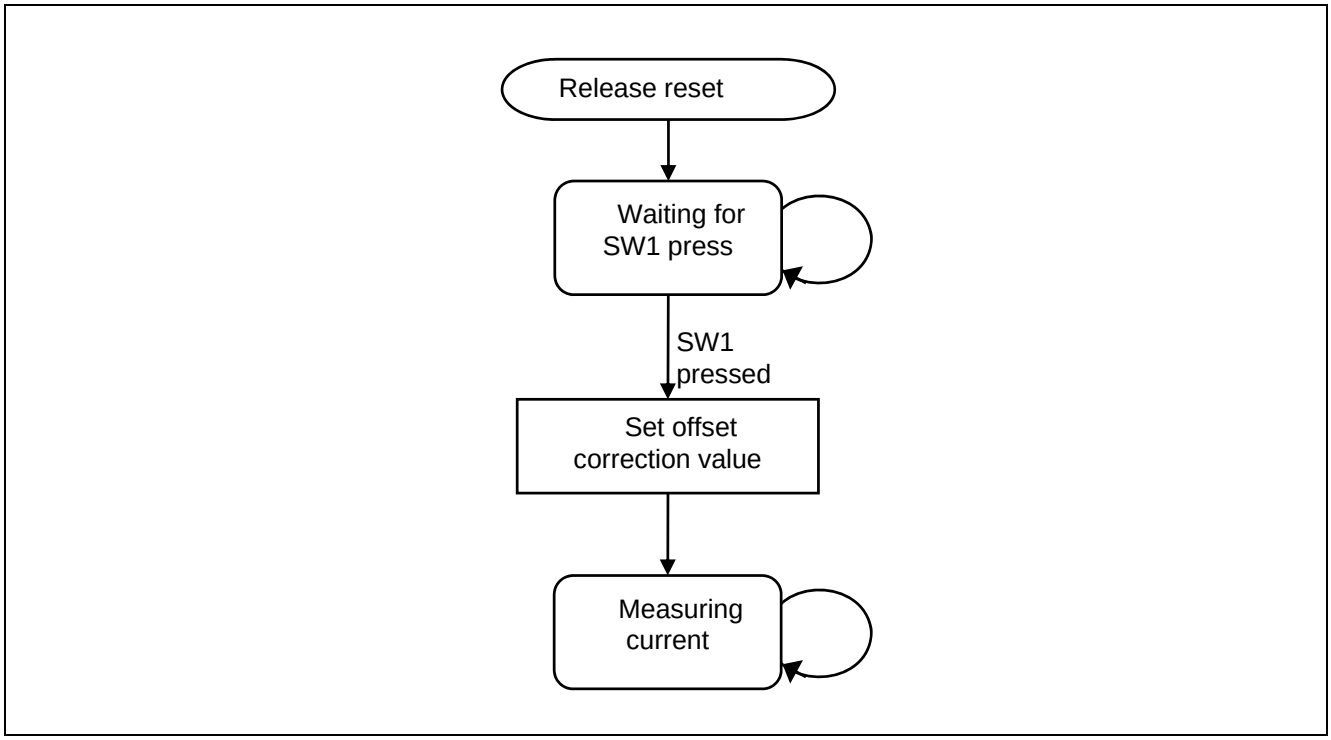

Figure 1.1 State Transition Diagram

2. Operation Confirmation Conditions

The sample code described in this application note has been confirmed under the following conditions.

Table 2.1 Operation Confirmation Conditions

Item	Description
MCU used	RL78/G1F (R5F11BLE)
Operating frequency	● High-speed on-chip oscillator clock (f_{HOCO}): 32 MHz, (f_{IH}): 32 MHz ● CPU/peripheral hardware clock (f_{CLK}): 32 MHz
Operating voltage	5.0V (Operation is possible over a voltage range of 2.9 V to 5.5 V） LVD operation (V_{LVD}): Reset mode which uses 2.81V(2.75 V to 2.81V)
Integrated development environment (CS+)	CS+ for CA,CX V3.00.01 from Renesas Electronics Corp.
C compiler (CS+)	CA78K0R V1.71 from Renesas Electronics Corp.
Integrated development environment (e2studio)	e2studio V4.02.008 from Renesas Electronics Corp.
C compiler (e2studio)	CC-RL V1.01.00 from Renesas Electronics Corp.
Board used	RL78/G1F target board (YQB-R5F11BLE-TB)

3. Related Application Notes

Other application notes related to this document are as follows. Please refer to them as needed.

RL78/G13 Initialization (R01AN0451E) Application Note

RL78/G13 A/D Converter (R01AN0452E) Application Note

4. Hardware Explanation

4.1 Hardware Configuration Example

Figure 4.1 shows the hardware described in this application note.

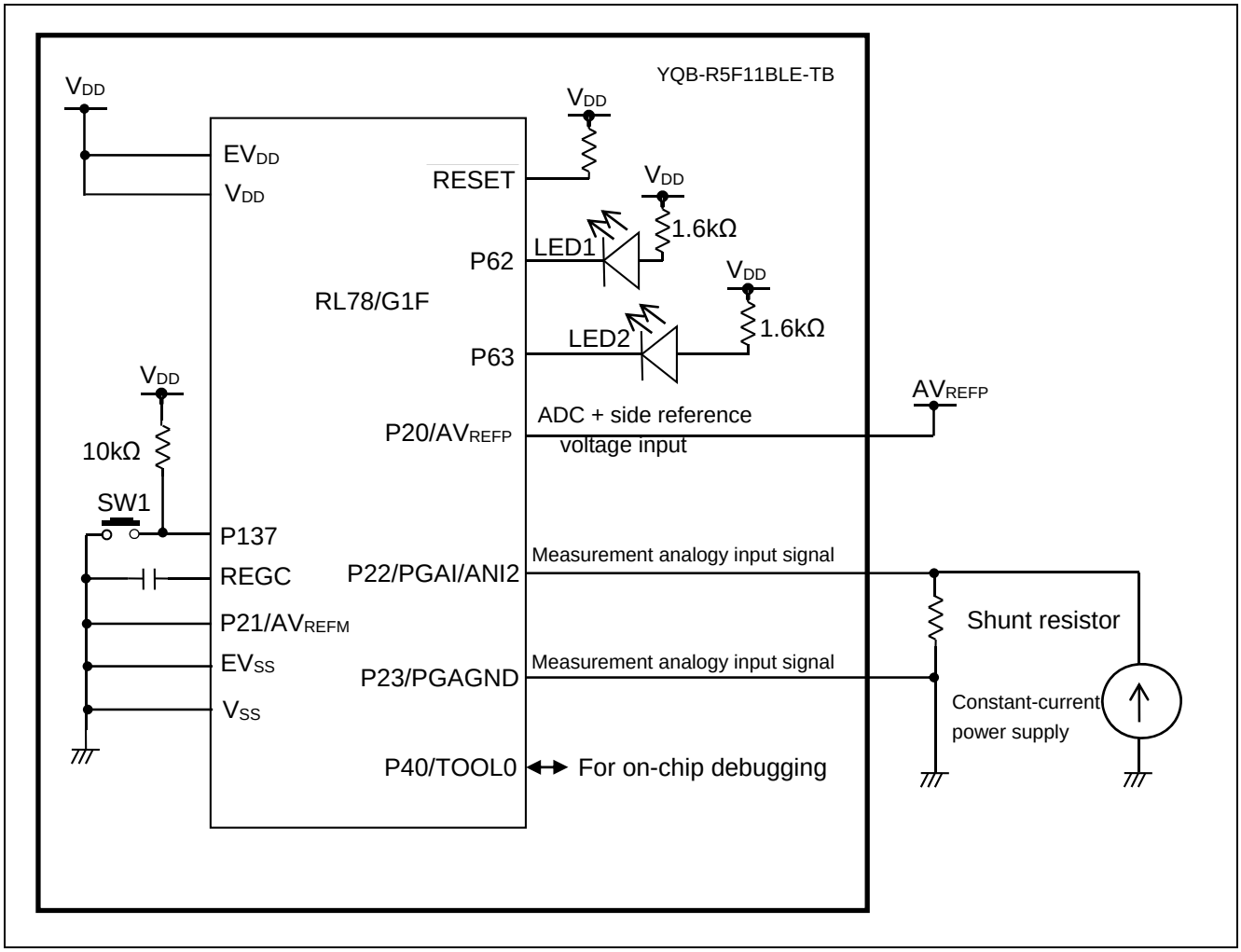

Figure 4.1 Hardware Configuration Example

Note 1 This circuit diagram has been simplified to show an overview of connections only.

When designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)

2 If the hardware includes a pin whose name starts with EV_{SS}, connect it to VSS; for a pin whose name starts with EV_{DD}, connect it to V_{DD}.

3 Set V_{DD} to LVD reset release voltage (V_{LVD}) or higher

4 Set PGAI/ANI2 input voltage to V_{DD} or lower.

5 Set P20/AV_{REFP} input voltage to V_{DD} or lower.

6 When not using pin P20/AV_{REFP} (VREF_AVREF is not defined), connect it to V_{DD} through a resistor.

7 When not using pin P21/AV_{REFM} (VREF_AVREF is not defined), connect it to V_{SS} through a resistor.

4.2 Pin List

Table 4.1 provides a list of the pins used in this document and their functions.

Table 4.1 List of Pins and Functions

Pin Name	Input/Output	Function
P20/AV_{REFP}	Input	Reference voltage (AV_{REFP}) A/D converter's +side reference voltage input Note 1
P21/AV_{REFM}	Input	Reference voltage (AV_{REFM}) A/D converter's - side reference voltage input Note 1
P22/PGAI/ANI2	Input	PGA(+)input / ADC input
P23/PGAGND	Input	PGA(-)input
P62	Output	LED1 control (ON: offset correction value setting complete)
P63	Output	LED2 control (Flashing: current measurement in process)
P137	Input	SW1 input

Note 1 Only valid when constant VREF_AVREF has been defined.

5. Software Explanation

5.1 Operation Overview

This application uses the PGA and ADC to measure the voltage of one end of a shunt resistor and convert the result into the current value. When there is no current, the A/D conversion value is stored in RAM as the offset correction value to eliminate the effect of the PGA input offset voltage. After the voltage is converted to a current value, the current is measured in 1 second intervals. The offset correction value stored in RAM is subtracted from the measurement result and the current value is calculated. The three most recently measurement current values are retained in RAM.

Detailed specifications are as follows:

- Select the optimal gain (x1, x4, x8, x16, or x32) and measure the voltage of one end of the shunt resistor at the highest gain possible. (When x1: PGA is not used.)
- Use PGAGND as PGA(-) input.
- The PGA input offset correction is only applied to the + side. Input offset voltage is measured 10 times for each gain x1 to x32. The resulting mean value is stored in RAM as the gain x1 to x32 offset correction value.
- The ADC reference voltage setting can be changed by the constant definition.

Constant VREF_AVREF is defined as the default; ADC reference voltage $AV_{REF}(+)$ is set to AV_{REFP} and $AV_{REF}(-)$ to AV_{REFM}. If this definition is removed, $AV_{REF}(+)$ is set to V_{DD} and $AV_{REF}(-)$ to V_{SS}

The user can also choose whether to set the AV_{REF} value in a constant or calculate it in a program. Constant VREF_FIX is defined as the default, and AV_{REF} is set in constant VREF_VOLTAGE. If this definition is removed, AV_{REF} is calculated from the A/D conversion results of the internal reference voltage (1.45 V). We do not recommend using the internal reference voltage (1.45 V) for this application as it has an approximate -4.8% to +3.4% error which may affect the accuracy of the current measurement.

The processing flow for this application is described below (1 to 22).

(1) Initialize ports.

- Set P62 and P63 to high-level output, turn LED1 and LED2 off.
- Set P137 to input.

(2) Initialize TAU0.

< Settings >

- Channel 0 timer operation mode: interval timer mode
- Interval time: 1000ms
- INTTM00 interrupt generation: on completion of Timer channel 0 counter
- Interrupt priority: level 3

(3) Initialize A/D converter.

< Settings >

- Enable comparator operation.
- Resolution: 10 bits
- $V_{REF}(+)$:

  When defining constant VREF_AVREF, use AV_{REFP}.

  When defining constant VREF_AVREF, use V_{DD}.

- $V_{REF}(-)$

  When defining constant VREF_AVREF, use AV_{REFM}.

  When defining constant VREF_AVREF, use V_{SS}.
- Trigger mode: software trigger mode
- Operation mode: one-shot select mode
- Analog input pin: only AN12 (Cannot be selected with code generation tool due to use of PGA.)
- Conversion start channel: PGAOUT
- Conversion time mode: reference 1
- Conversion time: $1216/f_{CLK}$(38μs)
- Conversion result maximum/minimum values: interrupt request signal (INTAD) is generated when ADLL ≤ ADCRH ≤ ADUL)
- A/D interrupt: enabled
- Interrupt priority: level 3

(4) Initialize comparator/programmable gain amplifier.

< Settings >

- Programmable gain amplifier enabled
- Programmable gain amplifier GND: use PGAGND
- Gain setting: x4

(5) Initialize main processing.

< Settings >

- Initialize variables.
  - Current value storage buffer number variable g_current_cnt: set to “0”

(6) Start PGA.

- PGACTL register PGAEN bit: set to “1” (programmable gain amplifier operation is enabled)

(7) Start ADC.

- IF1H register ADIF bit: set to “0” (interrupt request signal is not generated)
- MK1H register ADMK bit: set to “0” (interrupt processing is enabled)
- ADM0 register ADCS bit: set to “1” (conversion operation is enabled)

(8) Start TAU0 timer.

(9) Enable interrupts.

(10) Transition to SW1 press wait state

(11) Set gain

For gain x1:

- Set ADS register to “02H” (P22/ANI2).

For gains x4 to x32:

- Set ADS register to “19H” (PGAOUT).

For gain x4:

- Set PGACTL register bits GAVG1 and PGAVG0 to “00B” (x4).

For gain x8:

- Set PGACTL register bits PGAVG1 and PGAVG0 to “01B” (x8).

For gain x16:

- Set PGACTL register bits PGAVG1 and PGAVG0 to “10B” (x16).

For gain x32:

- Set PGACTL register bits PGAVG1 and PGAVG0 to “11B” (x32).

(12) Get offset correction value.

Get offset correction values corresponding to set gains (average of 10 A/D conversion values) and store in RAM.

(13) Repeat steps (11) and (12) to acquire offset correction values for factors x1, x4, x8, x16, and x32.

(14) Turn on LED1 (indicating offset correction value setting is complete)

(15) Set V_{REF} voltage.

・When constant VREF_FIX is defined (default):

【VREF】= VREF_VOLTAGE

・When not defined as above, calculate from internal reference voltage (1.45 V).

Get A/D conversion value of internal reference voltage (1.45 V).

- Set ADS register to “81H” (internal reference voltage).
- Get average of 10 A/D conversion values.

Calculate V_{REF} with following expression.

[VREF] = ([VREFA/D conversion value (0x3FF)] x [1.45 V]) / [A/D conversion value of internal reference voltage (1.45 V)]

(16) Reset the current value storage buffer number if buffer is at maximum (DATACNT).

(17) Select the optimum gain (x1, x4, x8, x16, or x32) to get the A/D conversion value (refer to section **5.2 Gain Selection**).

- Get the A/D conversion value.
- Correct the A/D conversion value with the offset correction value of the selected gain.

- If the corrected A/D conversion value is equal to or less than the minimum A/D conversion result defined for the corresponding gain, increase the factor and repeat step (17).
- If the corrected A/D conversion value is the higher than the maximum A/D conversion result defined for the corresponding gain, decrease the factor and repeat step (17).

(18) Calculate ADC input voltage value.

Input voltage is calculated with the following expression:

[ADC input voltage] = ([ADC input voltage A/D conversion value] x [VREF]) / [VREF A/D conversion value (0x3FF)]

(19) Calculate input voltage (PGAI/ANI2) value.

[Input voltage] = [ADC input voltage] / [gain]

(20) Calculate current value, then store in RAM.

[Current value] = [input voltage] / [shunt resistor]

(21) Invert LED2 display (current measurement in process)

(22) Repeat steps (16) to (21).

5.2 Gain Selection

This section explains how to select the gain.

The PGA gain is increased or decreased after judging the A/D conversion value. Each gain must be set with thresholds to indicate whether the factor should be increased or decreased. Table 5.1 provides the list of threshold values, while Figure 5.1 shows the threshold calculation method. Refer to Figure 5.34 Gain Setting for instructions on how to select the gain.

Table 5.1 Gain Selection Conditions

Gain	A/D Conversion Value (Threshold)	
	Minimum value	Maximum value
x1	220	1023
x4	450	920
x8	450	920
x16	450	920
x32	0	920

If the measured, A/D conversion value is within the range of values stated in Table 5.1, the gain is fixed.

If the value is equal to or less than the minimum value, (excluding x32), the gain is increased and re-judged.

If the value is higher than the maximum value, (excluding x1), the gain is decreased and re-judged.

Figure 5.1 shows the calculation method for determining the threshold of each gain.

A/D conversion value (min):

$$\text{Minimum value} = \frac{(0.9 \times \text{【VREF】})}{\text{[next factor]}} \times \text{[factor]} \times \frac{1023}{\text{【VREF】}} = \frac{\text{[factor]}}{\text{[next factor]}} \times 0.9 \times 1023$$

$$\text{min (if x1)} = \frac{1}{4} \times 0.9 \times 1023 \fallingdotseq 230 - 10(*1) = 220$$

$$\text{max (if x4 to x32)} = \frac{1}{2} \times 0.9 \times 1023 \fallingdotseq 460 - 10(*1) = 450$$

∗1 The minimum value is decreased by 10 to avoid instances where the value range is too close to the threshold to be determined.

A/D conversion value (max):

$$\text{Maximum value} = \frac{(0.9 * \text{【VREF】})}{\text{[factor]}} * \text{[factor]} * \frac{1023}{\text{【VREF】}} = 0.9 * 1023 \fallingdotseq 920$$

Figure 5.1 Threshold Calculation Method For Gain

5.3 Option Byte Settings

Table 5.2 provides the list of option byte settings.

Table 5.2 Option Byte Settings

Address	Setting Value	Description
000C0H/010C0H	1110 1111B	Watchdog timer disabled (count stopped after reset release)
000C1H/010C1H	1111 1111B	LVD operation: off
000C2H/010C2H	1110 1000B	HS (high-speed main) mode (f_{HOCO}) clock: 32MHz、(f_{IH}) clock: 32MHz
000C3H/010C3H	1000 0100B	On-chip debug enabled Erases flash memory data when on-chip debug security ID recognition fails.

5.4 Constants

Table 5.3 provides the list of constants used by the application.

Table 5.3 Constants

Constant Name	Setting Value	Description
VREF_AVREF	-	Defined (as default) when ADC uses AV_{REFP}/AV_{REFM} as AV_{REF}. When not defined, AV_{REF} is set to V_{DD}/V_{SS}. *To change, refer in Table 1.1
VREF_FIX	-	Defined (as default) when the voltage value defined in VREF_VOLTAGE is used as AV_{REF}. When not defined, AV_{REF} becomes the value calculated from the internal reference voltage. *To change, refer to Table 1.1 A/D Converter Reference Voltage Setting Changes Based on Constant Definitions
VREF_VOLTAGE	5.0	AV_{REF} voltage; used when VREF_FIX is defined. *To change, set voltage to V_{DD} or lower.
DATACNT	3	Number of current value data stored in RAM
AVGCNT	10	Number of A/D conversions executed per voltage measurement (A/D conversion is executed this number of times, then the current is subtracted from the average value.)
SHUNT	100	Shunt resistor value (Ohm)
IREFV	1.45	Internal reference voltage (1.45 V)
RESOLUTION	0x3FF	RL78/G1F ADC resolution (10 bits)
LED_ON	0	LED on
LED_OFF	1	LED off
WAIT_1_US	0x001F	1 μs wait time: A/D voltage stabilization wait time.
WAIT_5_US	0x009F	5 μs wait time: PGA operation stabilization wait time (x4, x8)
WAIT_10_US	0x013F	10 μs wait time: PGA operation stabilization wait time (x16, x32)

5.5 Structures and Unions

Figure 5.2 shows the structures and unions used in the sample code.

```
typedef struct
{
    uint8_t     gain;                   /* Gain x1 to x32 */
    uint8_t     pgavg;                  /* For setting PGACTL(PGAVG1,PGAVG0) */
    uint16_t    min;                    /* A/D conversion minimum value */
    uint16_t    max;                    /* A/D conversion maximum value */
    uint16_t    wait_time;              /* wait time */
} pga_gain_info_t;

pga_gain_info_t g_pga_gain_tbl[]=       /* Gain information */
{   {  1, 0, 220, 1023, 0 },            /* For x1 */
    {  4, 0, 450,  920, WAIT_5_US },    /* For x 4 */
    {  8, 1, 450,  920, WAIT_5_US },    /* For x 8 */
    { 16, 2, 450,  920, WAIT_10_US },   /* For x 16 */
    { 32, 3,   0,  920, WAIT_10_US }    /* For x 32 */
};
```

Figure 5.2 Structures and Unions Used in Sample Code

5.6 Variables

Table 5.4 provides the list of global variables used by the application.

Table 5.4 Global Variables

Type	Variable Name	Contents	Function Used
pga_gain_info_t	g_pga_gain_tbl	Gain information	get_adc_vin set_gain set_current_to_ram
uint8_t	g_pga_gain	Gain index	get_adc_vin set_gain
uint16_t	g_pga_offset[]	Offset correction value	set_offset_value set_current_to_ram
uint8_t	g_adc_end_flag	A/D conversion complete flag	get_adc_avg_value r_adc_interrupt
uint16_t	g_current_cnt	Current value storage buffer number	R_MAIN_UserInit set_current_to_ram
float	g_current[]	Current value	set_current_to_ram
float	g_vref	VREF voltage	main
uint16_t	g_adc_vin	Input voltage A/D conversion value	main set_current_to_ram
uint16_t	g_adc_v145	Internal reference voltage A/D conversion value	main
uint8_t	g_tau_1s_flag	1 second lapsed flag	main r_tau0_channel0_interrupt
uint8_t	g_tau_ch1_int_flag	TAU channel 1 interrupt flag	wait_time r_tau0_channel1_interrupt

5.7 Functions

Table 5.5 lists the functions used in this application.

Table 5.5 Function List

Function Name	Description
hdwinit	Initialization
R_Systeminit	Peripheral function initialization
R_PORT_Create	Port initialization
R_CGC_Create	CPU clock initialization
main	main processing
R_MAIN_UserInit	main initialization
R_COMPPGA_Create	Programmable gain amp initialization
R_PGA_Start	Programmable gain amp operation enable processing
R_PGA_Stop	Programmable gain amp operation disable processing
R_ADC_Create	A/D converter initialization processing
R_ADC_Start	A/D converter start processing
R_ADC_Stop	A/D converter stop processing
R_ADC_Set_OperationOn	A/D voltage comparator operation enable processing
R_ADC_Set_OperationOff	A/D voltage comparator operation stop processing
R_ADC_Get_Result	conversion result acquisition processing
r_adc_interrupt	A/D conversion complete interrupt processing
R_TAU0_Create	Timer array unit initialization processing
R_TAU0_Channel0_Start	Timer array unit channel 0 operation enable processing
R_TAU0_Channel0_Stop	Timer array unit channel 0 operation stop processing
R_TAU0_Channel1_Start	Timer array unit channel 1 operation enable processing
R_TAU0_Channel1_Stop	Timer array unit channel 1 operation stop processing
r_tau0_channel0_interrupt	Timer array unit channel 0 interrupt processing
r_tau0_channel1_interrupt	Timer array unit channel 1 interrupt processing
set_offset_value	PGA offset setting processing
get_adc_avg_value	Average A/D conversion value acquisition processing
get_adc_vin	Input voltage A/D conversion value acquisition processing
get_adc_v145	Reference voltage A/D conversion value acquisition processing
set_gain	Gain setting processing
set_current_to_ram	Current calculation processing
wait_time	Wait time processing

5.8 Function Specifications

The following are the specifications of functions used in the sample code.

Function name: hdwinit

Outline	Initialization
Header	None
Declaration	void hdwinit(void)
Description	Initializes peripheral functions.
Argument	None
Return value	None
Notes	None

Function name: R_Systeminit

Outline	Peripheral function initialization
Header	None
Declaration	void R_Systeminit(void)
Description	Initializes the peripheral functions used in this application.
Argument	None
Return value	None
Notes	None

Function name: R_PORT_Create

Outline	Port initialization
Header	r_cg_port.h
Declaration	void R_PORT_Create(void)
Description	Initializes ports
Argument	None
Return value	None
Notes	None

Function name: R_CGC_Create

Outline	CPU clock initialization
Header	r_cg_cgc.h
Declaration	void R_CGC_Create(void)
Description	Initializes the CPU clock.
Argument	None
Return value	None
Notes	None

Function name: main

Outline	main processing
Header	None
Declaration	void main(void)
Description	After the main initialization is executed, the CPU goes to SW1 press wait state. After SW1 is pressed, the PGA offset correction value is set and LED1 turns on. The VREF voltage value is then acquired and current measurement continues.
Argument	None
Return value	None
Notes	None

Function name: R_MAIN_UserInit

Outline	main initialization
Header	None

Declaration	void R_MAIN_UserInit(void)
Description	After PGA and ADC have been initialized, PGA operations are started, A/D voltage comparator is enabled, and EI instruction enables interrupts.
Argument	None
Return value	None
Notes	None

Function name: R_COMPPGA_Create

Outline	Programmable gain amplifier initialization processing
Header	r_cg_cmppga.h
Declaration	void R_COMPPGA_Create(void)
Description	Initializes programmable gain amplifier.
Argument	None
Return value	None
Notes	None

Function name: R_PGA_Start

Outline	Programmable gain amplifier operation enable processing
Header	r_cg_cmppga.h
Declaration	void R_PGA_Start(void)
Description	Enables programmable gain amplifier operation.
Argument	None
Return value	None
Notes	None

Function name: R_PGA_Stop

Outline	Programmable gain amplifier operation disable processing
Header	r_cg_cmppga.h
Declaration	void R_PGA_Stop(void)
Description	Stops programmable gain amplifier operation.
Argument	None
Return value	None
Notes	None

Function name: R_ADC_Create

Outline	A/D converter initialization processing
Header	r_cg_adc.h
Declaration	void R_ADC_Create(void)
Description	Executes the A/D converter initialization processing.
Argument	None
Return value	None
Notes	None

Function name: R_ADC_Start

Outline	A/D converter start processing
Header	r_cg_adc.h
Declaration	void R_ADC_Start(void)
Description	Executes the A/D converter start processing.
Argument	None
Return value	None
Notes	None

Function name: R_ADC_Stop

Outline	A/D converter stop processing
Header	r_cg_adc.h
Declaration	void R_ADC_Stop(void)
Description	Executes the A/D converter stop processing.
Argument	None
Return value	None
Notes	None

Function name: R_ADC_Set_OperationOn

Outline	A/D voltage comparator operation enable processing
Header	r_cg_adc.h
Declaration	void R_ADC_Set_OperationOn(void)
Description	Executes A/D voltage comparator operation enable process.
Argument	None
Return value	None
Notes	None

Function name: R_ADC_Set_OperationOff

Outline	A/D voltage comparator operation stop processing
Header	r_cg_adc.h
Declaration	void R_ADC_Set_OperationOff(void)
Description	Executes A/D voltage comparator operation stop processing.
Argument	None
Return value	None
Notes	None

Function name: R_ADC_Get_Result

Outline	A/D conversion result acquisition processing
Header	r_cg_adc.h
Declaration	void R_ADC_Get_Result(uint16_t * const buffer)
Description	Executes the A/D conversion result acquisition processing
Argument	buffer
Return value	None
Notes	None

Function name: r_adc_interrupt

Outline	A/D conversion complete interrupt processing
Header	None
Declaration	__interrupt static void r_adc_interrupt(void)
Description	Sets the A/D conversion complete flag.
Argument	None
Return value	None
Notes	None

Function name: R_TAU0_Create

Outline	Timer array unit initialization processing
Header	r_cg_tau.h
Declaration	void R_TAU0_Create(void)
Description	Executes timer array unit initialization processing.
Argument	None
Return value	None
Notes	None

Function name: R_TAU0_Channel0_Start

Outline	Timer array unit channel 0 operation enable processing
Header	r_cg_tau.h
Declaration	void R_TAU0_Channel0_Start(void)
Description	Executes Timer array unit channel 0 operation enable processing.
Argument	None
Return value	None
Notes	None

Function name: R_TAU0_Channel0_Stop

Outline	Timer array unit channel 0 operation stop processing
Header	r_cg_tau.h
Declaration	void R_TAU0_Channel0_Stop(void)
Description	Executes timer array unit channel 0 operation stop processing.
Argument	None
Return value	None
Notes	None

Function name: R_TAU0_Channel1_Start

Outline	Timer array unit channel 1 operation enable processing
Header	r_cg_tau.h
Declaration	void R_TAU0_Channel1_Start(void)
Description	Executes timer array unit channel 1 operation enable processing.
Argument	None
Return value	None
Notes	None

Function name: R_TAU0_Channel1_Stop

Outline	Timer array unit channel 1 operation stop processing
Header	r_cg_tau.h
Declaration	void R_TAU0_Channel1_Stop(void)
Description	Executes Timer array unit channel 1 operation stop processing.
Argument	None
Return value	None
Notes	None

Function name: r_tau0_channel0_interrupt

Outline	Timer array unit channel 0 interrupt processing
Header	None
Declaration	__interrupt static void r_tau0_channel0_interrupt(void)
Description	Sets the 1 second lapsed flag.
Argument	None
Return value	None
Notes	None

Function name: r_ tau0_channel1_interrupt

Outline	Timer array unit channel 1 interrupt processing
Header	None
Declaration	__interrupt static void r_tau0_channel1_interrupt(void)
Description	Sets the TAU channel 1 interrupt flag.
Argument	None
Return value	None
Notes	None

Function name: set_offset_value

Outline	PGA offset setting processing
Header	None
Declaration	void set_offset_value(void)
Description	Executes the PGA offset correction setting processing.
Argument	None
Return value	None
Notes	None

Function name: get_adc_avg_value

Outline	Average A/D conversion value acquisition processing	
Header	None	
Declaration	uint16_t get_adc_avg_value(uint16_t data_cnt)	
Description	Executes the average A/D conversion value acquisition processing.	
Argument	data_cnt	Data count (number of data)
Return value	Average A/D conversion value	
Notes	None	

Function name: get_adc_vin

Outline	Input voltage A/D conversion value acquisition processing
Header	None
Declaration	uint16_t get_adc_vin(void)
Description	Execute input voltage A/D conversion value acquisition processing.
Argument	None
Return value	Input voltage A/D conversion value
Notes	None

Function name: get_adc_v145

Outline	Reference voltage A/D conversion value acquisition processing	
Header	None	
Declaration	uint16_t get_adc_v145(void)	
Description	Executes reference voltage A/D conversion value acquisition processing.	
Argument	None	
Return value	Internal reference voltage A/D conversion value	
Notes	None	

Function name: set_gain

Outline	Gain setting processing	
Header	None	
Declaration	void set_gain(uint8_t gain)	
Description	Executes gain setting processing.	
Argument	gain	Gain
Return value	None	
Notes	None	

Function name: set_current_to_ram

Outline	Current calculation processing	
Header	None	
Declaration	void set_current_to_ram(void)	
Description	Executes current calculation processing. Calculates current value and stores in RAM.	
Argument	None	
Return value	None	
Notes	None	

Function name: wait_time

Outline	Wait time processing	
Header	None	
Declaration	void wait_time(uint16_t time)	
Description	Executes wait time processing.	
Argument	time	Wait time
Return value	None	
Notes	None	

5.9 Flowcharts

Figure 5.3 shows the overall flow of the sample code described in this application note.

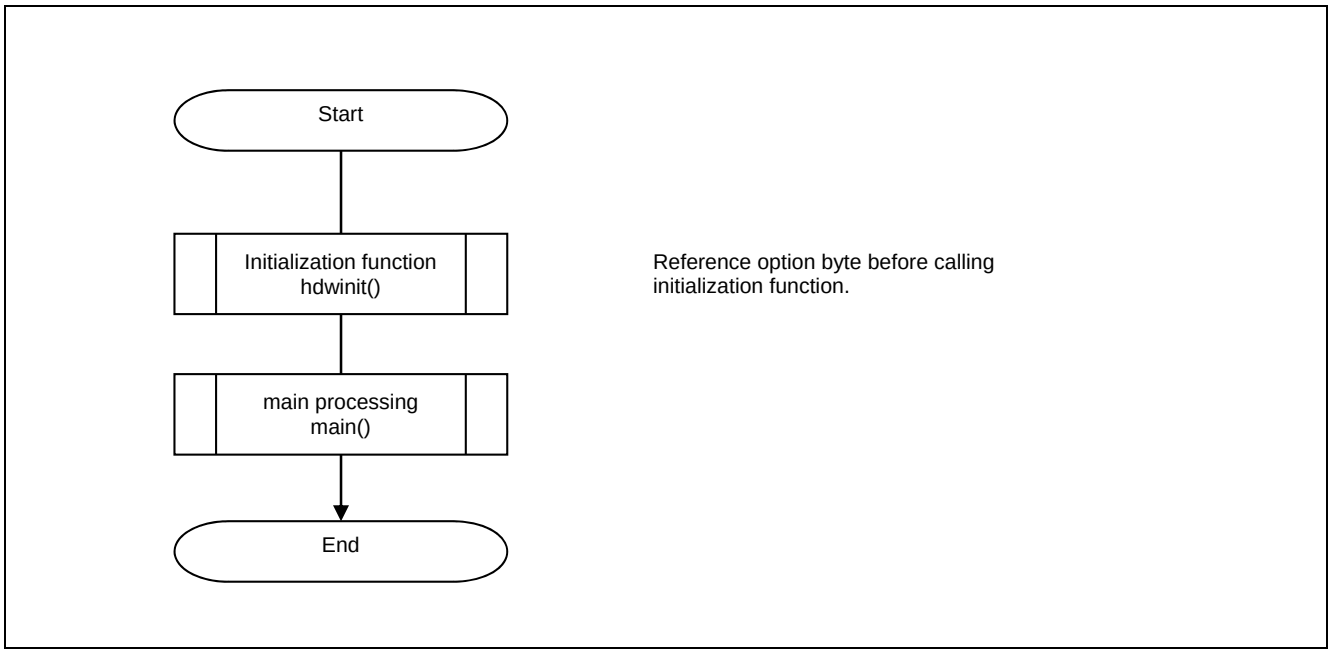

Figure 5.3 Overall Flow

5.9.1 Initialization

Figure 5.4 shows the flowchart for initialization.

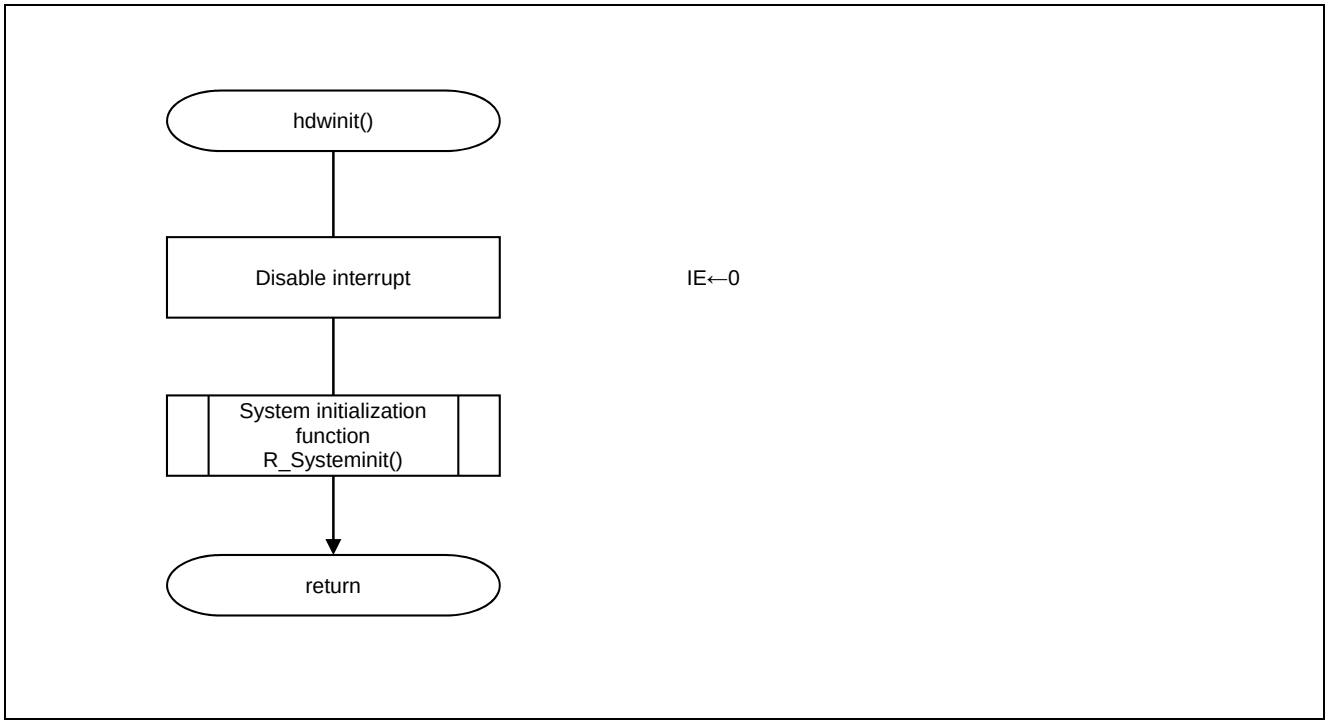

Figure 5.4 Initialization

5.9.2 Peripheral Function Initialization

Figure 5.5 shows the flowchart for setting the peripheral functions.

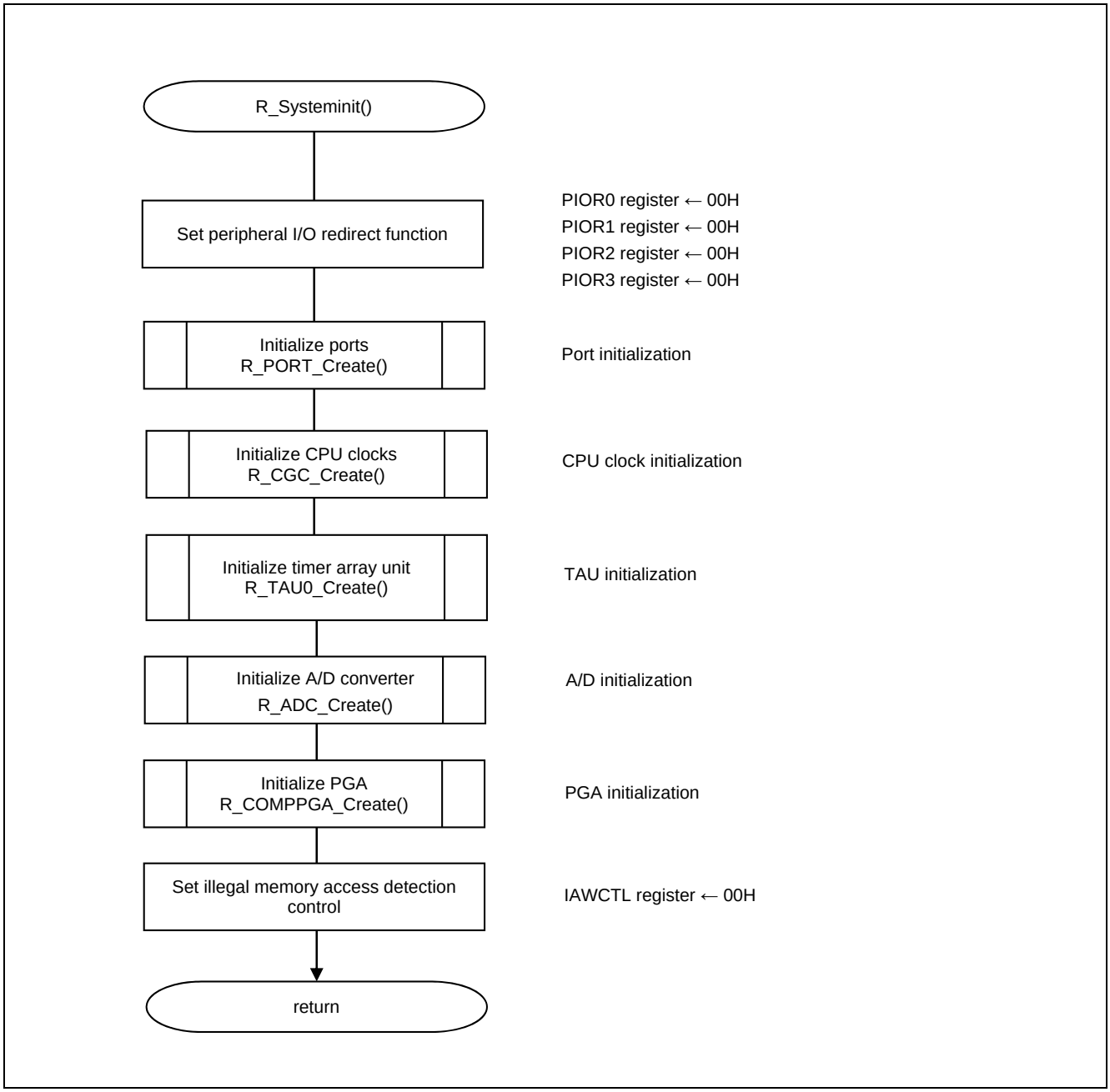

Figure 5.5 Peripheral Function Initialization

5.9.3 CPU Clock Initialization

Figure 5.6 shows the flowchart for initializing the CPU clocks.

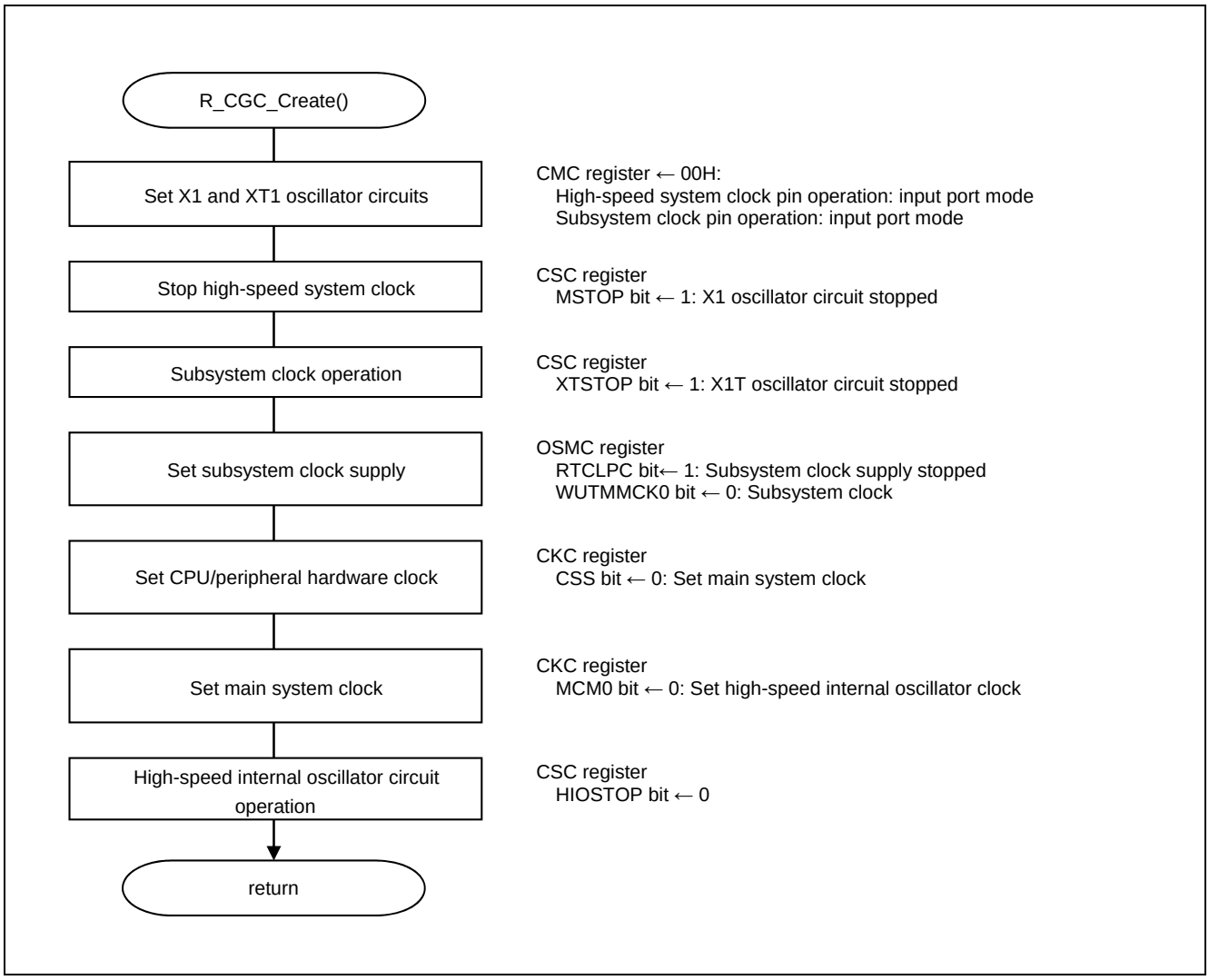

Figure 5.6 CPU Clock Initialization

5.9.4 Port Initialization

Figure 5.7 shows the flowchart for port initialization.

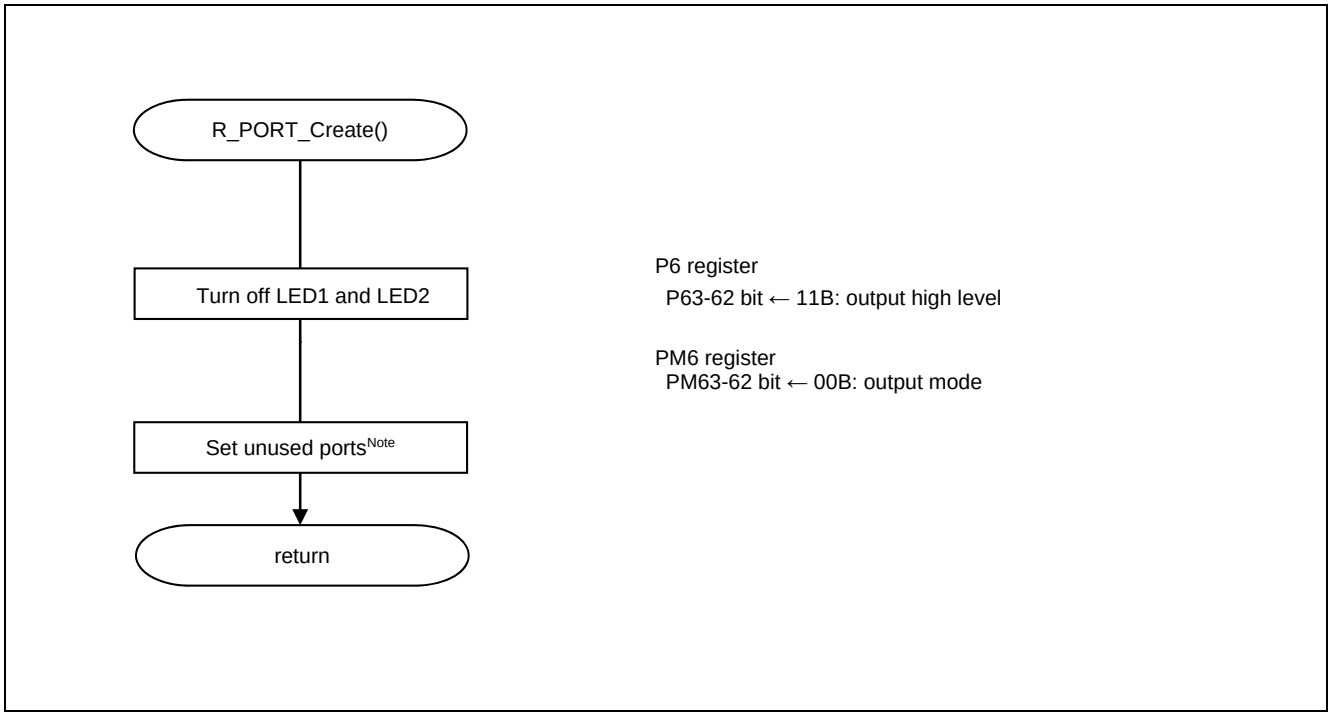

Figure 5.7 Port Initialization

Note To set unused ports, refer to the section on Flowcharts in the RL78/G13 Initialization (R01AN0451E) Application Note.

Caution When designing circuits, always make sure unused ports are properly processed and all electrical characteristics are met.

Also make sure each unused input-only port is connected to V_{DD} or V_{SS} through a resister.

5.9.5 TAU0 Initialization

Figure 5.8 and Figure 5.9 show the flowchart for TAU initialization.

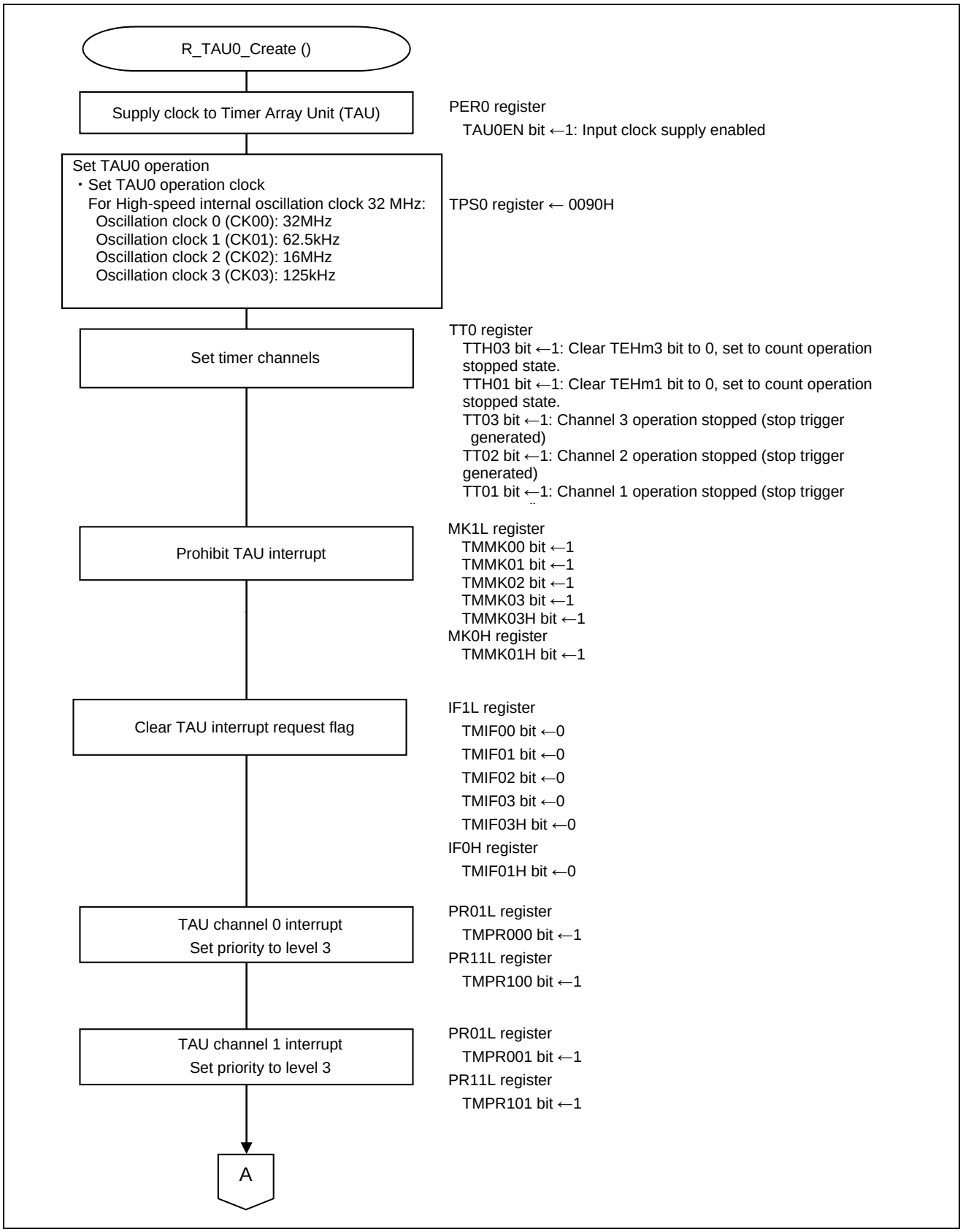

Figure 5.8 TAU0 Setting (1/2)

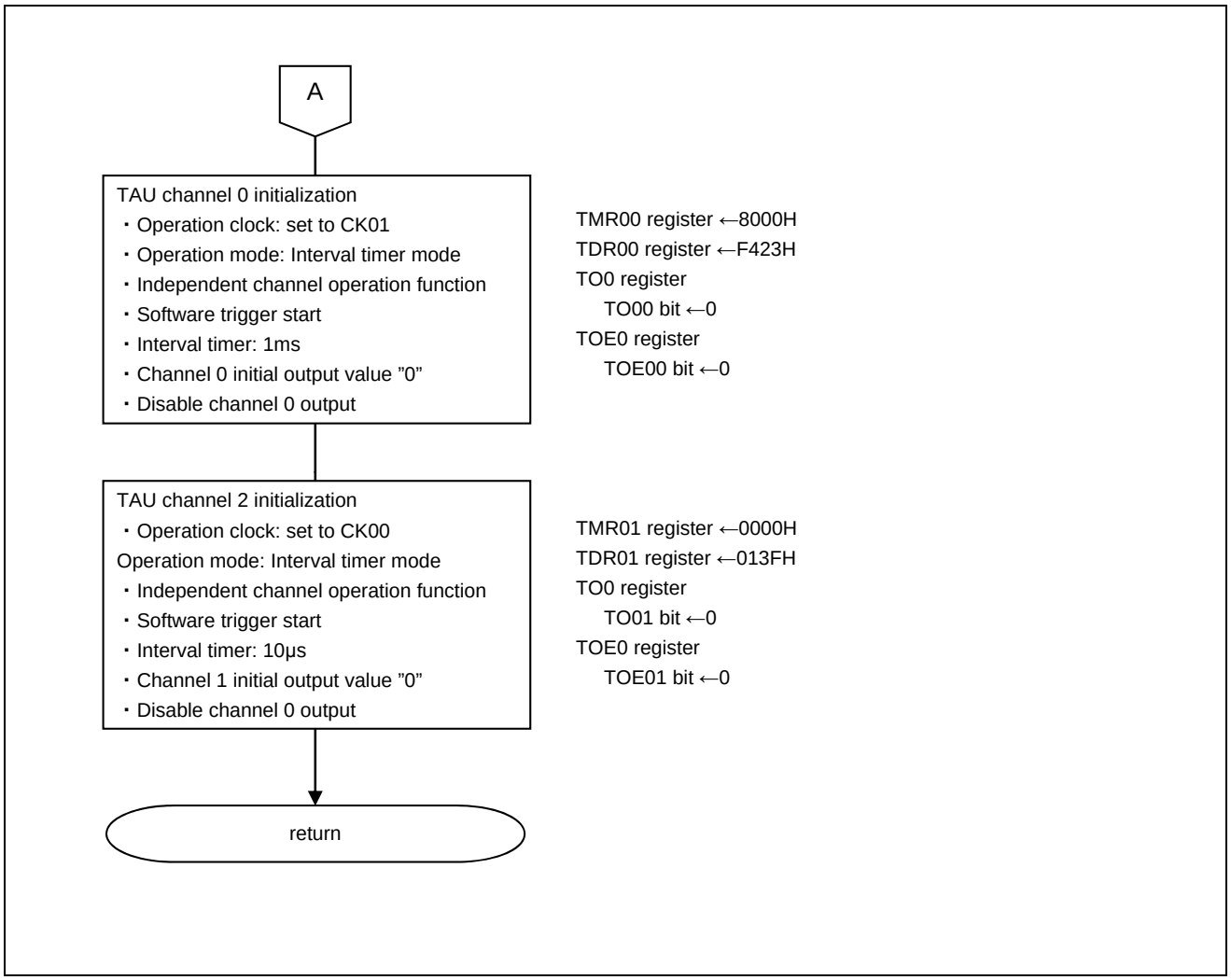

Figure 5.9 TAU0 Setting (2/2)

Start clock supply to timer array unit 0

・Peripheral enable register 0 (PER0)
Start clock supply to timer array unit.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IRDAEN	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN
x	x	x	x	x	x	0	**1**

Bit 5

TAU0EN	Control of A/D converter input clock
0	Stops input clock supply.
1	**Supplies input clock.**

Timer clock frequency setting

・Timer clock select register 0 (TPS0)
Select operation clock.

Symbol: TPS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	PRS 031	PRS 030	0	0	PRS 021	PRS 020	PRS 013	PRS 012	PRS 011	PRS 010	PRS 003	PRS 002	PRS 001	PRS 000
0	0	**0**	**0**	0	0	**0**	**0**	**1**	**0**	**0**	**1**	**0**	**0**	**0**	**0**

Bits 13-12

PRS 031	PRS 030	Selection of operation clock (CK03)Note					
			f_{CLK}= 2MHz	f_{CLK}= 4MHz	f_{CLK}= 8MHz	f_{CLK}= 20MHz	f_{CLK}= 32MHz
0	**0**	**$f_{CLK}/2^8$**	**7.81kHz**	**15.6kHz**	**31.25kHz**	**78.1kHz**	**125kHz**
0	1	$f_{CLK}/2^{10}$	1.95kHz	3.91kHz	7.81kHz	19.5kHz	31.3kHz
1	0	$f_{CLK}/2^{12}$	488Hz	977Hz	1.95kHz	4.88kHz	7.81kHz
1	1	$f_{CLK}/2^{14}$	122Hz	244Hz	488Hz	1.22kHz	1.95kHz

Bits 9-8

PRS 021	PRS 020	Selection of operation clock (CK02)Note					
			f_{CLK}= 2MHz	f_{CLK}= 4MHz	f_{CLK}= 8MHz	f_{CLK}= 20MHz	f_{CLK}= 32MHz
0	**0**	**$f_{CLK}/2$**	**1MHz**	**2MHz**	**4MHz**	**10MHz**	**16MHz**
0	1	$f_{CLK}/2^2$	500kHz	1MHz	2MHz	5MHz	8MHz
1	0	$f_{CLK}/2^4$	125kHz	250kHz	500kHz	1.25MHz	2MHz
1	1	$f_{CLK}/2^6$	31.3kHz	62.5kHz	125kHz	313kHz	500kHz

Bits 7-4

PRS 013	PRS 012	PRS 011	PRS 010		Selection of operation clock (CK01)Note				
					f_{CLK}= 2MHz	f_{CLK}= 4MHz	f_{CLK}= 8MHz	f_{CLK}= 20MHz	f_{CLK}= 32MHz
0	0	0	0	f_{CLK}	2MHz	4MHz	8MHz	20MHz	32MHz
0	0	0	1	$f_{CLK}/2$	1MHz	2MHz	4MHz	10MHz	16MHz
0	0	1	0	$f_{CLK}/2^2$	500kHz	1MHz	2MHz	5MHz	8MHz
0	0	1	1	$f_{CLK}/2^3$	250kHz	500kHz	1MHz	2.5MHz	4MHz
0	1	0	0	$f_{CLK}/2^4$	125kHz	250kHz	500kHz	1.25MHz	2MHz
0	1	0	1	$f_{CLK}/2^5$	62.5kHz	125kHz	250kHz	625kHz	1MHz
0	1	1	0	$f_{CLK}/2^6$	31.3kHz	62.5kHz	125kHz	313kHz	500kHz
0	1	1	1	$f_{CLK}/2^7$	15.6kHz	31.25kHz	62.5kHz	156kHz	250kHz
1	0	0	0	$f_{CLK}/2^8$	7.81kHz	15.6kHz	31.25kHz	78.1kHz	125kHz
1	**0**	**0**	**1**	**$f_{CLK}/2^9$**	**3.91kHz**	**7.81kHz**	**15.6kHz**	**39.1kHz**	**62.5kHz**
1	0	1	0	$f_{CLK}/2^{10}$	1.95kHz	3.91kHz	7.81kHz	19.5kHz	31.3kHz
1	0	1	1	$f_{CLK}/2^{11}$	977Hz	1.95kHz	3.91kHz	9.77kHz	15.6kHz
1	1	0	0	$f_{CLK}/2^{12}$	488Hz	977Hz	1.95kHz	4.88kHz	7.81kHz
1	1	0	1	$f_{CLK}/2^{13}$	244Hz	488Hz	977Hz	2.44kHz	3.91kHz
1	1	1	0	$f_{CLK}/2^{14}$	122Hz	244Hz	488Hz	1.22kHz	1.95kHz
1	1	1	1	$f_{CLK}/2^{15}$	61.0Hz	122Hz	244Hz	610Hz	977Hz

Bits 3-0

PRS 003	PRS 002	PRS 001	PRS 000		Selection of operation clock (CK00)Note				
					f_{CLK}= 2MHz	f_{CLK}= 4MHz	f_{CLK}= 8MHz	f_{CLK}= 20MHz	f_{CLK}= 32MHz
0	**0**	**0**	**0**	**f_{CLK}**	**2MHz**	**4MHz**	**8MHz**	**20MHz**	**32MHz**
0	0	0	1	$f_{CLK}/2$	1MHz	2MHz	4MHz	10MHz	16MHz
0	0	1	0	$f_{CLK}/2^2$	500kHz	1MHz	2MHz	5MHz	8MHz
0	0	1	1	$f_{CLK}/2^3$	250kHz	500kHz	1MHz	2.5MHz	4MHz
0	1	0	0	$f_{CLK}/2^4$	125kHz	250kHz	500kHz	1.25MHz	2MHz
0	1	0	1	$f_{CLK}/2^5$	62.5kHz	125kHz	250kHz	625kHz	1MHz
0	1	1	0	$f_{CLK}/2^6$	31.3kHz	62.5kHz	125kHz	313kHz	500kHz
0	1	1	1	$f_{CLK}/2^7$	15.6kHz	31.25kHz	62.5kHz	156kHz	250kHz
1	0	0	0	$f_{CLK}/2^8$	7.81kHz	15.6kHz	31.25kHz	78.1kHz	125kHz
1	0	0	1	$f_{CLK}/2^9$	3.91kHz	7.81kHz	15.6kHz	39.1kHz	62.5kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.95kHz	3.91kHz	7.81kHz	19.5kHz	31.3kHz
1	0	1	1	$f_{CLK}/2^{11}$	977Hz	1.95kHz	3.91kHz	9.77kHz	15.6kHz
1	1	0	0	$f_{CLK}/2^{12}$	488Hz	977Hz	1.95kHz	4.88kHz	7.81kHz
1	1	0	1	$f_{CLK}/2^{13}$	244Hz	488Hz	977Hz	2.44kHz	3.91kHz
1	1	1	0	$f_{CLK}/2^{14}$	122Hz	244Hz	488Hz	1.22kHz	1.95kHz
1	1	1	1	$f_{CLK}/2^{15}$	61.0Hz	122Hz	244Hz	610Hz	977Hz

Timer channel setting

・Timer channel stop register 0 (TT0)

Set each channel to stop count operation.

Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TTH03	0	TTH01	0	0	0	0	0	TT03	TT02	TT01	TT00
0	0	0	0	**1**	0	**1**	0	0	0	0	0	**1**	**1**	**1**	**1**

Bit 11

TTH03	Trigger to stop operation of the higher 8-bit timer when channel 3 is in the 8-bit timer mode
1	No trigger operation
1	TEH03 bit is cleared to 0 and the count operation is stopped.

Bit 9

TTH01	Trigger to stop operation of the higher 8-bit timer when channel 1 is in the 8-bit timer mode
1	No trigger operation
1	TEH01 bit is cleared to 0 and the count operation is stopped.

Bits 3-0

TT0n	Operation stop trigger of channel n
1	**TE0n bit is cleared to 0 and the count operation is stopped.**
1	Operation is stopped (stop trigger is generated). The bit is the trigger to stop operation of the lower 8-bit timer for TT01 and TT03 when channel 1 or 3 is in the 8-bit timer mode.

Note n: channel number (n = 0-3)

TAU interrupt disable

・Interrupt mask flag registers (MK1L, MK0H)
Disable TAU interrupt.

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
1	**1**	**1**	**1**	x	**1**	x	x

Bits 7-0

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol: : MK0H

7	6	5	4	3	2	1	0
SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	1	1	SREMK2	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
1	x	x	x	x	x	x	x

Bits 7-0

XXMKX	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

TAU interrupt request flag clear

・Interrupt request flag registers (IF1L, IF0H)
Clear TAU interrupt request flag.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
0	**0**	**0**	**0**	x	**0**	x	x

Bits 7-0

XXIFX	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status.

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	0	0	SREIF2	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
0	x	x	0	0	x	x	x

Bits 7-0

XXIFX	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status.

TAU interrupt priority setting

・Priority level specification flag register (PR01L, PR11L)
Set TAU interrupt priority level to 3.

Symbol: PR01L

7	6	5	4	3	2	1	0
TMPR003	TMPR002	TMPR001	TMPR000	IICAPR00	SREPR01 TMPR003H	SRPR01 CSIPR011 IICPR011	STPR01 CSIPR010 IICPR010
x	x	x	**1**	x	x	x	x

Symbol: PR11L

7	6	5	4	3	2	1	0
TMPR103	TMPR102	TMPR101	TMPR100	IICAPR10	SREPR11 TMPR103H	SRPR11 CSIPR111 IICPR111	STPR11 CSIPR110 IICPR110
x	x	x	**1**	x	x	x	x

Bit 4

TMPR100	TMPR000	Selection of priority level
0	**0**	**Specify level 0 (high priority level)**
0	**1**	Specify level 1
1	**0**	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

Channel 0 operation mode setting

・Timer mode register 00 (TMR00)
Set operation clock (f_{MCK}) to CK00.
Set to interval timer mode.
Set to software trigger start.

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
1	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bits 15-14

CKS 001	CKS 000	Selection of channel n operation clock (f_{MCK})
0	0	Operation clock CK00 set by timer clock select register 0 (TPS0)
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	**0**	Operation clock CK01 set by timer clock select register 0 (**TPS0)**
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CCS00	Selection of channel 0 count clock (f_{TCLK})
0	**Operation clock (f_{MCK}) specified by bits CKS000 and CKS001**
1	Valid edge of the input signal from the TI00 pin In channel 0: Valid edge of the input signal selected by TIS0 In channel 1: Valid edge of the input signal selected by TIS0 In channel 3: Valid edge of the input signal selected by ISC

Bits 10-8

STS 002	STS 001	STS 000	Setting of channel 0 start trigger or capture trigger
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected)**
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both edges of the TI00 pin are used as start triggers, one each for start and capture.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than the above			Setting prohibited

Bits 7-6

CIS 001	CIS 000	Selection of TI00 pin valid edge
0	**0**	**Rising edge**
0	1	Falling edge
1	0	Both edges (when low-level width is measured) Start trigger: falling edge; Capture trigger: rising edge
1	1	Both edges (when high-level width is measured) Start trigger: rising edge; Capture trigger: falling edge

Symbol: TMR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bits 3-1

MD 003	MD 002	MD 001	Operation mode of channel n	Corresponding function	Count operation of TCR
0	**0**	**0**	**Interval timer mode**	**Interval timer / Square wave output / Divider function / PWM output (master)**	**Counting down**
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than the above			Setting prohibited		

Bit 0

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD 000	Setting of starting counting and interrupt
· **Interval timer mode (0, 0, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either)**
· Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes)
· Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer does not change, either)
· One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation[Note 3]. At that time, interrupt is not generated.
· Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either) Start trigger is invalid during counting operation. At that time, interrupt is not generated.

Interval timer period setting

・Timer data register 00 (TDR00)
Set interval timer.

Symbol: TDR00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**1**

Timer output setting

・Timer output register 0 (TO0)
Set channel 0 initial output to “0”.

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TO03	TO02	TO01	TO00
0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**0**	**0**

Bit 0

TO00	Channel 0 timer output
0	**Timer output value is “0”.**
1	Timer output value is “1”.

Timer output disable setting

・Timer output enable register 0 (TOE0)
Set channel 0 to output disabled.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE 03	TOE 02	TOE 01	TOE 00
0	0	0	0	0	0	0	0	0	0	0	0	**0**	**0**	**0**	**0**

Bit 0

TOE00	Channel 0 timer output enable/disable
0	Timer output is disabled. Timer operation is not applied to the TOmn bit and the output is fixed. Writing to the TOmn bit is enabled and the level set in the TOmn bit is output from the TOmn pin.
1	Timer output is enabled. Timer operation is applied to the TOmn bit and an output waveform is generated. Writing to the TOmn bit is ignored.

Channel 1 operation mode setting

・Timer mode register 0 (TMR01)
Select operation clock ($f_{MCK.}$).
Set to interval timer mode.
Set to software trigger start

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	SPLIT 00	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bits 15-14

CKS 001	CKS 000	Selection of channel n operation clock (f_{MCK})
0	**0**	Operation clock CK00 set by timer clock select register 0 (**TPS0)**
0	1	Operation clock CK02 set by timer clock select register 0 (TPS0)
1	0	Operation clock CK01 set by timer clock select register 0 (TPS0)
1	1	Operation clock CK03 set by timer clock select register 0 (TPS0)

Bit 12

CSS00	Selection of channel 0 count clock (f_{TCLK})
0	**Operation clock (f_{MCK}) specified by bits CKS000 and CKS001**
1	Valid edge of the input signal from the TI00 pin In channel 0: Valid edge of the input signal selected by TIS0 In channel 1: Valid edge of the input signal selected by TIS0 In channel 3: Valid edge of the input signal selected by ISC

Bits 10-8

STS 002	STS 001	STS 000	Setting of channel 0 start trigger or capture trigger
0	**0**	**0**	**Only software trigger start is valid (other trigger sources are unselected)**
0	0	1	Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.
0	1	0	Both edges of the TI00 pin are used as start triggers, one each for start and capture.
1	0	0	Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).
Other than the above			Setting prohibited

Bits 7-6

CIS 001	CIS 000	Selection of TI00 pin valid edge
0	**0**	**Falling edge**
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: falling edge; Capture trigger: rising edge
1	1	Both edges (when high-level width is measured) Start trigger: rising edge; Capture trigger: falling edge

Symbol: TMR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CKS 001	CKS 000	0	CCS 00	0	STS 002	STS 001	STS 000	CIS 001	CIS 000	0	0	MD 003	MD 002	MD 001	MD 000
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bits 3-1

MD 003	MD 002	MD 001	Operation mode of channel n	Corresponding function	Count operation of TCR
0	**0**	**0**	**Interval timer mode**	**Interval timer / Square wave output / Divider function / PWM output (master)**	**Counting down**
0	1	0	Capture mode	Input pulse interval measurement	Counting up
0	1	1	Event counter mode	External event counter	Counting down
1	0	0	One-count mode	Delay counter / One-shot pulse output / PWM output (slave)	Counting down
1	1	0	Capture & one-count mode	Measurement of high-/low-level width of input signal	Counting up
Other than the above			Setting prohibited		

Bit 0

Operation mode (Value set by the MD003 to MD001 bits (see table above))	MD 000	Setting of starting counting and interrupt
· **Interval timer mode (0, 0, 0)**	**0**	**Timer interrupt is not generated when counting is started (timer output does not change, either)**
· Capture mode (0, 1, 0)	1	Timer interrupt is generated when counting is started (timer output also changes)
· Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer does not change, either)
· One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, interrupt is not generated.
	1	Start trigger is valid during counting operation[Note 3]. At that time, interrupt is not generated.
· Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either) Start trigger is invalid during counting operation. At that time, interrupt is not generated.

Interval timer period setting

・Timer data register 01 (TDR01)
Set interval timer

Symbol: TDR01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**	**1**	**1**	**1**	**1**

Timer output setting

・Timer output register 0 (TO0)
Set channel 1 initial output to “0”.

Timer output disable setting

Symbol: TO0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TO03	TO02	TO01	TO00
0	0	0	0	0	0	0	0	0	0	0	0	x	x	**0**	x

Bit 1

TO01	Channel 1 timer output
0	**Timer output value is “0”.**
1	Timer output value is “1”.

・Timer output enable register 0 (TOE0)
Set channel 1 to output disabled.

Symbol: TOE0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOE03	TOE02	TOE01	TOE00
0	0	0	0	0	0	0	0	0	0	0	0	x	x	**0**	x

Bit 1

TOE01	Channel 1 timer output enable/disable
0	**Timer output is disabled.** Timer operation is not applied to the TOmn bit and the output is fixed. Writing to the TOmn bit is enabled and the level set in the TOmn bit is output from the TOmn pin.
1	Timer output is enabled. Timer operation is applied to the TOmn bit and an output waveform is generated. Writing to the TOmn bit is ignored.

Timer output mode setting

・Timer output mode register 0 (TOM0)

Set channel output mode to master channel output mode.

Symbol: TOM0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOM03	TOM02	TOM01	0
0	0	0	0	0	0	0	0	0	0	0	0	x	x	**0**	x

Bit 1

TOM01	Control of timer output mode of channel 1
0	**Master channel output mode (toggle output by timer interrupt request signal (INTTM01))**
1	Slave channel output mode (output is set by the timer interrupt request signal (INTTM01) of the master channel, and reset by the timer interrupt request signal (INTTM0p) of the slave channel).

Note: p: slave channel number (p = 1, 2, 3)

Timer output level setting

・Timer output level register 0 (TOL0)

Set channel 1 output level to positive logic output.

Symbol: TOL0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0	0	0	0	TOL03	TOL02	TOL01	0
0	0	0	0	0	0	0	0	0	0	0	0	x	x	**0**	x

Bit 1

TOL01	Control of channel 1 timer output level
0	**Positive logic output (active-high)**
1	Negative logic output (active-low)

5.9.6 A/D Converter Initialization

Figure 5.10 and Figure 5.11 show the flowchart for A/D converter initialization.

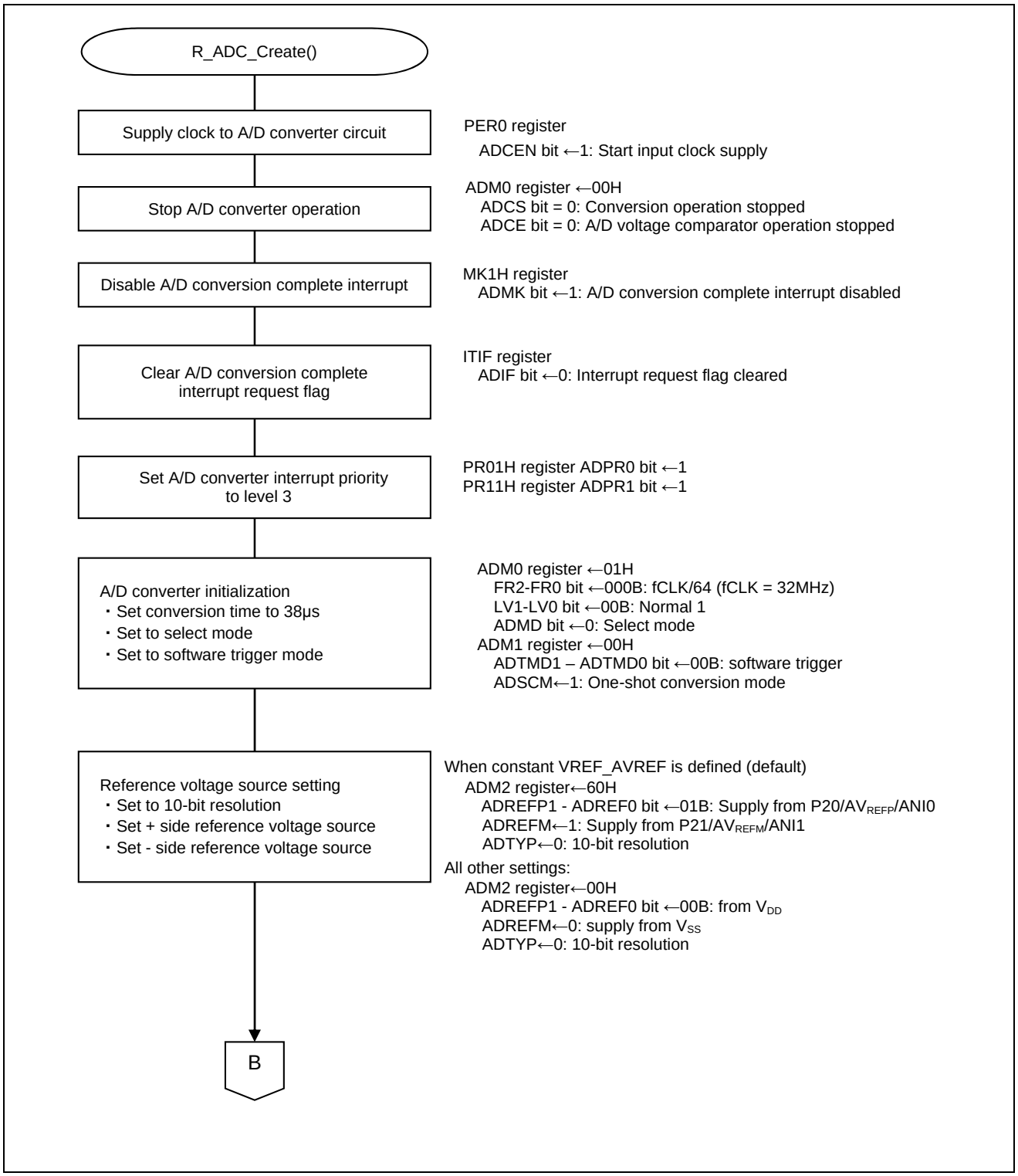

Figure 5.10 A/D Converter Setting (1/2)

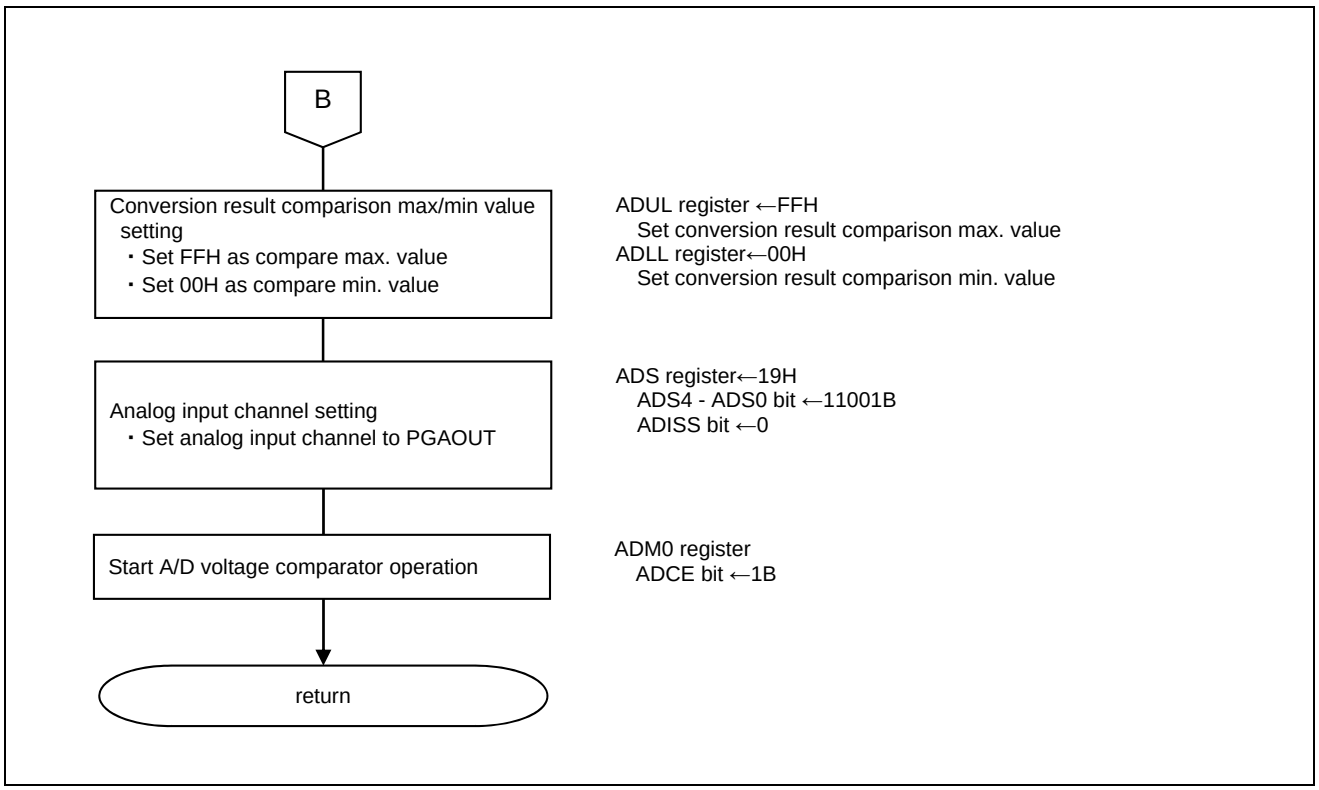

Figure 5.11 A/D Converter Setting (2/2)

A/D comparator clock supply start

・Peripheral enable register 0 (PER0)

Start clock supply to A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IRDAEN	ADCEN	IICA0EN	SAU1EN	SAU0EN	0	TAU0EN
x	x	**1**	x	x	x	0	x

Bit 5

ADCEN	Control of A/D converter input clock supply
0	Stops input clock supply.
1	**Enables input clock supply.**

A/D Conversion compete interrupt setting

- Interrupt request flag register (IF1H)
  Clear interrupt request flag.
- Interrupt mask flag register (MK1H)
  Disable interrupt processing.

Symbol: IF1H

7	6	5	4	3	2	1	0
0	TRJIF0	0	0	KRIF	ITIF	RTCIF	ADIF
0	x	0	0	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	No interrupt request signal is generated
1	Interrupt request is generated, interrupt request status.

Symbol: MK1H

7	6	5	4	3	2	1	0
1	TRJMK0	1	1	KRMK	ITMK	RTCMK	ADMK
1	x	1	1	x	x	x	**1**

Bit 0

ADMK	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

A/D conversion interrupt priority level setting

- Priority level flag register (PR11H, PR01H)
  Set to level 3 (lowest priority level).

Symbol: PR11H

7	6	5	4	3	2	1	0
1	TRJPR10	1	1	KRPR1	ITPR1	RTCPR1	ADPR1
1	x	1	1	x	x	x	**1**

Symbol: PR01H

7	6	5	4	3	2	1	0
1	TRJPR00	1	1	KRPR0	ITPR0	RTCPR0	ADPR0
1	x	1	1	x	x	x	**1**

Bit 0

ADPR1	ADPR0	Selection of priority level
0	0	**Specify level 0 (high priority level)**
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (low priority level)**

A/D conversion time and operation mode setting

- A/D converter mode register 0 (ADM0)
  Control of A/D conversion operation.
  Specify A/D conversion channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
0	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Bit 7

ADCS	A/D conversion operation control
0	**Stops conversion operation**
1	**Enables conversion operation**

Bit 6

ADMD	Specification of A/D conversion channel selection mode
0	**Selection mode**
1	Scan mode

Bits 5 -1

ADM0					Mode	Conver-sion Clock (f_{AD})	No. of Conver-sion Clocks	Conversion Time	Conversion Time Selection				
FR2	FR 1	FR 0	LV 1	LV 0					f_{CLK}= 1MHz	f_{CLK}= 4MHz	f_{CLK}= 8MHz	f_{CLK}= 16MHz	f_{CLK}= 32MHz
0	**0**	**0**	**0**	**0**	**Normal 1**	**f_{CLK}/64**	**$19f_{AD}$ (No. of sampling clocks: $7f_{AD}$)**	**$1216/f_{CLK}$**	Setting prohibited	Setting prohibited	Setting prohibited	76µs	**38µs**
0	0	1				f_{CLK}/32		$608/f_{CLK}$			76µs	38µs	19µs
0	1	0				f_{CLK}/16		$304/f_{CLK}$		76µs	38µs	19µs	9.5µs
0	1	1				f_{CLK}/8		$152/f_{CLK}$		38µs	19µs	9.5µs	4.75µs
1	0	0				f_{CLK}/6		$114/f_{CLK}$		28.5µs	14.25µs	7.125µs	3.5625µs
1	0	1				f_{CLK}/5		$95/f_{CLK}$	95µs	23.75µs	11.875µs	5.938µs	2.9688µs
1	1	0				f_{CLK}/4		$76/f_{CLK}$	76µs	19µs	9.5µs	4.75µs	2.375µs
1	1	1				f_{CLK}/2		$38/f_{CLK}$	38µs	9.5µs	4.75µs	2.375µs	Setting prohibited
0	0	0	0	1	Normal2	f_{CLK}/64	$17f_{AD}$ (No. of sampling clocks: $5f_{AD}$)	$1088/f_{CLK}$	Setting prohibited	Setting prohibited	Setting prohibited	68µs	34µs
0	0	1				f_{CLK}/32		$544/f_{CLK}$			68µs	34µs	17µs
0	1	0				f_{CLK}/16		$272/f_{CLK}$		68µs	34µs	17µs	8.5µs
0	1	1				f_{CLK}/8		$136/f_{CLK}$		34µs	17µs	8.5µs	4.25µs
1	0	0				f_{CLK}/6		$102/f_{CLK}$		25.5µs	12.75µs	6.375µs	3.1875µs
1	0	1				f_{CLK}/5		$85/f_{CLK}$	85µs	21.25µs	10.625µs	5.3125µs	2.6563µs
1	1	0				f_{CLK}/4		$68/f_{CLK}$	68µs	17µs	8.5µs	4.25µs	2.125µs
1	1	1				f_{CLK}/2		$34/f_{CLK}$	34µs	8.5µs	4.25s	2.125µs	Setting prohibited

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/ D voltage comparator operation
1	**Enables A/D voltage comparator operation**

A/D conversion trigger, conversion mode settings

・A/D converter mode register 1 (ADM1)
Selection of A/D conversion trigger mode.
Set A/D conversion operation mode.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
0	**0**	**1**	0	0	0	x	x

Bits 7, 6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	**0**	**Software trigger mode**
0	1	
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Bit 5

ADSCM	Specification of the A/D conversion operation mode
0	Sequential conversion mode
1	**One-shot conversion mode**

Reference voltage source setting

・A/D converter mode register 2 (ADM2)
A/D converter ＋ side reference voltage source selection
A/D converter －side reference voltage source selection
Conversion result max./min. value check
A/D conversion resolution setting

When constant VREF_AVREF is defined (default):

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADYTP
0	**1**	**1**	0	**0**	x	0	**0**

When constant VREF_AVREF is not defined:

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADYTP
0	**0**	**0**	0	**0**	x	0	**0**

Bits 7-6

ADREFP1	ADREFP0	Selection of the ＋ side reference voltage source of the A/D converter
0	**0**	**Supplied from V_{DD}** ● When VREF_AVREF is not defined
0	**1**	**Supplied from P20/AV_{REFP}/ANI0** ● When VREF_AVREF is defined
1	0	Supplied from the internal reference voltage (1.45 V)
1	1	Setting prohibited

Bit 5

ADREFM	Selection of the - side reference voltage source of the A/D converter
0	**Supplied from V_{SS}** ● When VREF_AVREF is not defined
1	**Supplied from P21/AV_{REFM}/ANI1** ● When VREF_AVREF is defined

Bit 3

ADRCK	Checking the upper limit and lower limit conversion result values
0	**The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register**
1	The interrupt signal (INTAD) is output when the ADCR register ＜the ADLL register or the ADUL register ＜ the ADCR register

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Conversion result comparison max/min value setting

- Conversion result comparison maximum value setting register (ADUL)
- Conversion result comparison minimum value setting register (ADLL)

Conversion result comparison max/min value setting

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Input channel specification

・Analog input channel specification register (ADS)
Specify the input channel of the analog voltage for A/SD conversion

Symbol： ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	0	0	**1**	**1**	**0**	**0**	**1**

Bits 7, 4-0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Selected Channel
0	0	0	0	0	0	ANI0
0	0	0	0	0	1	ANI1
0	0	0	0	1	0	ANI2
0	0	0	0	1	1	ANI3
0	0	0	1	0	0	ANI4
0	0	0	1	0	1	ANI5
0	0	0	1	1	0	ANI6
0	0	0	1	1	1	ANI7
0	1	0	0	0	0	ANI16
0	1	0	0	0	1	ANI17
0	1	0	0	1	0	ANI18
0	1	0	0	1	1	ANI19
0	1	0	1	0	0	ANI20
0	1	0	1	0	1	ANI21
0	1	0	1	1	0	ANI22
0	1	0	1	1	1	ANI23
0	1	1	0	0	0	ANI24
0	**1**	**1**	**0**	**0**	**1**	**PGAOUT (PGA output)**
1	0	0	0	0	0	Temperature sensor output Note 1, 2
1	0	0	0	0	1	Internal reference voltage output (1.45 V) Note 2
Other than the above						Setting prohibited

Note 1. Temperature sensor output cannot be selected when specifying internal reference voltage (1.45 V) as the comparator 0 or comparator 1 reference voltage.

Note 2. Only selectable in HS (high-speed main) mode.

5.9.7 Comparator/PGA Initialization

Figure 5.12 and Figure 5.13 show the flowchart for comparator/PGA initialization.

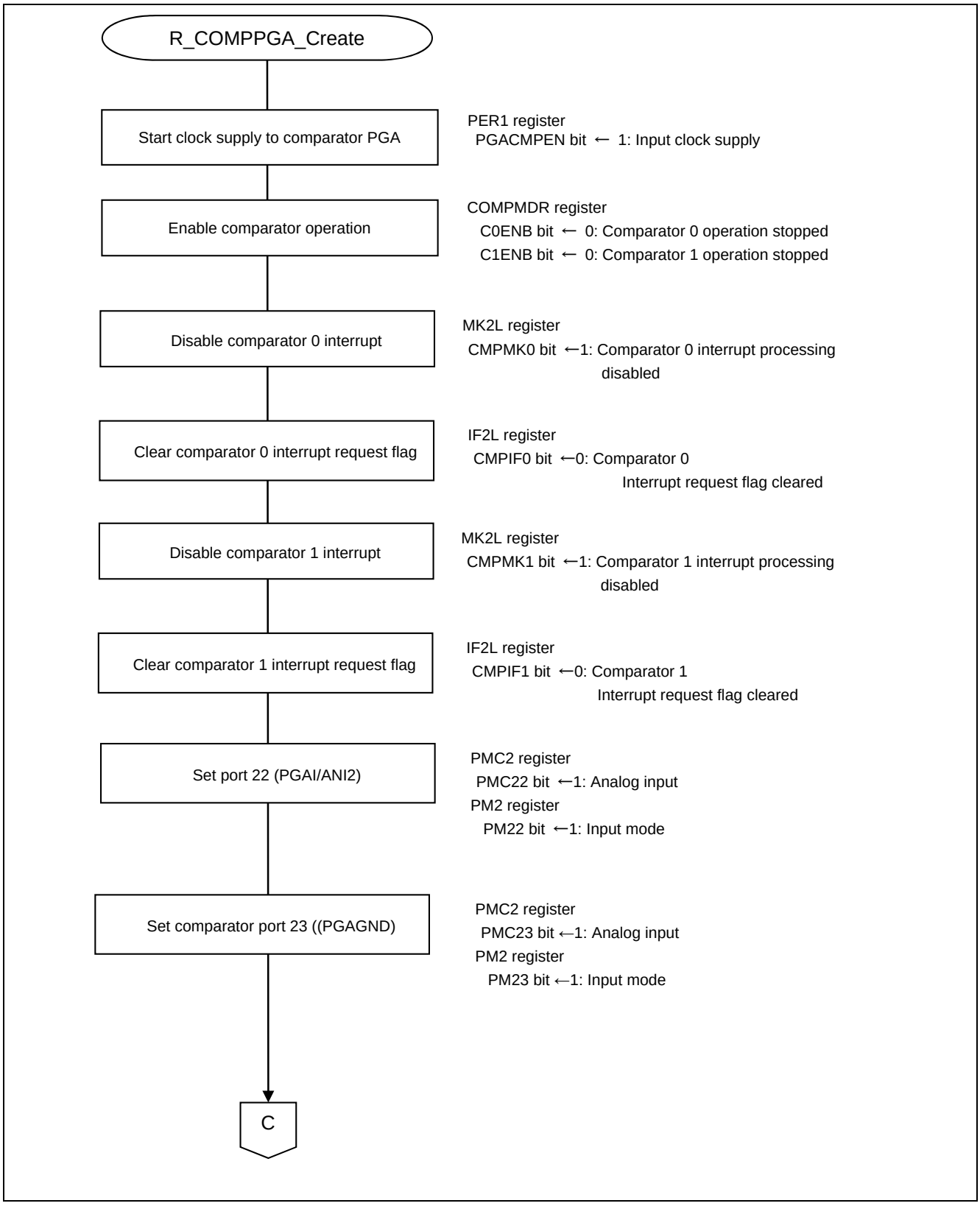

Figure 5.12 Comparator/PGA Initialization (1/2)

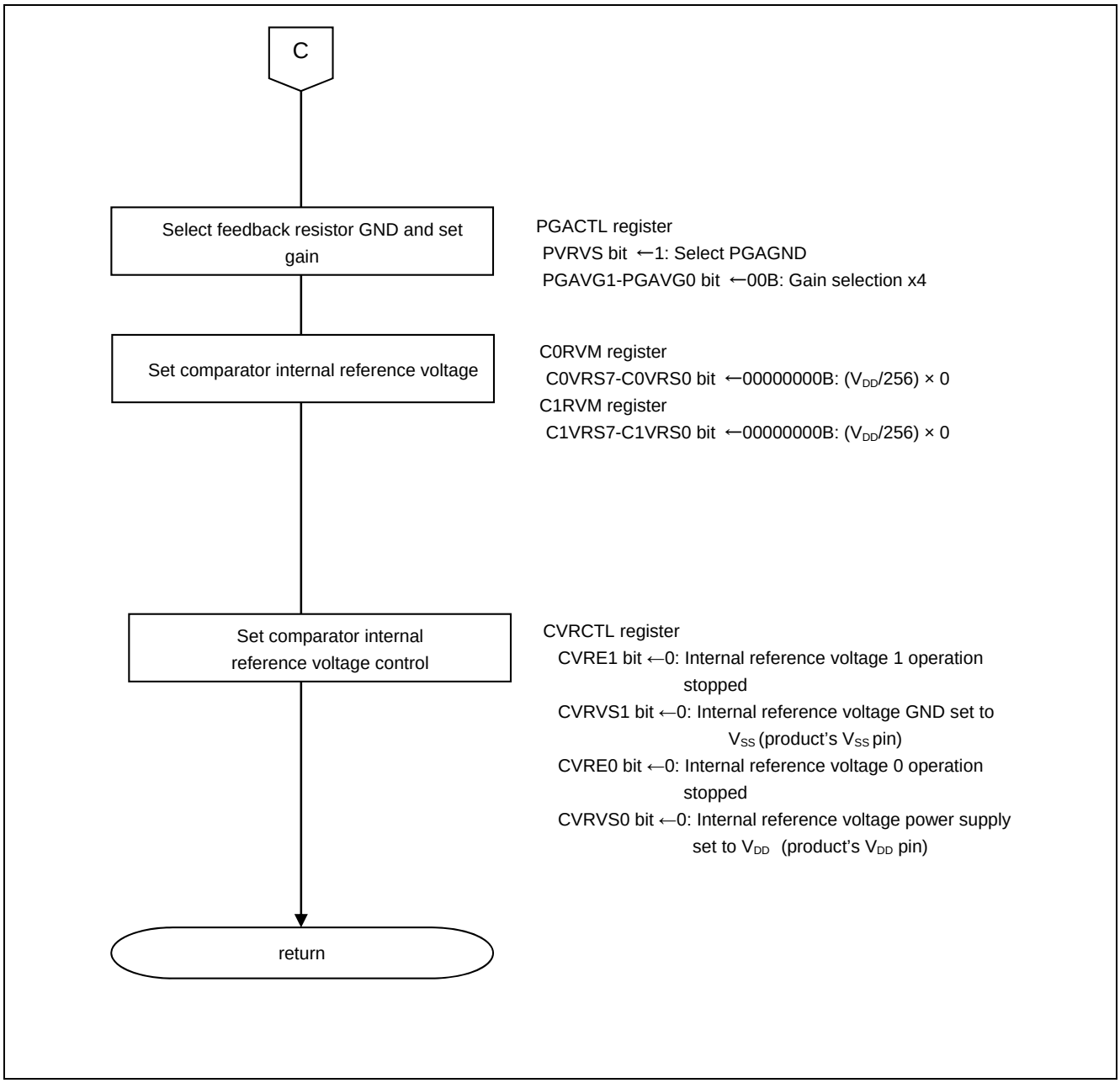

Figure 5.13 Comparator/PGA Initialization (2/2)

Comparator/PGA clock supply start

・Peripheral enable register 1 (PER1)
Start clock supply to comparator/PGA.

Symbol: PER1

7	6	5	4	3	2	1	0
DACEN	TRGEN	PGACMPEN	TRD0EN	DTCEN	PWMOPEN	TRXEN	TRJ0EN
x	x	**1**	x	x	x	x	x

Bit 5

PGACMPEN	Control of PGA and comparator input clock
0	Stops input clock supply
1	**Supplies input clock**

Comparator operation stop setting

・Comparator mode setting register (COMPMDR)
Set comparator 0 and 1 operations to stop.

Symbol: COMPMDR

7	6	5	4	3	2	1	0
C1MON	0	0	C1ENB	C0MON	0	0	C0ENB
x	x	x	**0**	x	x	x	**0**

Bit 4

C1ENB	Comparator 1 operation enable
0	**Comparator 1 operation disabled**
1	Comparator 1 operation enabled

Bit 0

C0ENB	Comparator 0 operation enable
0	**Comparator 0 operation disabled**
1	Comparator 0 operation enabled

Comparator interrupt setting

- Interrupt request flag registers (MK2L, MK2H)
  Disable comparators 0 and 1 interrupts.
- Interrupt request flag registers (IF2L, IF2H)
  Clear comparators 0 and 1 interrupt request flags.

Symbol: MK2L

7	6	5	4	3	2	1	0
PMK10 CMPMK0	PMK9	PMK8	PMK7	PMK6	1	1	1
1	x	x	x	x	1	1	1

Bit 7

CMPMK0	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol: MK2H

7	6	5	4	3	2	1	0
FLMK	1	1	TRXMK	TRGMK	TRDMK1	TRDMK0	PMK11 CMPMK1
x	1	1	x	x	x	x	**1**

Bit 0

CMPMK1	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

Symbol: IF2L

7	6	5	4	3	2	1	0
PIF10 CMPIF0	PIF9	PIF8	PIF7	PIF6	0	0	0
0	x	x	x	x	0	0	0

Bit 7

CMPIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status

Symbol: IF2H

7	6	5	4	3	2	1	0
FLIF	0	0	TRXIF	TRGIF	TRDIF1	TRDIF0	PIF11 CMPIF1
x	0	0	x	x	x	x	**0**

Bit 0

CMPIF1	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status

Comparator port register setting

- Port register (PMC2)
  Set to analog input.
- Port mode register (PM2)
  Set to input mode.

Symbol: PMC2

7	6	5	4	3	2	1	0
PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20
x	x	x	x	**1**	**1**	x	x

Bit 3

PMC23	P23 pin digital I/O/analog input selection
0	Digital I/O (alternate function other than analog input)
1	**Analog input**

Bit 2

PMC22	P22 pin digital I/O/analog input selection
0	Digital I/O (alternate function other than analog input)
1	**Analog input**

Symbol: PM2

7	6	5	4	3	2	1	0
PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
x	x	x	x	**1**	**1**	x	x

Bit 3

PM23	P23 pin I/O/analog input selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Bit 2

PM22	P22 pin I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

PGA operation stop/gain setting

- PGA control register (PGACTL)
  Set PGA operation to stop.
  Set feedback resistor GND to PGAGND.
  Set gain to x4.

Symbol: PGACTL

7	6	5	4	3	2	1	0
PGAEN	0	0	0	PVRVS	0	PGAVG1	PGAVG0
0	0	0	0	**1**	0	**0**	**0**

Bit 7

PGAEN	Programmable gain amplifier operation control
0	**Stops operation of programmable gain amplifier.**
1	Enables operation of programmable gain amplifier.

Bit 3

PVRVS	GND selection of feedback resistance of the programmable gain amplifier
0	Selects Vss.
1	**Selects PGAGND.**

Bits 1-0

PGAVG1	PGAVG0	Programmable gain amplifier amplification factor selection
0	**0**	**x4**
0	1	x8
1	0	x16
1	1	x32

Comparator internal reference voltage setting

・Comparator internal reference voltage selection register 0 (C0RVM)
Set to (AV_{REFP} or V_{DD})/256} x 0.

Symbol: C0RVM

7	6	5	4	3	2	1	0
C0VRS7	C0VRS6	C0VRS5	C0VRS4	C0VRS3	C0VRS2	C0VRS 1	C0VRS 0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bit 7-0

C0VRS7	C0VRS6	C0VRS5	C0VRS4	C0VRS3	C0VRS2	C0VRS1	C0VRS0	Comparator internal reference voltage setting
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**((AV_{REFP} or V_{DD})/256) x 0**
0	0	0	0	0	0	0	1	((AV_{REFP} or V_{DD})/256) x 1
0	0	0	0	0	0	1	0	((AV_{REFP} or V_{DD})/256) x 2
0	0	0	0	0	0	1	1	((AV_{REFP} or V_{DD})/256) x 3
			:					:
1	1	1	1	1	1	0	0	((AV_{REFP} or V_{DD})/256) x 252
1	1	1	1	1	1	0	1	((AV_{REFP} or V_{DD})/256) x 253
1	1	1	1	1	1	1	0	((AV_{REFP} or V_{DD})/256) x 254
1	1	1	1	1	1	1	1	((AV_{REFP} or V_{DD})/256) x 255

Comparator internal reference voltage setting

・Comparator internal reference voltage selection register 1 (C1RVM)
Set to {(AV_{REFP} or V_{DD})/256} x 0.

Symbol: C1RVM

7	6	5	4	3	2	1	0
C1VRS7	C1VRS6	C1VRS5	C1VRS4	C1VRS3	C1VRS2	C1VRS 1	C1VRS 0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Bits 7－0

C0VRS7	C0VRS6	C0VRS5	C0VRS4	C0VRS3	C0VRS2	C0VRS1	C0VRS0	Comparator internal reference voltage setting
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**((AV_{REFP} or V_{DD})/256) x 0**
0	0	0	0	0	0	0	1	((AV_{REFP} or V_{DD})/256) x 1
0	0	0	0	0	0	1	0	((AV_{REFP} or V_{DD})/256) x 2
0	0	0	0	0	0	1	1	((AV_{REFP} or V_{DD})/256) x 3
			:					:
1	1	1	1	1	1	0	0	((AV_{REFP} or V_{DD})/256) x 252
1	1	1	1	1	1	0	1	((AV_{REFP} or V_{DD})/256) x 253
1	1	1	1	1	1	1	0	((AV_{REFP} or V_{DD})/256) x 254
1	1	1	1	1	1	1	1	((AV_{REFP} or V_{DD})/256) x 255

Comparator internal reference voltage control setting

- Comparator internal reference voltage control register (CVRCTL)
  Set to internal reference voltage 1 operation stop.
  Select V_{SS} as internal reference voltage GND.
  Set to internal reference voltage 0 operation stop.
  Select V_{DD} as internal reference voltage power supply.

Symbol: CVRCTL

7	6	5	4	3	2	1	0
0	0	CVRE1	CVRVS1	0	0	CVRE0	CVRVS0
0	0	**0**	**0**	0	0	**0**	**0**

Bit 5

CVRE1	Control bit for internal reference voltage 1
0	**Internal reference voltage 1 operation stopped**
1	Internal reference voltage 1 operation enabled

Bit 4

CVRVS1	Ground selection bit for internal reference voltage
0	**V_{SS} selected as ground for internal reference voltage**
1	AV_{REFM} selected as ground for internal reference voltage[Note1]

Bit 2

CVRE0	Control bit for internal reference voltage 0
0	**Internal reference voltage 0 operation stopped**
1	Internal reference voltage 0 operation enabled

Bit 1

CVRVS0	Power supply selection bit for internal reference voltage
0	**V_{DD} selected as internal reference voltage power supply**
1	AV_{REFP} selected as power supply for internal reference voltage[Note 2]

Note 1. P21 is used by AV_{REFM} and IVCMP13. When the P21 pin is used as CMP1 input signal, setting CVRVS1 to 1 is prohibited.

Note 2. P20 is used by AV_{REFP} and IVCMP12. When the P20 pin is used as CMP1 input signal, setting CVRVS0 to 1 is prohibited.

5.9.8 Main Processing

Figure 5.14 shows the flowchart for the main processing.

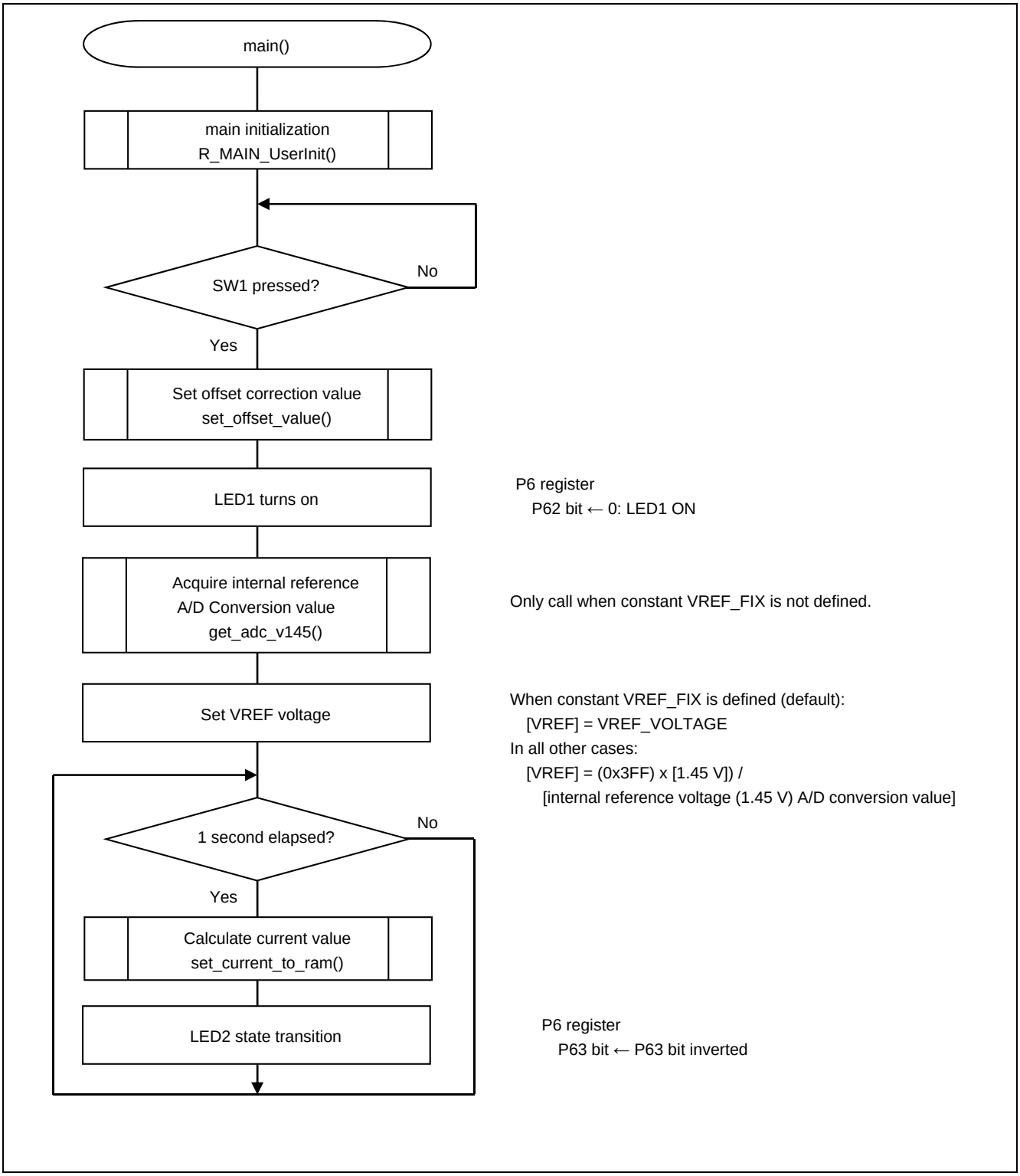

Figure 5.14 main Processing

5.9.9 main Initialization

Figure 5.15 shows the flowchart for the main initialization.

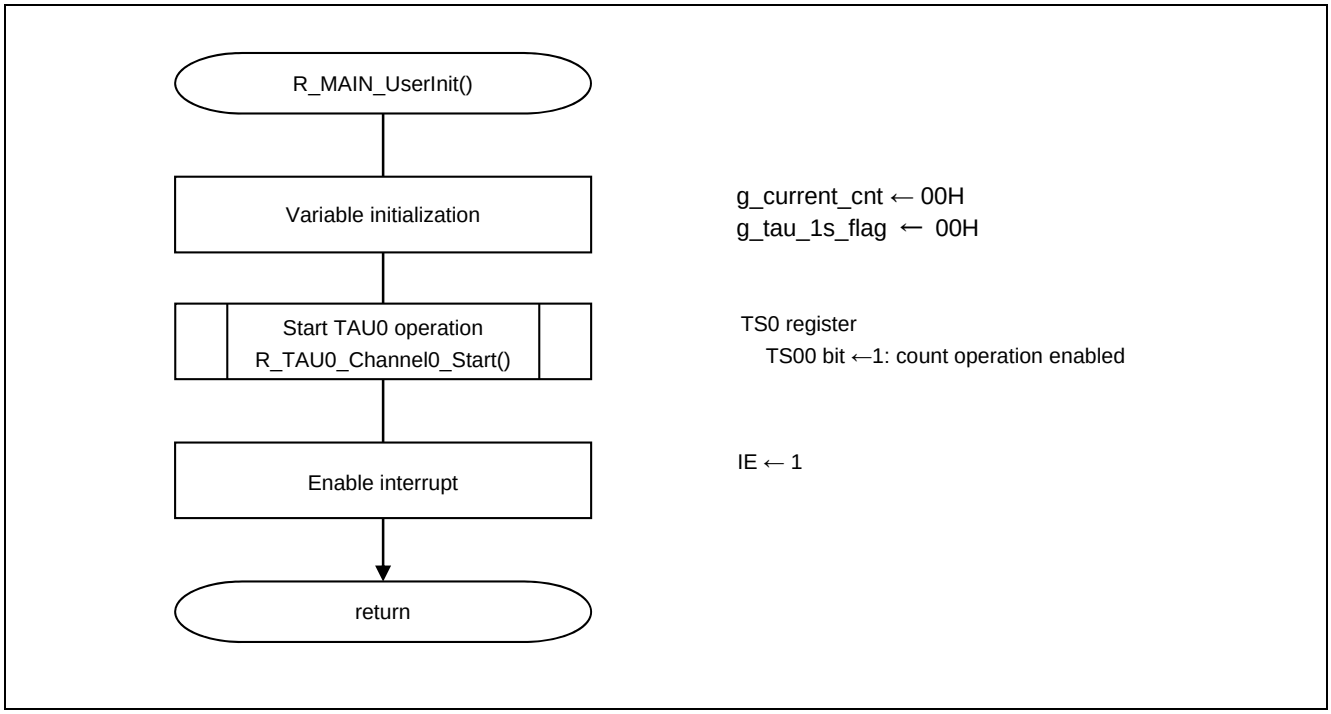

Figure 5.15 main Initialization

5.9.10 A/D Conversion Start

Figure 5.16 shows the flowchart for A/D conversion start.

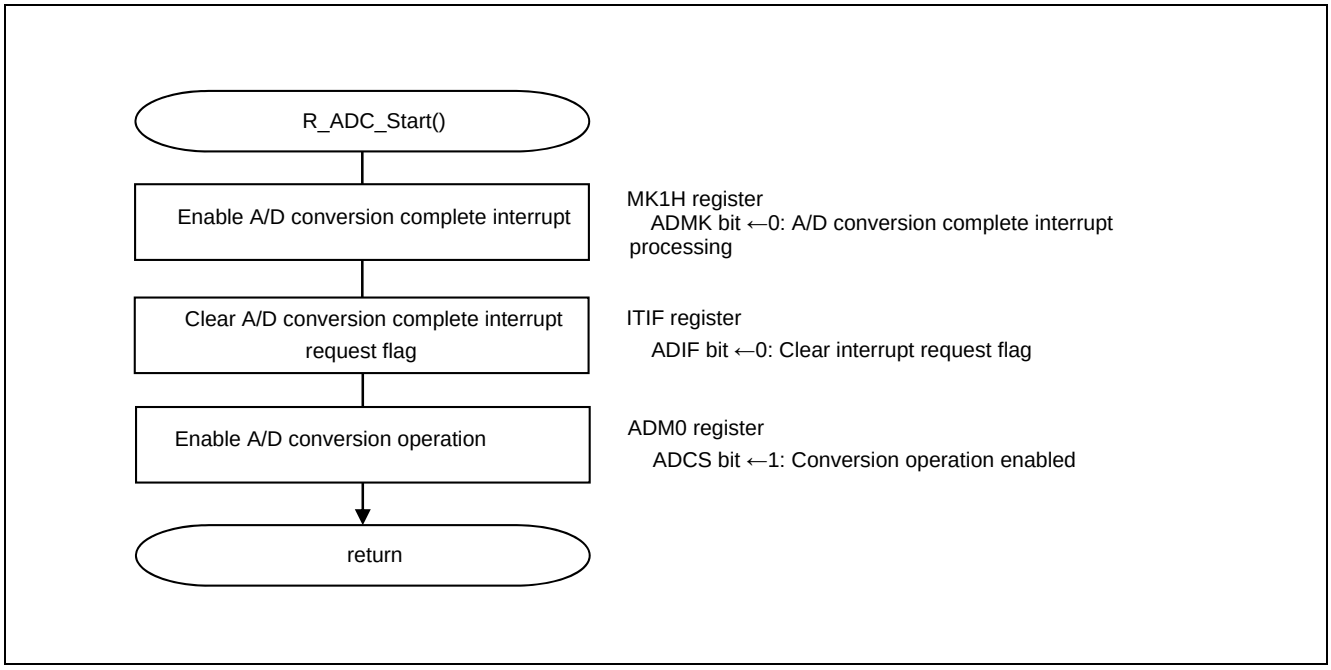

Figure 5.16 A/D Conversion Start

A/D conversion complete interrupt setting

- Interrupt request flag register (IF1H)
  Clear interrupt request flag.
- Interrupt mask flag register (MK1H)
  Enable interrupt processing.

Symbol: IF1H

7	6	5	4	3	2	1	0
0	TRJIF0	0	0	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status.

Symbol: MK1H

7	6	5	4	3	2	1	0
1	TRJMK0	1	1	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	x	x	**0**

Bit 0

ADMK	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Note For more details on register settings, refer to RL78/G1F User's Manual: Hardware.

A/D conversion operation control

・A/D converter mode register 0 (ADM0)
A/D conversion operation control.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
1	x	x	x	x	x	x	x

Bit 7

ADCS	A/D conversion operation control
0	Stops conversion operation
1	**Enables conversion operation**

5.9.11 A/D Conversion Stop

Figure 5.17 shows the flowchart for stopping the A/D conversion operation.

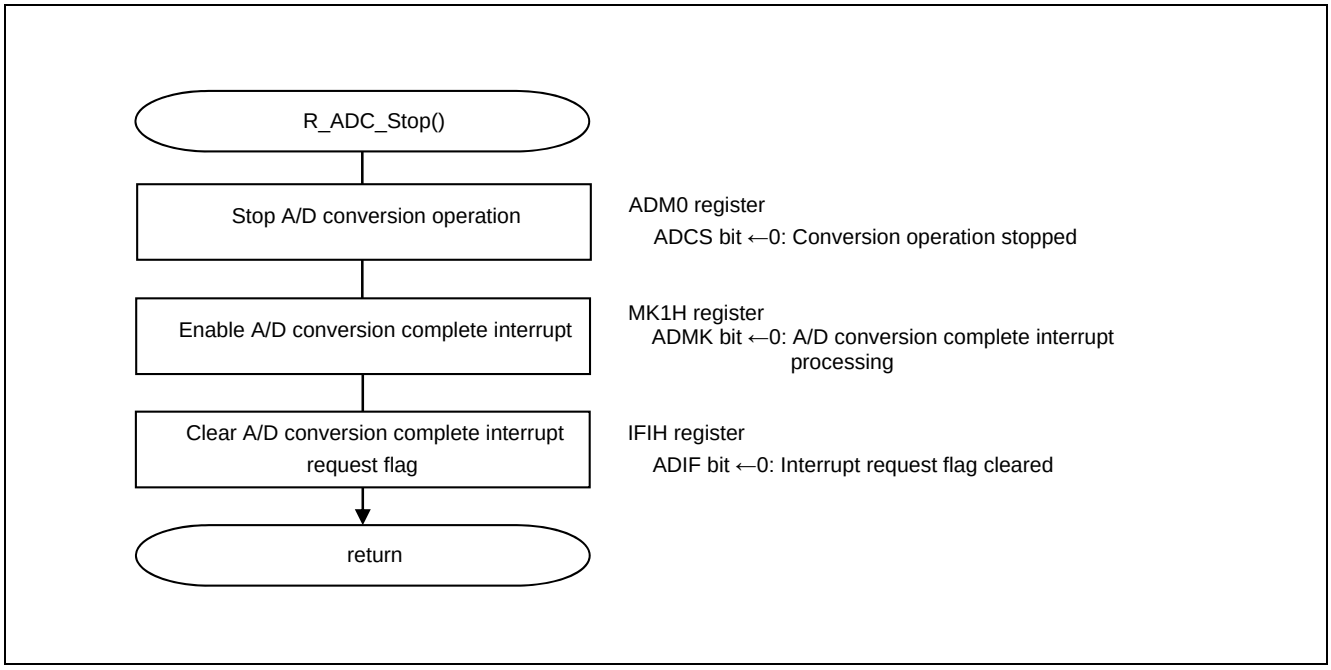

Figure 5.17 A/D Conversion Stop

A/D conversion complete interrupt setting

- Interrupt request flag register (IF1H)
  Clear interrupt request flag.
- Interrupt mask flag register (MK1H)
  Enable interrupt processing.

Symbol: F1H

7	6	5	4	3	2	1	0
0	TRJIF0	0	0	KRIF	ITIF	RTCIF	ADIF
0	x	0	0	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status.

Symbol: MK1H

7	6	5	4	3	2	1	0
1	TRJMK0	1	1	KRMK	ITMK	RTCMK	ADMK
1	x	1	1	x	x	x	**0**

Bit 0

ADMK	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Note For more details on register settings, refer to RL78/G1F User's Manual: Hardware.

A/D conversion operation control

・A/D converter mode register 0 (ADM0)
A/D conversion operation control.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
0	x	x	x	x	x	x	x

Bit 7

ADCS	A/D conversion operation control
0	**Stops conversion operation**
1	**Enables conversion operation**

5.9.12 A/D Voltage Comparator Operation Enable

Figure 5.18 shows the flowchart for enabling the A/D voltage comparator operation.

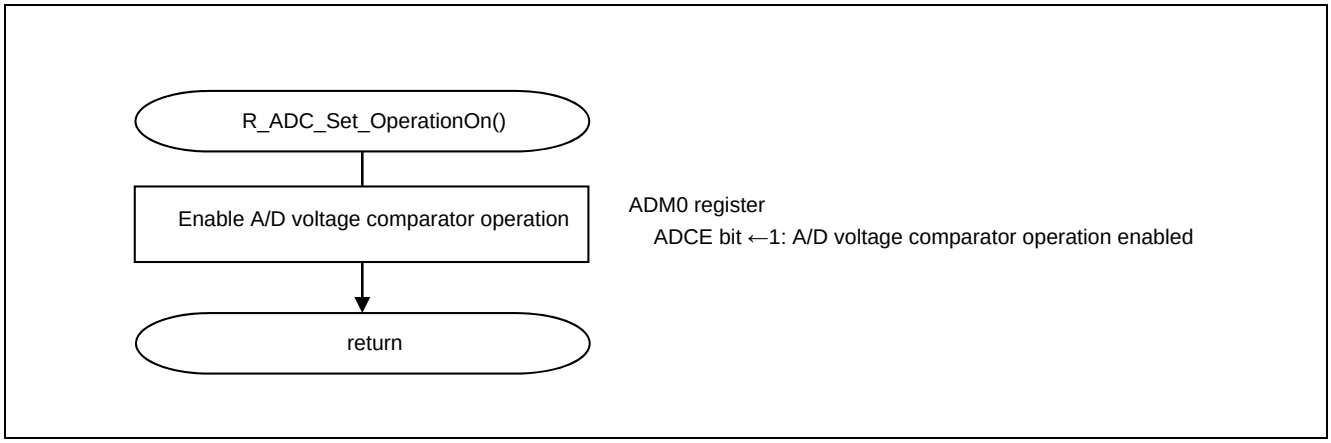

Figure 5.18 A/D Voltage Comparator Operation Enable

A/D voltage comparator operation enable

- A/D converter mode register 0 (ADM0)
  Control the A/D voltage comparator operation.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	x	x	x	x	x	x	**1**

Bit 0

ADCE	A/D voltage comparator operation control
0	Stops A/D voltage comparator operation
1	**Enables A/D voltage comparator operation**

5.9.13 A/D Voltage Comparator Operation Stop

Figure 5.19 shows the flowchart for stopping the A/D voltage comparator operation.

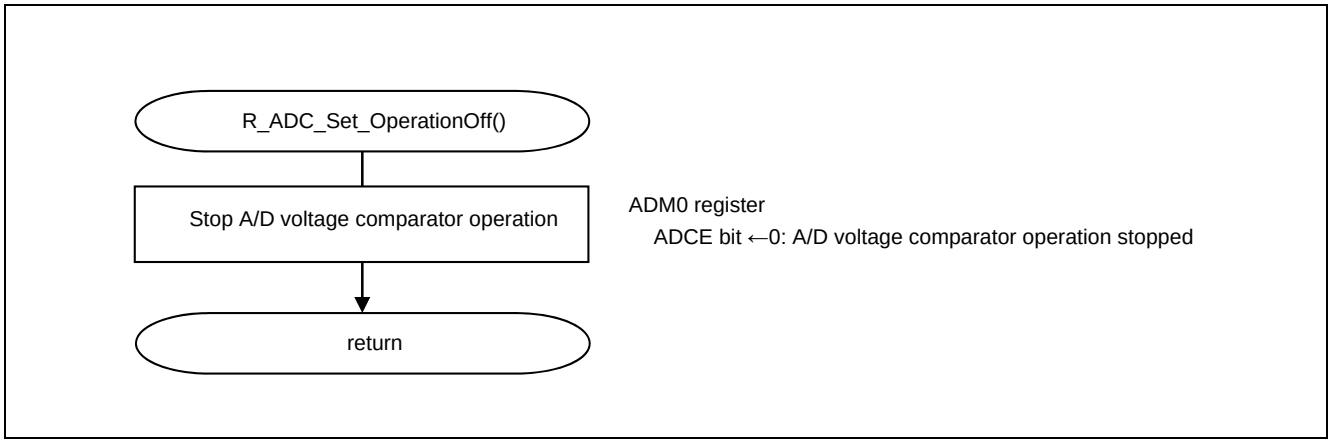

Figure 5.19 A/D Voltage Comparator Operation Stop

A/D voltage comparator operation stop

- A/D converter mode register 0 (ADM0)
  Control the A/D voltage comparator operation.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	x	x	x	x	x	x	**0**

Bit 0

ADCE	A/D voltage comparator operation control
0	**Stops A/D voltage comparator operation**
1	Enables A/D voltage comparator operation

5.9.14 A/D Conversion Result Acquisition

Figure 5.20 shows the flowchart for acquiring the A/D conversion result.

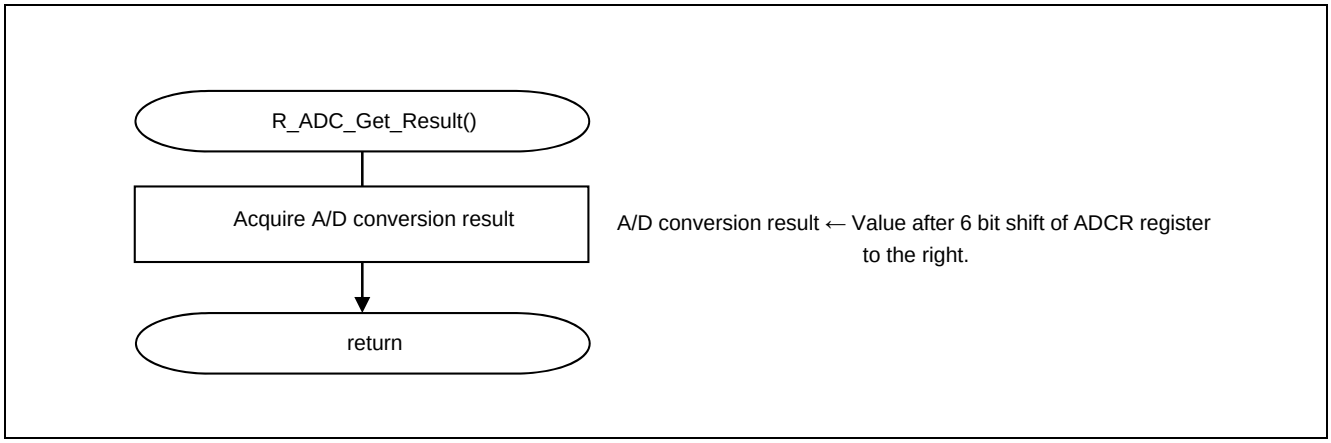

Figure 5.20 A/D Conversion Result Acquisition

5.9.15 A/D Conversion Complete Interrupt

Figure 5.21 shows the flowchart for the A/D conversion complete interrupt.

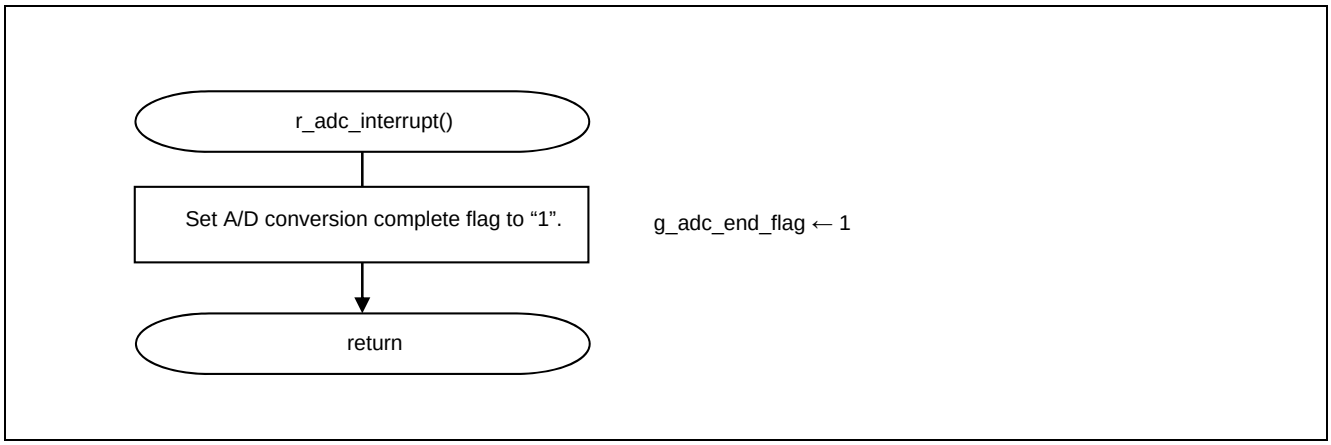

Figure 5.21 A/D Conversion Complete Interrupt

5.9.16 PGA Operation Enable

Figure 5.22 shows the flowchart for enabling the programmable gain amplifier (PGA) operation.

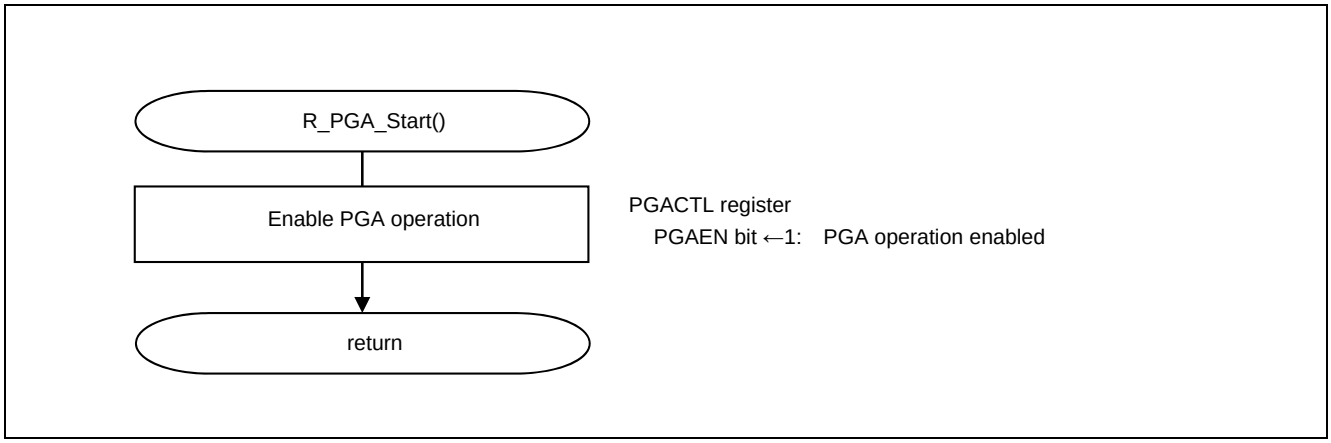

Figure 5.22 PGA Operation Enable

PGA operation enable

・PGA control register (PGACTL)
Control PGA operation.

Symbol: PGACTL

7	6	5	4	3	2	1	0
PGAEN	-	-	-	PVRVS	-	PGAVG1	PGAVG0
1	x	x	x	x	x	x	x

Bit 7

PGAEN	Programmable gain amplifier operation control
0	Stops operation of programmable gain amplifier.
1	**Enables operation of programmable gain amplifier.**

5.9.17 PGA Operation Stop

Figure 5.23 shows the flowchart for stopping the programmable gain amplifier (PGA) operation.

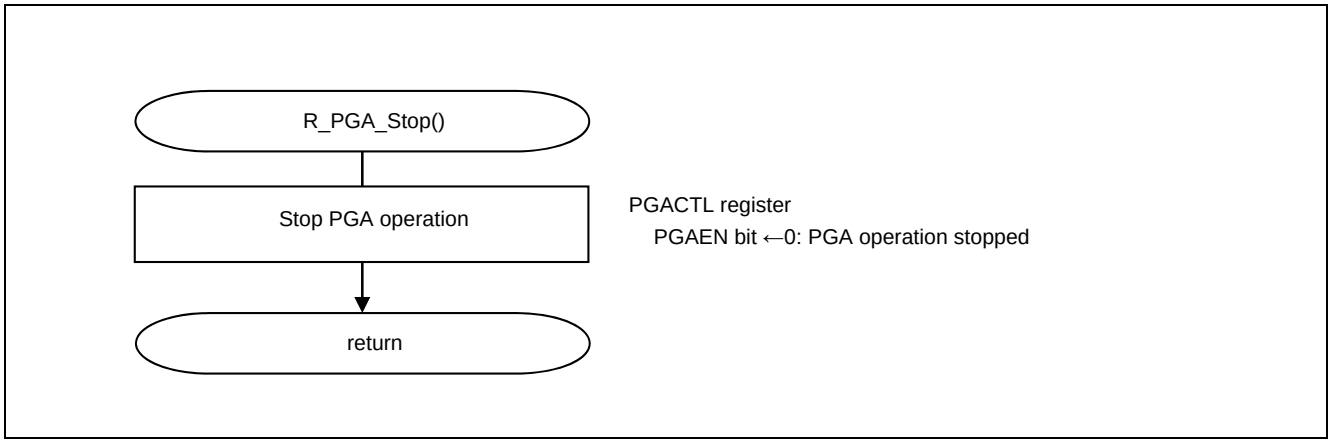

Figure 5.23 PGA Operation Stop

PGA operation stop

・PGA control register (PGACTL)
Control PGA operation.

Symbol: PGACTL

7	6	5	4	3	2	1	0
PGAEN	-	-	-	PVRVS	-	PGAVG1	PGAVG0
0	x	x	x	x	x	x	x

Bit 7

PGAEN	Programmable gain amplifier operation control
0	**Stops operation of programmable gain amplifier.**
1	Enables operation of programmable gain amplifier.

5.9.18 TAU Channel 0 Start

Figure 5.24 shows the flowchart for starting TAU channel 0.

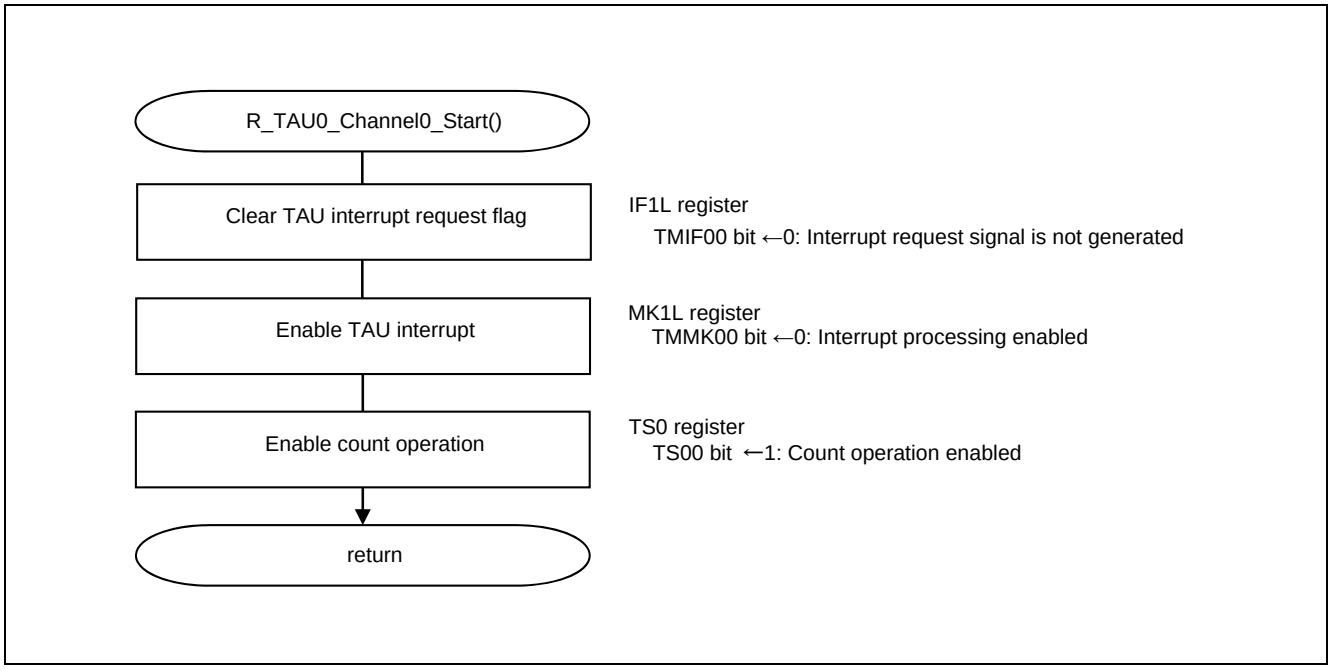

Figure 5.24 TAU Channel 0 Start

TAU interrupt request flag clear

- Interrupt request flag register (IF1L)
  Clear TAU interrupt request flag.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
x	x	x	**0**	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal generated**
1	Interrupt request signal is generated, interrupt request status

TAU interrupt enable

・Interrupt mask flag register (MK1L)
Enable TAU interrupt.

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
x	x	x	**0**	x	x	x	x

Bit 4

TMMK00	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Timer channel start

・Timer channel start register 0 (TS0)
Start channel 0 count operation.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH 03	0	TSH 01	0	0	0	0	0	TS03	TS02	TS01	TS00
0	0	0	0	x	0	x	0	0	0	0	0	x	x	x	**1**

Bit 0

TS00	Operation enable (start) trigger of Channel 0
0	No trigger operation
1	**The TE00 bit is set to 1 and the count operation becomes enabled.**

5.9.19 TAU Channel 0 Stop

Figure 5.25 shows the flowchart for stopping TAU channel 0.

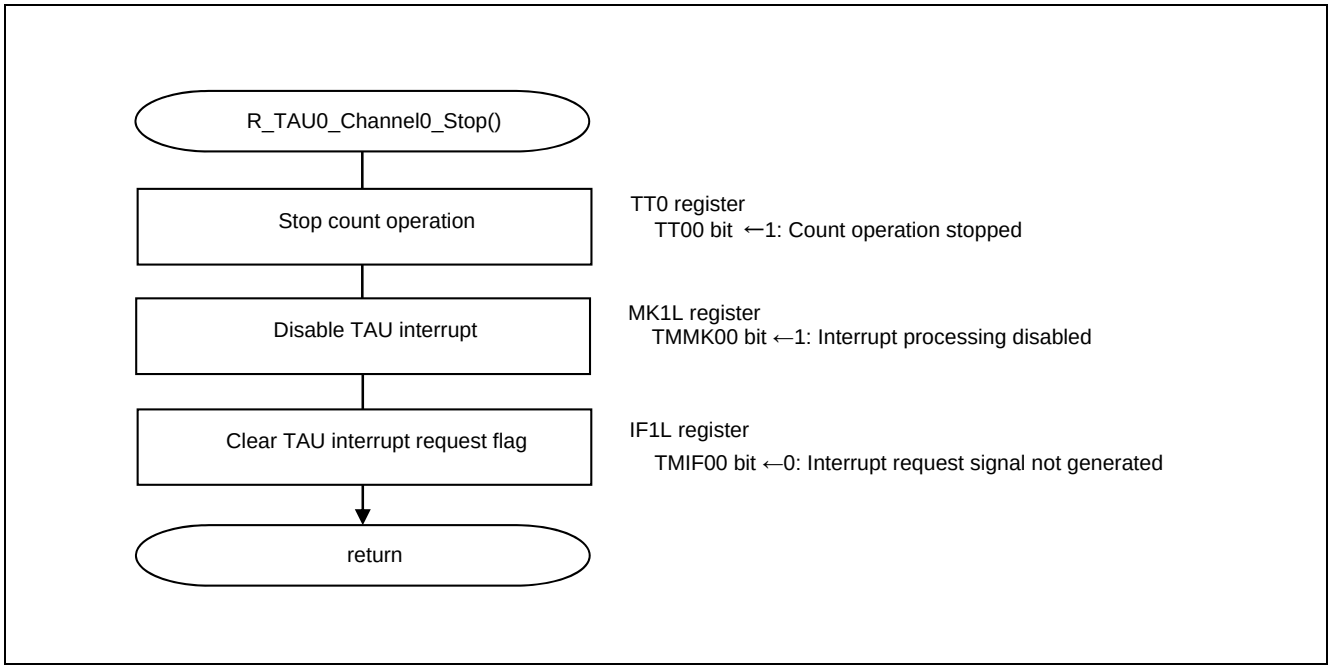

Figure 5.25 TAU Channel 0 Stop

Timer channel stop

・Timer channel stop register 0 (TT0)

Stop channel 0 count operation.

Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TTH03	0	TTH01	0	0	0	0	0	TT03	TT02	TT01	TT00
0	0	0	0	x	0	x	0	0	0	0	0	x	x	x	**1**

Bit 0

TT00	Operation stop trigger of channel 0
1	**TE00 bit is cleared to 0 and the count operation is stopped.**
1	**Operation is stopped (stop trigger is generated)** **This bit is the trigger to stop operation of the lower 8-bit timer for TT01 and TT03 when channel 1 or 3 is in the 8-bit timer mode.**

TAU interrupt disable

・Interrupt mask flag register (MK1L)
Disable TAU interrupt.

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
x	x	x	**1**	x	x	x	x

Bit 4

TMMK00	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

TAU interrupt request flag clear

・Interrupt request flag register (IF1L)
Clear TAU interrupt request flag.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
x	x	x	**0**	x	x	x	x

Bit 4

TMIF00	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status.

5.9.20 TAU Channel 1 Start

Figure 5.26 shows the flowchart for starting the TAU channel 1 operation.

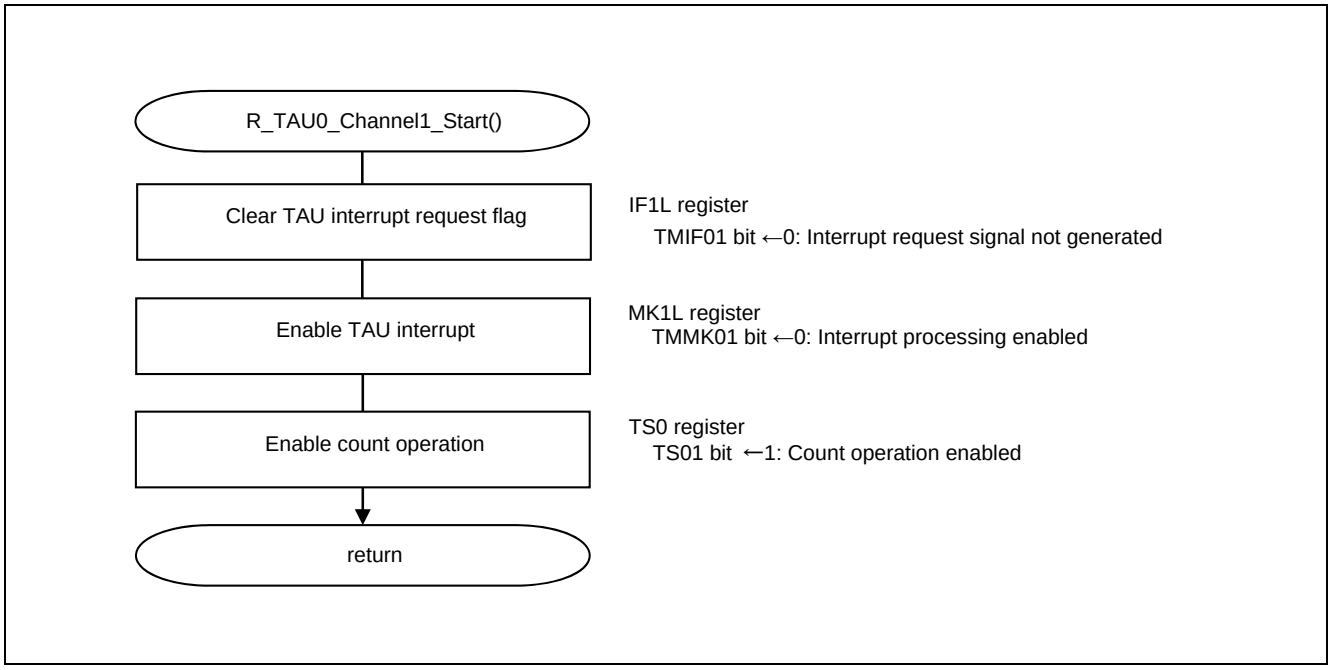

Figure 5.26 TAU Channel 1 Start

TAU interrupt request flag clear

- Interrupt request flag register (IF1L)
  Clear TAU interrupt request flag.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
x	x	**0**	x	x	x	x	x

Bit 5

TMIF01	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status.

TAU interrupt enable

・Interrupt mask flag register (MK1L)
Enable TAU interrupt.

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
x	x	**0**	x	x	x	x	x

Bit 5

TMMK01	Interrupt servicing control
0	**Interrupt servicing enabled**
1	Interrupt servicing disabled

Timer channel start

・Timer channel start register 0 (TS0)
Start channel 1 count operation.

Symbol: TS0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TSH 03	0	TSH 01	0	0	0	0	0	TS03	TS02	TS01	TS00
0	0	0	0	x	x	x	0	0	0	0	0	x	x	**1**	x

Bit 1

TS01	Operation enable (start) trigger of channel 1
0	No trigger operation
1	**The TE01 bit is set to 1 and the count operation becomes enabled.**

5.9.21 TAU Channel 1 Stop

Figure 5.27 shows the flowchart for stopping TAU channel 1.

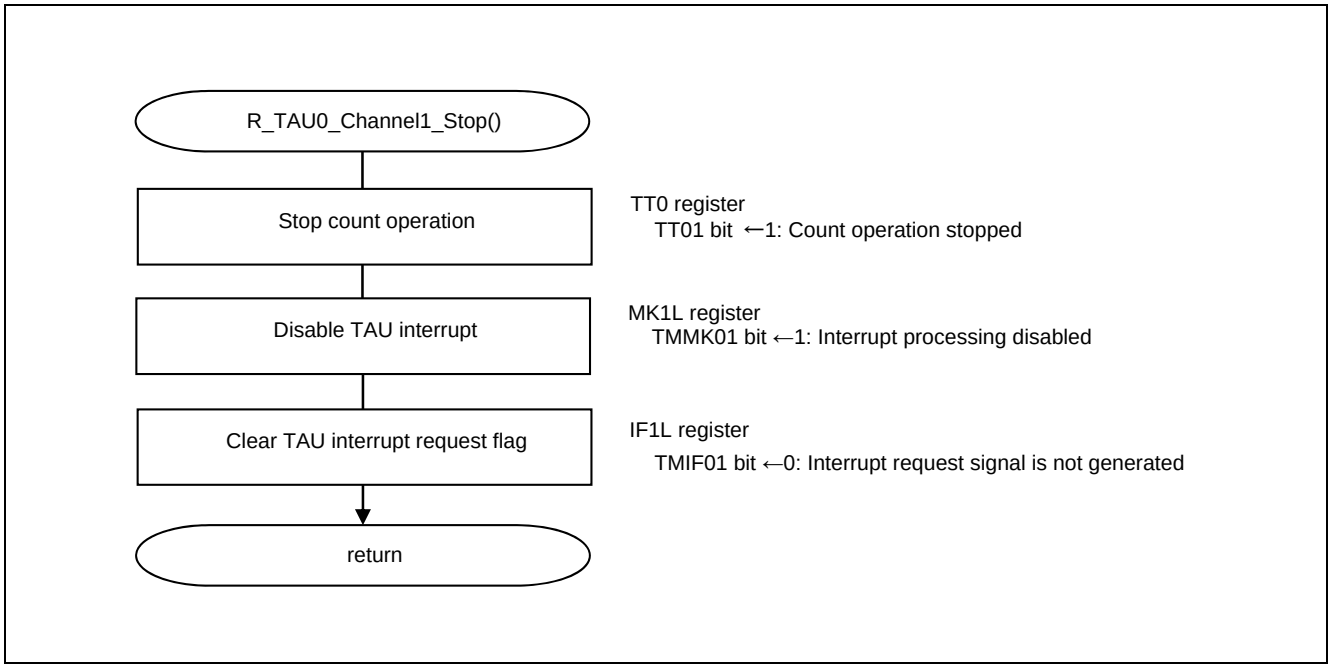

Figure 5.27 TAU Channel 1 Stop

Timer channel stop

・Timer channel stop register 0 (TT0)

Stop channel 1 count operation.

Symbol: TT0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	TTH03	0	TTH01	0	0	0	0	0	TT03	TT02	TT01	TT00
0	0	0	0	x	0	x	0	0	0	0	0	x	x	**1**	x

Bit 1

TT01	Operation stop trigger of channel 1
1	**TE01 bit cleared to 0 and the count operation is stopped.**
1	**Operation is stopped (stop trigger is generated)** **This bit is the trigger to stop operation of the lower 8-bit timer for TTm1 and TTm3 when channel 1 or 3 is in the 8-bit timer mode.**

TAU interrupt disable

・Interrupt mask flag register (MK1L)
Disable TAU interrupt.

Symbol: MK1L

7	6	5	4	3	2	1	0
TMMK03	TMMK02	TMMK01	TMMK00	IICAMK0	SREMK1 TMMK03H	SRMK1 CSIMK11 IICMK11	STMK1 CSIMK10 IICMK10
x	x	**1**	x	x	x	x	x

Bit 5

TMMK01	Interrupt servicing control
0	Interrupt servicing enabled
1	**Interrupt servicing disabled**

TAU interrupt request flag clear

・Interrupt request flag register (IF1L)
Clear TAU interrupt request flag.

Symbol: IF1L

7	6	5	4	3	2	1	0
TMIF03	TMIF02	TMIF01	TMIF00	IICAIF0	SREIF1 TMIF03H	SRIF1 CSIIF11 IICIF11	STIF1 CSIIF10 IICIF10
x	x	**0**	x	x	x	x	x

Bit 5

TMIF01	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status

5.9.22 TAU Channel 0 Interrupt

Figure 5.28 shows the flowchart for the TAU channel 0 interrupt.

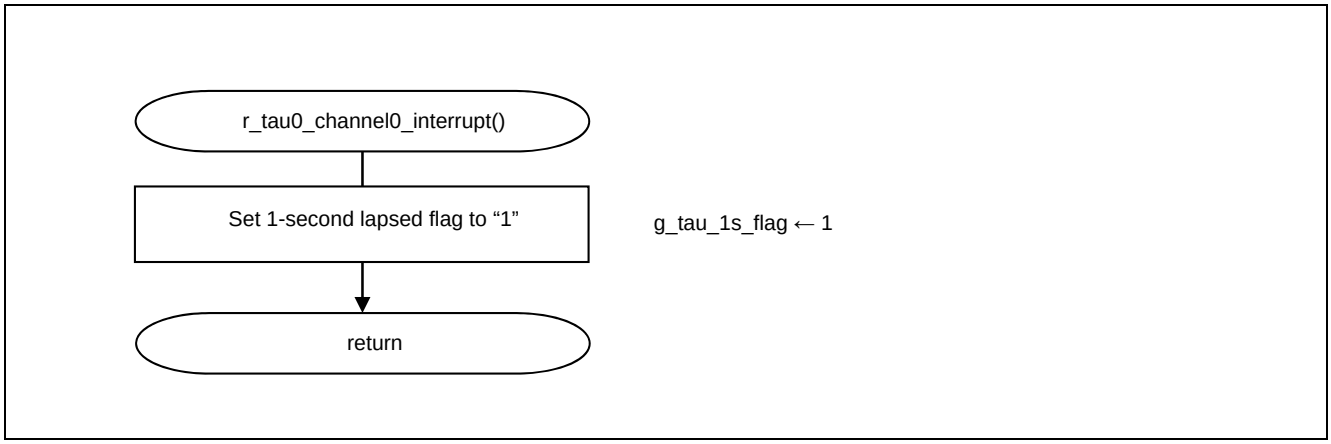

Figure 5.28 TAU Channel 0 Interrupt

5.9.23 TAU Channel 1 Interrupt

Figure 5.29 shows the flowchart for the TAU channel 1 interrupt.

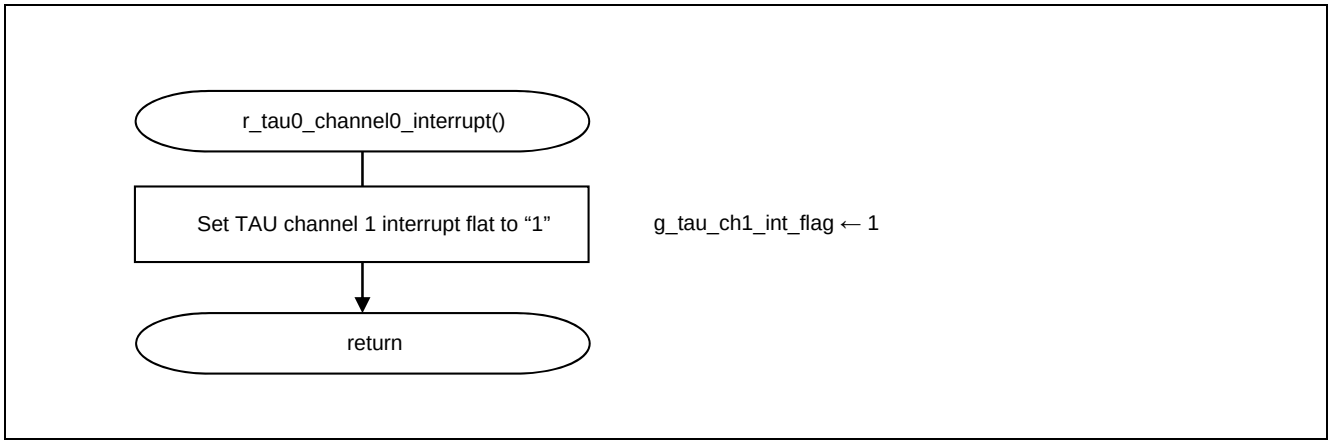

Figure 5.29 TAU Channel 1 Interrupt

5.9.24 Offset Correction Value Setting

Figure 5.30 shows the flowchart for setting the offset correction value.

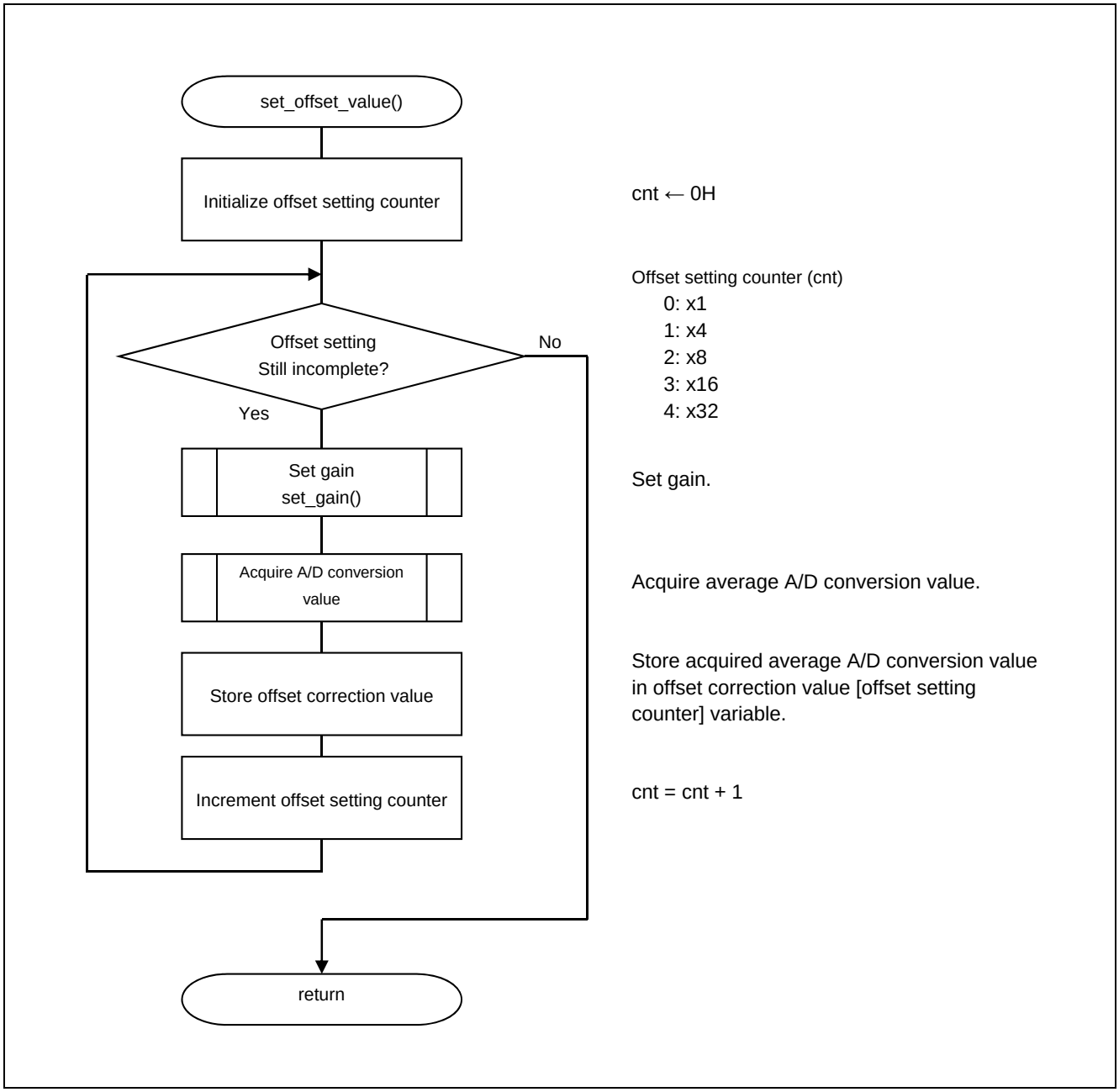

Figure 5.30 Offset Correction Value Setting

5.9.25 Acquire Average A/D Conversion Value

Figure 5.31 shows the flowchart for acquiring average A/D conversion value.

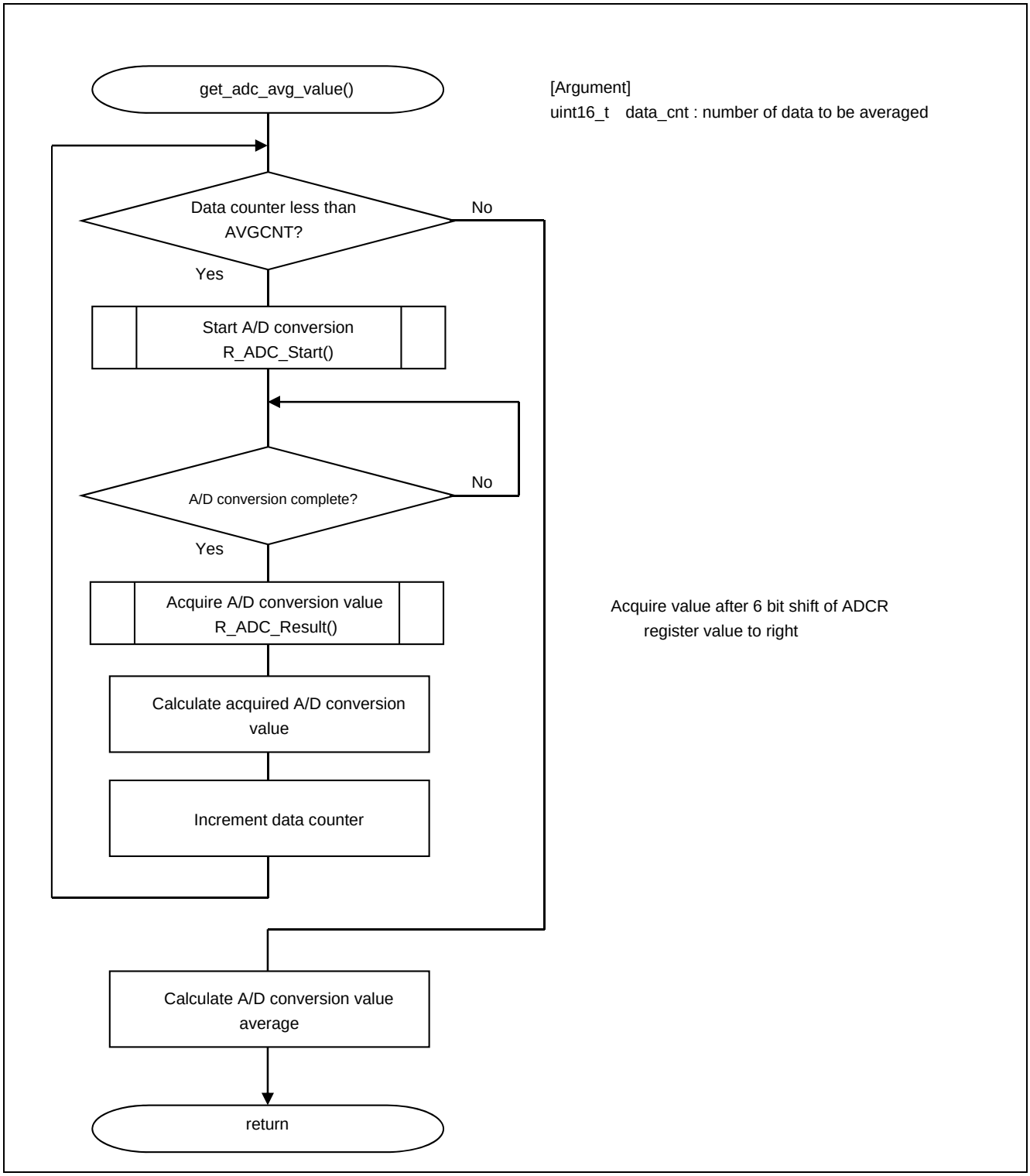

Figure 5.31 Acquire Average A/D Conversion Value

5.9.26 Acquire Input Voltage A/D Conversion Value

Figure 5.32 shows the flowchart for acquiring the input voltage A/D conversion value.

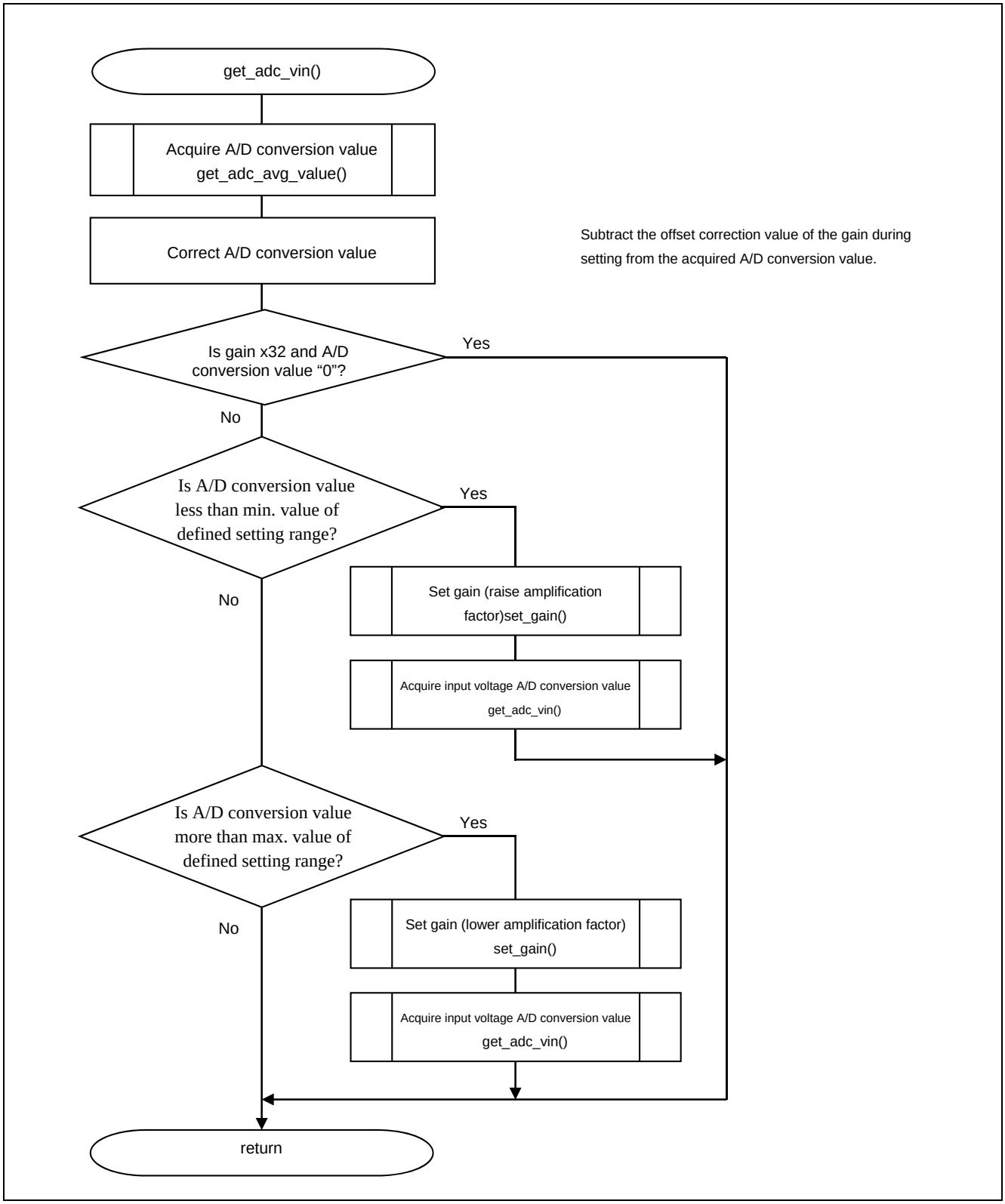

Figure 5.32 Acquire Input Voltage A/D Conversion Value

5.9.27 Acquire Internal Reference Voltage A/D Conversion Value

Figure 5.33 shows the flowchart for acquiring the internal reference voltage A/D conversion value.

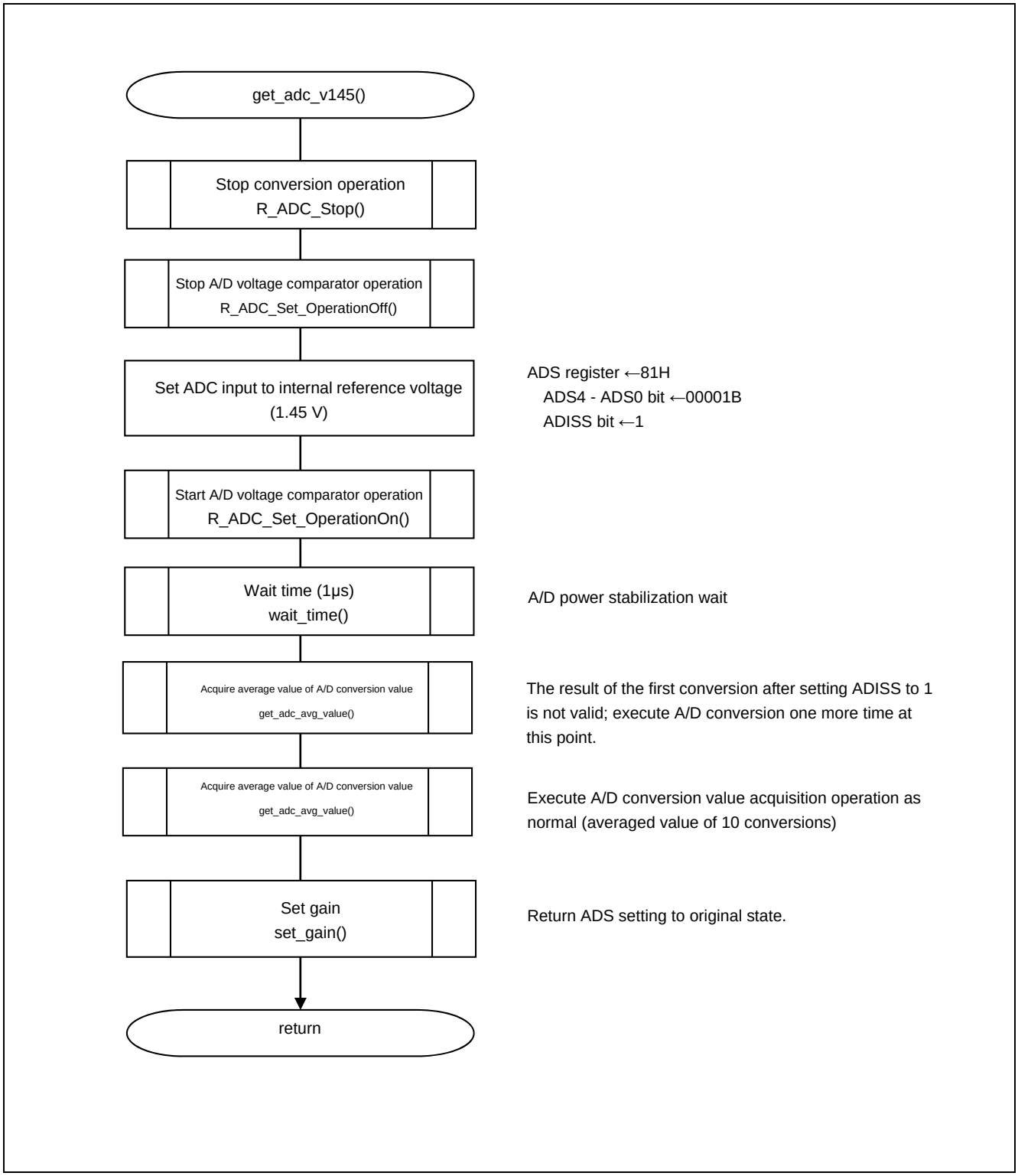

Figure 5.33 Acquire Internal Reference Voltage A/D Conversion Value

Setting ADC input channel to internal reference voltage output (1.45 V)

- Analog input channel specification register (ADS)
  Set analog voltage input channel for A/D conversion to internal reference voltage output (1.45 V)

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
1	**0**	**0**	**0**	**0**	**0**	**0**	**1**

Bits 7, 4 - 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Selected channel
0	0	0	0	0	0	ANI0
0	0	0	0	0	1	ANI1
0	0	0	0	1	0	ANI2
0	0	0	0	1	1	ANI3
0	0	0	1	0	0	ANI4
0	0	0	1	0	1	ANI5
0	0	0	1	1	0	ANI6
0	0	0	1	1	1	ANI7
0	1	0	0	0	0	ANI16
0	1	0	0	0	1	ANI17
0	1	0	0	1	0	ANI18
0	1	0	0	1	1	ANI19
0	1	0	1	0	0	ANI20
0	1	0	1	0	1	ANI21
0	1	0	1	1	0	ANI22
0	1	0	1	1	1	ANI23
0	1	1	0	0	0	ANI24
0	1	1	0	0	1	PGAOUT (PGA output)
1	0	0	0	0	0	Temperature sensor output voltage Note 1, 2
1	**0**	**0**	**0**	**0**	**1**	**Internal reference voltage (1.45 V)Note 2**
Other than above						Setting prohibited

Note 1. If the internal reference voltage (1.45 V) is selected as the reference voltage of comparator 0 or comparator 1, the temperature sensor output cannot be selected.

Note 2. Operation is possible only in HS (high-speed main) mode.

5.9.28 Gain Setting

Figure 5.34 and Figure 5.35 show the flowcharts for setting the gain.

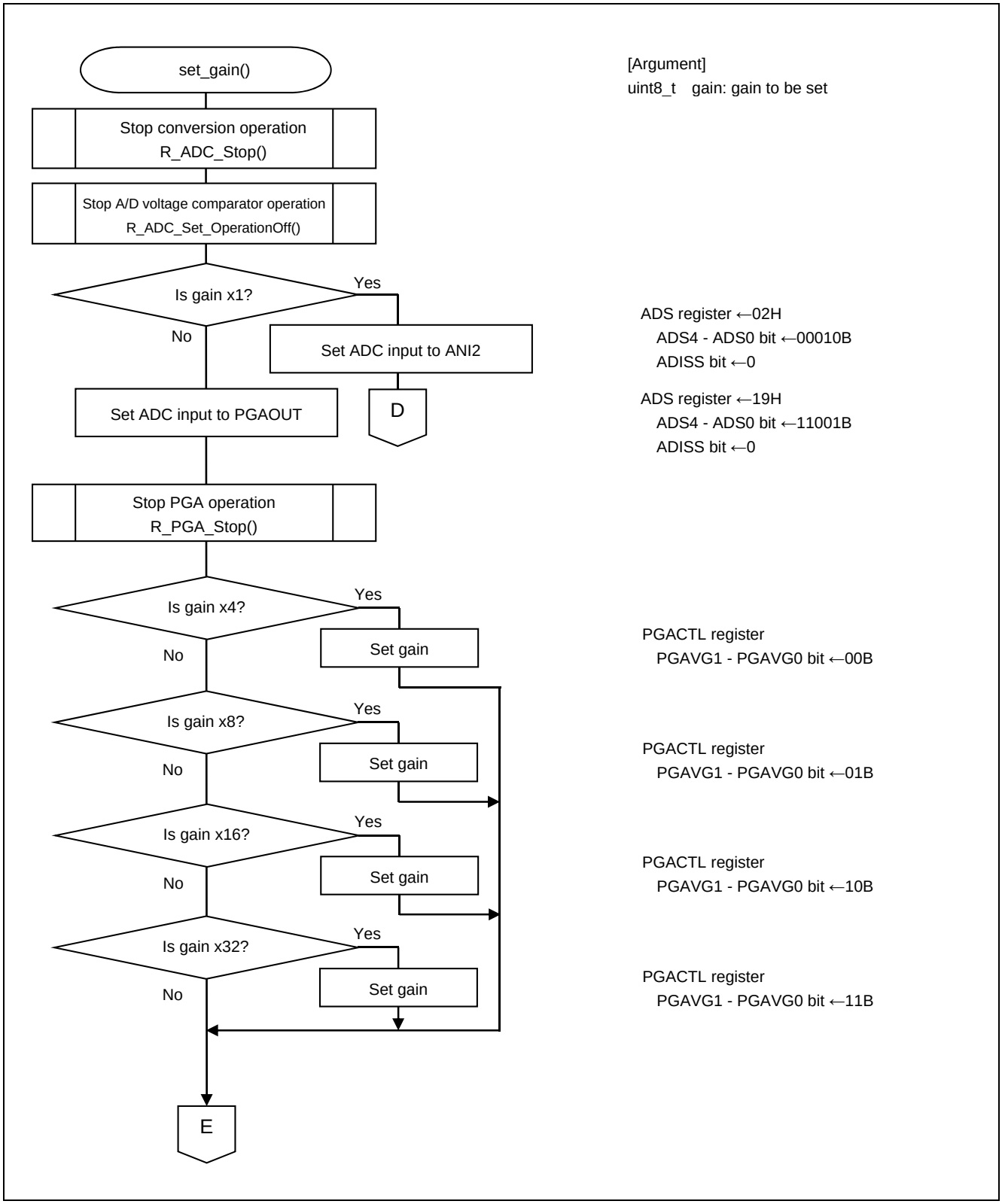

Figure 5.34 Gain Setting (1/2)

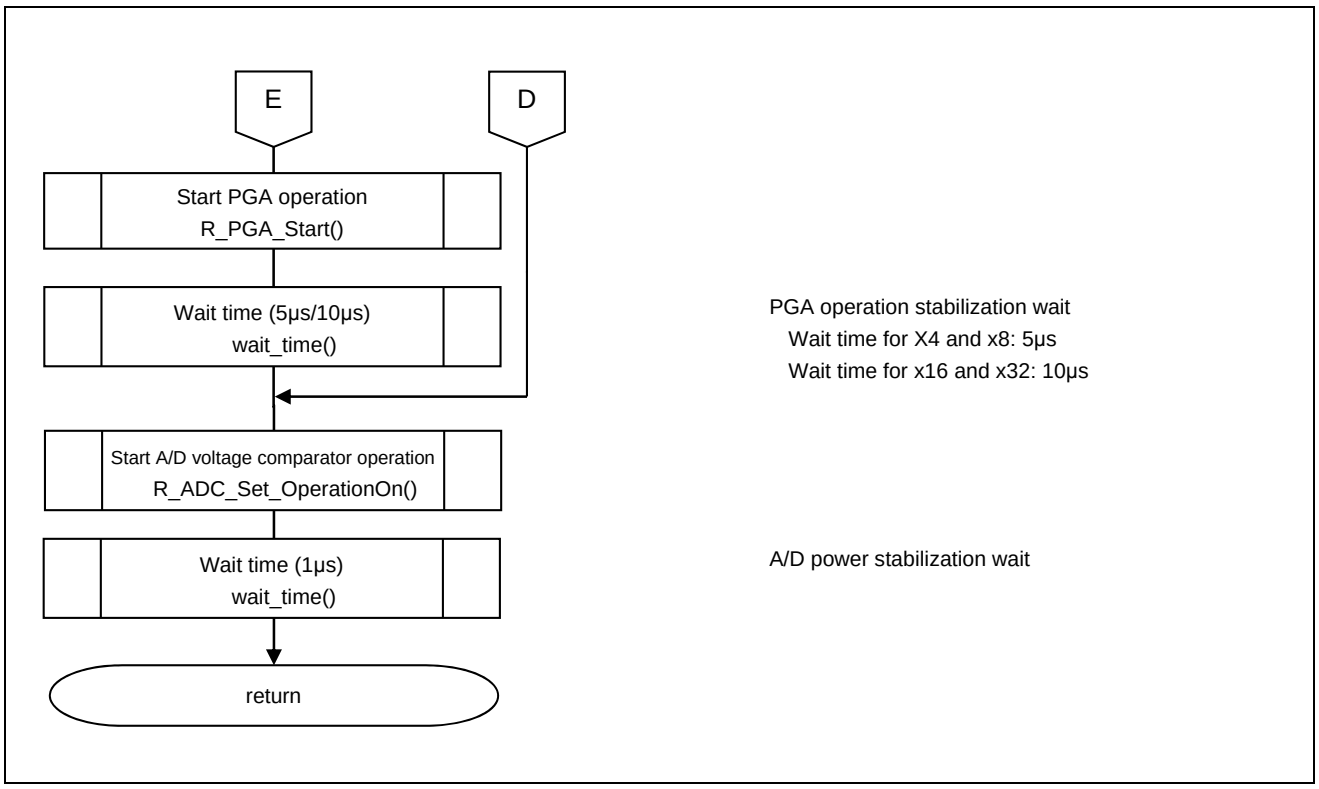

Figure 5.35 Gain Setting (2/2)

Setting ADC input channel to ANI2

- Analog input channel specification register (ADS)
  Set analog voltage input channel for A/D conversion to ANI2.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	**0**	**0**	**0**	**0**	**0**	**1**	**0**

Bits 7, 4 - 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Selected channel
0	0	0	0	0	0	ANI0
0	0	0	0	0	1	ANI1
0	**0**	**0**	**0**	**1**	**0**	**ANI2**
0	0	0	0	1	1	ANI3
0	0	0	1	0	0	ANI4
0	0	0	1	0	1	ANI5
0	0	0	1	1	0	ANI6
0	0	0	1	1	1	ANI7
0	1	0	0	0	0	ANI16
0	1	0	0	0	1	ANI17
0	1	0	0	1	0	ANI18
0	1	0	0	1	1	ANI19
0	1	0	1	0	0	ANI20
0	1	0	1	0	1	ANI21
0	1	0	1	1	0	ANI22
0	1	0	1	1	1	ANI23
0	1	1	0	0	0	ANI24
0	1	1	0	0	1	PGAOUT (PGA output)
1	0	0	0	0	0	Temperature sensor output voltage Note 1, 2
1	0	0	0	0	1	Internal reference voltage (1.45 V) Note 2
Other than above						Setting prohibited

Note 1. If the internal reference voltage (1.45 V) is selected as the reference voltage of comparator 0 or comparator 1, the temperature sensor output cannot be selected.

Note 2. Operation is possible only in HS (high-speed main) mode.

Setting ADC input channel to PGAOUT

- Analog input channel specification register (ADS)
  Set analog voltage input channel for A/D conversion to PGAOUT.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	**0**	**0**	**1**	**1**	**0**	**0**	**1**

Bits 7, 4 - 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Selected channel
0	0	0	0	0	0	ANI0
0	0	0	0	0	1	ANI1
0	0	0	0	1	0	ANI2
0	0	0	0	1	1	ANI3
0	0	0	1	0	0	ANI4
0	0	0	1	0	1	ANI5
0	0	0	1	1	0	ANI6
0	0	0	1	1	1	ANI7
0	1	0	0	0	0	ANI16
0	1	0	0	0	1	ANI17
0	1	0	0	1	0	ANI18
0	1	0	0	1	1	ANI19
0	1	0	1	0	0	ANI20
0	1	0	1	0	1	ANI21
0	1	0	1	1	0	ANI22
0	1	0	1	1	1	ANI23
0	1	1	0	0	0	ANI24
0	**1**	**1**	**0**	**0**	**1**	**PGAOUT (PGA output)**
1	0	0	0	0	0	Temperature sensor output voltage Note 1, 2
1	0	0	0	0	1	Internal reference output (1.45V) Note 2
Other than above						Setting prohibited

Note 1. If the internal reference voltage (1.45 V) is selected as the reference voltage of comparator 0 or comparator 1, the temperature sensor output cannot be selected.

Note 2. Operation is possible only in HS (high-speed main) mode.

PGA operation stop/gain setting (x4)

・PGA control register (PGACTL)
Set gain to x4.

Symbol: PGACTL

7	6	5	4	3	2	1	0
PGAEN	0	0	0	PVRVS	0	PGAVG1	PGAVG0
x	0	0	0	x	0	**0**	**0**

Bits 1-0

PGAVG1	PGAVG0	Function
0	**0**	**x4**
0	1	x8
1	0	x16
1	1	x32

PGA operation stop/gain setting (x8)

・PGA control register (PGACTL)
Set gain to x8.

Symbol: PGACTL

7	6	5	4	3	2	1	0
PGAEN	0	0	0	PVRVS	0	PGAVG1	PGAVG0
x	0	0	0	x	0	**0**	**1**

Bits 1-0

PGAVG1	PGAVG0	Function
0	0	x4
0	**1**	**x8**
1	0	x16
1	1	x32

PGA operation stop/gain setting (x16)

・PGA control register (PGACTL)
Set gain to x16.

Symbol: PGACTL

7	6	5	4	3	2	1	0
PGAEN	0	0	0	PVRVS	0	PGAVG1	PGAVG0
x	0	0	0	x	0	**1**	**0**

Bits 1-0

PGAVG1	PGAVG0	Function
0	0	x4
0	1	x8
1	**0**	**x16**
1	1	x32

PGA operation stop/gain setting (x32)

・PGA control register (PGACTL)
Set gain to x32.

Symbol: PGACTL

7	6	5	4	3	2	1	0
PGAEN	0	0	0	PVRVS	0	PGAVG1	PGAVG0
x	0	0	0	x	0	**1**	**1**

Bits 1-0

PGAVG1	PGAVG0	Function
0	0	x4
0	1	x8
1	0	x16
1	**1**	**x32**

5.9.29 Current Value Calculation

Figure 5.36 shows the flowchart for calculating the current value.

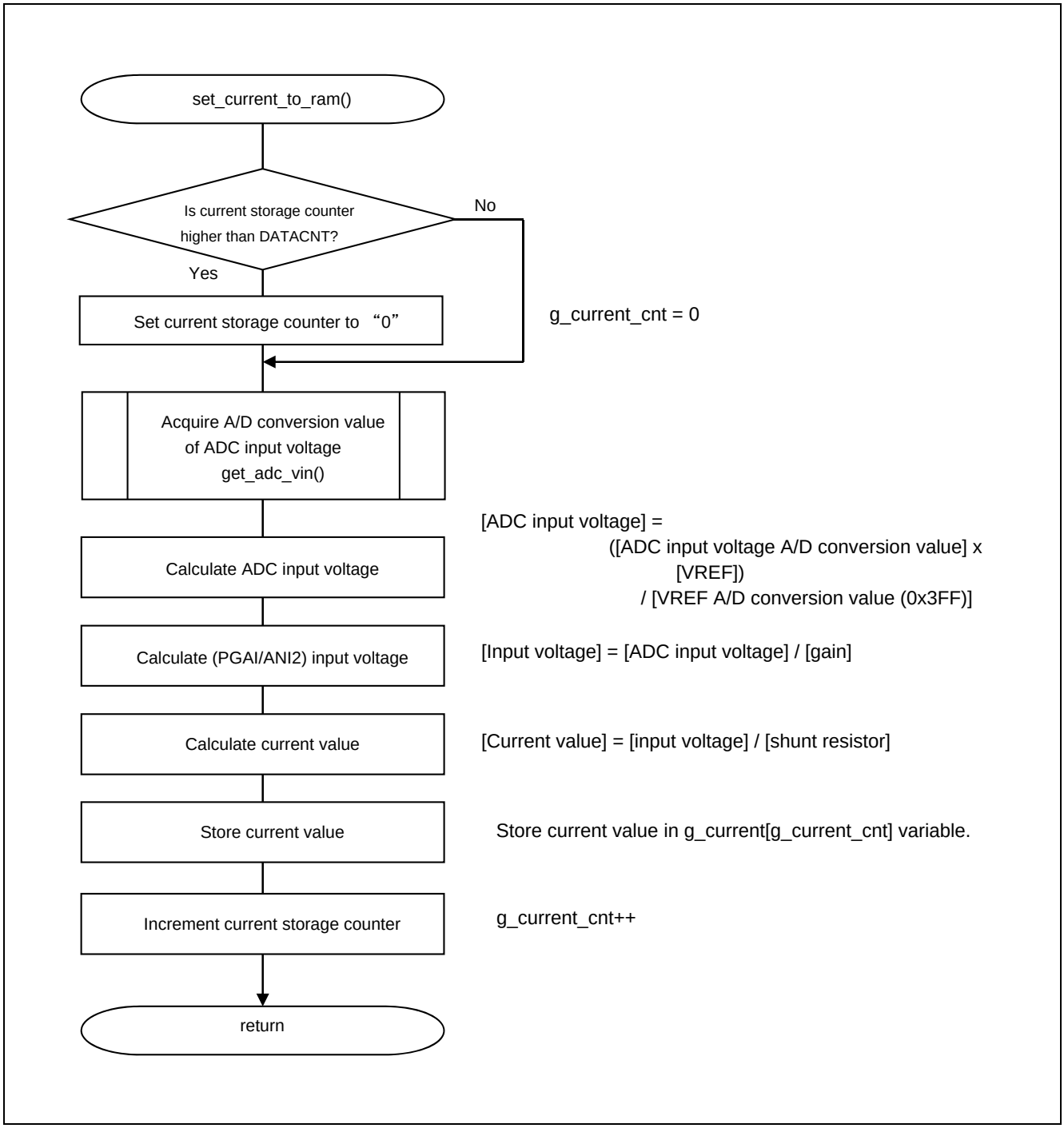

Figure 5.36 Calculate Current Value

5.9.30 Wait Time

Figure 5.37 shows the flowchart for wait time.

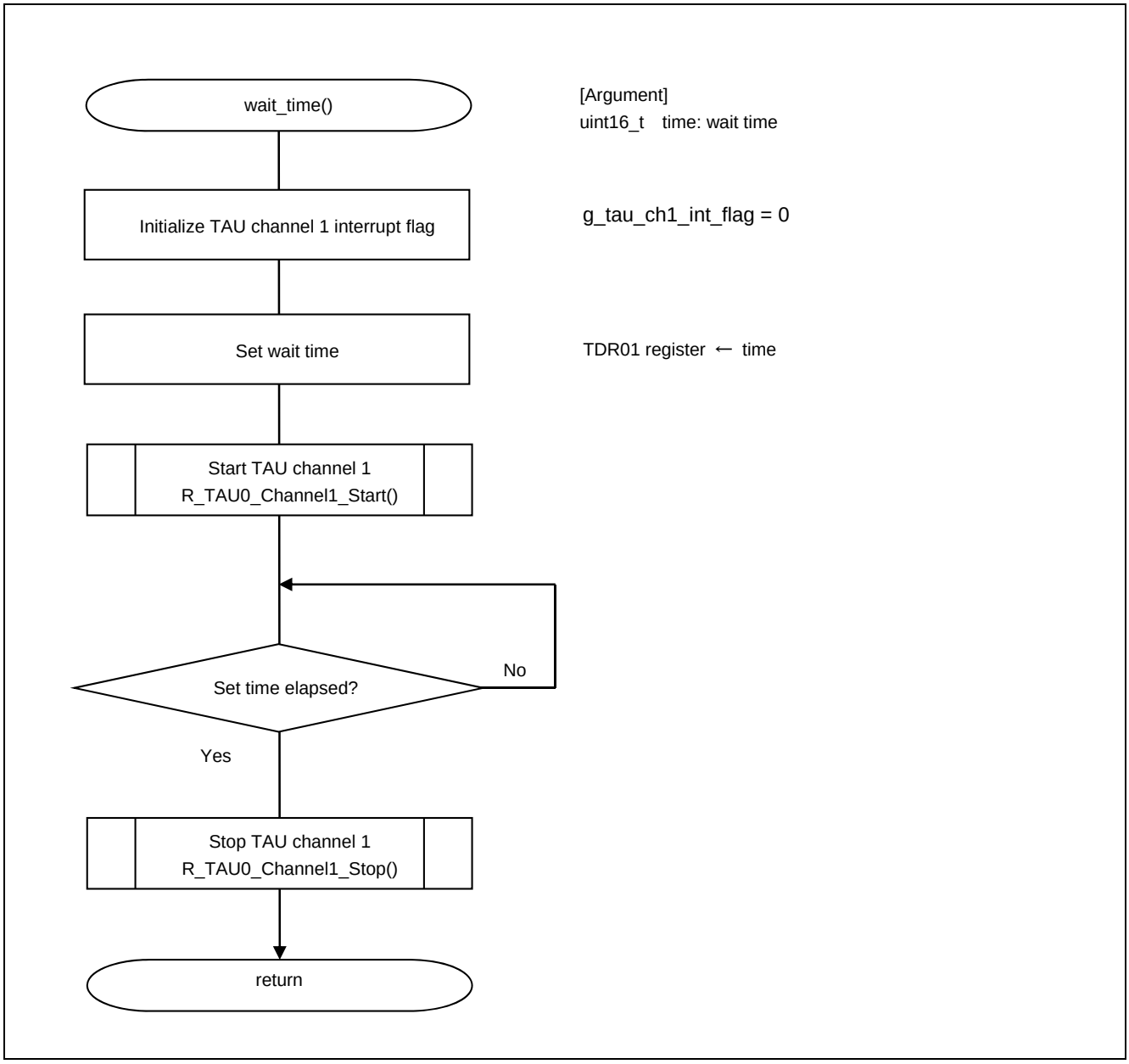

Figure 5.37 Wait Time

6. Sample Code

Please download the sample code from the Renesas Electronics website.

7. Reference Documents

RL78/G1F User's Manual: Hardware Rev.1.00 (R01UH0516E)

RL78 Family User's Manual: Software Rev.2.20 (R01US0015E)

(Download the latest version from the Renesas Electronics website.)

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Revision History	RL78/G1F Current Measurement with Programmable gain amplifier (PGA) CC-RL

Rev.	Date	Description	
		Page	Summary
1.00	Sep.24, 2015	—	First edition issued.
2.00	Feb.10, 2016	5	Second edition issued. Added e2studio in Operation Confirmation Conditions update

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

- 1. Handling of Unused Pins

  Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

  — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

- 2. Processing at Power-on

  The state of the product is undefined at the moment when power is supplied.

  — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
  In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
  In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

- 3. Prohibition of Access to Reserved Addresses

  Access to reserved addresses is prohibited.

  — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

- 4. Clock Signals

  After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

  — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

- 5. Differences between Products

  Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

  — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

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Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HALII Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

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