RL78/G14, R8C/36M Group

Migration Guide from R8C to RL78: Power Control

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Introduction

This document describes how to migrate the power control (setting CPU clock operation mode) of the R8C/36M Group to setting CPU clock operation mode of the RL78/G14 (a 64-pin product is taken as an example in this document).

Target Device

RL78/G14, R8C/36M Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Migration Method from R8C Family to RL78 Family

The following sections describe how to implement the power control of the R8C/36M group by using the CPU clock operation mode setting of the RL78/G14. This application note only summarizes the operation modes to which transition is possible. For the specific conditions for operation mode transition, refer to the relevant user's manual.

Table 1.1 shows Power Control in R8C/36M Group (Summary). Figure 1.1 shows Power Control Status Transition in R8C/36M Group (Summary).

Table 1.2 shows Setting CPU Clock Operation Mode in RL78/G14 (Summary). Figure 1.2 shows CPU Clock Status Transition in RL78/G14 (Summary).

For more detailed status transition diagram than Figure 1.1 and Figure 1.2, refer to the following user's manuals and application notes.

R8C/36M Group User's Manual: Hardware (R01UH0259)
Figure "State Transitions in Power Control Mode" in chapter "Clock Generation Circuit"
RL78/G14 User's Manual: Hardware (R01UH0186)
Figure "CPU Clock Status Transition Diagram" in chapter "Clock Generator"
Application Note
RL78/G13 CPU Clock Changing and Standby Settings (C Language) CC-RL (R01AN3128)

With the R8C/36M group, the low-speed on-chip oscillator is selected as the CPU clock source immediately after a reset release, whereas the high-speed on-chip oscillator clock is selected with the RL78/G14.

With the RL78/G14, the low-speed on-chip oscillator clock cannot be used as the CPU clock source (it can only be uses as the clock for the watchdog timer, real-time clock, 12-bit interval timer, and timer RJ).

Table 1.3 shows the Correspondences between Power control in R8C/36M Group and Setting CPU Clock Operation Mode in RL78/G14.

Table 1.1 Power Control in R8C/36M Group (Summary)

Power Control in R8C/36M Group	
Mode	**Function**
Standard Operating Mode (All modes other than wait mode and stop mode)	Standard operating mode is separated into four modes (high-/low-speed clock mode, high-/low-speed on-chip oscillator mode). In standard operating mode, the CPU clock and peripheral function clock (fi (i = 1, 2, 4, 8, 32)) are supplied to operate the CPU and the peripheral functions.
Wait Mode	Since the CPU clock stops in wait mode, the CPU operating with the CPU clock and the watchdog timer when count source protection mode is disabled stop. Since the XIN clock, XCIN clock, and on-chip oscillator clock do not stop, the peripheral functions using these clocks continue operating.
Stop Mode	Since all oscillator circuits except fOCO-WDT stop in stop mode, the CPU and peripheral function clocks stop and the CPU and the peripheral functions operating with these clocks also stop. The least power required to operate the MCU is in stop mode.

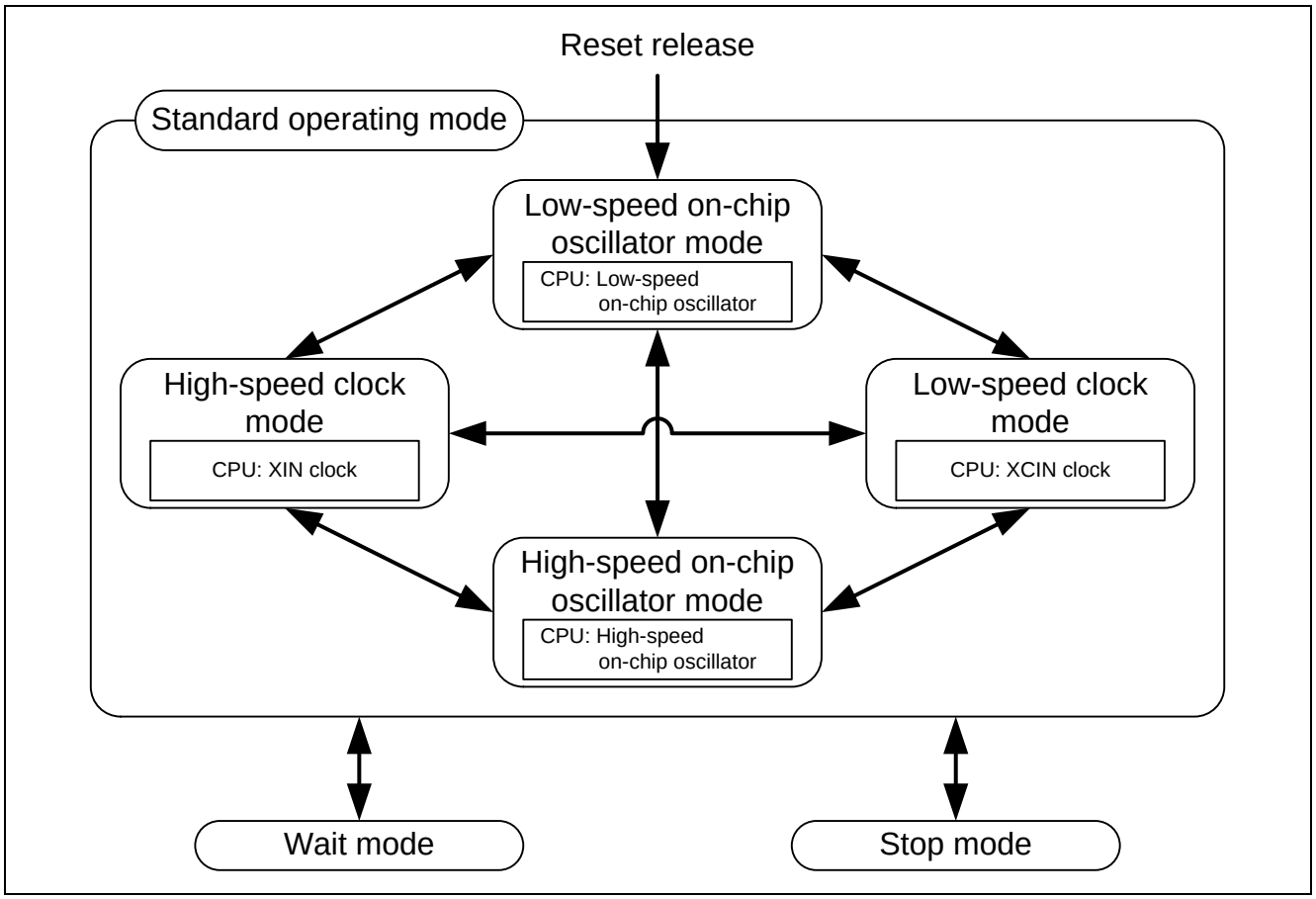

Figure 1.1 Power Control Status Transition in R8C/36M Group (Summary)

Table 1.2 Setting CPU Clock Operation Mode in RL78/G14 (Summary)

Setting CPU Clock Operation Mode in RL78/G14	
Mode	**Function**
Normal operation mode (All modes other than HALT mode, STOP mode and SNOOZE mode)	In normal operation mode, the main system clock (high-speed on-chip oscillator clock, high-speed system clock) or subsystem clock can be used as the CPU clock. To use the peripheral functions after a reset release, set the pertinent bits in the PER0 and PER1 registers to enable clock supply to the corresponding peripheral functions. After a reset release, each bit in the PER0 and PER1 register is 0 (clock supply to each peripheral function is disabled).
HALT mode	The CPU operation clock is stopped. If the high-speed system clock oscillator, high-speed on-chip oscillator, or subsystem clock oscillator is operating before the HALT mode is set, oscillation of each clock continues. If WDSTBYON bit of the option byte is 0, the watchdog timer stops operation.
STOP mode	The high-speed system clock oscillator and high-speed on-chip oscillator stop, stopping the whole system. If WDSTBYON bit of the option byte is 0, the watchdog timer stops operation.
SNOOZE mode	In the case of CSI or UART data reception, an A/D conversion request by the timer trigger signal (the interrupt request signal (INTRTC/INTIT) or ELC event input), and DTC start source, the STOP mode is exited, the CSI or UART data is received without operating the CPU, A/D conversion is performed, and DTC start source.

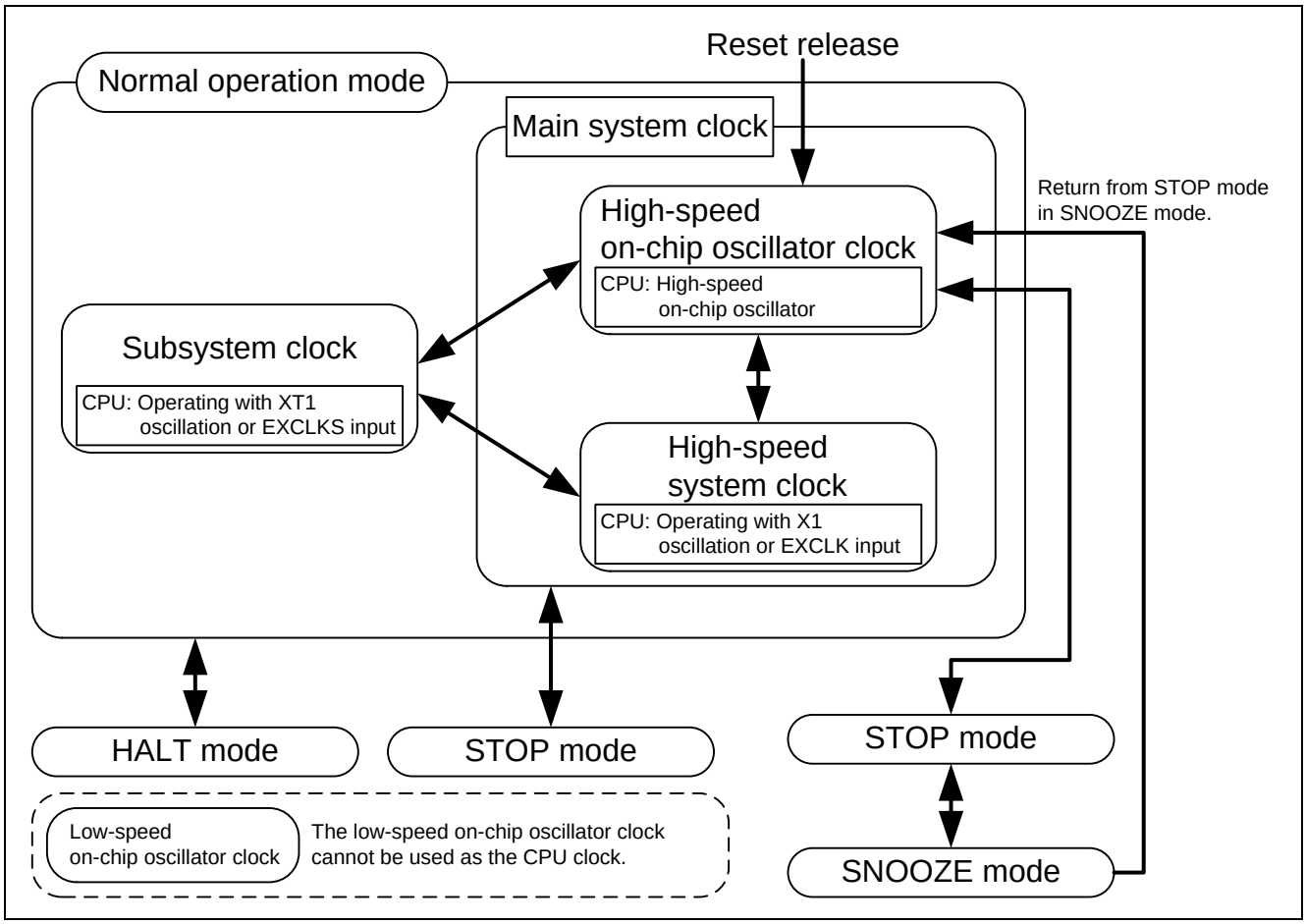

Figure 1.2 CPU Clock Status Transition in RL78/G14 (Summary)

Table 1.3 Correspondences between Power control in R8C/36M Group and Setting CPU Clock Operation Mode in RL78/G14

Power control in R8C/36M Group		Setting CPU Clock Operation Mode in RL78/G14
Operation mode name		Operation mode name
Standard Operating Mode (All modes other than wait mode and stop mode)	High-speed clock mode	Normal operation mode (All modes other than HALT mode, STOP mode and SNOOZE mode)
	Low-speed clock mode	
	High-speed on-chip oscillator mode	
	Low-speed on-chip oscillator mode	
Wait Mode		HALT mode
Stop Mode		STOP mode
—		SNOOZE mode

1.1 Differences in Low Power Consumption Setting

The R8C/36M group and RL78/G14 are provided with a specific function for reducing power consumption of a microcontroller. The following sections describe the differences between wait mode and stop mode of the R8C/36M group and HALT mode and STOP mode of the RL78/G14.

1.1.1 Differences between Wait Mode and HALT Mode

In HALT mode of the RL78/G14, the CPU operation clock is halted without stopping the oscillation of the high-speed on-chip oscillator clock, high-speed system clock (X1 clock or external main system clock), subsystem clock (XT1 clock or external subsystem clock), and low-speed on-chip oscillator clock. This mode is equivalent to wait mode of the R8C/36M group.

Executing the HALT instruction sets HALT mode and issuing an interrupt request allows the CPU to exit HALT mode. Table 1.4 and Table 1.5 compare the functions of R8C/36M group wait mode and RL78/G14 HALT mode.

Table 1.4 Comparison between Functions of R8C/36M Group Wait Mode and RL78/G14 HALT Mode (1/2)

Item	R8C/36M Group Wait Mode	RL78/G14 HALT Mode
Clocks stopped in wait mode/HALT mode	Clock supply to the CPU is stopped.	Clock supply to the CPU is stopped.
Enabling/disabling clock supply to peripheral hardware (setting possible in any of wait, stop, HALT, STOP, and SNOOZE mode)	• Either enabling or disabling clock supply to peripheral functions is possible. [Setting method] Set the pertinent MSTCR register bits (corresponding to SSU, I²C bus, timer RD, timer RC, and timer RG).	• Either enabling or disabling clock supply to peripheral functions is possible. (Note 1) [Setting method] Set the pertinent PER0 and PER1 register bits corresponding to the peripheral functions.
Setting operations of peripheral function clocks in wait mode/HALT mode	• Clock supply can be stopped to the peripheral functions that use a peripheral function clock (f1, f2, f4, f8, or f32) as a clock source. [Setting method] Set the CM02 bit in the CM0 register to 1 (peripheral function clock stops in wait mode). • Watchdog timer stops when count source protect mode is disabled.	• Subsystem clock supply can be stopped to the peripheral functions except the real-time clock and 12-bit interval timer. [Setting method] Set the RTCLPC bit in the OSMC register to 1 when the CPU is operating with the subsystem clock.

Note 1. After a reset release, each bit in the PER0 and PER1 register is 0 (clock supply to the corresponding peripheral function is disabled).

Table 1.5 Comparison between Functions of R8C/36M Group Wait Mode and RL78/G14 HALT Mode (2/2)

Item	R8C/36M Group Wait Mode	RL78/G14 HALT Mode
Method of entering wait mode/HALT mode	Either of the following two methods can be used. • Execute the WAIT instruction (when exiting wait mode by using an interrupt). → Set the I flag to 1 (enable maskable interrupts) and then execute the WAIT instruction. • Write 1 to the CM30 bit in the CM3 register (when exiting wait mode by an interrupt request). → Set the I flag to 0 (disable maskable interrupts) and then write 1 to the CM30 bit.	Execute the HALT instruction (Note 1) • When exiting HALT mode by using an interrupt → Set the IE flag to enable interrupts and then execute the HALT instruction. • When exiting HALT mode by an interrupt request → Set the IE flag to disable interrupts and then execute the HALT instruction.
Method of exiting wait mode/HALT mode	• Interrupt requests from peripheral functions • Reset	• Interrupt requests from peripheral functions • Reset
Pin status in wait mode/HALT mode	Remains the status before entering wait mode.	Remains the status before entering HALT mode.
CPU clock source after exiting wait mode/HALT mode	• CPU clock immediately before entering wait mode (CM37 and CM36 bits = 00b) • XIN clock (CM37 and CM36bits = 11b)	• CPU/peripheral hardware clock immediately before entering HALT mode
CPU clock division ratio after exiting wait mode/HALT mode	• No division (CM35 bit = 1) • Division ratio set with the CM06, CM16, and CM17 bits (CM35 bit = 0)	• Continues to use the division ratio immediately before entering HALT mode.

Note 1. For the interrupt to be used as the source of exiting HALT mode, the pertinent interrupt mask flag register should be set to enable the interrupt processing before entering HALT mode.

1.1.2 Differences in STOP Mode

In STOP mode of the RL78/G14, the high-speed on-chip oscillator clock and high-speed system clock (X1 clock or external main system clock) are stopped to stop the entire system. This mode is equivalent to stop mode of the R8C/36M group.

Executing the STOP instruction sets STOP mode and issuing an interrupt request allows the CPU to exit STOP mode. Table 1.6 and Table 1.7 compare the functions of R8C/36M group stop mode and RL78/G14 STOP mode.

Table 1.6 Comparison between Functions of R8C/36M Group Stop Mode and RL78/G14 STOP Mode (1/2)

Item	R8C/36M Group Stop Mode	RL78/G14 STOP Mode
Clocks stopped in stop mode/STOP mode	All the oscillators stop except fOCO-WDT.	High-speed system clock oscillator and high-speed on-chip oscillator stop.
Method of entering stop mode/STOP mode	• Write 1 to the CM10 bit. → Since an interrupt is used to exit stop mode, set the I flag to 1 (enable maskable interrupts) and then write 1 to the CM10 bit.	Execute the STOP instruction (Note 1) • When exiting STOP mode by using an interrupt → Set the IE flag to enable interrupts and then execute the STOP instruction. • When exiting STOP mode by an interrupt request → Set the IE flag to disable interrupts and then execute the STOP instruction.
Method of exiting stop mode/STOP mode	• Interrupt requests from peripheral functions • Reset	• Interrupt requests from peripheral functions • Reset

Note 1. For the interrupt to be used as the source of exiting STOP mode, the pertinent interrupt mask flag register should be set to enable the interrupt processing before entering STOP mode.

Table 1.7 Comparison between Functions of R8C/36M Group Stop Mode and RL78/G14 STOP Mode (2/2)

Item	R8C/36M Group Stop Mode	RL78/G14 STOP Mode
Pin status in stop mode/STOP mode	Remains the status before entering stop mode.	Remains the status before entering STOP mode.
CPU clock source after exiting stop mode/STOP mode	• Clock immediately before entering stop mode (Note 1) (CM37 and CM36 bits = 00b) • XIN clock (CM37 and CM36 bits = 11b)	• Main system clock immediately before entering STOP mode
CPU clock division ratio after exiting stop mode/STOP mode	• Divide by 8 (When entering stop mode, the CM06 bit is set to 1 (divide-by-8 mode).)	• Continues to use the division ratio immediately before entering STOP mode.
Main clock oscillation stabilization time after exiting stop mode/STOP mode	• Create a loop counter with software to secure the oscillation stabilization time.	• For the high-speed on-chip oscillator, the oscillation stabilization time is secured within the STOP mode release time. • For X1 oscillation A dedicated timer is provided to measure the X1 clock oscillation stabilization time. [To secure the oscillation stabilization time that can be selected with the OSTS register] Setting the OSTS register before entering STOP mode allows the oscillation stabilization time secured (the count can be checked with the OSTC register). [To secure the oscillation stabilization time that cannot be selected with the OSTS register] Create a loop counter with software to secure the oscillation stabilization time.

Note 1. If the high-speed on-chip oscillator mode is selected as the system clock, do not enter stop mode with the CM37 and CM36 bits set to 00b.

1.2 Reducing Power Consumption

For reduction of power consumption of the R8C/36M group and the RL78/G14, refer to the relevant sections in the following user's manuals and consider the suitable implementation for your system.

R8C/36M Group User's Manual: Hardware (R01UH0259)
Section "Power Control" in chapter "Clock Generation Circuit"
Chapter "Reducing Power Consumption"

RL78/G14 User's Manual: Hardware (R01UH0186)
Chapter "Standby Function"

2. Reference Application Note

RL78/G13 CPU Clock Changing and Standby Settings (C Language) CC-RL (R01AN3128)
RL78/G14, R8C/36M Group Migration Guide from R8C to RL78: Clock Generator (R01AN1386)
The latest versions can be downloaded from the Renesas Electronics website.

3. Reference Documents

User's Manual: Hardware
RL78/G14 User's Manual: Hardware (R01UH0186)
R8C/36M Group User's Manual: Hardware (R01UH0259)
The latest versions can be downloaded from the Renesas Electronics website.

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Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	Sep. 05, 2018	-	First edition issued

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1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

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