RL78/G14, H8/36109

Migration Guide from H8 to RL78: IIC2

Introduction

This application note describes how to migrate the I^2C Bus Interface 2 (IIC2) of the H8/36109 to the serial interface IICA of the RL78/G14 (100-pin package).

Target Device

RL78/G14, H8/36109

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Functions of I²C Bus Interface 2 (IIC2) of H8/36109 and serial interface IICA of RL78/G14

Table 1.1 shows the functions of the I2C Bus Interface 2 (IIC2) of H8/36109, and Table 1.2 shows the functions of the serial interface IICA of RL78/G14.

Table 1.1 Functions of I²C Bus Interface 2 (IIC2)

Function	Explanation
I²C bus format communication	Communication conforming to the I²C bus format
Clocked synchronous serial format communication	Clocked synchronous serial communication (8-bit data, MSB- or LSB-first selectable)

Table 1.2 Functions of serial interface IICA

Function	Explanation
I²C bus mode (multimaster supported)	This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLAn) line and a serial data bus (SDAAn) line. This mode complies with the I2C bus format and the master device can generated “start condition”, “address”, “transfer direction specification”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received status and data by hardware. This function can simplify the part of application program that controls the I2C bus.

Remarks1. For RL78/G14, n: Channel number (n = 0, 1)

Remarks2. Different products are provided with different functions. For details, refer to the appropriate user’s manuals (hardware).

Table 1.3 shows the serial interface IICA of RL78/G14 functions corresponding to the I2C Bus Interface 2 (IIC2) of H8/361094.

Table 1.3 Correspondence between Functions

H8/36109 IIC2	RL78/G14 IICA
I²C bus format communication	I²C bus mode
Clocked synchronous serial format communication	Substituted by 3-wire serial I/O (CSI) of SAU

I²C bus format communication of I²C bus interface 2 (IIC2) corresponds to I²C bus mode of IICA.

Clocked synchronous serial format communication of I²C bus interface 2 (IIC2) virtually corresponds to the 3-wire serial I/O (CSI) of the serial array unit (SAU).

2. Summary of Differences between Functions

Table 2.1 summarizes the differences between the functions IIC2 and IICA.

Table 2.1 Summary of Differences between Functions

Item	H8/36109 I²C bus interface 2 (IIC2)	RL78/G14 Serial interface IICA
Communication format	I²C bus format	I²C bus format
Input / output pin	- SCL (Input/output) IIC serial clock input/output - SDA (Input/output) IIC serial data input/output	- SCLA0, SCLA1 (Note) Serial clock input/output of serial interface IICA0, IICA1 (Note) - SDAA0, SDAA1 (Note) Serial data input/output of serial interface IICA0, IICA1 (Note)
Transfer clock	Internal clock (In master mode) / External clock (In slave mode)	Internal clock (In master mode) / External clock (In slave mode)
Interrupt generation timing	- Transmit data empty (including slave-address match), - Transmit end - Receive data full (including slave-address match) - Arbitration lost - NACK detection - Stop condition detection	- Falling edge of eighth or ninth clock of the serial clock (set by the WTIMn bit) (Note) - Interrupt request generated when a stop condition is detected (set by the SPIEn bit)
Detection of ACK / NACK	Yes	Yes
Bit synchronization / wait function	Yes	Yes
Detection of arbitration lost	Yes	Yes
Selection of acknowledge output levels when receiving	Yes	Yes
Noise canceler	Yes	Yes
Return from standby mode (STOP mode)	None	Yes (In slave mode)

Note. 80, 100-pin products only.

3. Comparison between Registers

Table 3.1 to Table 3.3 compares the registers for the H8/36109 IIC2 and the registers for the RL78/G14 IICA.

Table 3.1 Comparison between Registers (1/3)

Item	H8/36109 I²C bus interface 2 (IIC2)	RL78/G14 Serial interface IICA
Control of IIC2 input clock supply	MSTCR1 register MSTIIC bit	None
Control of serial interface IICAn input clock supply	None	PER0 register IICA1EN bit (Note), IICA0EN bit
I²C bus control register 1	ICCR1 register	None
I²C Bus Interface Enable	ICCR1 register ICE bit	IICCTLn0 register IICEn bit
Reception Disable	ICCR1 register RCVD bit	None
Master/Slave Select	ICCR1 register MST bit, TRS bit	None - Master communication state is entered when a start condition (ST) is detected after ST is generated. - Slave state is entered when a match of the slave address is detected.
Transfer Clock Select	ICCR1 register CKS3 - CKS0 bit	IICCTLn1 register PRSn bit IICWLn register IICWHn register
I²C Bus Control Register 2	ICCR2 register	None
Bus Busy	ICCR2 register BBSY bit	IICFn register IICBSYn bit
Start/Stop Issue Condition Disable	ICCR2 register SCP bit	IICCTLn0 register STTn bit, SPTn bit
SDA Output Value Control	ICCR2 register SDAO bit	IICCTLn1 register DADn bit
SDAO Write Protect	ICCR2 register SDAOP bit	None
SCL output level monitor	ICCR2 register SCLO bit	IICCTLn1 register CLDn bit
IIC Control Part Reset	ICCR2 register IICRST bit	IICCTLn0 register IICEn bit
I²C Bus Mode Register	ICMR register	None
MSB-First / LSB-First Select	ICMR register MLS bit	None
Wait Insertion Bit	ICMR register WAIT bit	IICCTLn0 register WTIMn bit
BC Write Protect	ICMR register BCWP bit	None
Bit Counter	ICMR register BC2 - BC0 bit	None

Note. 80, 100-pin products only.

Remark. For RL78/G14, n = 0, 1

Table 3.2 Comparison between Registers (2/3)

Item	H8/36109 I²C bus interface 2 (IIC2)	RL78/G14 Serial interface IICA
I²C Bus Interrupt Enable Register	ICIER register	None
Transmit Interrupt Enable	ICIER register TIE bit	None
Transmit End Interrupt Enable	ICIER register TEIE bit	IICCTLn0 register WTIMn bit
Receive Interrupt Enable	ICIER register RIE bit	IICCTLn0 register WTIMn bit
NACK Receive Interrupt Enable	ICIER register NAKIE	None
Stop Condition Detection Interrupt Enable	ICIER register STIE bit	IICCTLn0 register SPIEn bit
Acknowledge Bit Judgment Select	ICIER register ACKE bit	None
Receive Acknowledge	ICIER register ACKBR bit	IICSn register ACKDn bit
Transmit Acknowledge	ICIER register ACKBT bit	IICCTLn0 register ACKEn bit
I²C Bus Status Register	ICSR register	None
Transmit Data Register Empty	ICSR register TDRE bit	None
Transmit End	ICSR register TEND bit	None
Receive Data Register Full	ICSR register RDRF bit	None
No Acknowledge Detection Flag	ICSR register NACKF bit	None
Stop Condition Detection Flag	ICSR register STOP bit	IICSn register SPDn bit
Arbitration Lost Flag / Overrun Error Flag	ICSR register AL/OVE bit	IICSn register ALDn bit
Slave Address Recognition Flag	ICSR register AAS bit	IICSn register COIn bit
General Call Address Recognition Flag	ICSR register ADZ bit	IICSn register EXCn bit
Slave Address Register	SAR register	None
Slave Address	SAR register SVA6 - SVA0 bit	SVAn register Upper 7 bits (bit 0 fixed to 0)
Format Select	SAR register FS bit	None
I²C Bus Transmit Data Register	ICDRT register	IICAn register

Remark. For RL78/G14, n = 0, 1

Table 3.3 Comparison between Registers (3/3)

Item	H8/36109 I²C bus interface 2 (IIC2)	RL78/G14 Serial interface IICA
Exit from communications	None	IICCTLn0 register LRELn bit
Wait cancellation	None	IICCTLn0 register WRELn bit
Master status check flag	None	IICSn register MSTSn bit
Detection of transmit/receive status	None	IICSn register TRCn bit
Detection of start condition	None	IICSn register STDn bit
STTn clear flag	None	IICFn register STCFn bit
Initial start enable trigger	None	IICFn register STCENn bit
Communication reservation function disable bit	None	IICFn register IICRSVn bit
Control of address match wakeup	None	IICCTLn1 register WUPn bit
Operation mode switching	None	IICCTLn1 register SMCn bit
Digital filter operation control	None	IICCTLn1 register DFCn bit

Remark. For RL78/G14, n = 0, 1

4. Sample Code for Serial interface IICA

The sample code for the serial interface IICA is explained in the following application notes.

- RL78/G13 Serial Interface IICA (for Master Transmission/Reception) CC-RL (R01AN2759)
- RL78/G13 Serial Interface IICA (for Slave Transmission/Reception) CC-RL (R01AN2760)

5. Documents for Reference

User's Manual:

- RL78/G14 User's Manual: Hardware (R01UH0186)
- H8/36109 Group User's Manual: Hardware (R01UH0294)

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun.08, 2020	-	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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