RL78/G13

Multiplier and Divider/Multiply-Accumulator (A/D Converter in Sequential Conversion Mode) CC-RL

R01AN2802EJ0100
Rev. 1.00
Apr. 16, 2015

Introduction

This application note explains how to use the multiplier and divider/multiply-accumulator in the multiply-accumulator mode (unsigned). The sample application covered in this application note multiplies the conversion results (for four channels) provided by the A/D converter by different multipliers and accumulates their calculation results for each channel. The application turns on the LED when all of the accumulated values of all the channels exceed a predetermined value.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note explains how to use the multiplier and divider/multiply-accumulator in the multiply-accumulator mode (unsigned). The sample application covered in this application note sets up the multiplier and divider/multiply-accumulator for multiply-accumulator mode (unsigned) operation, multiplies the conversion results (ANI0, ANI1, ANI2, and ANI3) from the A/D converter by the multipliers (10, 11, 12, and 13) assigned to the respective analog input channels, and accumulates their calculation results for each channel. When all of the accumulated values of all the channels exceed a predetermined value (10,000), the application turns on the LED, stops the A/D converter to place in the HALT mode.

Table 1.1 shows the peripheral functions to be used and their uses. Figure 1.1 shows the outline of the multiply-accumulator operation.

Table 1.1 Peripheral Functions to be Used and their Uses

Peripheral Function	Use
Multiplier and divider/multiply-accumulator	Performs multiply-accumulator operation on the A/D conversion results.
A/D converter	Converts the level of the analog signal inputs to pins P20/ANI0 to P23/ANI3.

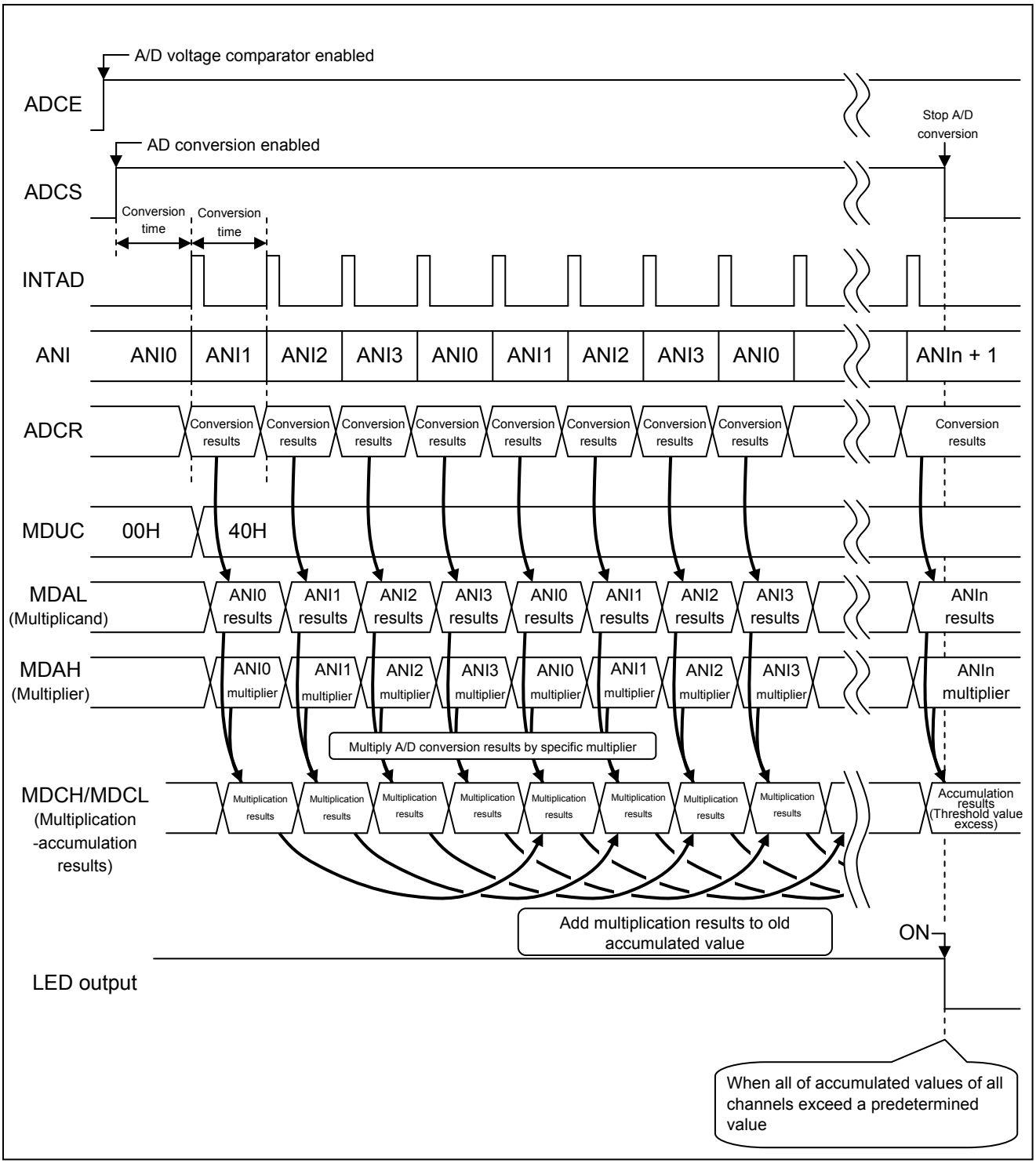

Figure 1.2 Outline of Multiplication-Accumulation Operation

2. Operation Check Conditions

The sample code contained in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (can run on a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 2.81 V (2.76 V to 2.87 V)
Integrated development environment (CS+)	CS+ V3.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.

3. Related Application Note

The application notes that are related to this application note are listed below for reference.

RL78/G13 Initialization (R01AN2575E) Application Note
RL78/G13 A/D Converter (Software Trigger and Sequential Conversion Modes) (R01AN2581E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of hardware configuration that is used for this application note.

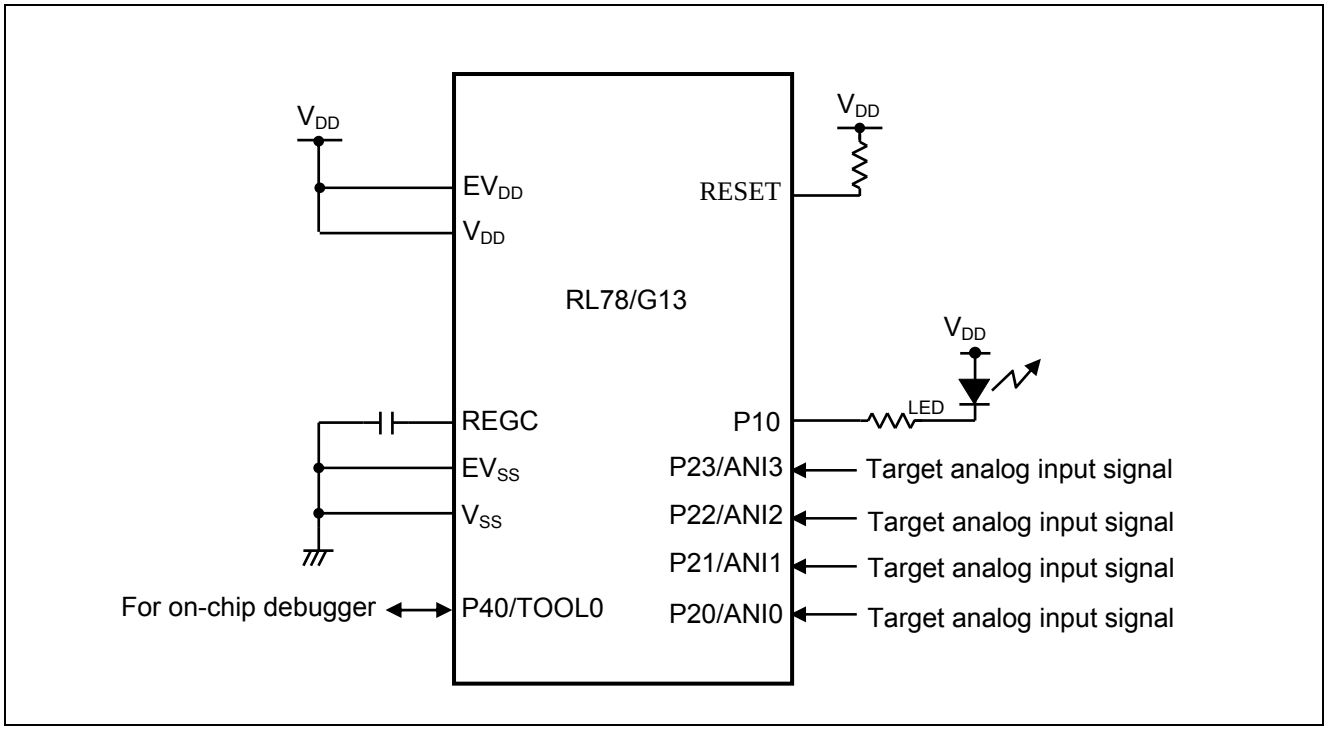

Figure 4.1 Hardware Configuration

Cautions: 1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).

2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P20/ANI0 to P23/ANI3	Input	A/D converter analog input port
P10	Output	LED lighting control port

5. Description of the Software

5.1 Operation Outline

This application note explains how to use the multiplier and divider/multiply-accumulator in the multiply-accumulator mode (unsigned). The sample application covered in this application note sets up the multiplier and divider/multiply-accumulator for multiply-accumulator mode (unsigned) operation, multiplies the conversion results (ANI0, ANI1, ANI2, and ANI3) from the A/D converter by the multipliers (10, 11, 12, and 13) assigned to the respective analog input channels, and accumulates their calculation results for each channel. When all of the accumulated values of all the channels exceeds a predetermined value (10,000), the application turns on the LED, stops the A/D converter to place in the HALT mode.

(1) Initialize the A/D converter.
<Conditions for setting>

- Use pins P20/ANI0 to P23/ANI3 for the analog inputs.
- Set A/D conversion channel selection mode to scan mode.
- Set A/D conversion operation mode to sequential conversion mode.
- Start A/D conversion by using the software trigger.
- Set A/D conversion time to 19 us.
- Use the A/D conversion end interrupt (INTAD).

(2) The sample program sets the ADCS bit in the ADM0 register to 1 (A/D conversion start) to start A/D conversion and executes the HALT instruction to enter the HALT mode and waits for an A/D conversion end interrupt (INTAD).
(3) When the A/D conversion on one channel is completed, its A/D conversion results are transferred to the ADCR register. The HALT mode is exited by the occurrence of an A/D conversion end interrupt (INTAD).
(4) The application places the multiplier and divider/multiply-accumulator in multiply-accumulator mode and multiplies the A/D conversion results by preassigned multiplier. It stores the results of the multiplication in the on-chip RAM, sets up the HALT mode again, and waits for an A/D conversion end interrupt (INTAD).
(5) Subsequently, the application repeats, for each channel, the cycle of multiplying the A/D conversion results by a preassigned multiplier and accumulating its results on each completion of A/D conversion on one channel. When the results of the accumulated values exceed 10,000, the application stops the multiplication-accumulation cycle.
(6) When all of the accumulated values of all channels exceed 10,000, the application turns on the LED connected to P10. The application then stops the A/D converter and transitions to the HALT mode.

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	01101110B	Disables the watchdog timer. (Stops counting after the release from the reset status.)
000C1H/010C1H	01111111B	LVD reset mode, 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11101000B	HS mode HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.3 List of Constants

Table 5.2 lists constants that are used by this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
CHNUM	4	Number of analog input channels to be used
BUFSIZE	64	Size of buffer to store accumulation results
THRESHOLD	0x00010000	Threshold of accumulation results
multiplier_table[4]	10,11,12,13	Values to be used as multipliers

5.4 List of Variables

Table 5.3 lists the global variables that are used by this sample program.

Table 5.3 Global Variable

Type	Variable Name	Contents	Function Used
uint16_t	adc_buffer[4]	Buffer to store A/D conversion results	main()
uint8_t	ch_counter	Counter for the analog input channels	main()
uint32_t	mac_buffer[4] [64]	Buffer to store accumulation results	main()
uint8_t	mac_counter	Counter for counting the number of accumulation	main()
uint8_t	threshold_flag[4]	Threshold value excess flag	main()

5.5 List of Functions

Table 5.4 lists the functions that are used in this sample program.

Table 5.4 Functions

Function Name	Outline
R_ADC_Set_OperationOn	Enables the A/D voltage comparator for operation.
R_ADC_Start	Starts A/D conversion.
R_ADC_Get_Result	Gets the A/D conversion results.
R_ADC_Stop	Stops A/D conversion.

5.6 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] R_ADC_Set_OperationOn

Synopsis	Enable A/D voltage comparator
Header	r_cg_adc.h
Declaration	void R_ADC_Set_OperationOn(void)
Explanation	This function enables the A/D voltage comparator for operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Start

Synopsis	Starts A/D conversion.
Header	r_cg_adc.h
Declaration	void R_ADC_Start(void)
Explanation	This function starts the A/D conversion operation.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Get_Result

Synopsis	Gets the A/D conversion results.
Header	r_cg_adc.h
Declaration	void R_ADC_Get_Result(uint16_t * const buffer)
Explanation	This function gets the A/D conversion results.
Arguments	buffer : Address of RAM area to store conversion results
Return value	None
Remarks	None

[Function Name] R_ADC_Stop

Synopsis	Stops A/D conversion.
Header	r_cg_adc.h
Declaration	void R_ADC_Stop(void)
Explanation	This function stops the A/D conversion operation.
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

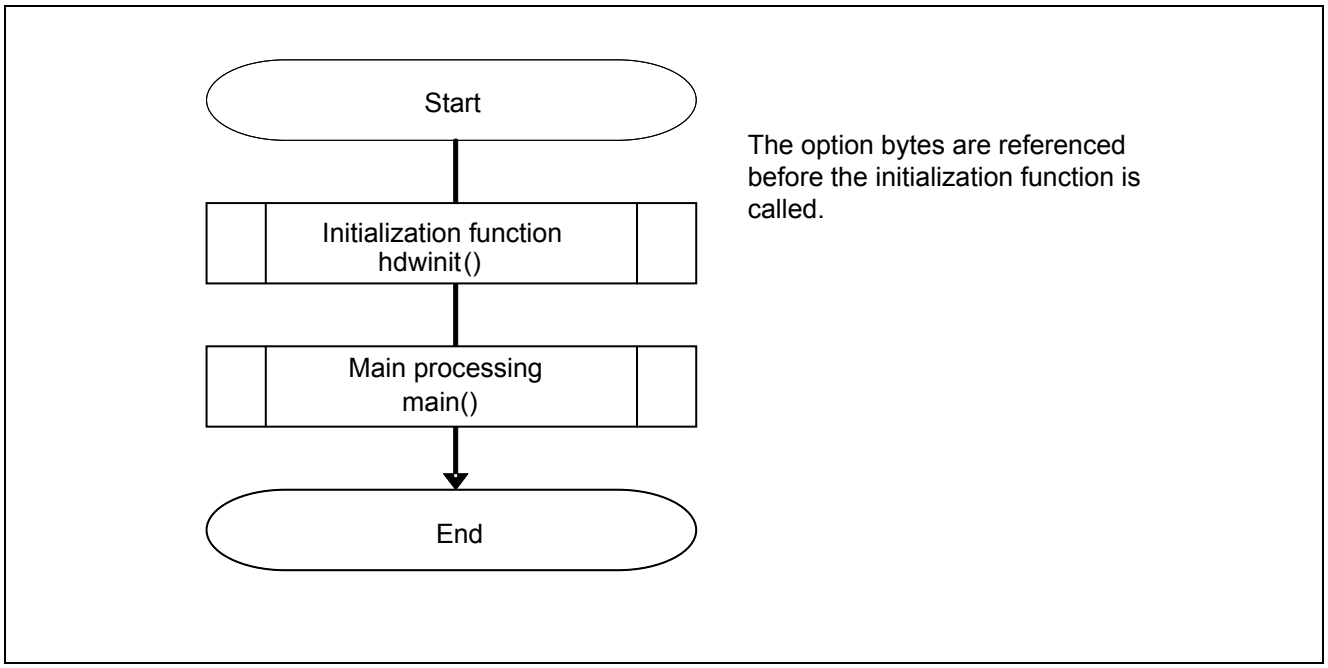

Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

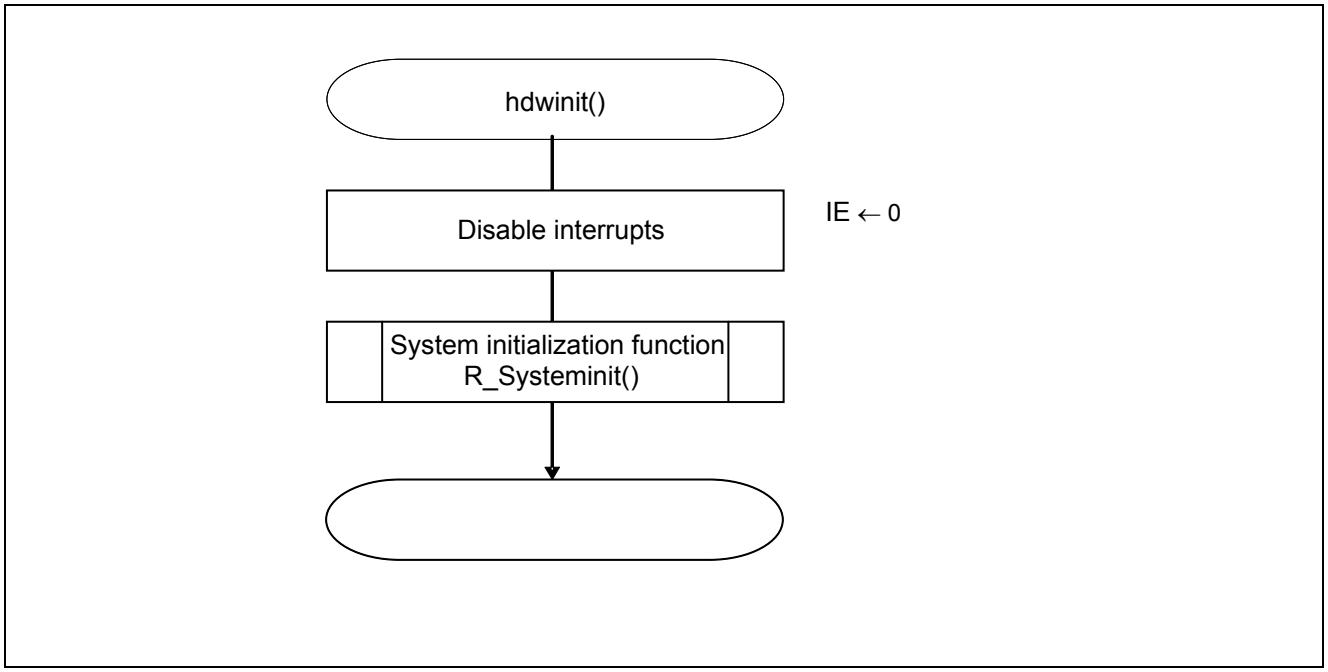

Figure 5.2 Initialization Function

5.7.2 System Initialization Function

Figure 5.3 shows the flowchart for the system initialization function.

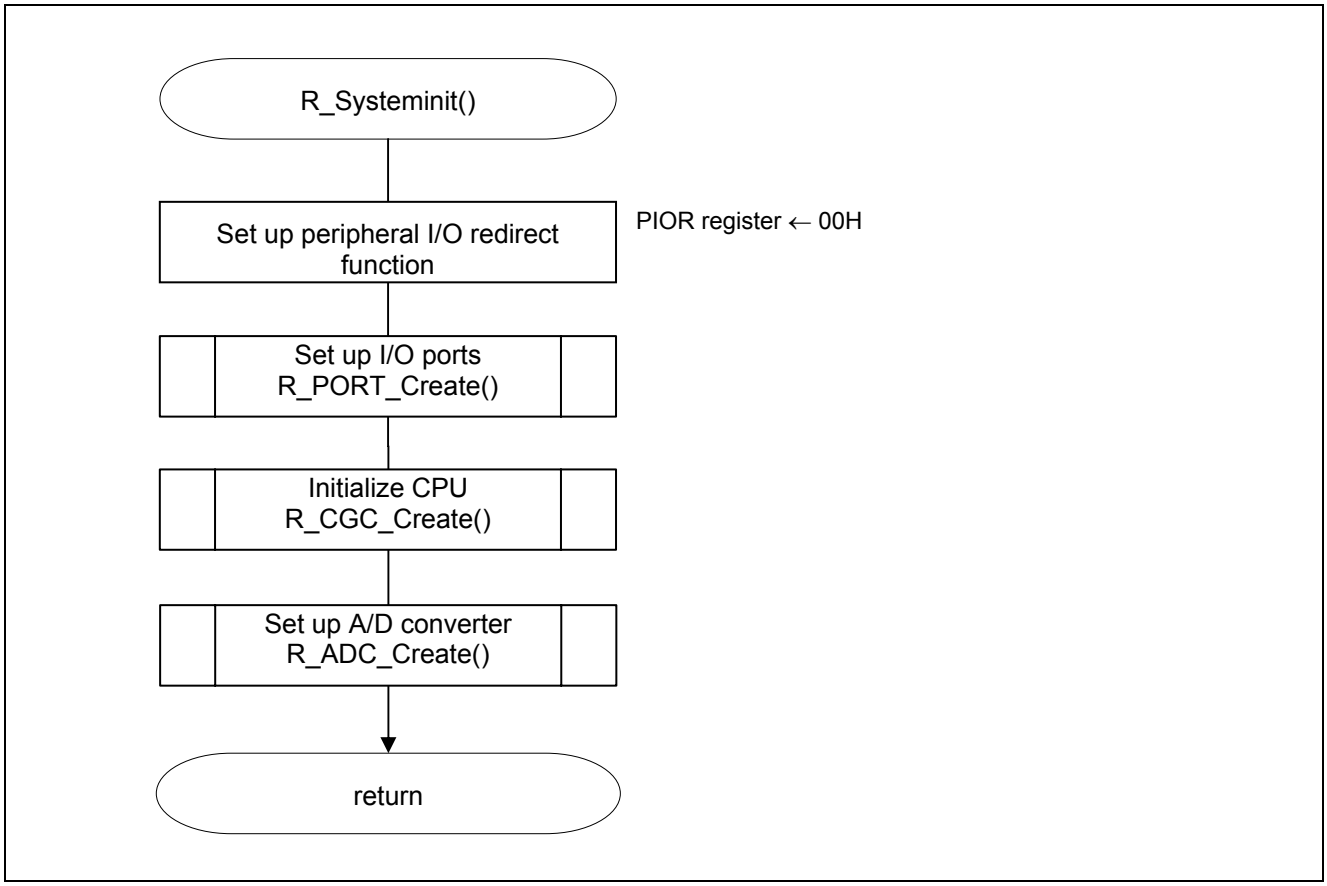

Figure 5.3 System Initialization Function

5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

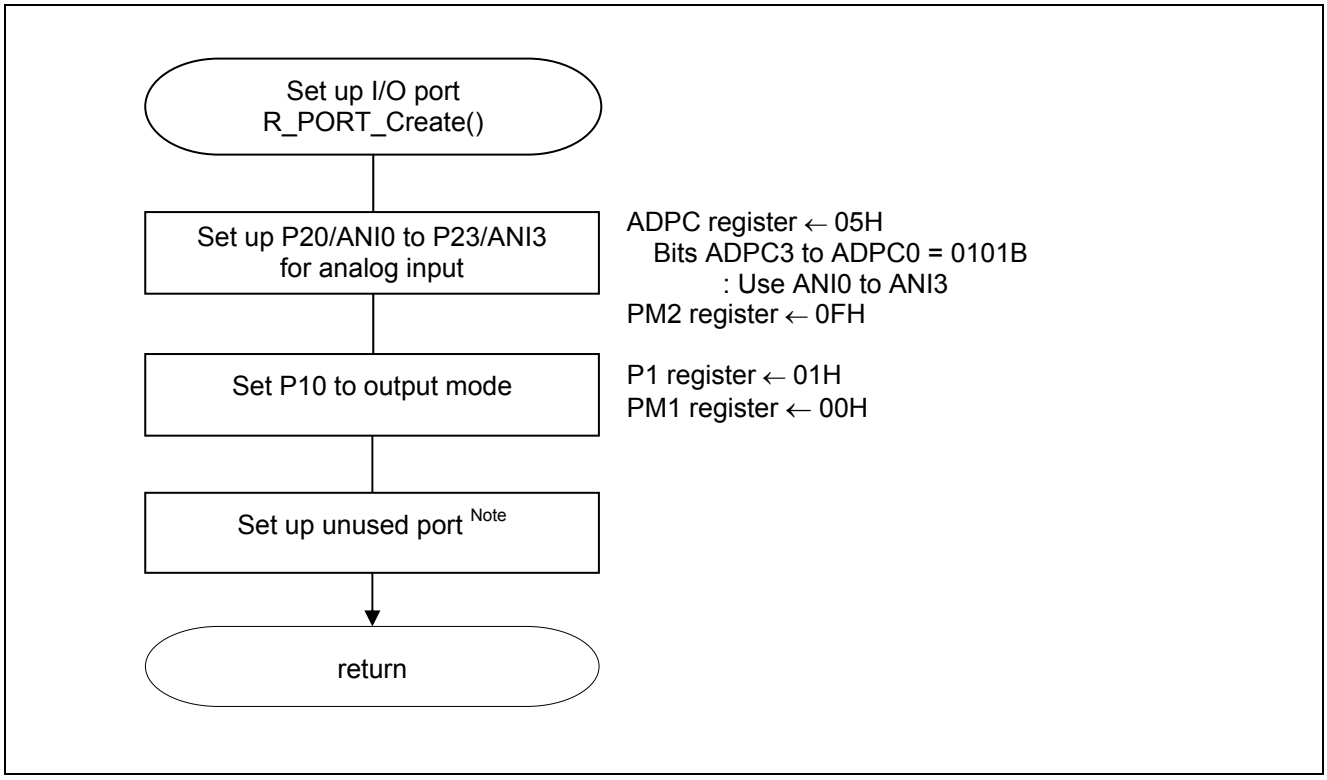

Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up the channel to be used for A/D conversion

- A/D port configuration register (ADPC)
  Switches between A/D converter analog input and port digital I/O.
- Port mode register 2 (PM2)
  Selects the I/O mode of each port.

Symbol: ADPC

7	6	5	4	3	2	1	0
0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0
0	0	0	0	**0**	**1**	**0**	**1**

Bits 3 to 0

ADPC3	ADPC2	ADPC1	ADPC0	Available analog input
0	0	0	0	ANI0 to ANI14
0	0	0	1	None
0	0	1	0	ANI0
0	0	1	1	ANI0 to ANI1
0	1	0	0	ANI0 to ANI2
0	**1**	**0**	**1**	**ANI0 to ANI3**
0	1	1	0	ANI0 to ANI4
0	1	1	1	ANI0 to ANI5
1	0	0	0	ANI0 to ANI6
1	0	0	1	ANI0 to ANI7
1	0	1	0	ANI0 to ANI8
1	0	1	1	ANI0 to ANI9
1	1	0	0	ANI0 to ANI10
1	1	0	1	ANI0 to ANI11
1	1	1	0	ANI0 to ANI12
1	1	1	1	ANI0 to ANI13
Other than above				Setting prohibited

Symbol: PM2

7	6	5	4	3	2	1	0
PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
x	x	x	x	**1**	**1**	**1**	**1**

Bits 3 to 0

PM23 to PM20	P23 to P20 I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up LED ports

- Port register 1 (P1)
- Port mode register 1 (PM1)

Symbol: P0

7	6	5	4	3	2	1	0
P17	P16	P15	P14	P13	P12	P11	P10
0	0	0	0	0	0	0	**1**

Bit 0

P10	P10 pin output data control (in output mode)
0	Output 0
1	**Output 1**

Symbol: PM0

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
1	0	0	0	0	0	0	**0**

Bit 0

PM10	P10 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

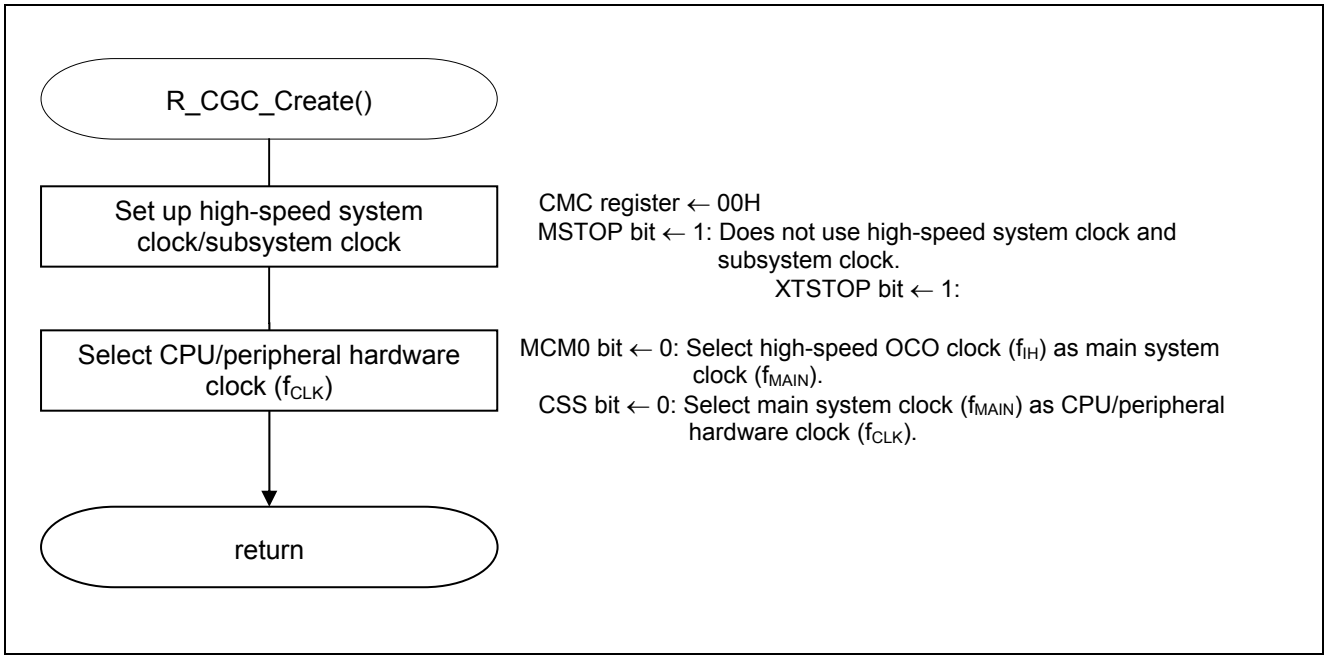

Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E).

5.7.5 A/D Converter Setup

Figure 5.6 shows the flowchart for setting up the A/D converter.

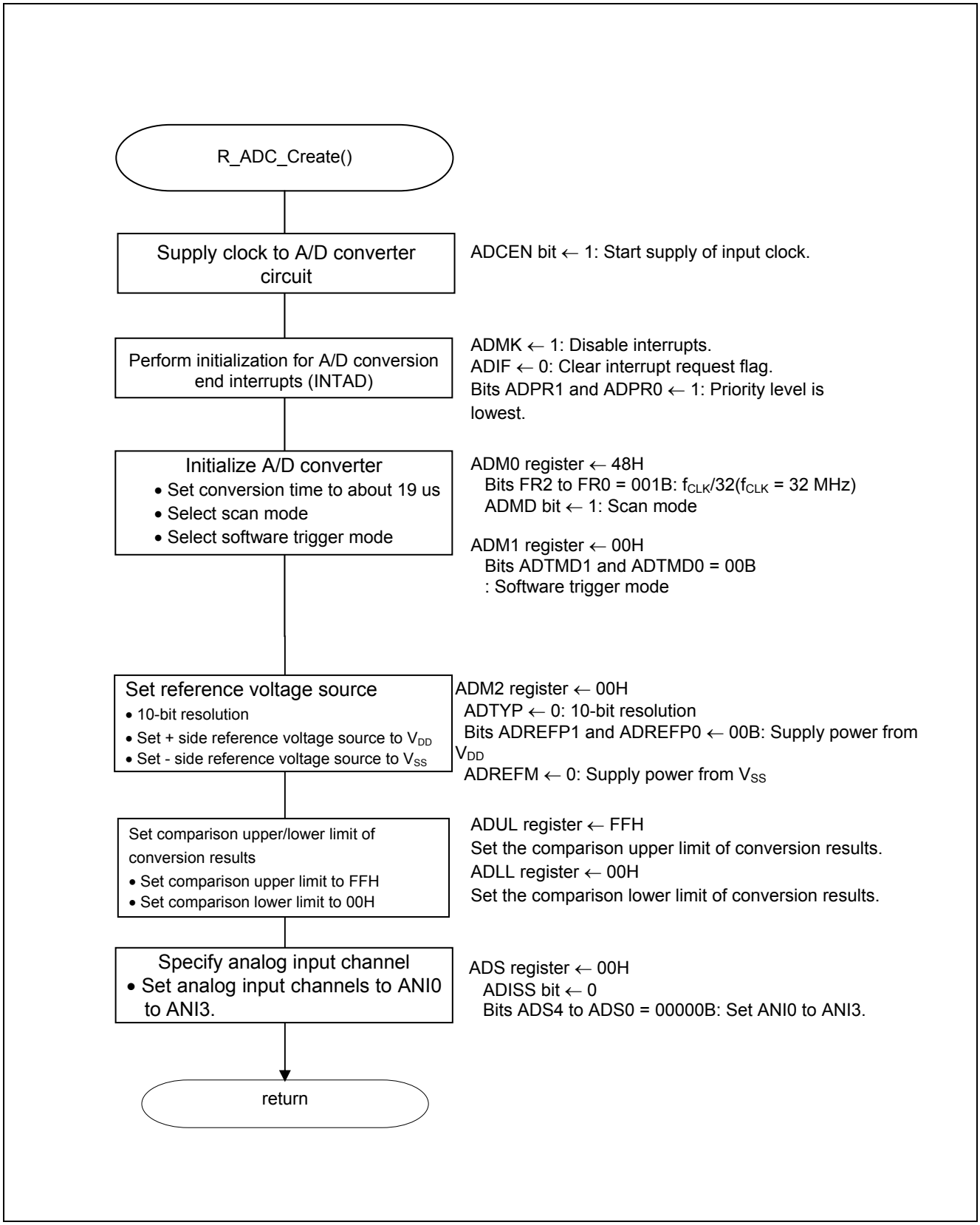

Figure 5.6 A/D Converter Setup

Starting the supply of clock to the A/D converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

  Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	**1**	x	x	x	x	x

  Bit 5

ADCEN	A/D converter input clock control
0	Stops supply of input clock.
1	**Starts supply of input clock.**

  Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the A/D conversion time and operating mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion operation.
  Specifies the A/D channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**1**	**0**	**0**	**1**	**0**	**0**	x

Bit 6

ADMD	Specification of the A/D channel selection mode
0	Select mode
1	**Scan mode**

Bits 5 to 1

ADM0					Mode	Conversion Time Selection						Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	f_{CLK} = 32 MHz	
0	0	0	**0**	**0**	Normal 1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	38 µs	$f_{CLK}/64$
0	**0**	**1**								38 µs	**19 µs**	**$f_{CLK}/32$**
0	1	0							38 µs	19 µs	9.5 µs	$f_{CLK}/16$
0	1	1						38 µs	19 µs	9.5 µs	4.75 µs	$f_{CLK}/8$
1	0	0						28.5 µs	14.25 µs	7.125 µs	3.5625 µs	$f_{CLK}/6$
1	0	1						23.75 µs	11.875 µs	5.938 µs	2.9688 µs	$f_{CLK}/5$
1	1	0					38 µs	19 µs	9.5 µs	4.75 µs	2.375 µs	$f_{CLK}/4$
1	1	1				38 µs	19 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited	$f_{CLK}/2$
0	0	0	0	1	Normal 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	34 µs	$f_{CLK}/64$
0	0	1								34 µs	17 µs	$f_{CLK}/32$
0	1	0							34 µs	17 µs	8.5 µs	$f_{CLK}/16$
0	1	1						34 µs	17 µs	8.5 µs	4.25 µs	$f_{CLK}/8$
1	0	0						25.5 µs	12.75 µs	6.375 µs	3.1875 µs	$f_{CLK}/6$
1	0	1						21.25 µs	10.625 µs	5.3125 µs	2.6536 µs	$f_{CLK}/5$
1	1	0					34 µs	17 µs	8.5 µs	4.25 µs	2.125 µs	$f_{CLK}/4$
1	1	1				34 µs	17 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited	$f_{CLK}/2$
x	x	x	1	0	Low-voltage 1	Setting prohibited						—
x	x	x	1	1	Low-voltage 2	Setting prohibited						—

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the A/D conversion trigger

- A/D converter mode register 1 (ADM1)
  Selects the A/D conversion trigger mode.
  Selects the A/D conversion operating mode.

  Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
0	**0**	**0**	0	0	0	0	0

  Bits 7 and 6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	**—**	**Software trigger mode**
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

  Bit 5

ADSCM	Selection of the A/D conversion mode
0	**Sequential conversion mode**
1	One-shot conversion mode

  Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the reference voltage

- A/D converter mode register 2 (ADM2)
  Sets up the reference voltage source.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADCRK	AWC	0	ADTYP
0	**0**	**0**	0	**0**	**0**	0	**0**

Bits 7 and 6

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	**0**	**Supplied from V_{DD}**
0	1	Supplied from P20/AV_{REFP}/ANI0
1	0	Supplied from internal reference voltage (1.45 V)
1	1	Setting prohibited

Bit 5

ADREFM	Selection of the - side reference voltage source of the A/D converter
0	**Supplied from V_{SS}**
1	Supplied from P21/AV_{REFM}/ANI1

Bit 3

ADCRK	Checking the upper limit and lower limit conversion result values
0	**Interrupt signal (INTAD) occurs when ADLL register ≦ ADCR register ≦ ADUL register.**
1	Interrupt signal (INTAD) occurs when ADCR register < ADLL register and ADUL register < ADCR register.

Bit 2

AWC	Specification of the wakeup (SNOOZE mode) function
0	**Does not use the SNOOZE mode function.**
1	Uses the SNOOZE mode function.

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the conversion result comparison upper limit/lower limit

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison lower limit setting register (ADLL)
  Sets up the conversion result comparison upper and lower limits.

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Specifying the input channel

- Analog input channel register (ADS)
  Specifies the input channel for the analog signal to be subjected to A/D.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	0	0	**0**	**0**	**0**	**0**	**0**

Bits 7 and 4 to 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog Input Channel			
						Scan 0	Scan 1	Scan 2	Scan 3
0	**0**	**0**	**0**	**0**	**0**	**ANI0**	**ANI1**	**ANI2**	**ANI3**
0	0	0	0	0	1	ANI1	ANI2	ANI3	ANI4
0	0	0	0	1	0	ANI2	ANI3	ANI4	ANI5
0	0	0	0	1	1	ANI3	ANI4	ANI5	ANI6
:						:			
0	0	1	0	1	0	ANI10	ANI11	ANI12	ANI13
0	0	1	0	1	1	ANI11	ANI12	ANI13	ANI14
Other than above						Setting prohibited			

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.6 Main Processing

Figures 5.7 show the flowchart for the main processing.

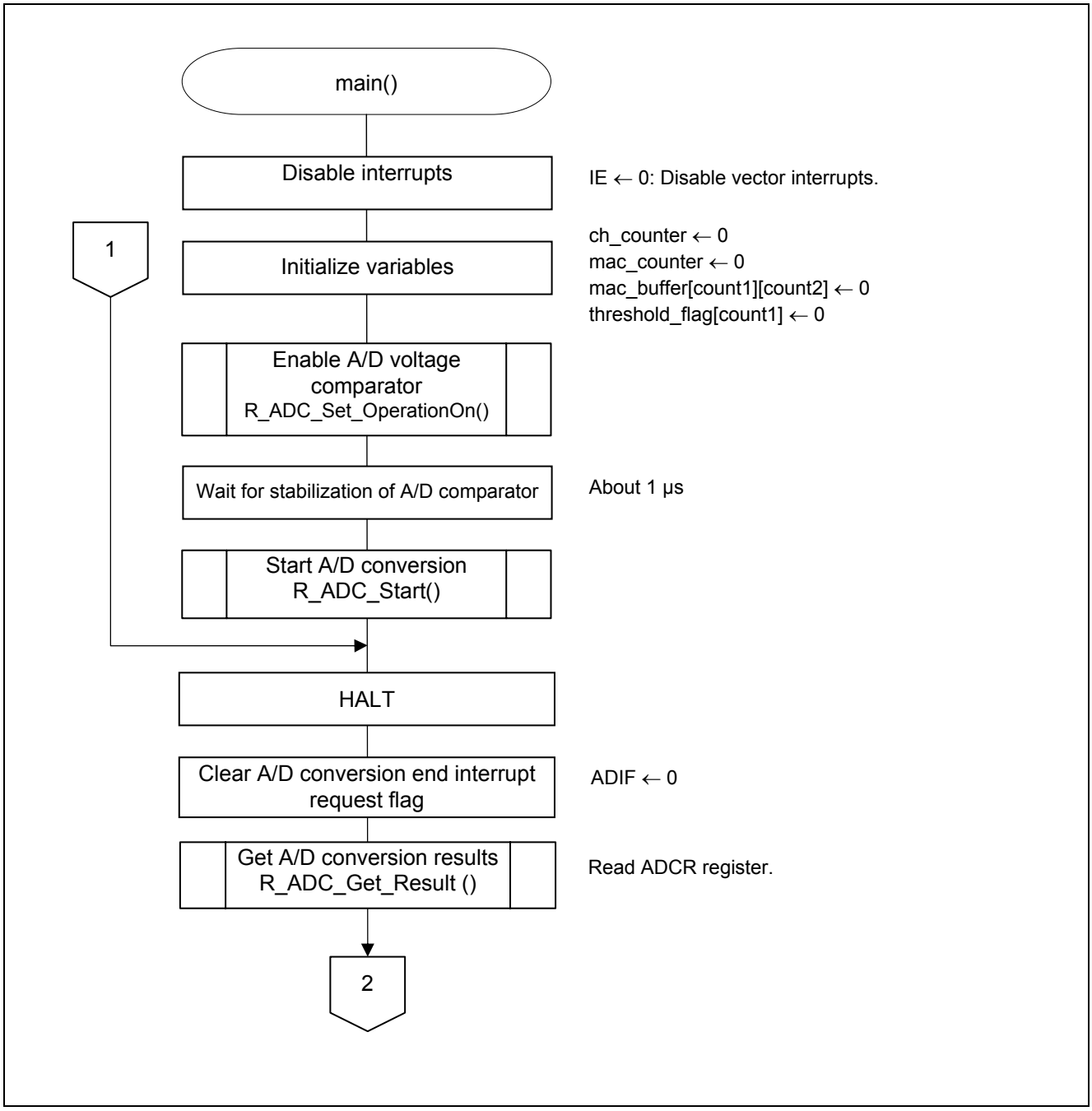

Figure 5.7 Main Processing (1/2)

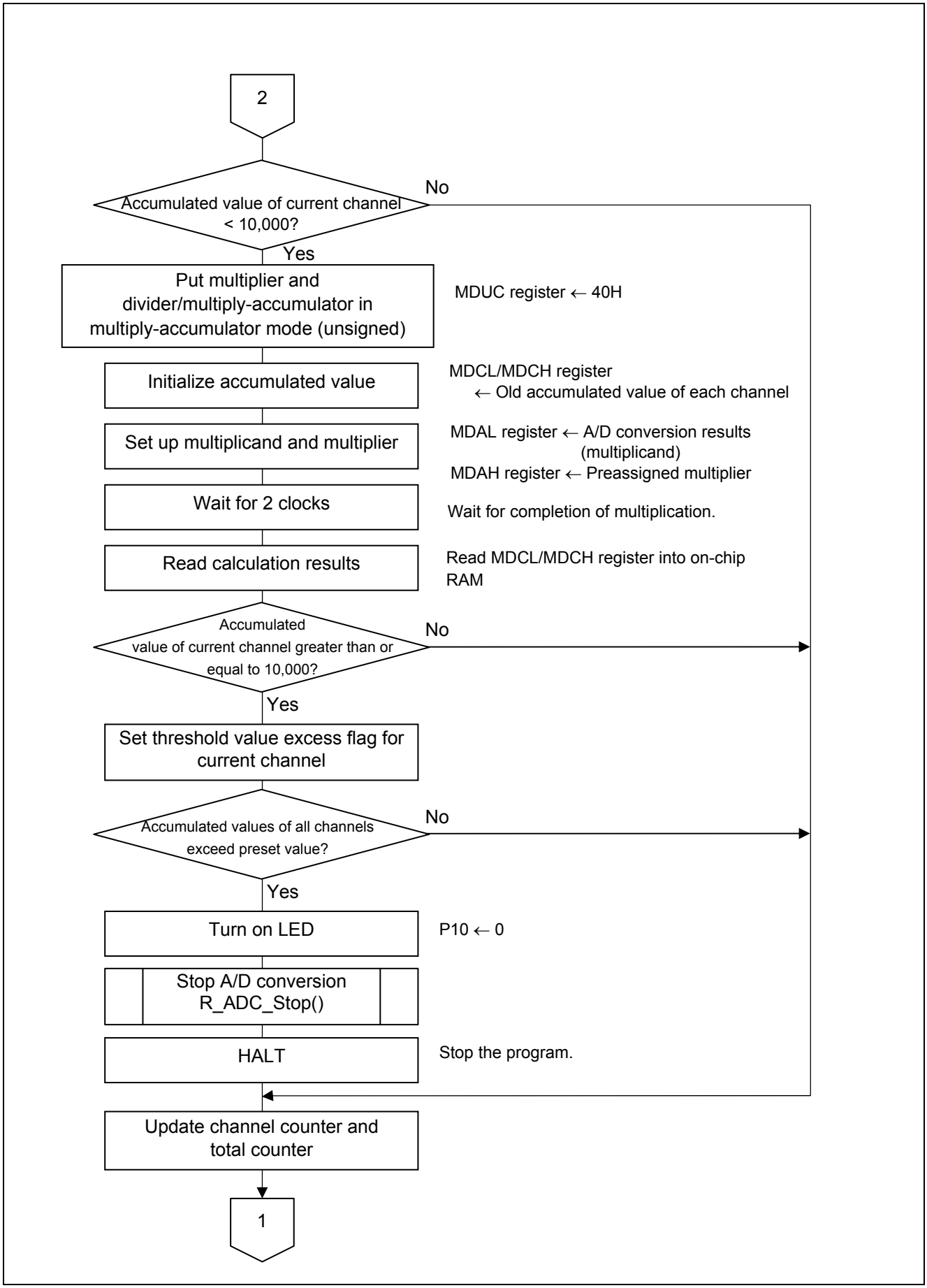

Figure 5.7 Main Processing (2/2)

Setting up multiply-accumulator mode

- Multiplication/division control register 0 (MDUC)
  Control the operation of the multiplier and divider/multiply-accumulator.

Symbol: MDUC

7	6	5	4	3	2	1	0
DIVMODE	MACMODE	0	0	MDSM	MDCOF	MACSF	DIVST
0	**1**	0	0	**0**	x	x	x

Bits 7, 6 and 3

DIVMODE	MACMODE	MDSM	Operation mode select
0	0	0	Multiplication mode (unsigned) (default)
0	0	1	Multiplication mode (signed)
0	**1**	**0**	**Multiply-accumulator mode (unsigned)**
0	1	1	Multiply-accumulator mode (signed)
1	0	0	Division mode (unsigned), division completion interrupt (INTMD generated)
1	1	0	Division mode (unsigned), division completion interrupt (no INTMD generated)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up values for multiplication-accumulation

- Multiplication/division data register A (MDAH, MDAL)
  Set up values to be used for multiplication/division.
- Multiplication/division data register C (H) (MDCH)
- Multiplication/division data register C (L) (MDCL)
  Set up initial accumulated value.

Symbol: MDAH

MDAH15	MDAH14	MDAH13	MDAH12	MDAH11	MDAH10	MDAH9	MDAH8	MDAH7	MDAH6	MDAH5	MDAH4	MDAH3	MDAH2	MDAH1	MDAH0

Symbol: MDAL

MDAL15	MDAL14	MDAL13	MDAL12	MDAL11	MDAL10	MDAL9	MDAL8	MDAL7	MDAL6	MDAL5	MDAL4	MDAL3	MDAL2	MDAL1	MDAL0

Remarks: For multiply-accumulator mode (unsigned) operation, load MDAL with the multiplicand (unsigned) and MDAH with the multiplier (unsigned).

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Symbol: MDCH

MDCH15	MDCH14	MDCH13	MDCH12	MDCH11	MDCH10	MDCH9	MDCH8	MDCH7	MDCH6	MDCH5	MDCH4	MDCH3	MDCH2	MDCH1	MDCH0

Symbol: MDCL

MDCL15	MDCL14	MDCL13	MDCL12	MDCL11	MDCL10	MDCL9	MDCL8	MDCL7	MDCL6	MDCL5	MDCL4	MDCL3	MDCL2	MDCL1	MDCL0

Remarks: In multiply-accumulator mode (unsigned), MDCH is loaded with the upper 16 bits of the accumulated value (unsigned) and MDCL with the lower 16 bits of the accumulated value (unsigned) after the operation is completed.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.7 Enabling A/D Voltage Comparator

Figure 5.8 shows the flowchart for enabling the A/D voltage comparator.

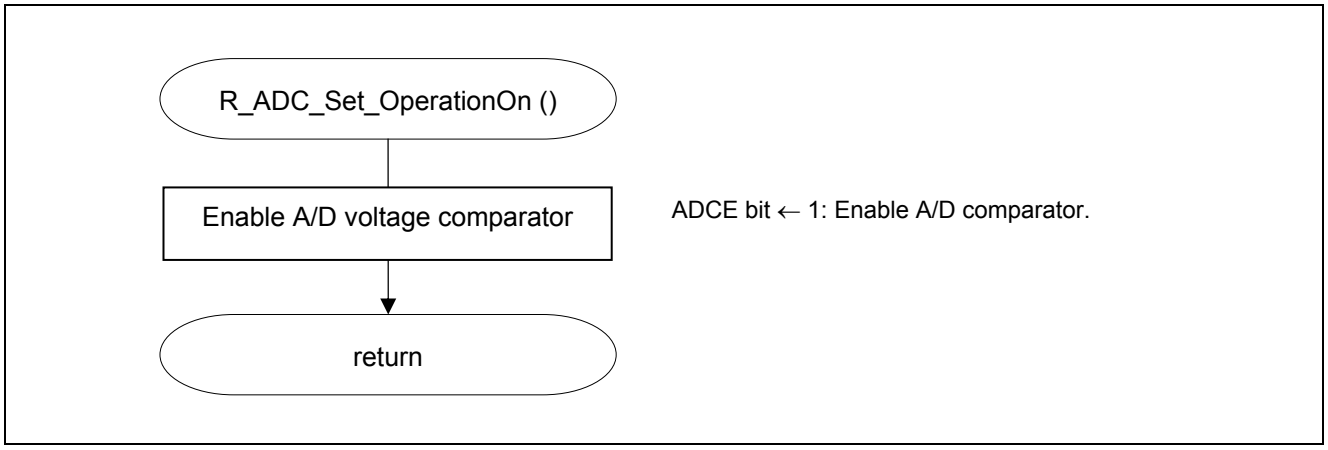

Figure 5.8 Enabling A/D Voltage Comparator

5.7.8 Starting A/D Conversion

Figure 5.9 shows the flowchart for starting A/D conversion.

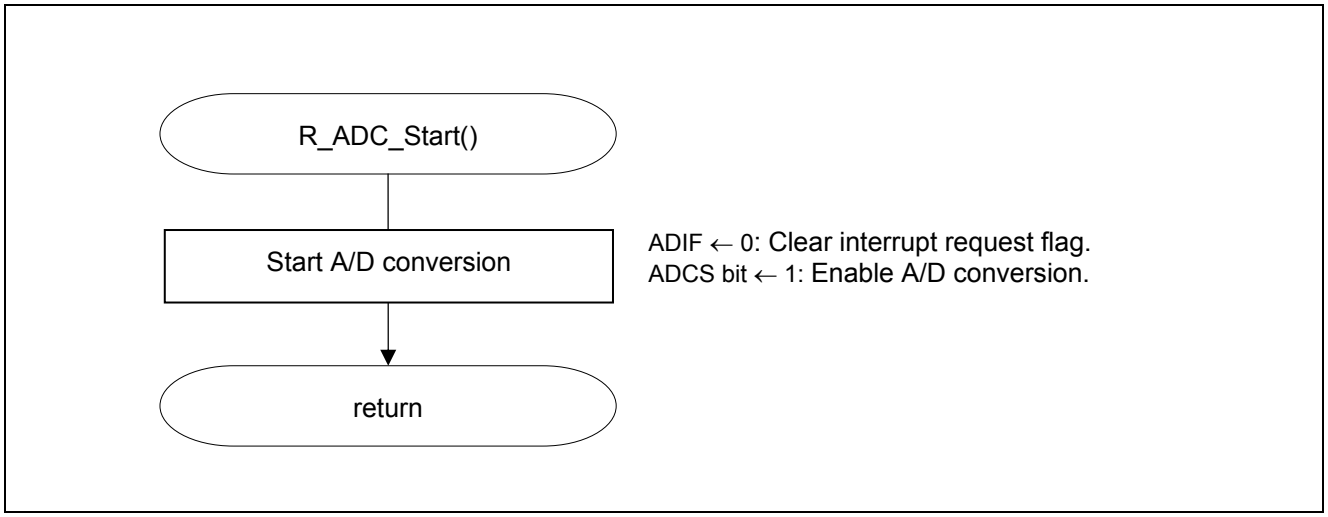

Figure 5.9 Starting A/D Conversion

5.7.9 Getting A/D Conversion Results

Figure 5.10 shows the flowchart for getting the A/D conversion results.

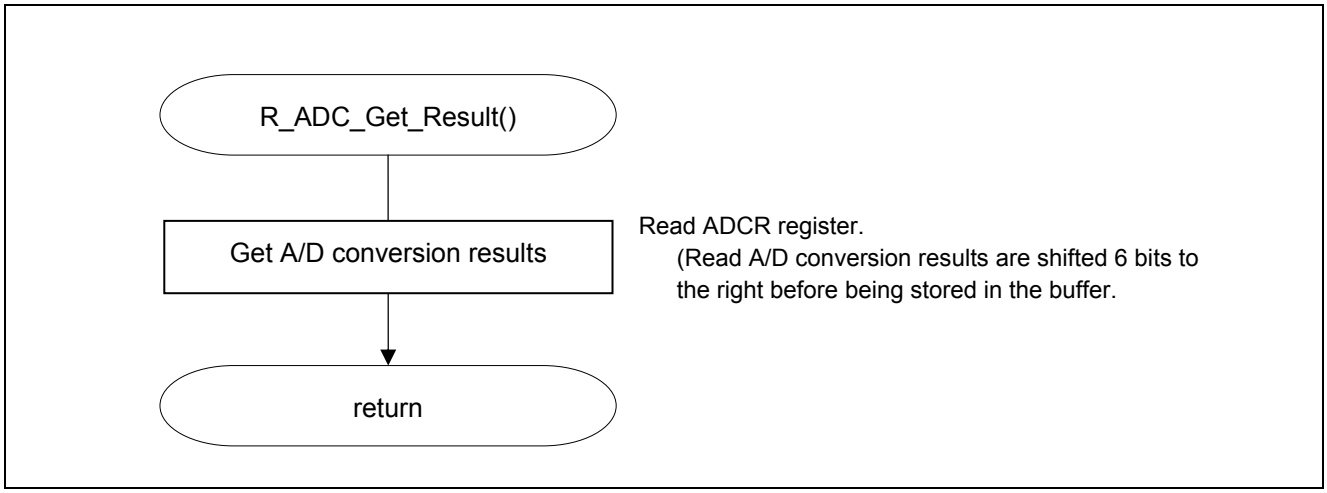

Figure 5.10 Getting A/D Conversion Results

5.7.10 Stopping A/D Conversion

Figure 5.11 shows the flowchart for stopping A/D conversion.

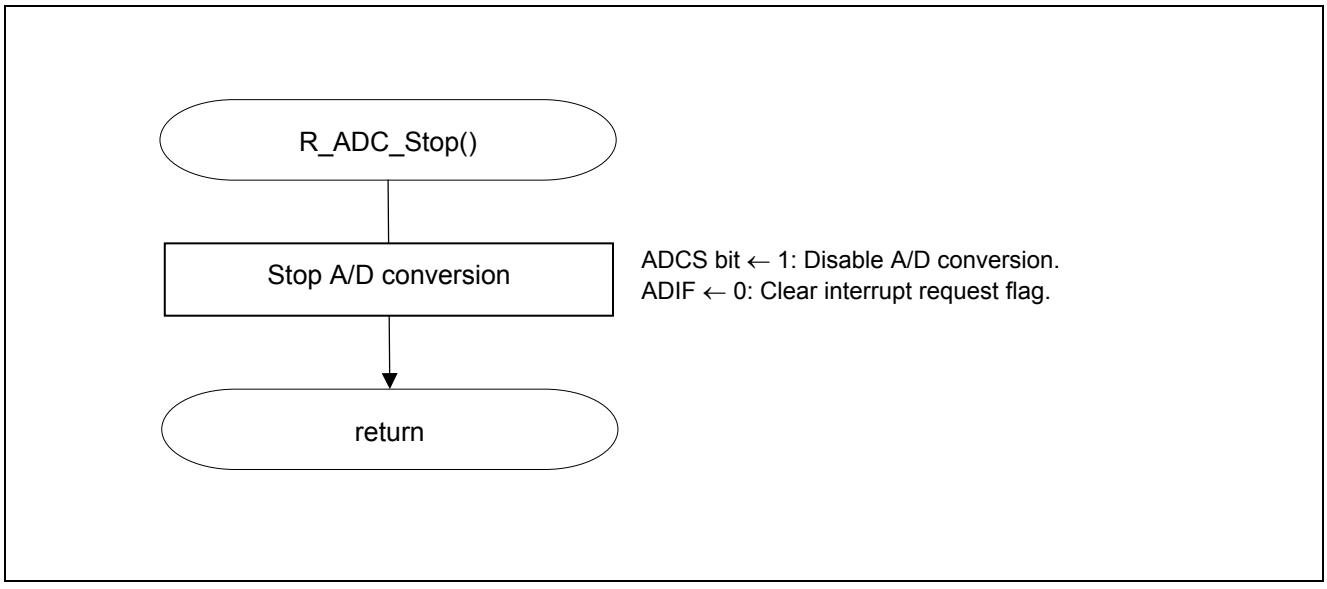

Figure 5.11 Stopping A/D Conversion

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Revision Record	RL78/G13 Multiplier and Divider/Multiply-Accumulator (A/D Converter in Sequential Conversion Mode)

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 16, 2015	—	First edition issued.

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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