RL78/G13

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DMA Controller (A/D Converter in Sequential Conversion Mode)

CC-RL

Introduction

This application note explains how to transfer data between the A/D converter and the on-chip RAM through the DMA controller. The A/D conversion results are transferred to the on-chip RAM through the DMA controller. The sample application covered in this application note performs A/D conversion on four channels of analog input voltages and stores the A/D conversion results in the on-chip RAM through the DMA controller. On the LED display, the sample application displays the number of the channel that has the largest total of the A/D conversion results.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note explains how to transfer data between the A/D converter and the on-chip RAM through the DMA controller. The A/D converter is used in scan mode. The sample application covered in this application note performs A/D conversion on four channels of analog input voltages and stores the A/D conversion results in the on-chip RAM through the DMA controller. The sample application performs A/D conversion on the four channels sequentially and repeats this cycle 10 times. The application totals 10 cycles of A/D conversion results for each channel. On the LED display, the application displays the number of the channel that has the largest total of the A/D conversion results.

Table 1.1 shows peripheral functions to be used and their uses. Table 1.2 lists an example of sampling results and LED indications. Figure 1.1 shows the outline of the A/D converter and DMA controller operations.

Table 1.1 Peripheral Functions to be Used and their Uses

Peripheral Function	Use
A/D converter	Converts the level of analog signal input.
DMA controller	Controls the transfer of A/D conversion results to RAM.
P10 and P11	Turns on and off LEDs (LED1 and LED2).

Table 1.2 Example of Sampling Results and LED Indications

Channel that has the Largest Total of A/D Conversion Results	LED Indication	
	LED1 (P10)	LED2 (P11)
Channel 0	Off	Off
Channel 1	On	Off
Channel 2	Off	On
Channel 3	On	On

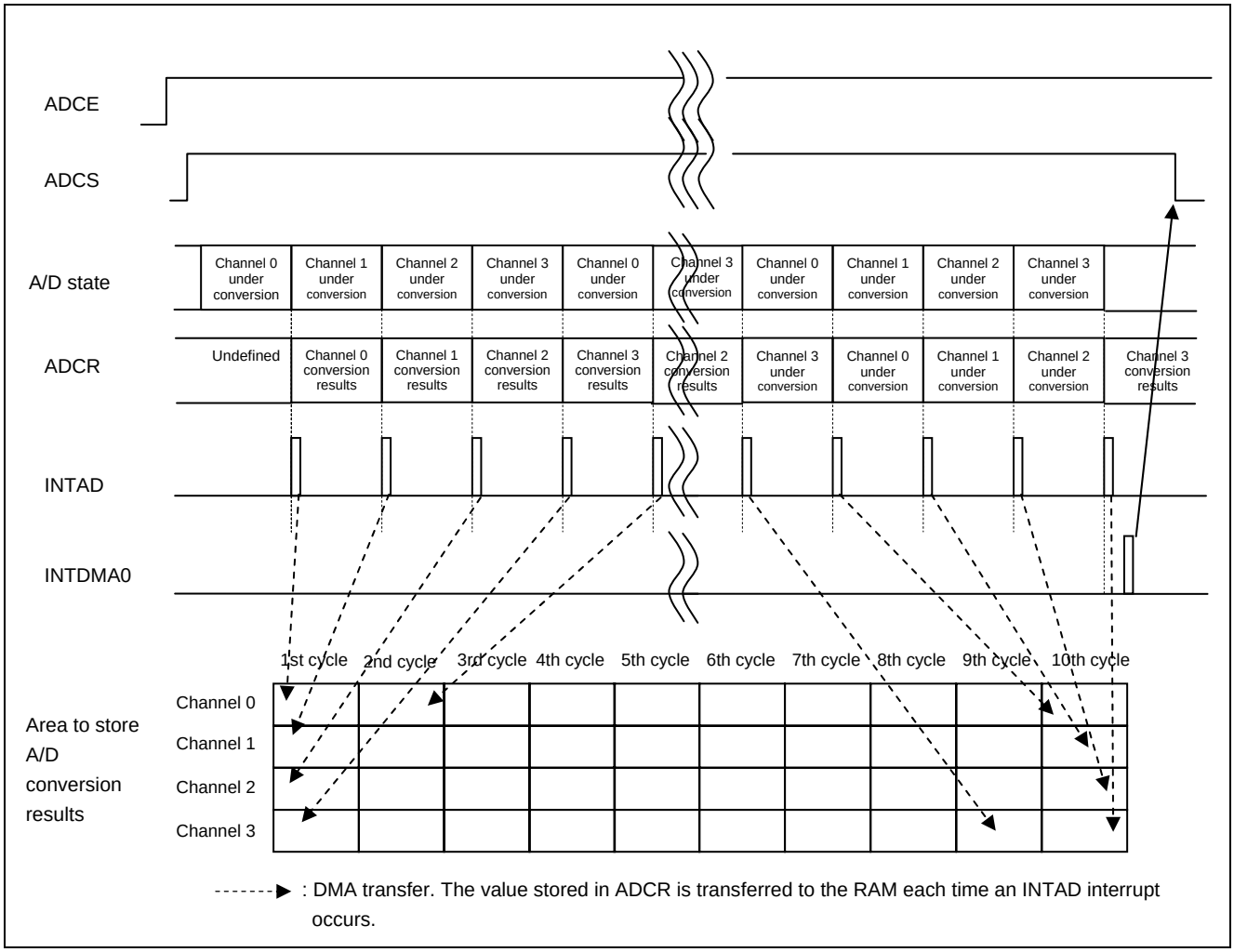

Figure 1.1 Outline of A/D Converter Conversion and DMA Controller Operations

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G13 (R5F100LEA)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 32 MHz • CPU/peripheral hardware clock: 32 MHz
Operating voltage	5.0 V (can run on a voltage range of 3.8 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode 3.75 V (3.68 V to 3.82 V)
Integrated development environment (CS+)	CS + V3.01.00 from Renesas Electronics Corp.
C compiler (CS+)	CC-RL V1.01.00 from Renesas Electronics Corp.
Integrated development environment (e^2 studio)	e^2 studio V4.0.0.26 from Renesas Electronics Corp.
C compiler (e^2 studio)	CC-RL V1.01.00 from Renesas Electronics Corp.

3. Related Application Notes

The application notes that are related to this application note are listed below for reference.

RL78/G13 Initialization (R01AN2575E) Application Note
RL78/G13 A/D Converter (Software Trigger and Sequential Conversion Modes) (R01AN2581E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.

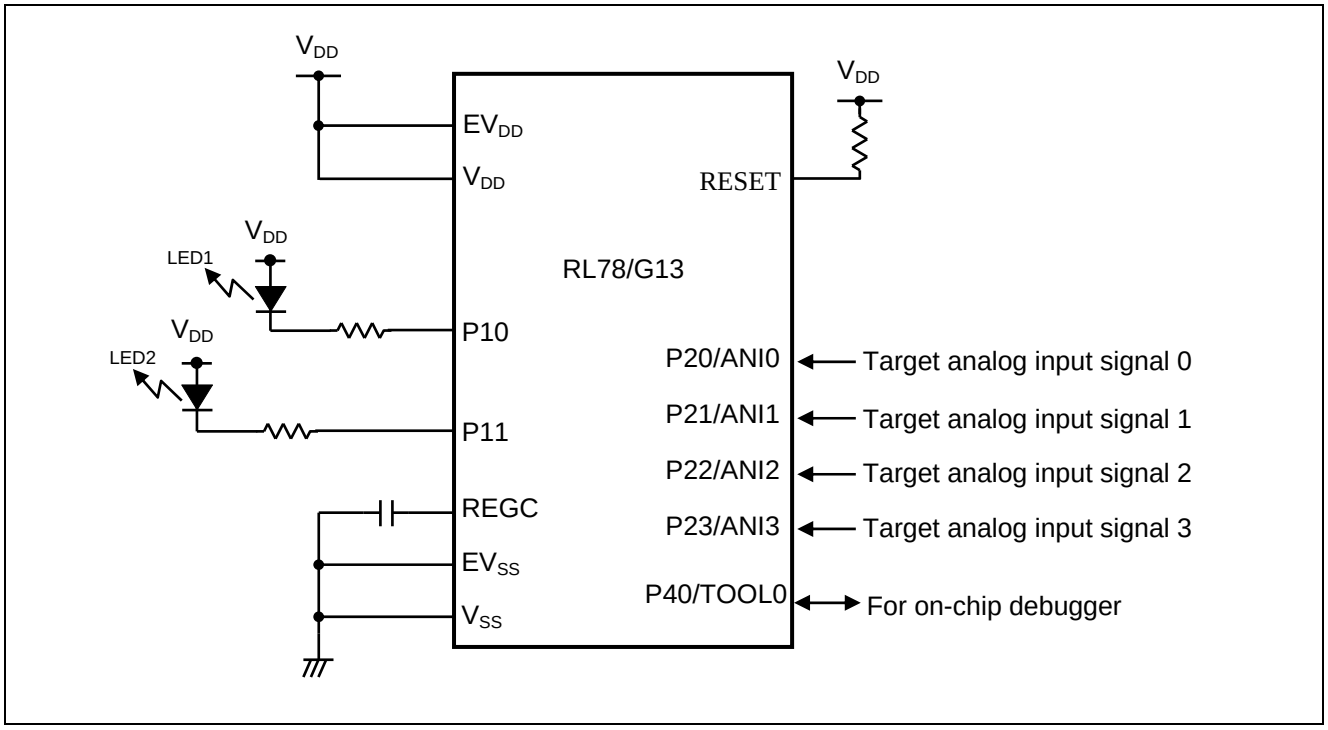

Figure 4.1 Hardware Configuration

Cautions:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).
2. Connect any pins whose name begins with EV_{SS} to V_{SS} and any pins whose name begins with EV_{DD} to V_{DD}, respectively.
3. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists the pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P20/ANI0	Input	A/D converter analog input port 0
P21/ANI1	Input	A/D converter analog input port 1
P22/ANI2	Input	A/D converter analog input port 2
P23/ANI3	Input	A/D converter analog input port 3
P10	Output	LED lighting (LED1) control port
P11	Output	LED lighting (LED2) control port

5. Description of the Software

5.1 Operation Outline

The sample application covered in this application note uses the DMA controller to transfer the A/D conversion results to the on-chip RAM.

The application converts the analog voltage input to ANI0 to ANI3 into digital data using the software trigger, scan mode, and sequential conversion mode of the A/D converter. An A/D conversion end interrupt request is generated upon completion of an A/D conversion. This interrupt request is used as a DMA start source and starts the transfer of the A/D conversion results to the on-chip RAM.

The application performs A/D conversion on the channels sequentially and repeats this cycle 10 times. It totals 10 cycles of A/D conversion results for each channel. On the LED display, it displays the number of the channel that has the largest total of the A/D conversion results.

(1) Initialize the peripheral functions.
<A/D converter>

- Pins P20/ANI0 to P23/ANI3 are used for the analog inputs.
- Set A/D conversion channel selection mode to scan mode.
- Set A/D conversion operation mode to sequential conversion mode.
- Start A/D conversion by using the software trigger.

<DMA controller>

- Set the DMA transfer direction to "SFR to on-chip RAM."
- Use the A/D conversion end interrupt as a DMA start source.
- Set the ADCR register in which the A/D conversion results are stored to a DMA transfer source.
- Keep an area for storing 40 cycles (4 channels × 10 cycles) of A/D conversion results.
- Set the start address of the above area for storing A/D conversion results to a DMA transfer destination.

(2) Start the A/D conversion. When the A/D conversion ends, the A/D conversion results are transferred to the ADCR register and an A/D conversion end interrupt (INTAD) is generated. The A/D conversion is performed on each of ANI0 to ANI3.
(3) DMA operation is triggered by the occurrence of the INTAD. The A/D conversion results are read from the ADCR register and stored in the designated locations in the area for storing the A/D conversion results sequentially.
(4) A DMA end interrupt is generated when 40 cycles of DMA transfer end. The DMA end interrupt stops the A/D conversion.
(5) The application totals 10 cycles of A/D conversion results for each channel. On the LED display, it displays the number of the channel that has the largest total of the A/D conversion results. If there are two or more channels that have the largest total of the A/D conversion results, the smallest channel number is displayed.
(6) The application resets the DMA transfer source to the start address of the area for storing A/D conversion results. It also resets the number of DMA transfers to 40. Subsequently, the application repeats steps from step (2).

5.2 List of Option Byte Settings

Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

Address	Value	Description
000C0H/010C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset status.)
000C1H/010C1H	01010011B	LVD reset mode which uses 3.75 V (3.68 V to 3.82 V)
000C2H/010C2H	11101000B	HS mode, HOCO: 32 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger.

5.3 List of Constants

Table Table 5.2 lists the constants that are used in this sample program.

Table 5.2 Constants for the Sample Program

Constant	Setting	Description
ADC_USED_CH_NUM	4U	Number of channels targeted for A/D conversion
ADC_EXEC_TIMES	10U	Number of A/D conversion cycles
REQ_DISP_RESULT_EXIST	1U	A/D conversion result display request present. (Specified number of A/D conversions completed.)
REQ_DISP_RESULT_NOT_EXIST	0U	A/D conversion result display request not present. (Specified number of A/D conversions not completed)

5.4 List of Variables

Table Table 5.3 lists the global variables that are used by this sample program.

Table 5.3 Global Variables

Type	Variable Name	Contents	Function Used
uint16_t	g_AdResult[ADC_EXEC_TIMES][ADC_USED_CH_NUM]	Area for storing the 10-bit A/D conversion results	main() GetTotalAdcResult()
uint8_t	g_ReqDispResult	A/D conversion result display request	main() R_DMAC0_Interrupt()

5.5 List of Functions

Table 5.4 lists the functions that are used in this sample program.

Table 5.4 Functions

Function Name	Outline
R_DMAC0_Create_UserInit	Makes initial settings for DMA transfer.
R_ADC_Set_OperationOn	Enables the operation of the A/D voltage comparator.
R_DMAC0_Start	Starts the DMA controller.
R_ADC_StartConv	Starts A/D conversion.
R_DMAC0_Stop	Stops the DMA controller.
GetMaxAdChNum	Gets the number of the channel that has the largest total of the A/D conversion results.
GetTotalAdcResult	Gets the total of the A/D conversion results.
r_dmac0_interrupt	Performs DMA transfer end interrupt processing.
R_ADC_Stop	Stops A/D conversion.

5.6 Function Specifications

This section describes the specifications for the functions that are used in the sample code.

[Function Name] R_DMAC0_Create_UserInit

Synopsis	Makes initial settings for DMA transfer.
Header	r_cg_dmac.h
Declaration	void R_DMAC0_Create_UserInit(void)
Explanation	This function sets a DMA destination address in the on-chip RAM and the number of transfer cycles.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Set_OperationOn

Synopsis	Enables the operation of the A/D voltage comparator.
Header	r_cg_adc.h
Declaration	void R_ADC_Set_OperationOn(void)
Explanation	This function enables the operation of the A/D voltage comparator.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_DMAC0_Start

Synopsis	Starts the DMA controller.
Header	r_cg_dmac.h
Declaration	void R_DMAC0_Start(void)
Explanation	This function starts the control of DMA transfer. It performs the following processing: • Clears the DMA transfer end interrupt request. • Enables DMA transfer end interrupts. • Enables DMA transfer and transitions to the DMA transfer trigger wait mode.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_StartConv

Synopsis	Starts A/D conversion.
Header	r_cg_adc.h
Declaration	void R_ADC_StartConv(void)
Explanation	This function starts A/D conversion. It performs the following processing: • Clears the A/D conversion end interrupt request. • Disables A/D conversion end interrupts. • Starts A/D conversion.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_DMAC0_Stop

Synopsis	Stops the DMA controller.
Header	r_cg_dmac.h
Declaration	void R_DMAC0_Stop(void)
Explanation	This function stops the control of DMA transfer. It performs the following processing: • Disables DMA transfer. • Disables DMA transfer end interrupts.
Arguments	None
Return value	None
Remarks	None

[Function Name] GetMaxAdChNum

Synopsis	Gets the number of the channel that has the largest total of the A/D conversion results.
Header	—
Declaration	static uint8_t GetMaxAdChNum(void)
Explanation	This function returns the number of the channel that has the largest total of 10 cycles of A/D conversion results. If there are two or more channels that has the largest total of the A/D conversion results, the smallest channel number is returned.
Arguments	None
Return value	Number of the channel that has the largest total of the A/D conversion results (0 to 3).
Remarks	This function may be executed before the A/D conversion is completed. In that case, no correct result can be obtained. This function should be executed after a specified number of A/D conversion cycles is executed.

[Function Name] GetTotalAdcResult

Synopsis	Gets the total of the A/D conversion results.
Header	—
Declaration	static uint16_t GetTotalAdcResult(uint8_t adc_ch)
Explanation	This function returns the total of 10 cycles of A/D conversion results performed on the channel with the channel number specified by the arguments. The value of ADCR is stored in the on-chip RAM without modification as the A/D conversion results. The value stored in the on-chip RAM is shifted by 6 bits to the right before being subjected to arithmetic operation (addition).
Arguments	Number of the channel on which the A/D conversions were performed (0 to 3)
Return value	Total of 10 cycles of A/D conversion results
Remarks	If an invalid argument is given, 0 is returned.

[Function Name] r_dmac0_interrupt

Synopsis	Performs DMA transfer end interrupt processing.
Header	r_cg_dmac.h
Declaration	static void __near r_dmac0_interrupt(void)
Explanation	This interrupt processing is executed when a specified number of DMA transfer cycles is executed. The function stops the A/D converter and issues a request to display the A/D conversion results.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_ADC_Stop

Synopsis	Stops A/D conversion.
Header	r_cg_adc.h
Declaration	void R_ADC_Stop(void)
Explanation	This function stops A/D conversion. It performs the following processing: • Stops A/D conversion. • Disables A/D conversion end interrupts. • Clears the A/D conversion end interrupt request.
Arguments	None
Return value	None
Remarks	None

5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

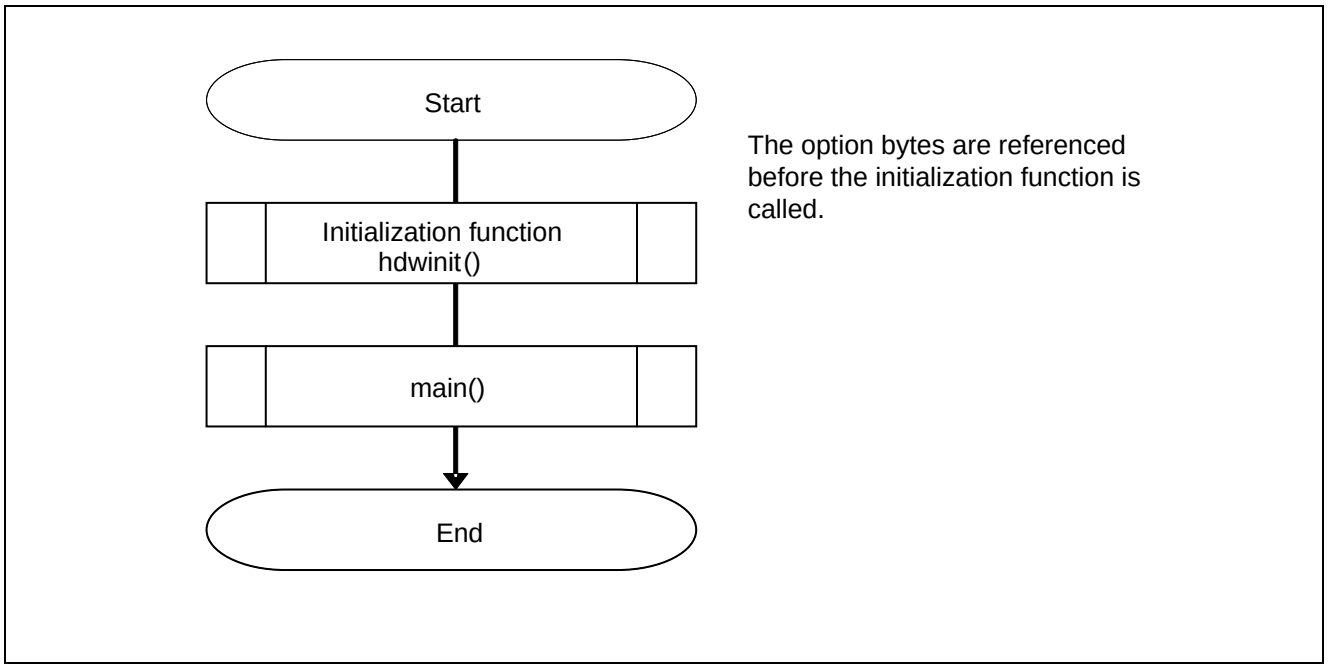

Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

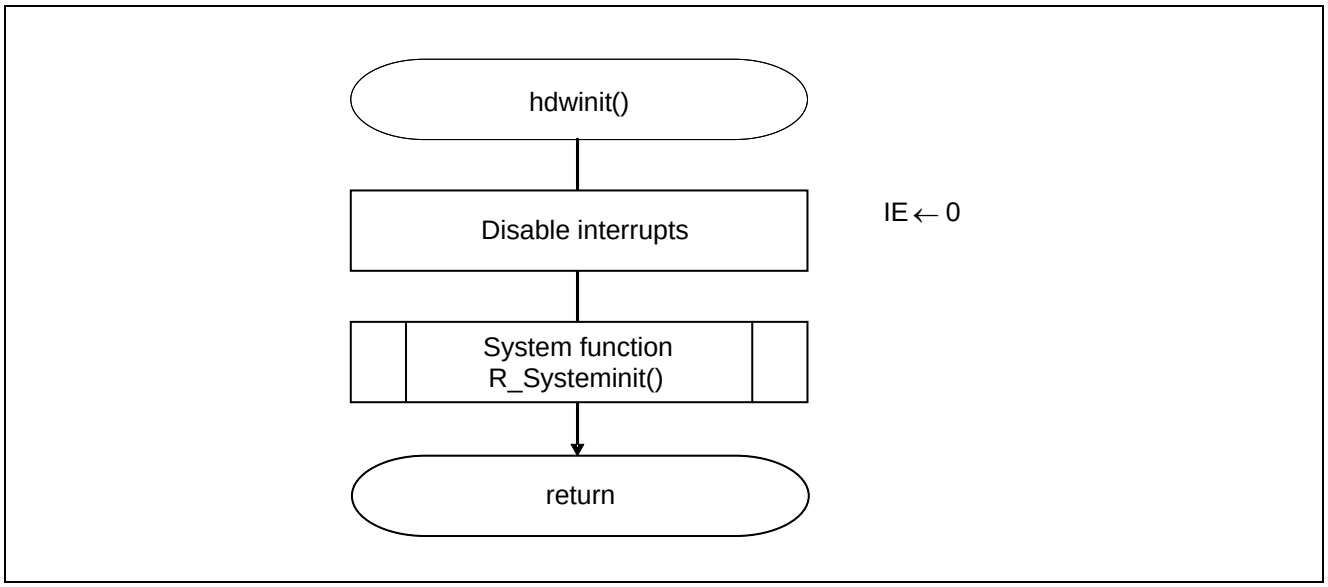

Figure 5.2 Initialization Function

5.7.2 System Initialization Function

Figure 5.2 shows the flowchart for the system initialization function.

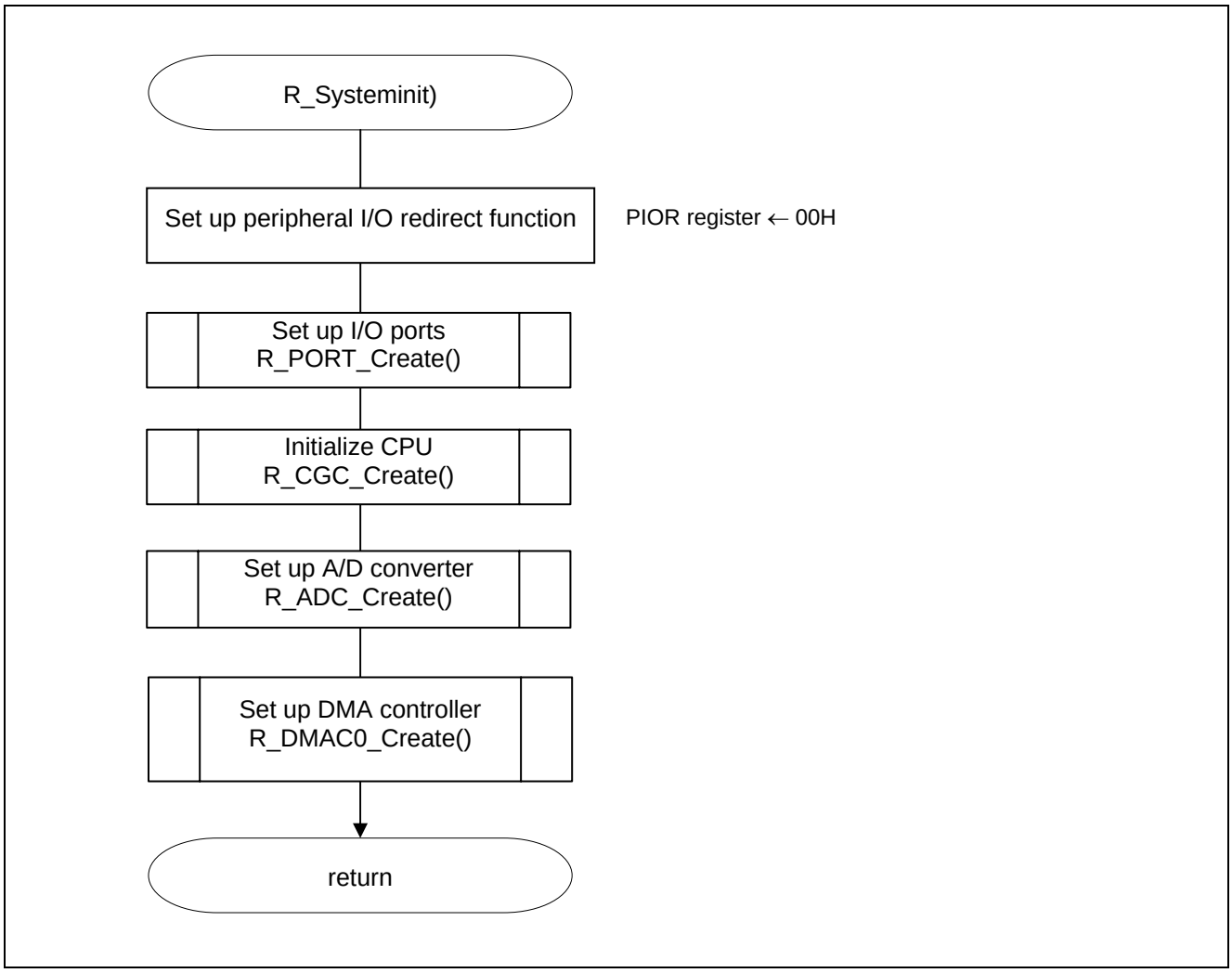

Figure 5.3 System Initialization Function

5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for I/O port setup.

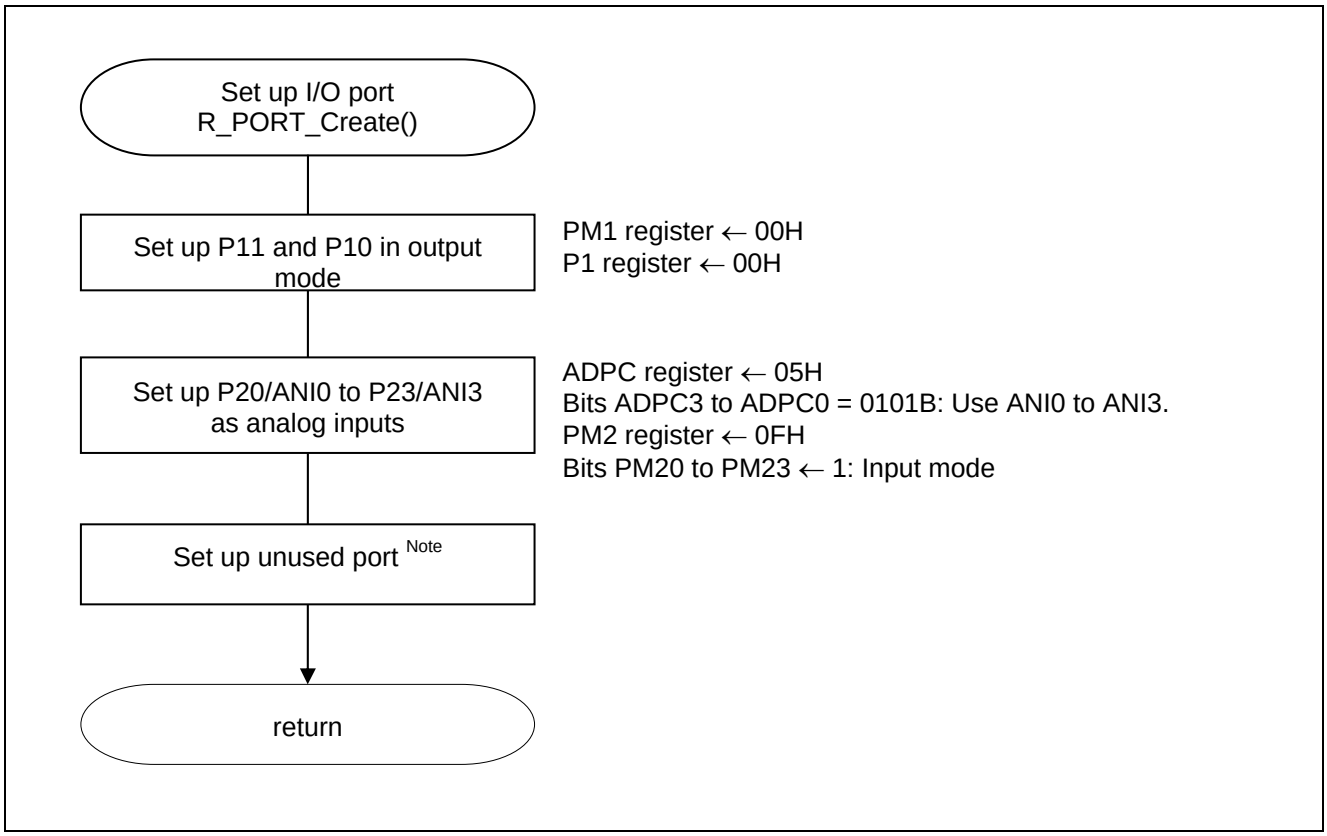

Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E) for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are met. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

Setting up LED ports

- Port mode register 1 (PM1)

Symbol: PM1

7	6	5	4	3	2	1	0
PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10
0	0	0	0	0	0	**0**	**0**

Bit 1

PM11	P11 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Bit 0

PM10	P10 pin I/O mode selection
0	**Output mode (output buffer on)**
1	Input mode (output buffer off)

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the channel to be used for A/D conversion

- A/D port configuration register (ADPC)
  Switches between A/D converter analog input and port digital I/O.
- Port mode register 2 (PM2)
  Selects the I/O mode of each port.

Symbol: ADPC

7	6	5	4	3	2	1	0
0	0	0	0	ADPC3	ADPC2	ADPC1	ADPC0
0	0	0	0	**0**	**1**	**0**	**1**

Bits 3 to 0

ADPC3	ADPC2	ADPC1	ADPC0	Available analog input
0	0	0	0	ANI0 to ANI14
0	0	0	1	None
0	0	1	0	ANI0
0	0	1	1	ANI0 and ANI1
0	1	0	0	ANI0 to ANI2
0	**1**	**0**	**1**	**ANI0 to ANI3**
0	1	1	0	ANI0 to ANI4
0	1	1	1	ANI0 to ANI5
1	0	0	0	ANI0 to ANI6
1	0	0	1	ANI0 to ANI7
1	0	1	0	ANI0 to ANI8
1	0	1	1	ANI0 to ANI9
1	1	0	0	ANI0 to ANI10
1	1	0	1	ANI0 to ANI11
1	1	1	0	ANI0 to ANI12
1	1	1	1	ANI0 to ANI13
Other than above				Setting prohibited

Symbol: PM2

7	6	5	4	3	2	1	0
PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20
x	x	x	x	**1**	**1**	**1**	**1**

Bits 3 to 0

PM23 to PM20	P23 to P20 I/O mode selection
0	Output mode (output buffer on)
1	**Input mode (output buffer off)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

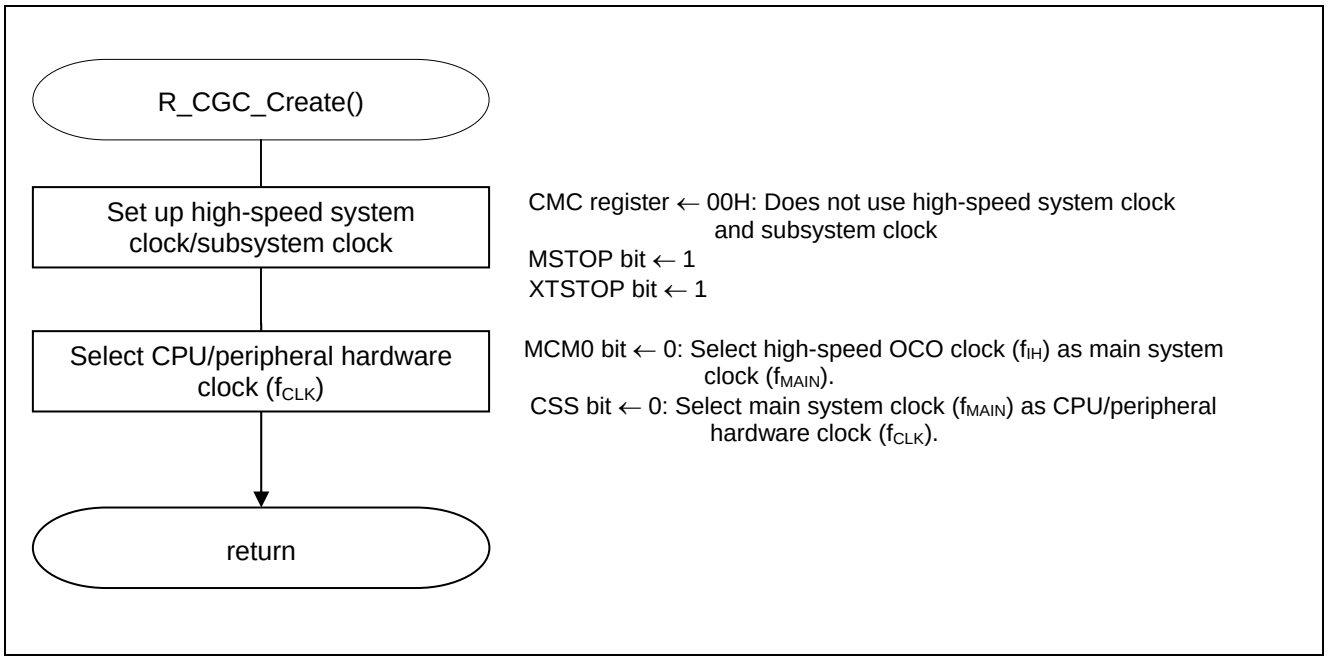

Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN2575E).

5.7.5 A/D Converter Setup

Figure 5.6 shows the flowchart for setting up the A/D converter.

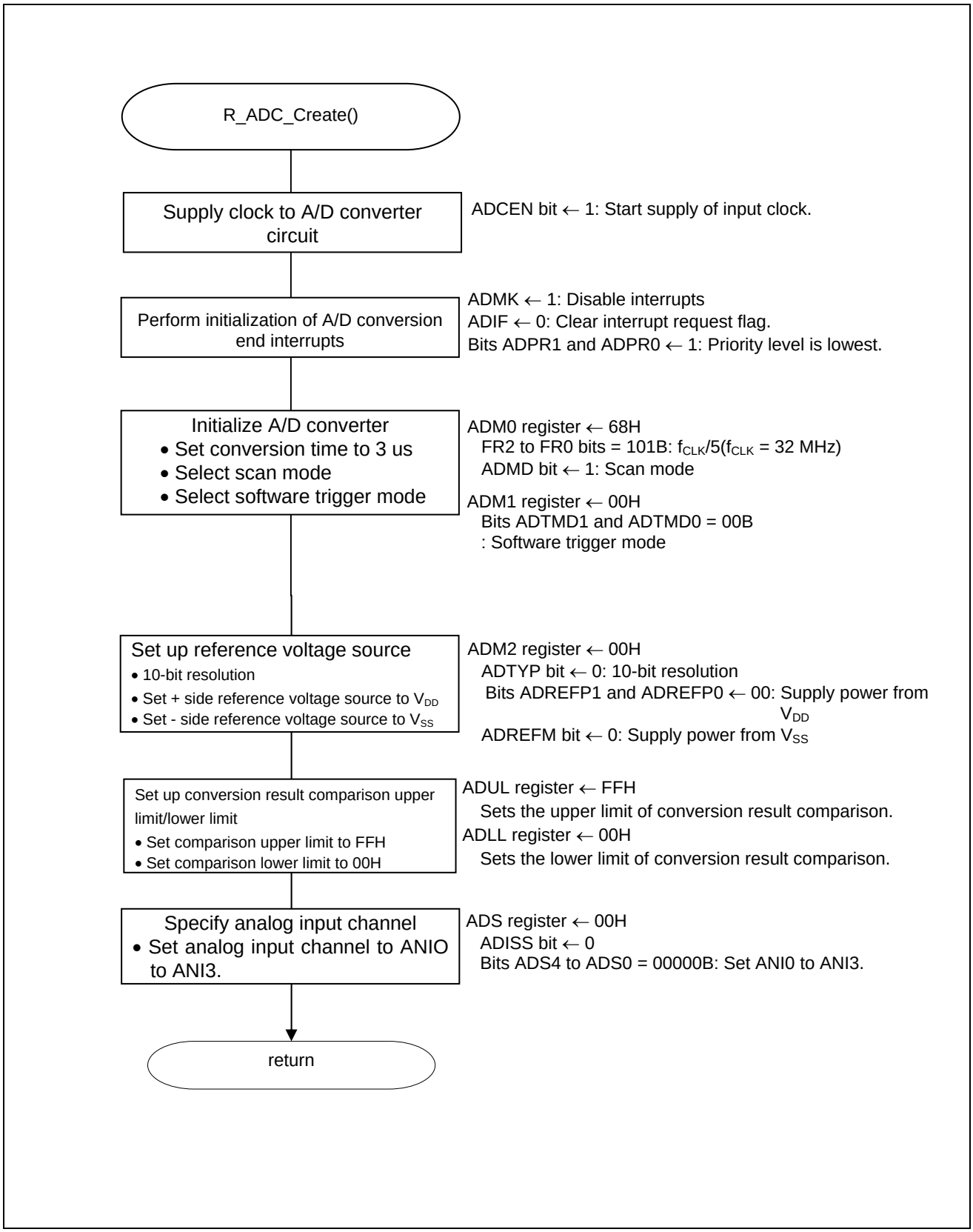

Figure 5.6 A/D Converter Setup

Starting the supply of clock to the A/D converter

- Peripheral enable register 0 (PER0)
  Starts the supply of the clock to the A/D converter.

Symbol: PER0

7	6	5	4	3	2	1	0
RTCEN	IICA1EN	ADCEN	IICA0EN	SAU1EN	SAU0EN	TAU1EN	TAU0EN
x	x	**1**	x	x	x	x	x

Bit 5

ADCEN	A/D converter input clock control
0	Stops supply of input clock.
1	**Starts supply of input clock.**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Controlling A/D conversion interrupt

- Interrupt mask flag register (MK1H)
- Interrupt request flag register (IF1H)
- Priority specification flag register (PR01H, PR11H)
  Make settings for A/D conversion interrupts.

Symbol: MK1H

7	6	5	4	3	2	1	0
TMMK04	TMMK13	SRMK3 CSIMK31 IICMK31	STMK3 CSIMK30 IICMK30	KRMK	ITMK	RTCMK	ADMK
x	x	x	x	x	x	x	**1**

Bit 0

ADMK	Interrupt processing control
0	Enables interrupts.
1	**Disables interrupts.**

Symbol: IF1H

7	6	5	4	3	2	1	0
TMIF04	TMIF13	SRIF3 CSIIF31 IICIF31	STIF3 CSIIF30 IICIF30	KRIF	ITIF	RTCIF	ADIF
x	x	x	x	x	x	x	**0**

Bit 0

ADIF	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request signal is generated, interrupt request status

Symbol: PR01H

7	6	5	4	3	2	1	0
TMPR004	TMPR013	SRPR03 CSIPR031 IICPR031	STPR03 CSIPR030 IICPR030	KRPR0	ITPR0	RTCPR0	ADPR0
x	x	x	x	x	x	x	**1**

Symbol: PR11H

7	6	5	4	3	2	1	0
TMPR104	TMPR113	SRPR13 CSIPR131 IICPR131	STPR13 CSIPR130 IICPR130	KRPR1	ITPR1	RTCPR1	ADPR1
x	x	x	x	x	x	x	**1**

Bit 0

ADPR0	ADPR1	Priority level selection
0	0	Specify level 0 (highest level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (lowest level)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the A/D conversion time and operating mode

- A/D converter mode register 0 (ADM0)
  Controls the A/D conversion.
  Specifies the A/D channel selection mode.

Symbol: ADM0

7	6	5	4	3	2	1	0
ADCS	ADMD	FR2	FR1	FR0	LV1	LV0	ADCE
x	**1**	**1**	**0**	**1**	**0**	**0**	x

Bit 6

ADMD	A/D channel selection mode select
0	Select mode
1	**Scan mode**

Bits 5 to 1

ADM0					Mode	Conversion Time Selection						Conversion Clock (f_{AD})
FR2	FR1	FR0	LV1	LV0		f_{CLK} = 1 MHz	f_{CLK} = 2 MHz	f_{CLK} = 4 MHz	f_{CLK} = 8 MHz	f_{CLK} = 16 MHz	**f_{CLK} = 32 MHz**	
0	0	0	**0**	**0**	**Standard 1**	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	38 µs	f_{CLK}/64
0	0	1								38 µs	19 µs	f_{CLK}/32
0	1	0							38 µs	19 µs	9.5 µs	f_{CLK}/16
0	1	1						38 µs	19 µs	9.5 µs	4.75 µs	f_{CLK}/8
1	0	0						28.5 µs	14.25 µs	7.125 µs	3.5625 µs	f_{CLK}/6
1	**0**	**1**						23.75 µs	11.875 µs	5.938 µs	**2.9688 µs**	**f_{CLK}/5**
1	1	0					38 µs	19 µs	9.5 µs	4.75 µs	2.375 µs	f_{CLK}/4
1	1	1				38 µs	19 µs	9.5 µs	4.75 µs	2.375 µs	Setting prohibited	f_{CLK}/2
0	0	0	0	1	Standard 2	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited	34 µs	f_{CLK}/64
0	0	1								34 µs	17 µs	f_{CLK}/32
0	1	0							34 µs	17 µs	8.5 µs	f_{CLK}/16
0	1	1						34 µs	17 µs	8.5 µs	4.25 µs	f_{CLK}/8
1	0	0						25.5 µs	12.75 µs	6.375 µs	3.1875 µs	f_{CLK}/6
1	0	1						21.25 µs	10.625 µs	5.3125 µs	2.6536 µs	f_{CLK}/5
1	1	0					34 µs	17 µs	8.5 µs	4.25 µs	2.125 µs	f_{CLK}/4
1	1	1				34 µs	17 µs	8.5 µs	4.25 µs	2.125 µs	Setting prohibited	f_{CLK}/2
x	x	x	1	0	Low voltage 1		Setting prohibited					—
x	x	x	1	1	Low voltage 2		Setting prohibited					—

Note: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the A/D conversion trigger mode

- A/D converter mode register 1 (ADM1)
  Selects the A/D conversion trigger mode.
  Selects the A/D conversion operating mode.

Symbol: ADM1

7	6	5	4	3	2	1	0
ADTMD1	ADTMD0	ADSCM	0	0	0	ADTRS1	ADTRS0
0	**0**	**0**	0	0	0	**0**	**0**

Bits 1 and 0

ADTRS1	ADTRS0	Selection of the hardware trigger signal
0	**0**	**Do not use the hardware trigger.**
0	1	End of timer channel 1 count or capture end interrupt signal (INTTM01)
1	0	Real-time clock interrupt signal (INTRTC)
1	1	Interval timer interrupt signal (INTIT)

Bit 5

ADSCM	Specification of the A/D conversion mode
0	**Sequential conversion mode**
1	One-shot conversion mode

Bits 7 and 6

ADTMD1	ADTMD0	Selection of the A/D conversion trigger mode
0	**—**	**Software trigger mode**
1	0	Hardware trigger no-wait mode
1	1	Hardware trigger wait mode

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the reference voltage

- A/D converter mode register 2 (ADM2)
  Sets up the reference voltage source.

Symbol: ADM2

7	6	5	4	3	2	1	0
ADREFP1	ADREFP0	ADREFM	0	ADRCK	AWC	0	ADTYP
0	**0**	**0**	0	**0**	**0**	0	**0**

Bit 0

ADTYP	Selection of the A/D conversion resolution
0	**10-bit resolution**
1	8-bit resolution

Bit 2

AWC	Specification of the wakeup function (SNOOZE mode)
0	**Do not use the SNOOZE mode function.**
1	Use the SNOOZE mode function.

Bit 3

ADCRK	Checking the upper limit and lower limit conversion results
0	**The interrupt signal (INTAD) is output when the ADLL register ≤ the ADCR register ≤ the ADUL register.**
1	Interrupt signal (INTAD) is output when ADCR register < ADLL register and ADUL register < ADCR register.

Bit 5

ADREFM	Selection of the – side reference voltage source of the A/D converter
0	**Supplied from V_{SS}.**
1	Supplied from P21/AV_{REFM}/ANI1.

Bits 7 and 6

ADREFP1	ADREFP0	Selection of the + side reference voltage source of the A/D converter
0	**0**	**Supplied from V_{DD}.**
0	1	Supplied from P20/AV_{REFP}/ANI0.
1	0	Supplied from internal reference voltage (1.44 V).
1	1	Setting prohibited

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up the conversion result comparison upper limit/lower limit

- Conversion result comparison upper limit setting register (ADUL)
- Conversion result comparison low limit setting register (ADLL)
  Sets up the conversion result comparison upper and lower limits.

Symbol: ADUL

7	6	5	4	3	2	1	0
ADUL7	ADUL6	ADUL5	ADUL4	ADUL3	ADUL2	ADUL1	ADUL0
1	**1**	**1**	**1**	**1**	**1**	**1**	**1**

Symbol: ADLL

7	6	5	4	3	2	1	0
ADLL7	ADLL6	ADLL5	ADLL4	ADLL3	ADLL2	ADLL1	ADLL0
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**

Specifying the input channel

- Analog input channel register (ADS)
  Specifies the input channel for the analog signal targeted for A/D conversion.

Symbol: ADS

7	6	5	4	3	2	1	0
ADISS	0	0	ADS4	ADS3	ADS2	ADS1	ADS0
0	0	0	**0**	**0**	**0**	**0**	**0**

Bit 7, 4 to 0

ADISS	ADS4	ADS3	ADS2	ADS1	ADS0	Analog Input Channel			
						Scan 0	Scan 1	Scan 2	Scan 3
0	**0**	**0**	**0**	**0**	**0**	**ANI0**	**ANI1**	**ANI2**	**ANI3**
0	0	0	0	0	1	ANI1	ANI2	ANI3	ANI4
0	0	0	0	1	0	ANI2	ANI3	ANI4	ANI5
0	0	0	0	1	1	ANI3	ANI4	ANI5	ANI6
0	0	0	1	0	0	ANI4	ANI5	ANI6	ANI7
Other than above						Setting prohibited			

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.6 Initializing the DMA Controller

Figure 5.7 shows the flowchart for initializing the DMA controller.

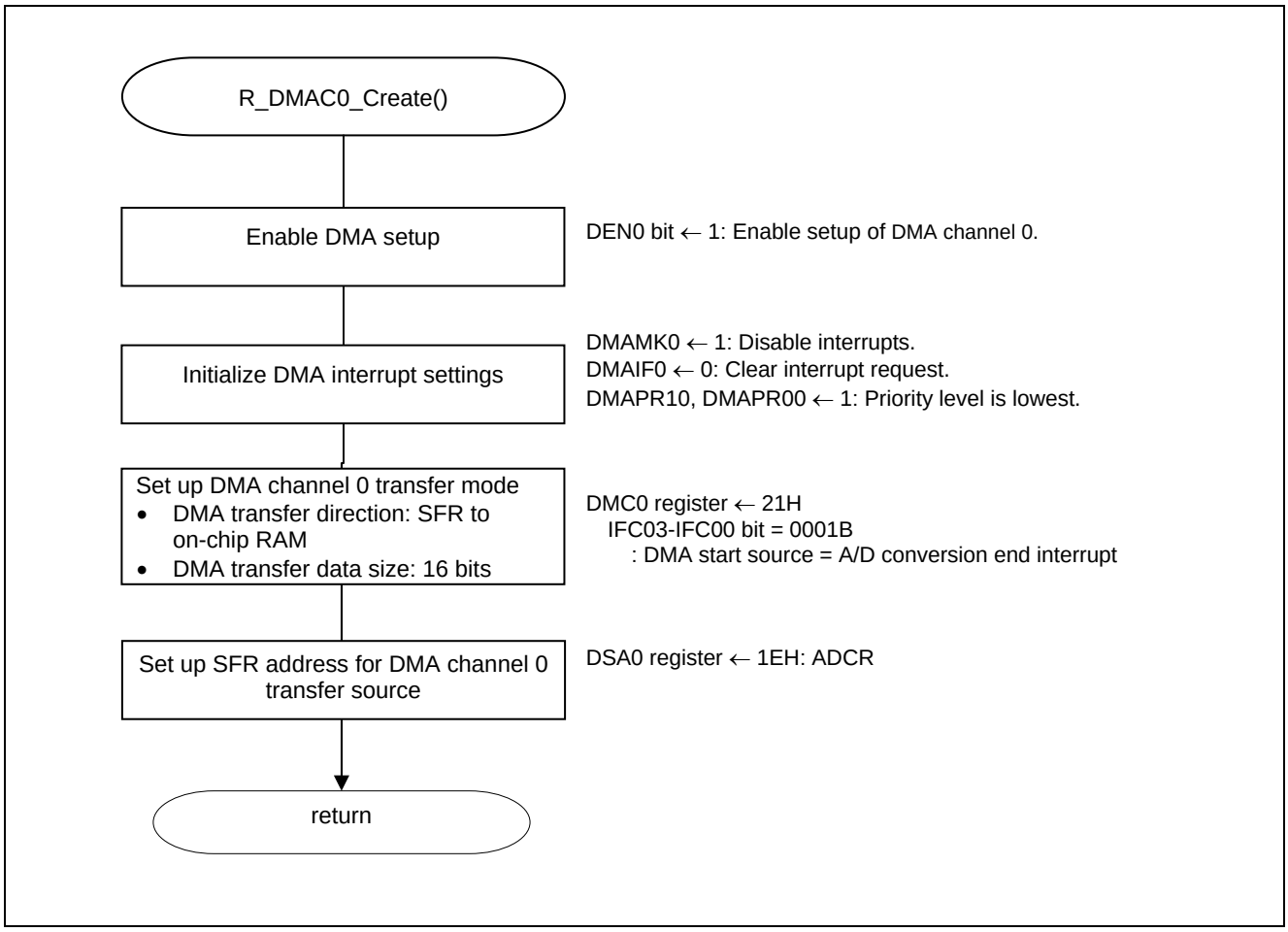

Figure 5.7 DMA Controller Initialization

Disabling DMA channel 0

- DMA operation control register (DRC0)

Symbol: DRC0

7	6	5	4	3	2	1	0
DEN0	0	0	0	0	0	0	DST0
1/0	0	0	0	0	0	0	**0**

Bit 7

DEN0	DMA operation enable flag
0	**Disables DMA channel 0 (stops operating clock of DMA).** Disables DMA setup processing.
1	Enables DMA channel 0. **Enables DMA setup processing.**

Bit 0

DST0	DMA transfer mode flag
0	**DMA transfer of DMA channel 0 is completed.**
1	DMA transfer of DMA channel 0 is not completed (still under execution).

Initialization for DMA transfer end interrupts

- Interrupt request flag register (IF0H)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0H)
  Clear interrupt mask.
- Priority specification flag register (PR00H, PR10H)
  Interrupt level: Level 3 (lowest level)

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2 TMIF11H	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
x	x	x	x	**0**	x	x	x

Bit 3

DMAIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MK0H

7	6	5	4	3	2	1	0
SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK1	DMAMK0	SREMK2 TMMK11H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
x	x	x	x	**1**	x	x	x

Bit 3

DMAMK0	Interrupt processing control
0	Enables interrupts.
1	**Disables interrupts.**

Symbol: PR00H

7	6	5	4	3	2	1	0
SREPR00 TMPR001H	SRPR00 CSIPR001 IICPR001	STPR00 CSIPR000 IICPR000	DMAPR01	DMAPR00	SREPR02 TMPR011H	SRPR02 CSIPR021 IICPR021	STPR02 CSIPR020 IICPR020
x	x	x	x	**1**	x	x	x

Symbol: PR10H

7	6	5	4	3	2	1	0
SREPR10 TMPR101H	SRPR10 CSIPR101 IICPR101	STPR10 CSIPR100 IICPR100	DMAPR11	DMAPR10	SREPR12 TMPR111H	SRPR12 CSIPR121 IICPR121	STPR12 CSIPR120 IICPR120
x	x	x	x	**1**	x	x	x

Bit 3

DMAPR10	DMAPR00	Priority level selection
0	0	Specify level 0 (highest level)
0	1	Specify level 1
1	0	Specify level 2
1	**1**	**Specify level 3 (lowest level)**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up DMA channel 0 transfer mode

- DMA mode control register (DMC0)
  Set DMA transfer direction to SFR to on-chip RAM.
  Set transfer data size to 16 bits.
  Specify DMA transfer on DMA startup request.
  Select UART0 transfer end interrupt as DMA startup source.

Symbol: DMC0

7	6	5	4	3	2	1	0
STG0	DRS0	DS0	DWAIT0	IFC03	IFC02	IFC01	IFC00
0	**0**	**0**	**0**	**0**	**1**	**1**	**1**

Bit 6

DRS0	Selection of DMA transfer direction
0	**SFR to on-chip RAM**
1	On-chip RAM to SFR

Bit 5

DS0	Specification of transfer data size for DMA transfer
0	8 bits
1	**16 bits**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Bit 4

DWAIT0	Pending of DMA transfer
0	**Executes DMA transfer upon DMA start request (not held pending).**
1	Holds DMA start request pending if any.

Bits 3 to 0

IFC03	IFC02	IFC01	IFC00	Selection of DMA start source	
				Trigger Signal	Trigger contents
0	0	0	0	—	Disable DMA transfer by interrupt. (Only software trigger is allowed.)
0	**0**	**0**	**1**	**INTAD**	**A/D conversion end interrupt**
0	0	1	0	INTTM00	End of timer channel 0 count end or capture interrupt
0	0	1	1	INTTM01	End of timer channel 1 count end or capture interrupt
0	1	0	0	INTTM02	End of timer channel 2 count end or capture interrupt
0	1	0	1	INTTM03	End of timer channel 3 count end or capture interrupt
0	1	1	0	INTST0/INTCSI00	UART0 transmission transfer end or buffer empty interrupt/CSI00 transfer end or buffer empty interrupt
0	1	1	1	INTSR0/INTCSI01	UART0 reception transfer end interrupt/CSI01 transfer end, or buffer empty interrupt
1	0	0	0	INTST1/INTCSI10	UART1 transmission transfer end, buffer empty interrupt/CSI10 transfer end, or buffer empty interrupt
1	0	0	1	INTSR1/INTCSI11	UART1 reception transfer end interrupt/CSI11 transfer end or buffer empty interrupt
1	0	1	0	INTST2/INTCSI20	UART2 transmission transfer end interrupt/CSI20 transfer end or buffer empty interrupt
1	0	1	1	INTSR2/INTCSI21	UART2 reception transfer end interrupt/CSI21 transfer end or buffer empty interrupt
Other than above				Setting prohibited	

Setting up SFR for source of DMA channel 0 transfer

- DMA SFR address register 0 (DSA0)
  Set SFR for the source of DMA transfer to ADCR (0x1E).

  Symbol: DSA0

7	6	5	4	3	2	1	0
0	**0**	**0**	**1**	**1**	**1**	**1**	**0**

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.7 User's Initialization Function

Figure 5.8 shows the flowchart for the user's initialization function.

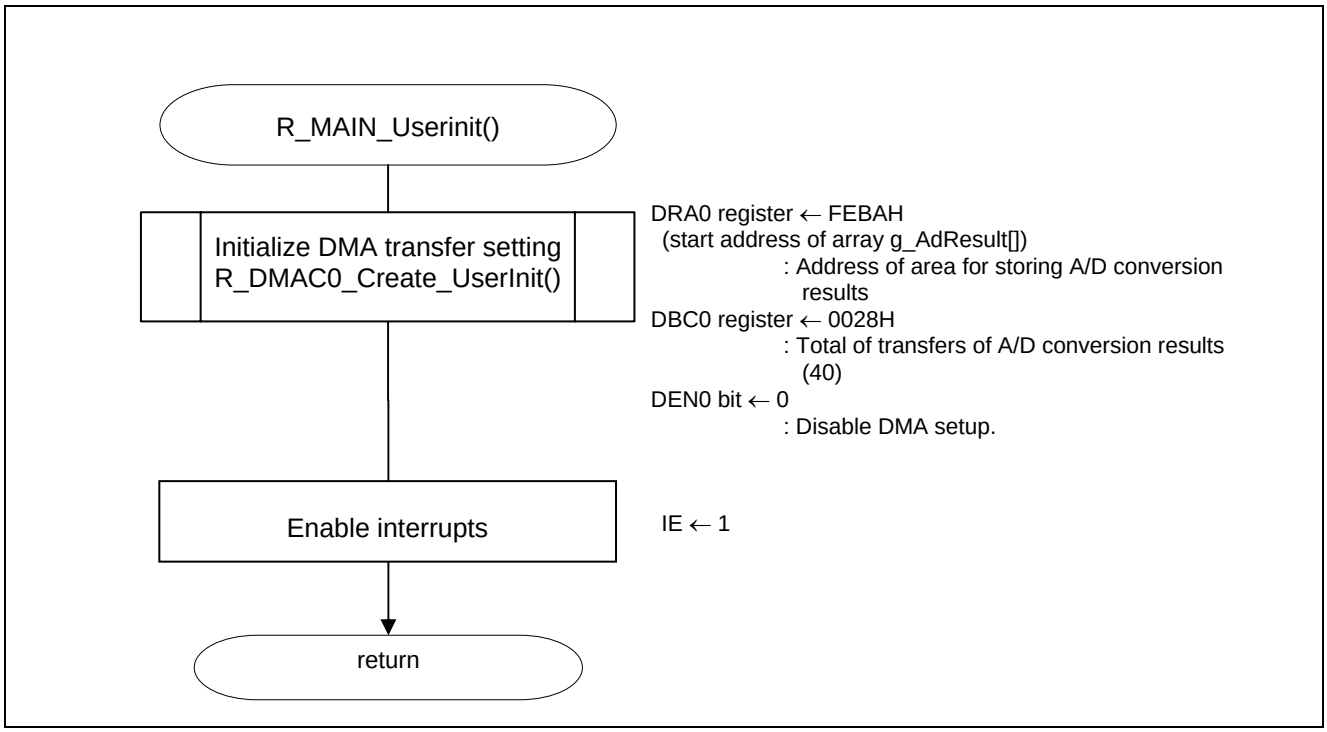

Figure 5.8 User's Initialization Function

Setting up DMA channel 0 destination RAM address

- DMA RAM address register 0 (DRA0)
  Set up the RAM address of DMA transfer destination.

Symbol: DRA0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Set up the start address of array g_AdResult[].

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

Setting up DMA channel 0 transfer count

- DMA byte count register 0 (DBC0)
  Specify DMA transfer count.

Symbol: DBC0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	0	0	**0**	**0**	**0**	**0**	**1**	**0**	**1**	**0**	**0**	**0**

Set the number of DMA transfers to 40 times.

Caution: For details on the register setup procedures, refer to RL78/G13 User's Manual: Hardware.

5.7.8 Main Processing

Figure 5.9 shows the flowchart for the main processing.

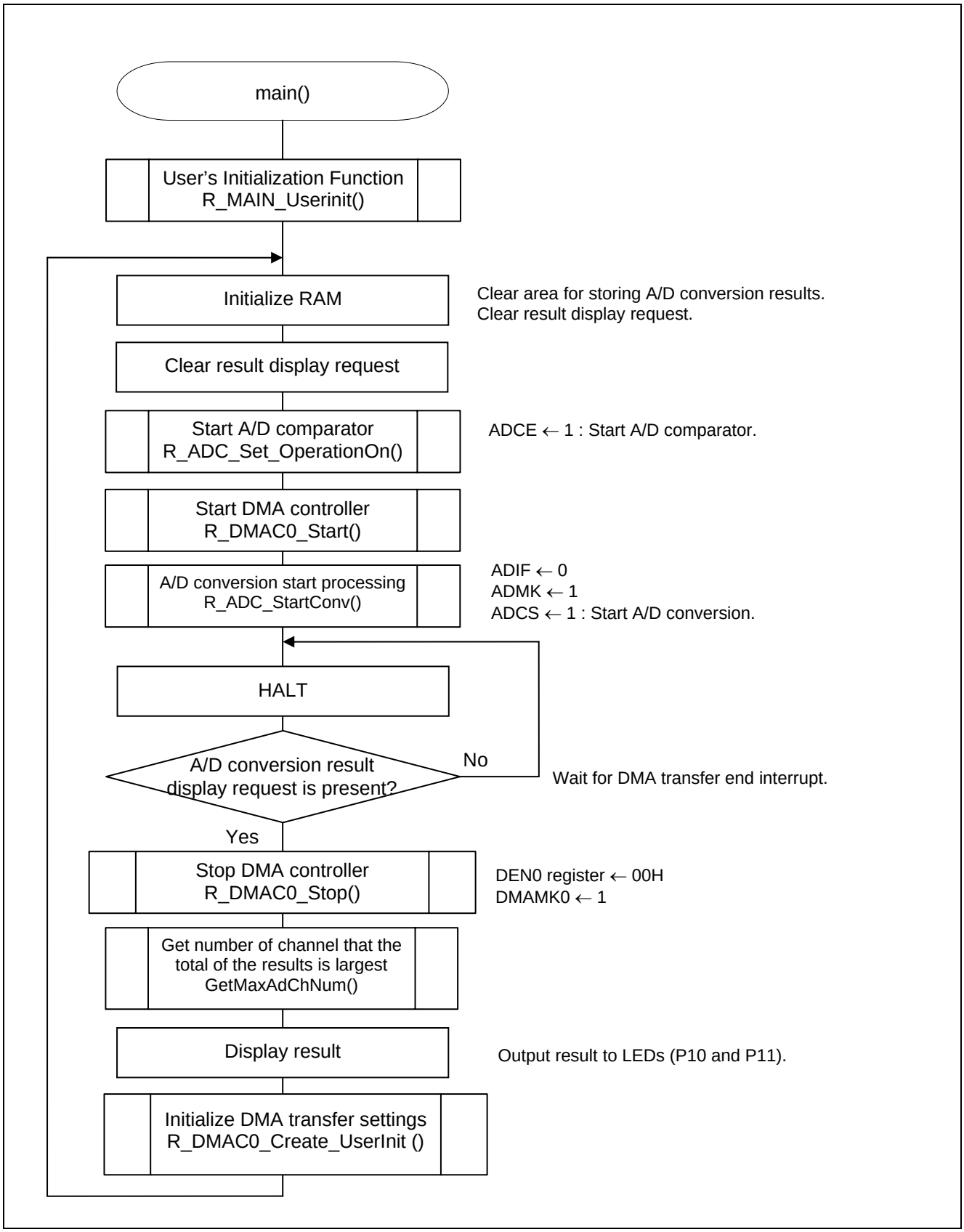

Figure 5.9 Main Processing

5.7.9 Enabling the A/D Voltage Comparator

Figure 5.10 shows the flowchart for enabling the A/D voltage comparator.

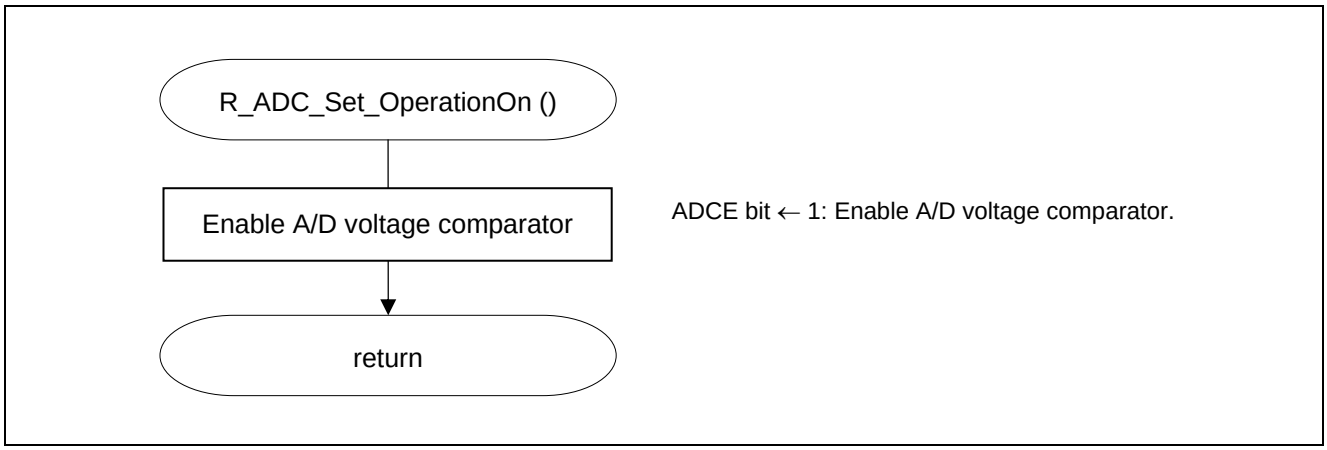

Figure 5.10 Enabling the A/D Voltage Comparator

5.7.10 Starting the DMA Controller

Figure 5.11 shows the flowchart for starting the DMA controller.

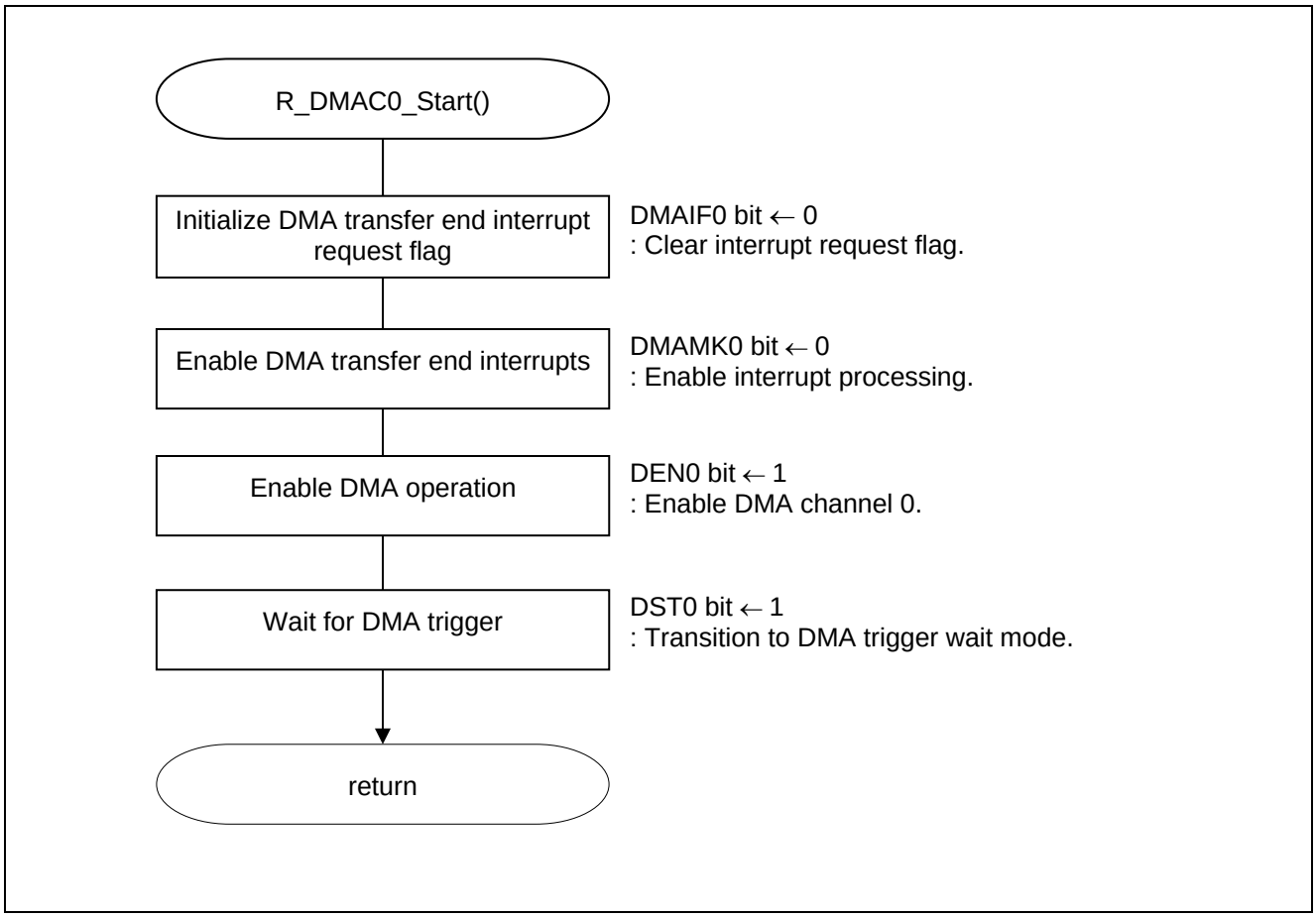

Figure 5.11 Starting the DMA Controller

Preparing for enabling DMA transfer end interrupts

- Interrupt request flag register (IF0H)
  Clear interrupt request flag.
- Interrupt mask flag register (MK0H)
  Clear interrupt mask.

Symbol: IF0H

7	6	5	4	3	2	1	0
SREIF0 TMIF01H	SRIF0 CSIIF01 IICIF01	STIF0 CSIIF00 IICIF00	DMAIF1	DMAIF0	SREIF2 TMIF11H	SRIF2 CSIIF21 IICIF21	STIF2 CSIIF20 IICIF20
x	x	x	x	**0**	x	x	x

Bit 3

DMAIF0	Interrupt request flag
0	**No interrupt request signal is generated**
1	Interrupt request is generated, interrupt request status

Symbol: MKH

7	6	5	4	3	2	1	0
SREMK0 TMMK01H	SRMK0 CSIMK01 IICMK01	STMK0 CSIMK00 IICMK00	DMAMK 1	DMAMK 0	SREMK2 TMMK11 H	SRMK2 CSIMK21 IICMK21	STMK2 CSIMK20 IICMK20
x	x	x	x	**0**	x	x	x

Bit 3

DMAMK0	Interrupt processing control
0	**Enables interrupts.**
1	Disables interrupts.

Setting up DMA channel 0 operation trigger wait mode

- DMA operation control register (DRC0)

Symbol: DRC0

7	6	5	4	3	2	1	0
DEN0	0	0	0	0	0	0	DST0
1	0	0	0	0	0	0	**1**

Bit 7

DEN0	DMA operation enable flag
0	Disables operation of DMA channel 0 (stop DMA operation clock). Disables DMA setup processing.
1	**Enables operation of DMA channel 0.** **Enables DMA setup processing.**

Bit 0

DST0	DMA transfer mode flag
0	DMA transfer of DMA channel 0 is completed.
1	**DMA transfer of DMA channel 0 is not completed (still under execution).**

DMAC waits for a DMA trigger when DST0 = 1 after DMA operation is enabled (DEN0 = 1).

5.7.11 Starting A/D Conversion

Figure 5.12 shows the flowchart for starting A/D conversion.

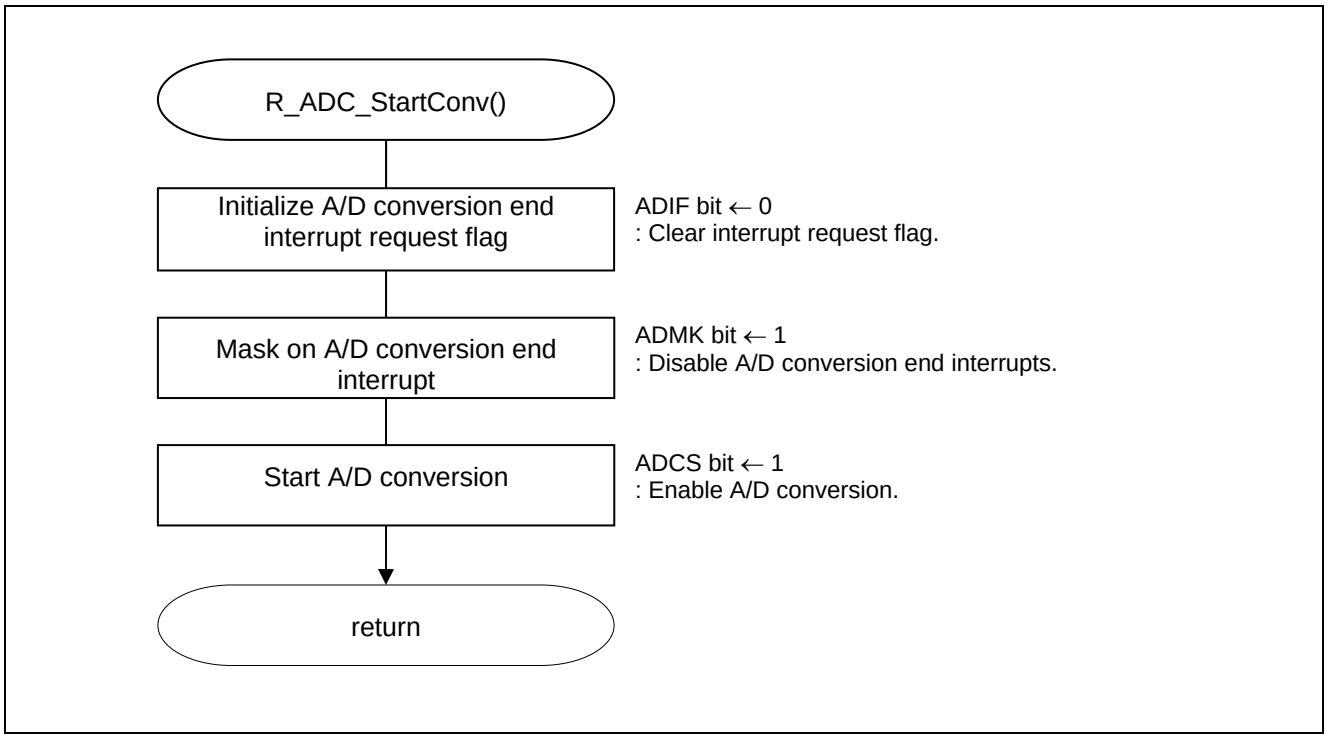

Figure 5.12 Starting A/D Conversion

5.7.12 Stopping the DMA Controller

Figure 5.13 shows the flowchart for stopping the DMA controller.

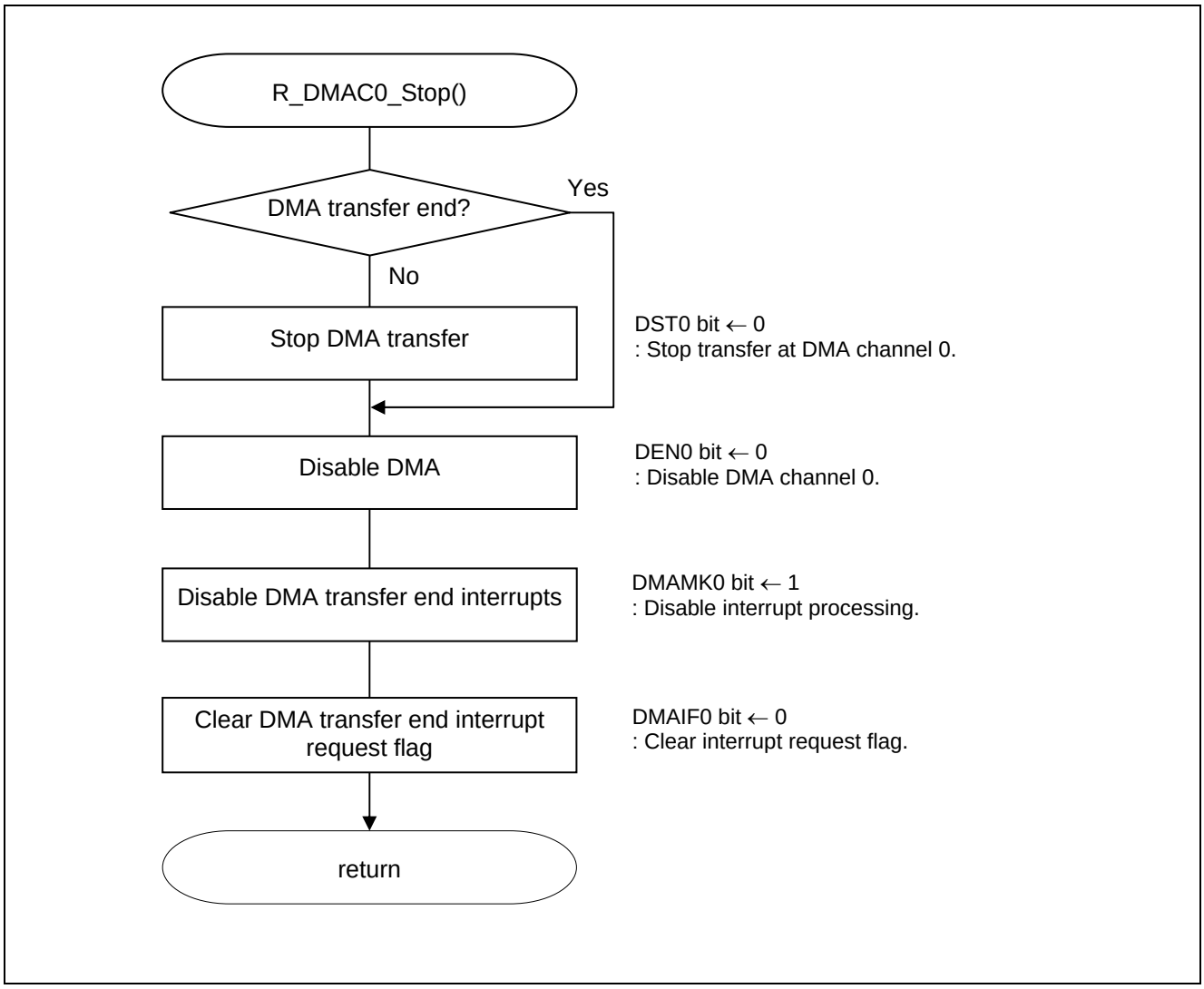

Figure 5.13 Stopping the DMA Controller

5.7.13 Getting the Number of the Channel that has the Largest Total of the A/D Conversion Results

Figure 5.14 shows the flowchart for getting the number of the channel that has the largest total of A/D conversion results.

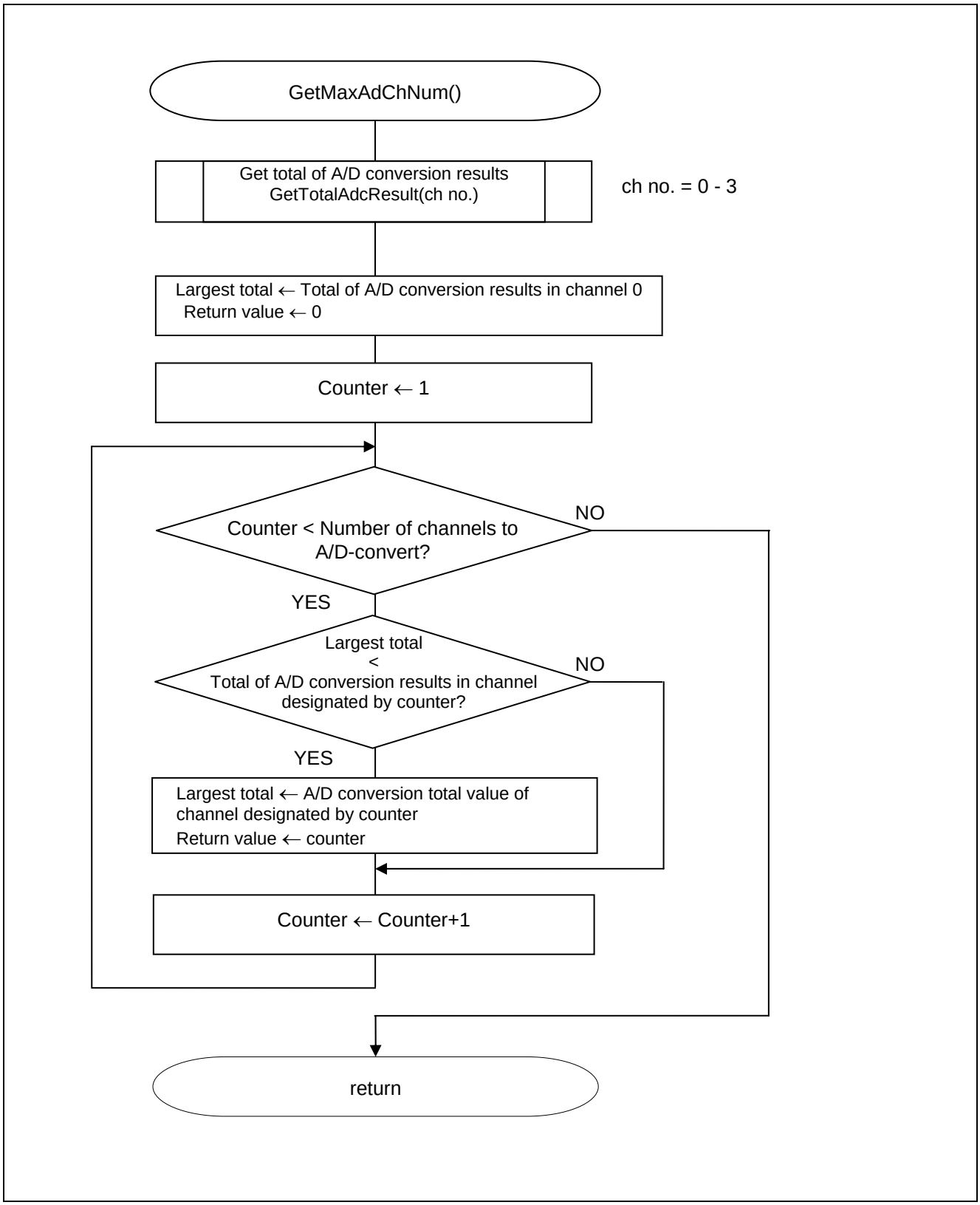

Figure 5.14 Getting the Number of the Channel that the has the Largest Total of A/D Conversion Results

5.7.14 Getting the Total of A/D Conversion Results

Figure 5.15 shows the flowchart for getting the total of A/D conversion results.

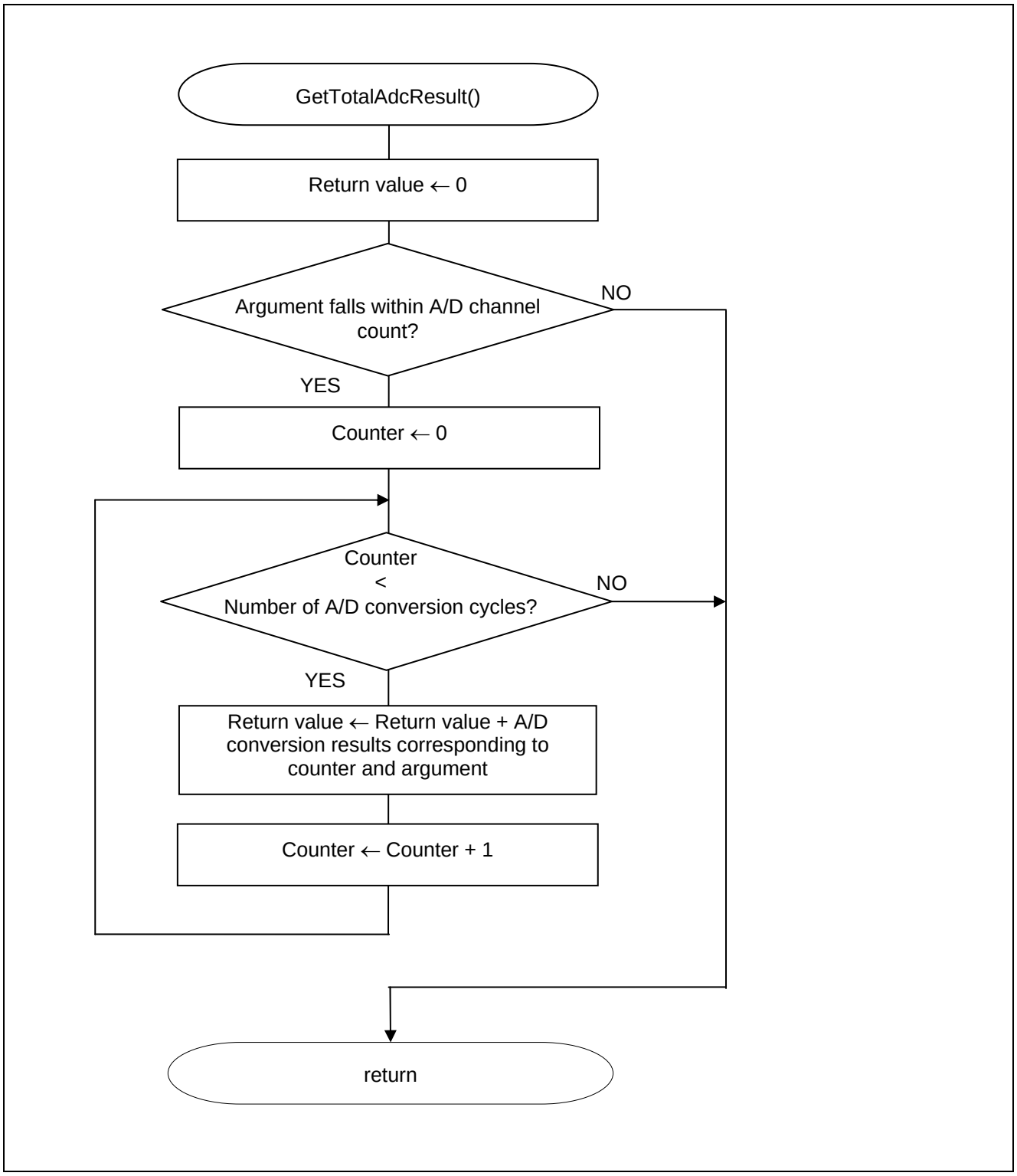

Figure 5.15 Getting the Total of A/D Conversion Results

5.7.15 DMA Transfer End Interrupt Processing

Figure 5.16 shows the flowchart for the DMA transfer end interrupt processing.

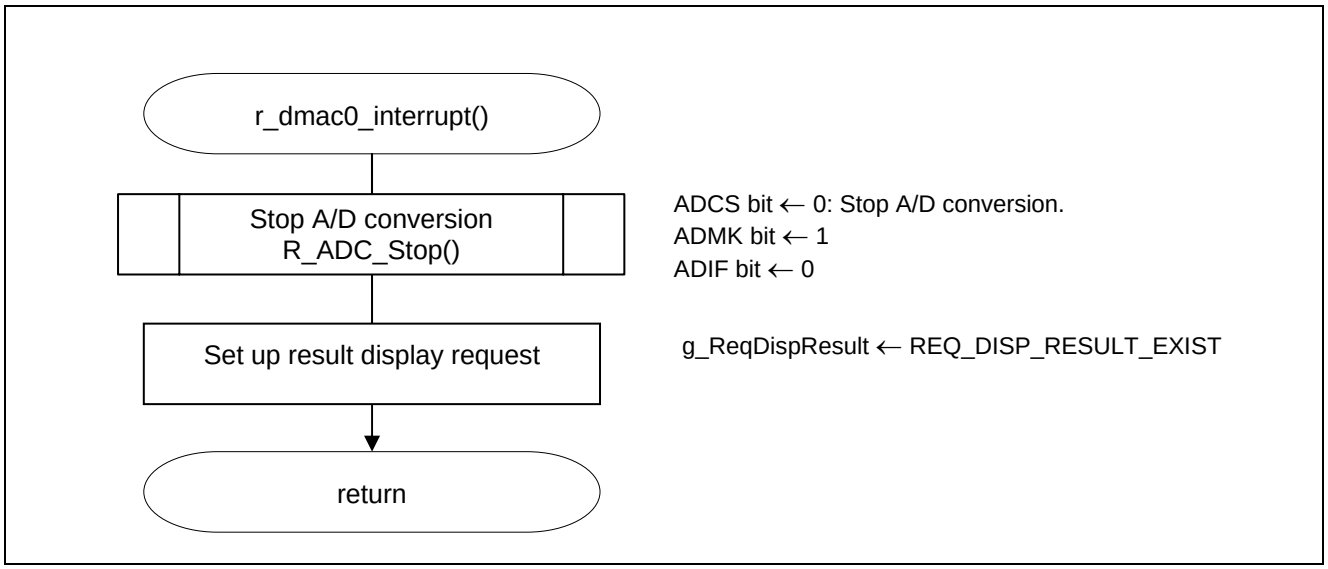

Figure 5.16 DMA Transfer End Interrupt Processing

5.7.16 Stopping A/D Conversion

Figure 5.17 shows the flowchart for stopping A/D conversion.

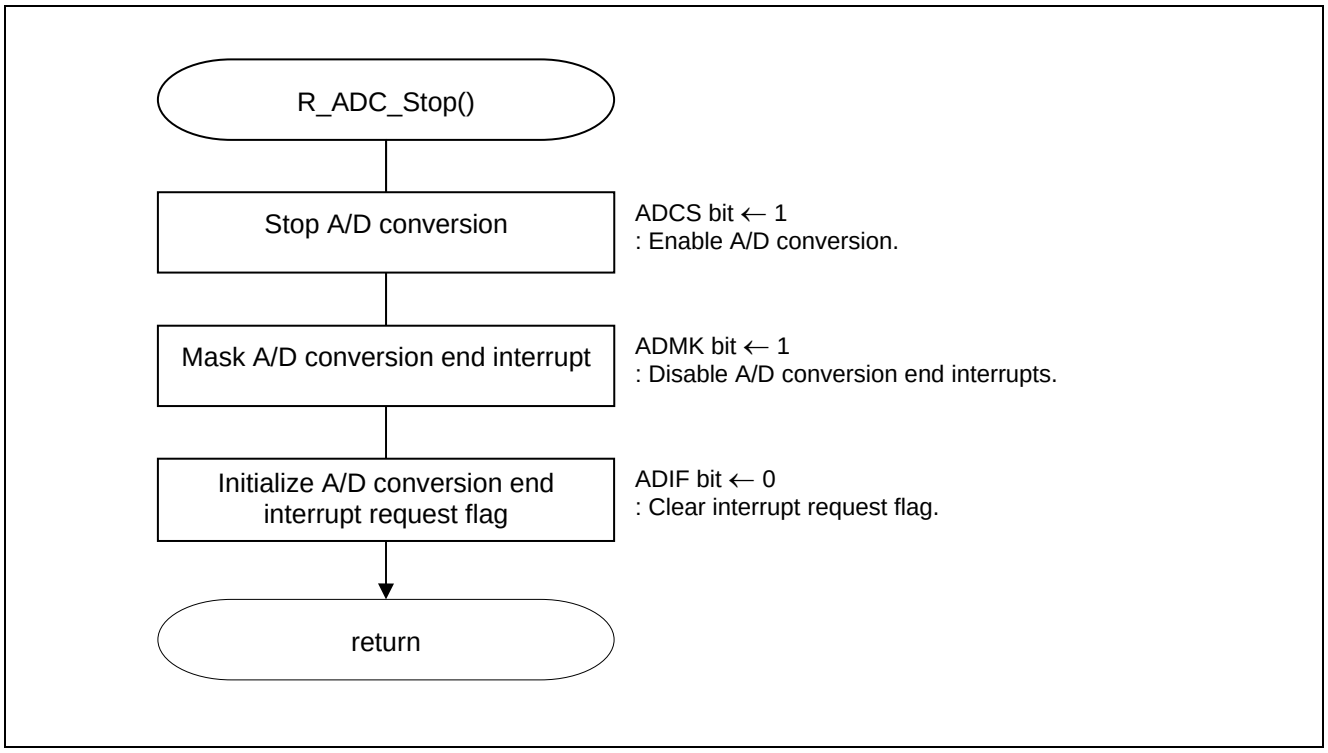

Figure 5.17 Stopping A/D Conversion

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G13 User's Manual: Hardware (R01UH0146E)

RL78 Family User's Manual: Software (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

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Revision Record	RL78/G13 DMA Controller (A/D Converter in Sequential Conversion Mode)

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 16, 2015	—	First edition issued

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The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

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