RL78/G12

Self-Programming (Received Data via CSI)

R01AN1360EJ0110
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Introduction

This application note gives the outline of flash memory reprogramming using a self-programming technique. In this application note, flash memory is reprogrammed using the flash memory self-programming library Type01.

The sample program described in this application note limits the target of reprogramming to the boot area. For details on the procedures for performing self-programming and for reprogramming the entire area of code flash memory, refer to RL78/G13 Microcontroller Flash Memory Self-Programming Procedures (R01AN0718E) Application Note.

Target Device

RL78/G12

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

This application note explains a sample program that performs flash memory reprogramming using a self-programming library.

The sample program displays the information about the current version of the library on the LCD. Subsequently, the program receives data (reprogramming data) from the sending side and, after turning on the LED indicating that it is accessing flash memory, carries out self-programming to rewrite the code flash memory with the reprogramming data. When the rewrite is completed, the sample program turns off the LED and displays the information about the new version on the LCD.

Table 1.1 lists the peripheral functions to be used and their uses.

Table 1.1 Peripheral Functions to be Used and their Uses

Peripheral Function	Use
Channel 0 of serial array unit 0	Receives data via CSI.
Port I/O	Turns on and off the LED. Outputs the BUSY signal. Note

Note: The BUSY signal indicates whether communication is enabled or disabled. When it is set to 0, it indicates communication is enabled. When it is set to 1, it indicates communication is disabled.

1.1 Outline of the Flash Memory Self-Programming Library

The flash memory self-programming library is a software product that is used to reprogram the data in the code flash memory using the firmware installed on the RL78 microcontroller.

The contents of the code flash memory can be reprogrammed by calling the flash memory self-programming library from a user program.

To do flash memory self-programming, it is necessary for the user program to perform initialization for flash memory self -programming and to execute the C or assembler functions that correspond to the library functions to be used.

1.2 Code Flash Memory

The configuration of the RL78/G12 (R5F1026A) code flash memory is shown below.

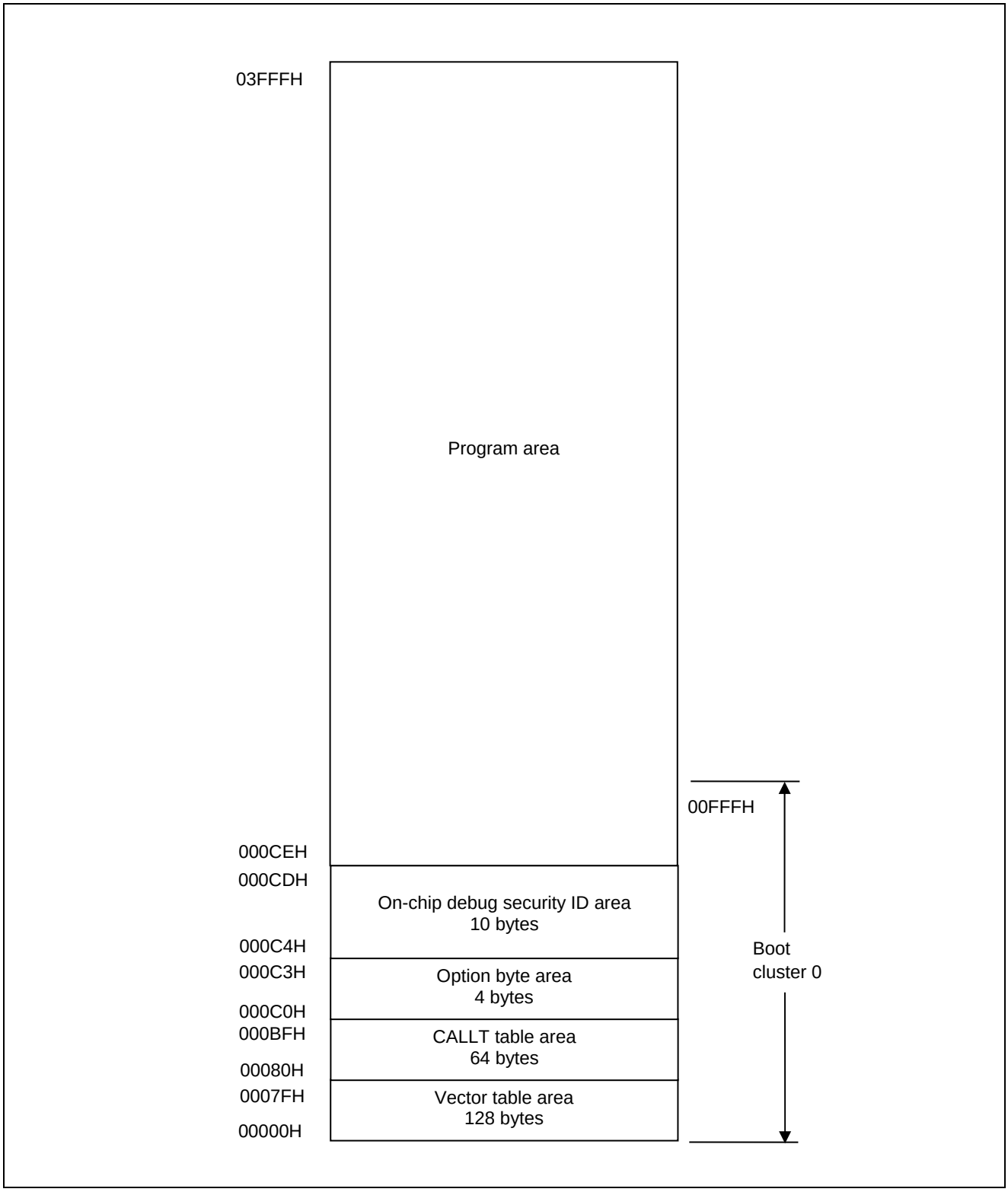

Figure 1.1 Code Flash Memory Configuration

The features of the RL78/G13 code flash memory are summarized below.

Table 1.2 Features of the Code Flash Memory

Item	Description
Minimum unit of erasure and verification	1 block (1024 bytes)
Minimum unit of programming	1 word (4 bytes)
Security functions	Block erasure, programming, and boot area reprogramming protection are supported. (They are enabled at shipment)
	Security settings programmable using the flash memory self-programming library

Caution: The boot area reprogramming protection setting and the security settings are disabled during flash memory self-programming.

1.3 Flash Memory Self-Programming

The RL78/G13 is provided with a library for flash memory self-programming. Flash memory self-programming is accomplished by calling functions of the flash memory self-programming library from the reprogramming program.

The flash memory self-programming library for the RL78/G13 controls flash memory reprogramming using a sequencer (a dedicated circuit for controlling flash memory). The code flash memory cannot be referenced while control by the sequencer is in progress. When the user program needs to be run while the sequencer control is in progress, therefore, it is necessary to relocate part of the segments for the flash memory self-programming library and the reprogramming program in RAM when erasing or reprogramming the code flash memory or making settings for the security flags. If there is no need to run the user program while the sequencer control is in progress, it is possible to keep the flash memory self-programming library and reprogramming program on ROM (code flash memory) for execution.

1.3.1 Flash Memory Reprogramming

The RL78/G12 does not have the boot swap function. When reprogramming, using the flash memory self-programming function, of the area where vector table data, the basic functions of the program, and flash memory self-programming library are allocated fails due to a temporary power blackout or a reset caused by an external factor, the data that is being reprogrammed will be corrupted, as the result of which the restarting of the user program or reprogramming cannot be accomplished when a reset is subsequently performed.

This subsection describes the outline image of reprogramming using the flash memory self-programming technique. The program that performs flash memory self-programming is placed in boot cluster 0.

The sample program described in this application note limits the target of reprogramming to a part of the code flash memory (addresses 0x3BFC to 0x3BFF) and uses the other part of the code flash memory as a data area. For details on the procedures for perform self-programming and for reprogramming the entire area of code flash memory, refer to RL78/G13 Microcontroller Flash Memory Self-Programming Execution (R01AN0718E) Application Note.

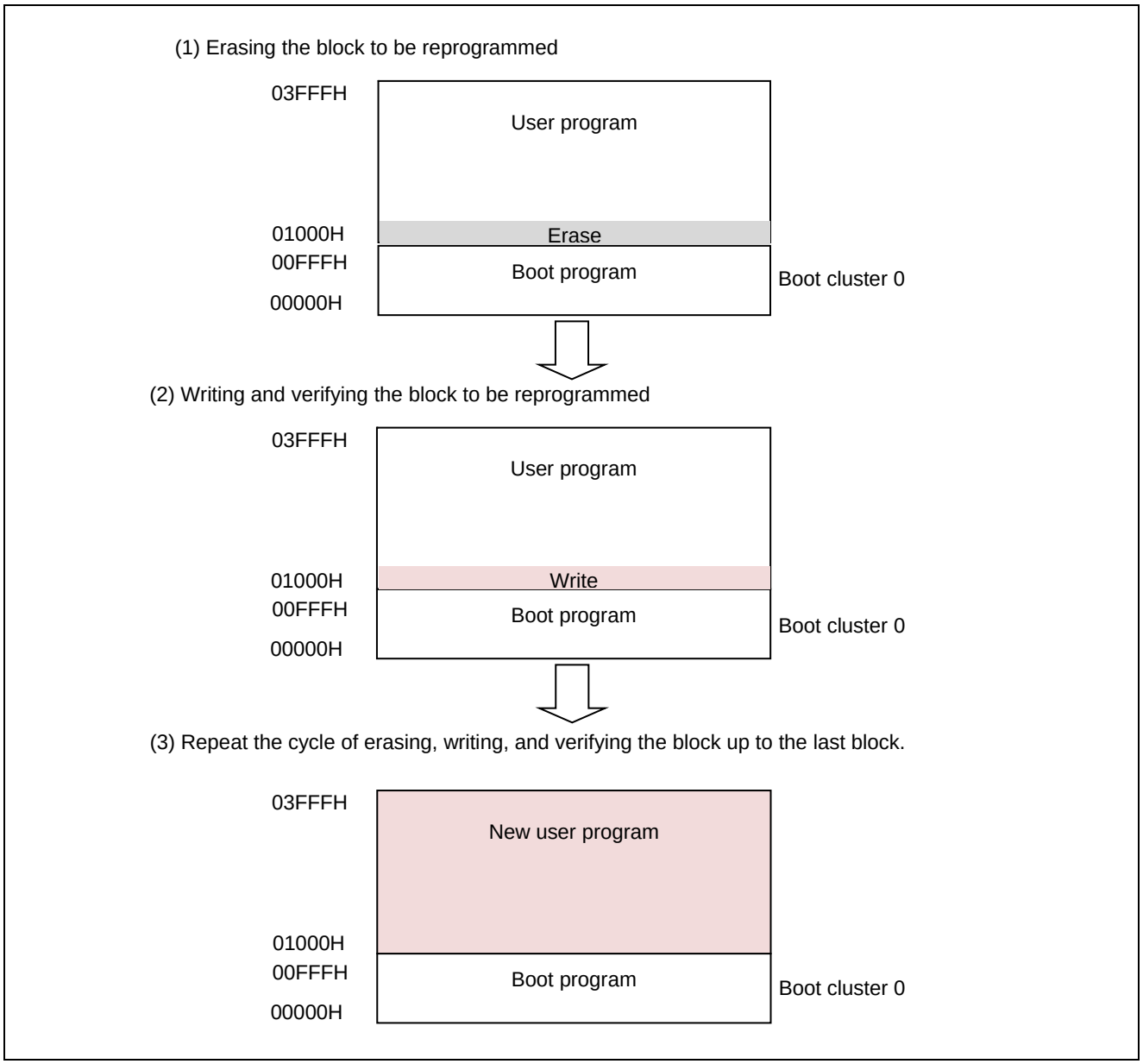

Figure 1.2 Outline of Flash Memory Reprogramming

1.4 How to Get the Flash Memory Self-Programming Library

Before compiling the sample program, please download the latest flash self-programming library and copy the library files to the following folder below “Workspace”.

incrl78 folder : fsl.h, fsl.inc, fsl_types.h

librl78 folder : fsl.lib

The flash memory self-programming library is available on the Renesas Electronics Website.

Please contact your local Renesas Electronics sales office or distributor for more information.

2. Operation Check Conditions

The sample code described in this application note has been checked under the conditions listed in the table below.

Table 2.1 Operation Check Conditions

Item	Description
Microcontroller used	RL78/G12 (R5F1026A)
Operating frequency	• High-speed on-chip oscillator (HOCO) clock: 24 MHz • CPU/peripheral hardware clock: 24 MHz
Operating voltage	5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.) LVD operation (V_{LVD}): Reset mode which uses 2.81 V (2.76 V to 2.87 V)
Integrated development environment	CS+ for CA,CX V3.02.00 from Renesas Electronics Corp.
C compiler	CA78K0R V1.72 from Renesas Electronics Corp.
Board to be used	RL78/G12 target board (QB-R5F1026A-TB)
Flash memory self-programming library (Type, Ver)	FSLRL78 Type01, Ver 2.20 Note

Note: Use and evaluate the latest version.

3. Related Application Notes

The application notes that are related to this application note are listed below for reference.

- RL78/G12 Initialization (R01AN1030E) Application Note
- RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Master Transmission/Reception) (R01AN0460E) Application Note
- RL78/G13 Serial Array Unit for 3-Wire Serial I/O (Slave Transmission/Reception) (R01AN0461E) Application Note
- RL78 Microcontroller Flash Memory Self-Programming Library Type01 (R01AN0350E) Application Note

4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.

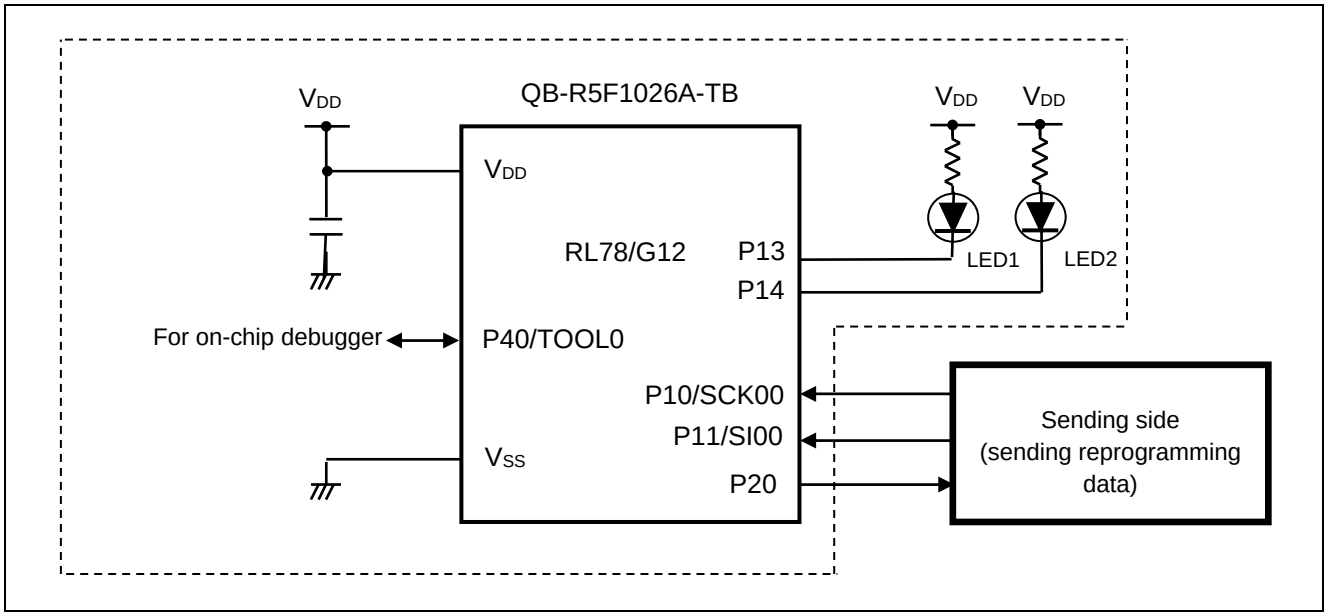

Figure 4.1 Hardware Configuration

Cautions:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to V_{DD} or V_{SS} via a resistor).
2. V_{DD} must be held at not lower than the reset release voltage (V_{LVD}) that is specified as LVD.

4.2 List of Pins to be Used

Table 4.1 lists pins to be used and their functions.

Table 4.1 Pins to be Used and their Functions

Pin Name	I/O	Description
P10/ANI16/PCLBUZ0/SCK00/SCL00	Input	CSI serial clock input pin
P11/ANI17/SI00/RxD0/SDA00/TOOLRxD	Input	CSI serial data receive pin
P13	Output	LED1 on/off control
P14	Output	LED2 on/off control
P20	Output	BUSY signal Note

Note: The BUSY signal indicates whether communication is enabled or disabled. When it is set to 0, it indicates communication is enabled. When it is set to 1, it indicates communication is disabled.

5. Description of the Software

5.1 Communication Specifications

The sample program covered in this application note receives reprogramming data via the CSI bus for flash memory self-programming. The sending side sends three commands, i.e., the START, WRITE, and END commands. The sample program takes actions according to the command it received, and, if the command terminates normally, sets the BUSY signal to the high level. If the command terminates abnormally, the sample program returns no response, turns on LED1 and LED2, and takes no subsequent action. This section describes the necessary CSI communication settings and the specifications for the commands.

Table 5.1 CSI Communication Settings

Transfer mode	Single transfer mode
Data bit length [bit]	8
Data transfer direction	MSB first
Data transmission/reception timing	Type 1
Transfer clock	External clock (slave) which operates with a clock from master

5.1.1 START Command

When the sample program receives the START command, it performs initialization processing for flash memory self-programming. When the command terminates normally, the program sets the BUSY signal to the high level. In the case of an abnormal termination, the sample program returns no response, turns on LED1 and LED2, and suppresses the execution of the subsequent operations.

START code (0x01)	Data length (0x0002)	Command (0x02)	Data (None)	Checksum (1 byte)

5.1.2 WRITE Command

When the sample program receives the WRITE command, it writes the data it received into flash memory. The sample program sets the BUSY signal to the high level on normal termination of the command. In the case of an abnormal termination, the sample program returns no response, turns on LED1 and LED2, and suppresses the execution of the subsequent operations.

START code (0x01)	Data length (0x0102)	Command (0x03)	Data (256 bytes)	Checksum (1 byte)

5.1.3 END Command

When the sample program receives the END command, it performs verify processing on the block that is currently being written. If the verification terminates abnormally, the program turns on LED1 and LED2 and suppresses the execution of the subsequent operations. When the sample program receives the END command, it returns no response to the sending side regardless of whether the command terminates normally or abnormally.

START code (0x01)	Data length (0x0002)	Command (0x04)	Data (None)	Checksum (1 byte)

* The checksum is the sum of the command and data fields in units of bytes.

5.1.4 Communication Sequence

This sample program takes actions according to the sequence described below upon receipt of a command from the sending side.

(1) Sample program:

Sets the BUSY signal to the high level to request a command.

(2) Sending side:

Sends the START command.

(3) Sample program:

Sets the BUSY signal to the low level, turns on LED2 to indicate that flash memory is being accessed, and performs initialization for flash memory self-programming. The program sets the BUSY signal to the high level to request the next command on normal termination of the initialization processing.

(4) Sending side:

Sends a WRITE command and data (4 bytes).

(5) Sample program:

Sets the BUSY signal to the low level and writes the received data (4 bytes) into program flash memory addresses 0x3BFC to 0x3BFF. The program sets the BUSY signal to the high level to request the next command on normal termination of the initialization processing.

(6) Sending side:

Sends the END command.

(7) Sample program:

Performs verify processing on the block that is currently subjected to reprogramming and turns off LED2 to indicate that flash memory is not being accessed.

5.2 Operation Outline

This application note explains a sample program that performs flash memory reprogramming using a self-programming library.

The sample program reads values from the code flash memory addresses 0x3BFC to 0x3BFF and sets the flashing interval of LED1 with the read value. Subsequently, the program receives data (4 bytes) from the sending side and carries out self-programming to rewrite the values that are stored in code flash memory addresses 0x3BFC to 0x3BFF with the received data. When reprogramming is completed, the sample program reads again the values that are stored in code flash memory addresses 0x3BFC to 0x3BFF and sets the flashing interval of LED1 with the read value.

LED1 flashes at the interval that is equal to the average value of the data (4 bytes) received from the sending side (sum of byte values stored in code flash memory addresses 0x3BFC to 0x3BFF divided by 4) × 10 [ms]. For example, if address 0x3BFC contains a value of "15," address 0x3BFD contains "150," address 0x3BFE contains "100," and address 0x3BFF contains "200," according to the calculation (15 + 150 + 100 + 200) / 4 * 10 = 1162.5, LED1 flashes at intervals of 1162.5 [ms].

LED2 indicates that flash memory is being accessed when it is on.

(1) Sets up the I/O port.

<Setting conditions>

- LED on/off control ports (LED1 and LED2): Sets P13 and P14 for output.
- BUSY signal output port: Sets P20 for output.

(2) Initializes the SAU0 channel 0.

<Setting conditions>

- Uses the SAU0 channel 2 as CSI.
- Uses the P11/SI00 pin for data input.
- Uses the P10/SCK00 pin for clock input.
- Sets the data length to 8 bits.
- Sets the order of data transfer mode to MSB first.
- Sets the data transmission/reception timing to type 1.
- Selects the external clock as a transfer clock.

(3) Starts the CSI00.

(4) Enables interrupts.

(5) Reads values from code flash memory addresses 0x3BFC to 0x3BFF, calculates an average of the values in addresses 0x3BFC to 0x3BFF, and turns on LED1.

(6) If the read values are greater than 0, sets the interval time of TAU0 channel 0 to the average value of values in addresses 0x3BFC to 0x3BFF × 10 [ms] and starts the TAU0 channel 0.

(7) Sets the BUSY signal to the high level, enters the HALT mode, and waits for data from the sending side.

- After setting the BUSY signal to the high level, switches into the normal operation mode from the HALT mode upon a CSI transfer end interrupt request or TAU0 channel 0 interrupt request. The program enters the HALT mode again if it returns from the HALT mode upon a TAU0 channel 0 interrupt request.

(8) Disables interrupts.

(9) Stops the TAU0 channel 0 if the read values are greater than 0.

(10) Sets the BUSY signal to the high level and waits for a START command (0x02) from the sending side. After receiving it, sets the BUSY signal to the low level and performs initialization for self-programming.

- Sets P14 to the low level to turn on LED2, indicating that flash memory is being accessed.
- Calls the FSL_Init function to initialize the flash memory self-programming environment and makes the following settings:
  Voltage mode : Full-speed mode
  CPU operating frequency : 24 [MHz]
  Status check mode : Status check internal mode
- Calls the FSL_Open function to start flash memory self-programming (starting the flash memory environment).
- Calls the FSL_PrepareFunctions function to make available the flash memory functions (standard reprogramming functions) that are necessary for the RAM executive.

(11) Sets the BUSY signal to the high level and waits for a WRITE command (0x03) and write data (4 bytes) from the sending side. After receiving them, sets the BUSY signal to the low level.

(12) Computes the reprogramming target block from the write destination address.

(13) Calls the FSL_BlankCheck function to check whether the reprogramming target block has already been reprogrammed.

(14) If the reprogramming target block is reprogrammed, calls the FSL_Erase function to erase the reprogramming target block.

(15) Calls the FSL_Write function to write the received data at the write destination address.

(16) Sets the BUSY signal to the high level and waits for an END command (0x04) from the sending side. After receiving it, sets the BUSY signal to the low level.

(17) Calls the FSL_IVerify function to verify the reprogramming target block.

(18) Sets P14 to the high level to turn off LED2, indicating that flash memory is not being accessed.

(19) Returns to step (4).

Caution: When flash memory self-programming could not be terminated normally (error occurring during processing), the sample program turns on LED1 and LED2 and suppresses the execution of the subsequent operations.

5.3 File Configuration

Table 5.2 lists the additional functions for files that are automatically generated in the integrated development environment and other additional files.

Table 5.2 List of Additional Functions and Files

File Name	Outline	Remarks
r_main.c	Main module	Additional functions: R_MAIN_LedBlink R_MAIN_ClearCsiFlag R_MAIN_PacketAnalyze R_MAIN_SelfExecute R_MAIN_SelfInitialize R_MAIN_WriteExecute
r_cg_serial_user.c	SAU module	Additional functions: R_CSI00_ReceiveStart

5.4 List of Option Byte Settings

Table 5.3 summarizes the settings of the option bytes.

Table 5.3 Option Byte Settings

Address	Setting	Description
000C0H/010C0H	11101111B	Disables the watchdog timer. (Stops counting after the release from the reset status.)
000C1H/010C1H	01111111B	LVD reset mode 2.81 V (2.76 V to 2.87 V)
000C2H/010C2H	11100000B	HS mode, HOCO: 24 MHz
000C3H/010C3H	10000100B	Enables the on-chip debugger Erases the data in the flash memory when on-chip debug security ID authentication fails.

The option bytes of the RL78/G12 comprise the user option bytes (000C0H to 000C2H) and on-chip debug option byte (000C3H).

The option bytes are automatically referenced and the specified settings are configured at power-on time or the reset is released.

5.5 Link Directive File

The reprogramming program that performs flash memory self-programming and the flash memory self-programming library are allocated to blocks 0 to 3 (boot cluster 0) by the link directive file. It is also used to make configuration so that the RAM area to be used by the flash memory self-programming library will not be used.

The outline of the link directive file that this sample program uses is shown below.

```
;************************************************************
; Redefined ROM area
;************************************************************
; ------------------------------------------------------------
; Define new memory entry for boot cluster 0
; ------------------------------------------------------------
MEMORY ROM          : ( 000000H, 003800H )
; ------------------------------------------------------------
; Define new memory entry for write-data area
; ------------------------------------------------------------
MEMORY OCDROM       : ( 003E00H, 000200H )

;************************************************************
; Library(fsl.lib) segment
;************************************************************
; ------------------------------------------------------------
; Merge FSL_FCD segment
; ------------------------------------------------------------
MERGE FSL_FCD    := ROM
; ------------------------------------------------------------
; Merge FSL_FECD segment
; ------------------------------------------------------------
; MERGE FSL_FECD := ROM
; ------------------------------------------------------------
; Merge FSL_RCD segment
; ------------------------------------------------------------
MERGE FSL_RCD    := ROM
; ------------------------------------------------------------
; Merge FSL_BCD segment
; ------------------------------------------------------------
MERGE FSL_BCD    := ROM
; ------------------------------------------------------------
; Merge FSL_BECD segment
; ------------------------------------------------------------
; MERGE FSL_BECD := ROM

;************************************************************
; Redefined RAM area
;************************************************************
; ------------------------------------------------------------
; Define new memory entry for self-RAM
; ------------------------------------------------------------
MEMORY SELFRAM      : ( 0FF900H, 00038AH )
; ------------------------------------------------------------
; Redefined default data segment RAM
; ------------------------------------------------------------
MEMORY RAM          : ( 0FFC8AH, 000196H )
; ------------------------------------------------------------
; Define new memory entry for saddr area
; ------------------------------------------------------------
MEMORY RAM_SADDR : ( 0FFE20H, 0001E0H )

;************************************************************
; run-time library segment ( 0000H - FFFFH )
;************************************************************
; ------------------------------------------------------------
; Merge @@LCODE,@@LCODEL(run-time library) segment
; ------------------------------------------------------------
MERGE @@LCODE    := ROM
MERGE @@LCODEL := ROM
```

Code area definition
The code is allocated to addresses 0x0000 to 0x37FF.
Addresses 0x3800 to 0x3BFF are used as a data area and not loaded with code.

OCD monitor area definition

Allocates the flash memory self-programming library to the boot area.

Makes definition so that the area to be used by the flash memory self-programming library will not be used as the standard RAM area

Standard RAM area definition

Makes definition so that the area to be used by the flash memory self-programming library will not be used as the standard RAM area.

Allocates the run-time library to the boot area.

5.6 List of Constants

Table 5.4 lists the constants for the sample program.

Table 5.4 Constants for the Sample Program

Constant	Setting	Description
LED1	P1.3	LED1 control port
LED2	P1.4	LED2 control port
LED_ON	0	LED is on.
LED_OFF	1	LED is off.
NORMAL_END	0x00	Normal termination
ERROR	0xFF	Abnormal termination
NO_RECIEVE	0x00	Command reception state: Not received
START_CODE	0x01	Command reception state: START code received
PACKET_SIZE	0x02	Command reception state: Data length received
START	0x02	START command
WRITE	0x03	WRITE command
END	0x04	END command
FULL_SPEED_MODE	0x00	Argument to flash memory self-programming library initialization function: Set operation mode to full-speed mode.
FREQUENCY_24M	0x18	Argument to flash memory self-programming library initialization function: RL78/G12's operating frequency = 24 MHz
INTERNAL_MODE	0x01	Argument to flash memory self-programming library initialization function: Turn on status check internal mode.
BLOCK_SIZE	0x400	One block size of code flash memory (1024 bytes)
TXSIZE	0x01	Size of response data to be sent to the sending side
RXSIZE	0x06	Size of receive buffer
WRITESIZE	0x01	Write data size (words)
WRITEADDR	0x3BFC	Write start address
READADDR	0x3BFC	Read start address

5.7 List of Variables

Table 5.5 lists the global variables that are used in this sample program.

Table 5.5 Global Variables for the Sample Program

Type	Variable Name	Contents	Function Used
uint8_t	g_intcsi00_flag	CSI transfer end interrupt flag	main R_MAIN_ ClearCsiFlag r_csi00_interrupt

5.8 List of Functions

Table 5.6 lists the functions that are used in this sample program.

Table 5.6 List of Functions

Function Name	Outline
R_CSI00_Start	Starts CSI00.
r_csi00_interrupt	CSI transfer end interrupt
R_MAIN_LedBlink	Sets LED1 flashing interval according to read values and starts LED1 flashing.
R_TAU0_Channel0_Start	Starts TAU0 channel 0.
r_tau0_channel0_interrupt	TAU0 channel 0 interrupt
R_CSI00_ReceiveStart	Receives data via CSI00.
R_MAIN_ClearCsiFlag	Clears CSI receive end interrupt flag and CSI receive error interrupt flag.
R_TAU0_Channel0_Stop	Stops TAU0 channel 0.
R_MAIN_PacketAnalyze	Analyzes receive data.
R_MAIN_SelfExecute	Executes flash memory self-programming.
R_MAIN_SelfInitialize	Executes initialization for flash memory self-programming.
R_MAIN_WriteExecute	Executes flash memory reprogramming.

5.9 Function Specifications

This section describes the specifications for the functions that are used in the sample program.

[Function Name] R_ UART0_Start

Synopsis	Start CSI00.
Header	r_cg_macrodriver.h r_cg_serial.h r_cg_userdefine.h
Declaration	void R_ CSI00_Start(void)
Explanation	This function starts channel 0 of the serial array unit 0 and places it in communication wait state.
Arguments	None
Return value	None
Remarks	None

[Function Name] r_uart_interrupt_receive

Synopsis	CSI00 receive end interrupt
Header	r_cg_macrodriver.h r_cg_serial.h r_cg_userdefine.h
Declaration	__interrupt void r_csi00_interrupt(void)
Explanation	This function sets the CSI00 receive end interrupt flag (flag g_intsr_flag) to 1 and sets P20 (BUSY signal) to the low level.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_MAIN_LedBlink

Synopsis	Set LED1 flashing interval according to read values and start LED1 flashing.	
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_serial.h r_cg_timer.h r_cg_userdefine.h	
Declaration	void R_MAIN_LedControl(float average)	
Explanation	This function sets the LED1 flashing interval to the value of argument average × 10 [ms] and starts flashing LED1.	
Arguments	average	Average of values in code flash memory addresses 0x3BFC to 0x3BFF
Return value	None	
Remarks	None	

[Function Name] R_TAU0_Channel0_Start

Synopsis	Start TAU0 channel 0.	
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h	
Declaration	void R_TAU0_Channel0_Start(void)	
Explanation	This function starts the TAU0 channel 0.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] r_tau0_channel0_interrupt

Synopsis	TAU0 channel 0 interrupt	
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h	
Declaration	__interrupt void r_tau0_channel0_interrupt(void)	
Explanation	This function inverts the state (ON/OFF) of LED1.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_CSI00_ReceiveStart

Synopsis	Receive data via CSI00.	
Header	r_cg_macrodriver.h r_cg_serial.h r_cg_userdefine.h	
Declaration	uint8_t R_CSI00_ReceiveStart(uint16_t *rxlength, uint8_t *rxbuf)	
Explanation	This function stores the receive data in the receive buffer (rxbuf) and the receive data length [bytes] in rxlength.	
Arguments	rxlength	Address of area for storing receive data length [bytes]
	rxbuf	Address of receive data buffer
Return value	Normal termination: NORMAL_END Abnormal termination: ERROR	
Remarks	None	

[Function Name] R_MAIN_ClearCsiFlag

Synopsis	Clear CSI transfer end interrupt flag.	
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_serial.h r_cg_timer.h r_cg_userdefine.h	
Declaration	void R_MAIN_ClearCsiFlag(void)	
Explanation	This function clears the CSI00 transfer end interrupt flag (g_intcsi00_flag).	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_TAU0_Channel0_Stop

Synopsis	Stop TAU0 channel 0.	
Header	r_cg_macrodriver.h r_cg_timer.h r_cg_userdefine.h	
Declaration	void R_TAU0_Channel0_Stop(void)	
Explanation	This function stops the TAU0 channel 0.	
Arguments	None	
Return value	None	
Remarks	None	

[Function Name] R_MAIN_PacketAnalyze

Synopsis	Analyze receive data.	
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_serial.h r_cg_timer.h r_cg_userdefine.h	
Declaration	uint8_t R_MAIN_PacketAnalyze(uint16_t rxlength, uint8_t *rxbuf)	
Explanation	This function checks the parameters of the command received, and computes and compares the checksum to check whether the received data is correct.	
Arguments	rxlength	Receive data length [bytes]
	rxbuf	Address of receive data buffer
Return value	START command received: START	
	WRITE command received: WRITE	
	END command received: END	
	Command parameter error or checksum error: ERROR	
Remarks	None	

[Function Name] R_MAIN_SelfExecute

Synopsis	Execute flash memory self-programming.
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_serial.h r_cg_userdefine.h fsl.h fsl_types.h
Declaration	void R_MAIN_SelfExecute(void)
Explanation	This function executes flash memory self-programming.
Arguments	None
Return value	None
Remarks	None

[Function Name] R_MAIN_SelfInitialize

Synopsis	Execute initialization for flash memory self-programming.
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_serial.h r_cg_userdefine.h fsl.h fsl_types.h
Declaration	uint8_t R_MAIN_SelfInitialize(void)
Explanation	This function executes initialization prior to flash memory self-programming.
Arguments	None
Return value	Normal termination: FSL_OK Parameter error: FSL_ERR_PARAMETER Erase error: FSL_ERR_ERASE Internal verify error: FSL_ERR_IVERIFY Write error: FSL_ERR_WRITE Flow error: FSL_ERR_FLOW
Remarks	None

[Function Name] R_MAIN_WriteExecute

Synopsis	Execute flash memory reprogramming.	
Header	r_cg_macrodriver.h r_cg_cgc.h r_cg_port.h r_cg_serial.h r_cg_userdefine.h fsl.h fsl_types.h	
Declaration	uint8_t R_MAIN_WriteExecute(uint32_t WriteAddr)	
Explanation	This function executes flash memory reprogramming.	
Arguments	WriteAddr	Write start address
Return value	Normal termination: FSL_OK Abnormal termination: ERROR	
Remarks	None	

5.10 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

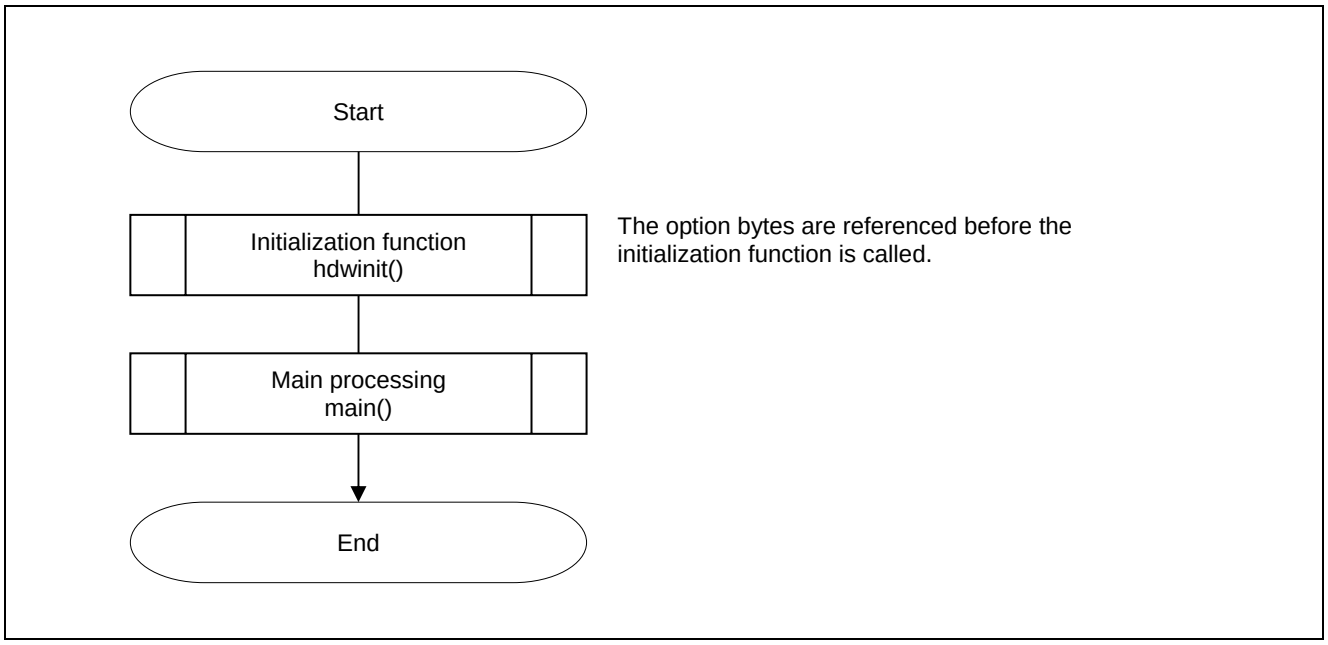

Figure 5.1 Overall Flow

5.10.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

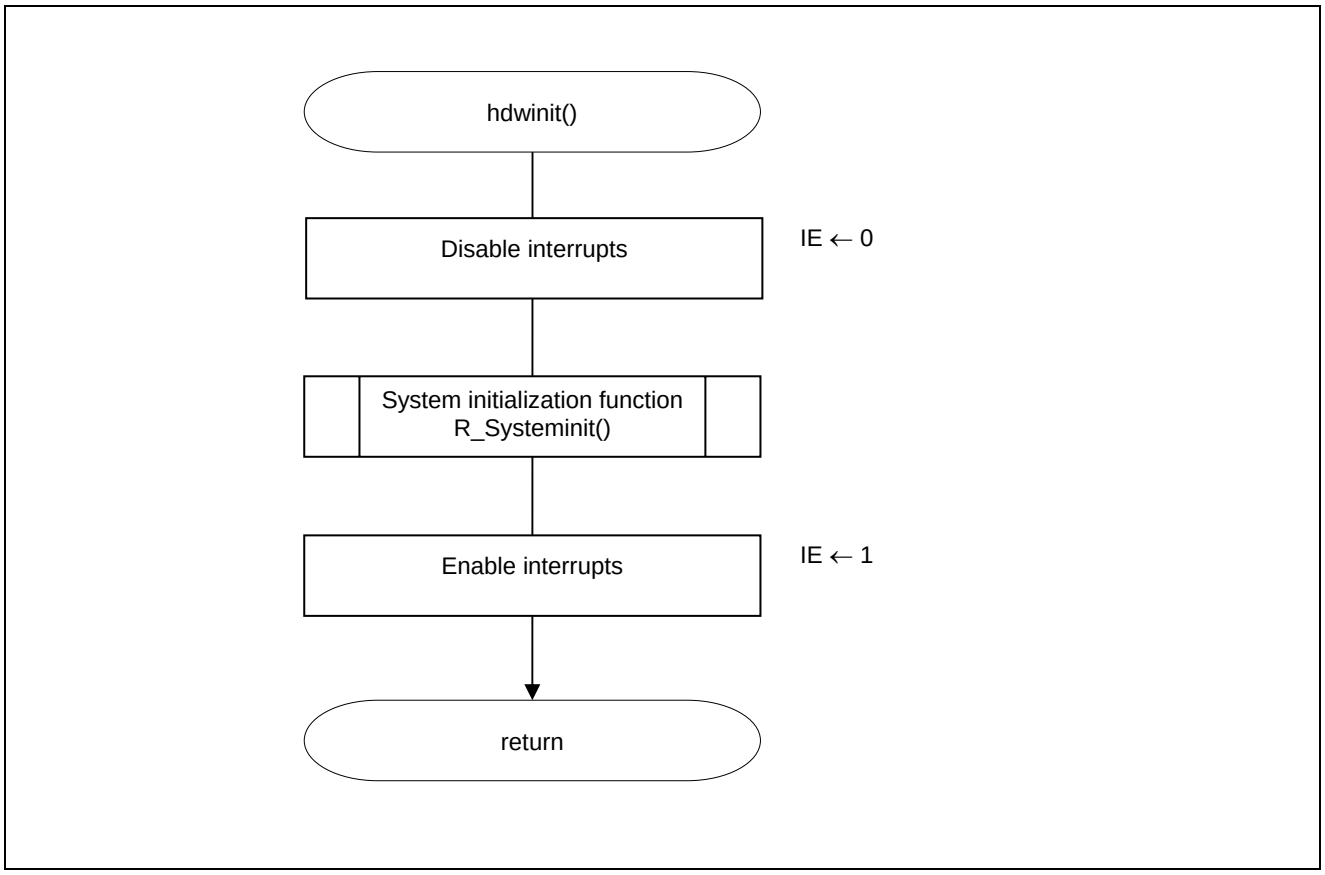

Figure 5.2 Initialization Function

5.10.2 System Initialization Function

Figure 5.3 shows the flowchart for the system initialization function.

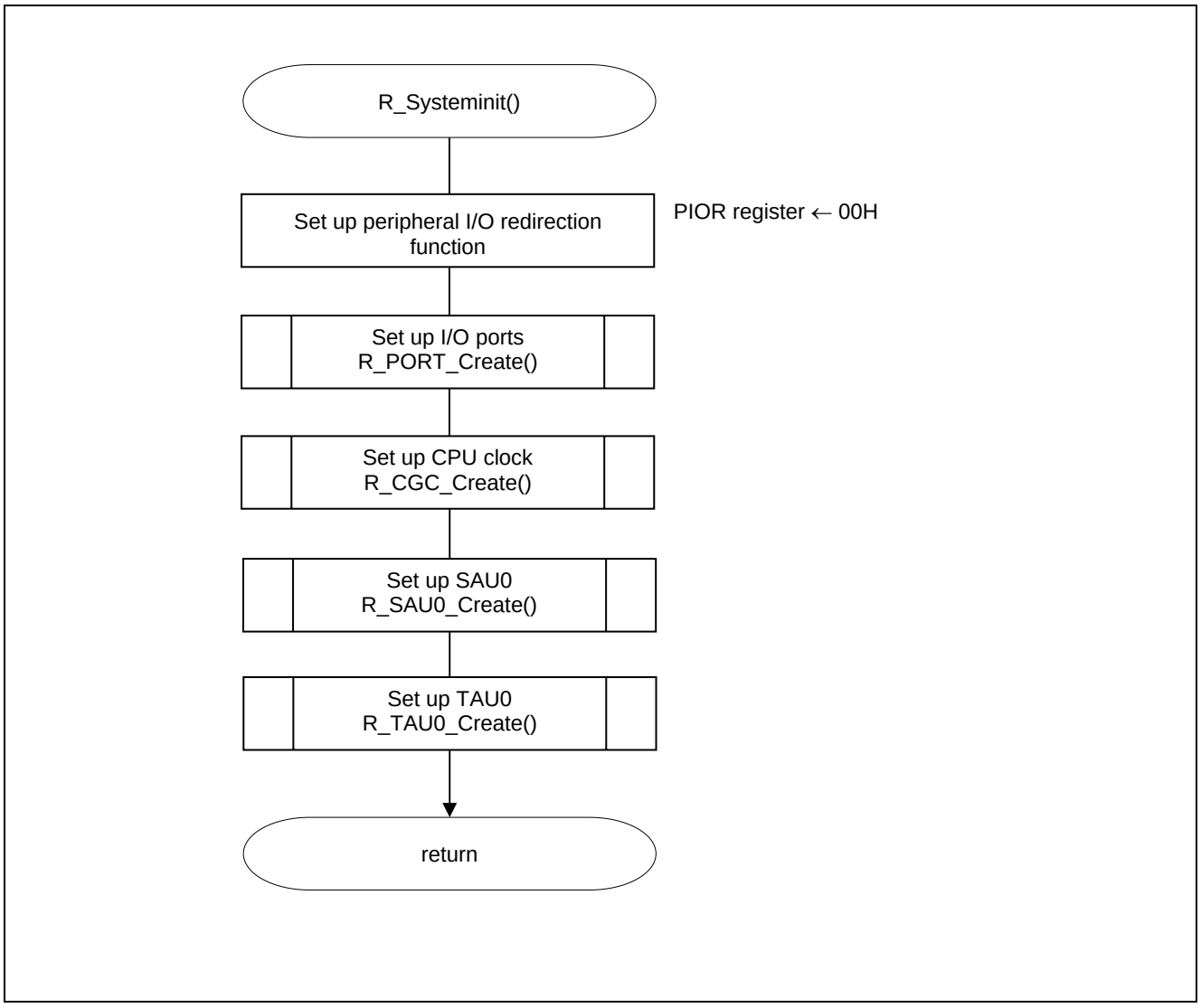

Figure 5.3 System Initialization Function

5.10.3 I/O Port Setup

Figure 5.4 shows the flowchart for I/O port setup.

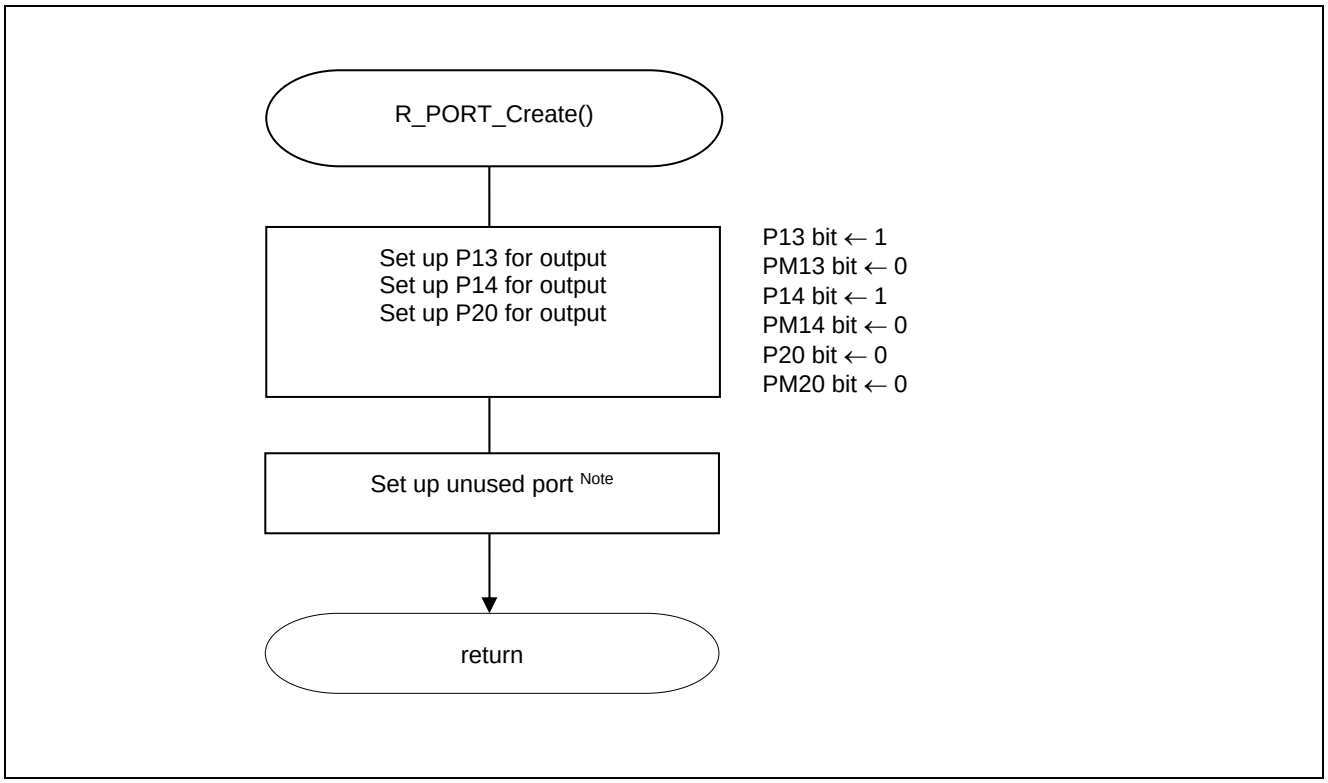

Figure 5.4 I/O Port Setup

Note: Refer to the section entitled "Flowcharts" in RL78/G12 Initialization (R01AN1030E) Application Note for the configuration of the unused ports.

Caution: Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_{DD} or V_{SS} via a separate resistor.

5.10.4 CPU Clock Setup

Figure 5.5 shows the flowchart for CPU clock setup.

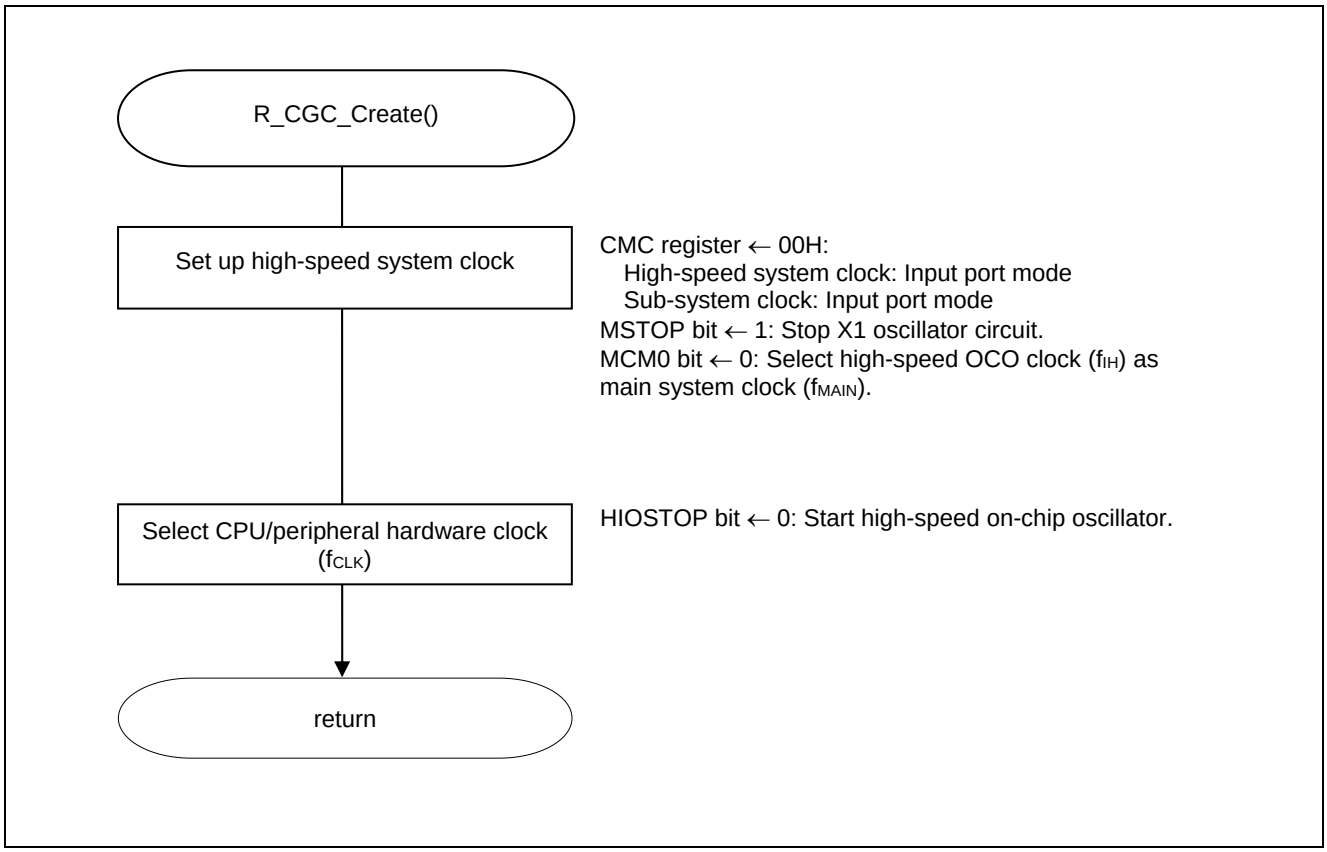

Figure 5.5 CPU Clock Setup

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create ()), refer to the section entitled "Flowcharts" in RL78/G12 Initialization (R01AN1030E) Application Note.

5.10.5 SAU0 Setup

Figure 5.6 shows the flowchart for SAU0 setup.

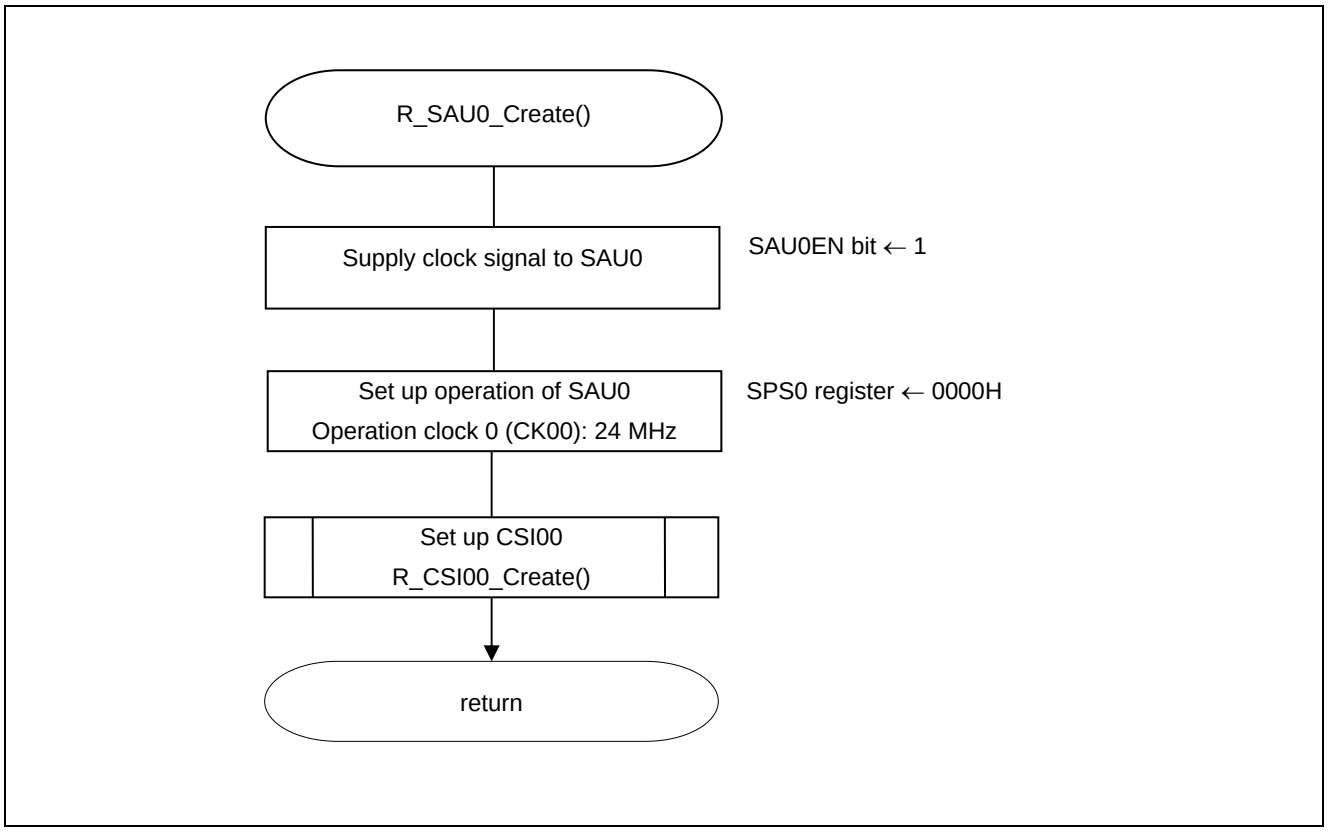

Figure 5.6 SAU0 Setup

5.10.6 CSI00 Setup

Figure 5.7 shows the flowchart for CSI00 setup (1/2). Figure 5.8 shows the flowchart for CSI00 setup (2/2).

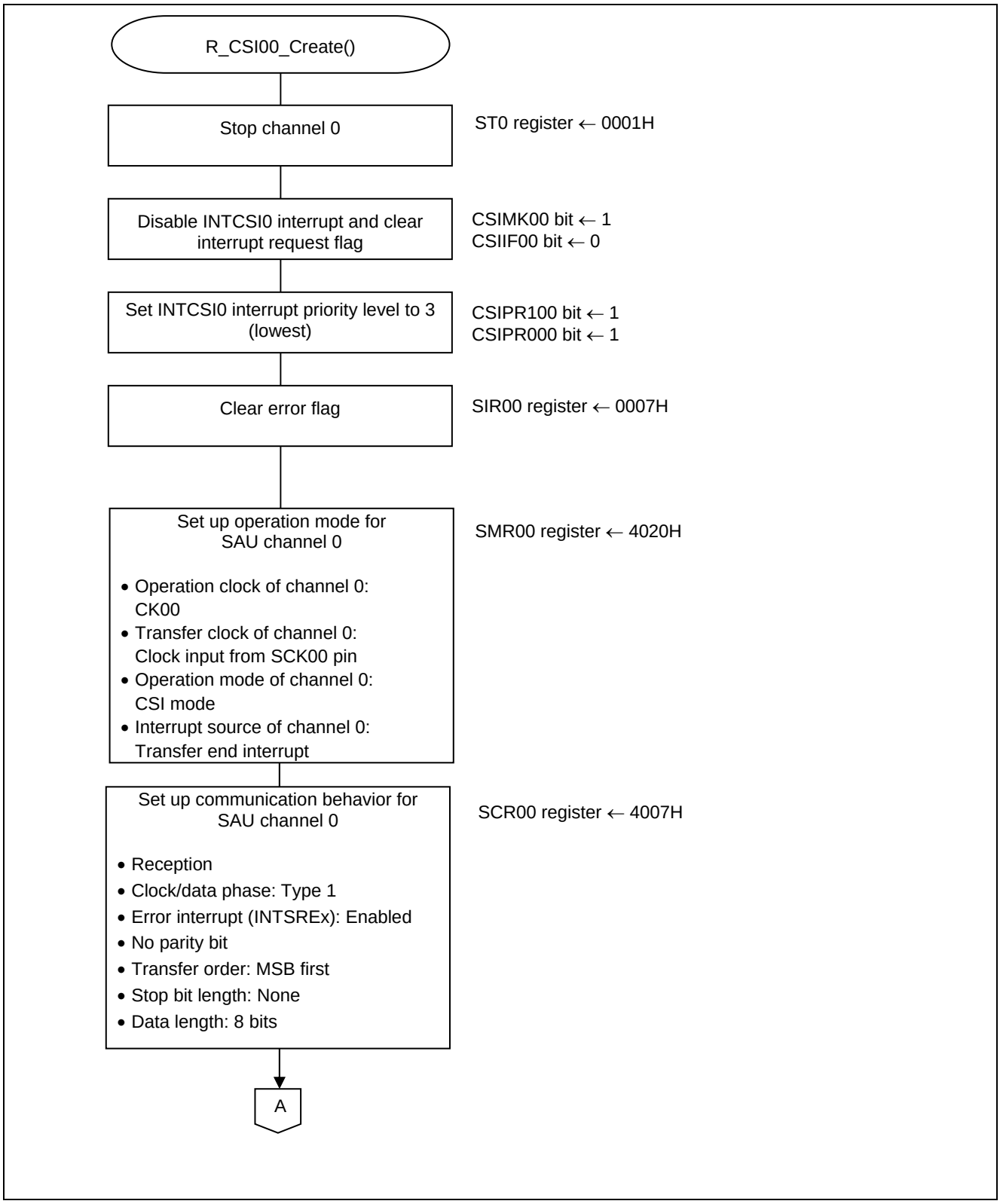

Figure 5.7 CSI00 Setup (1/2)

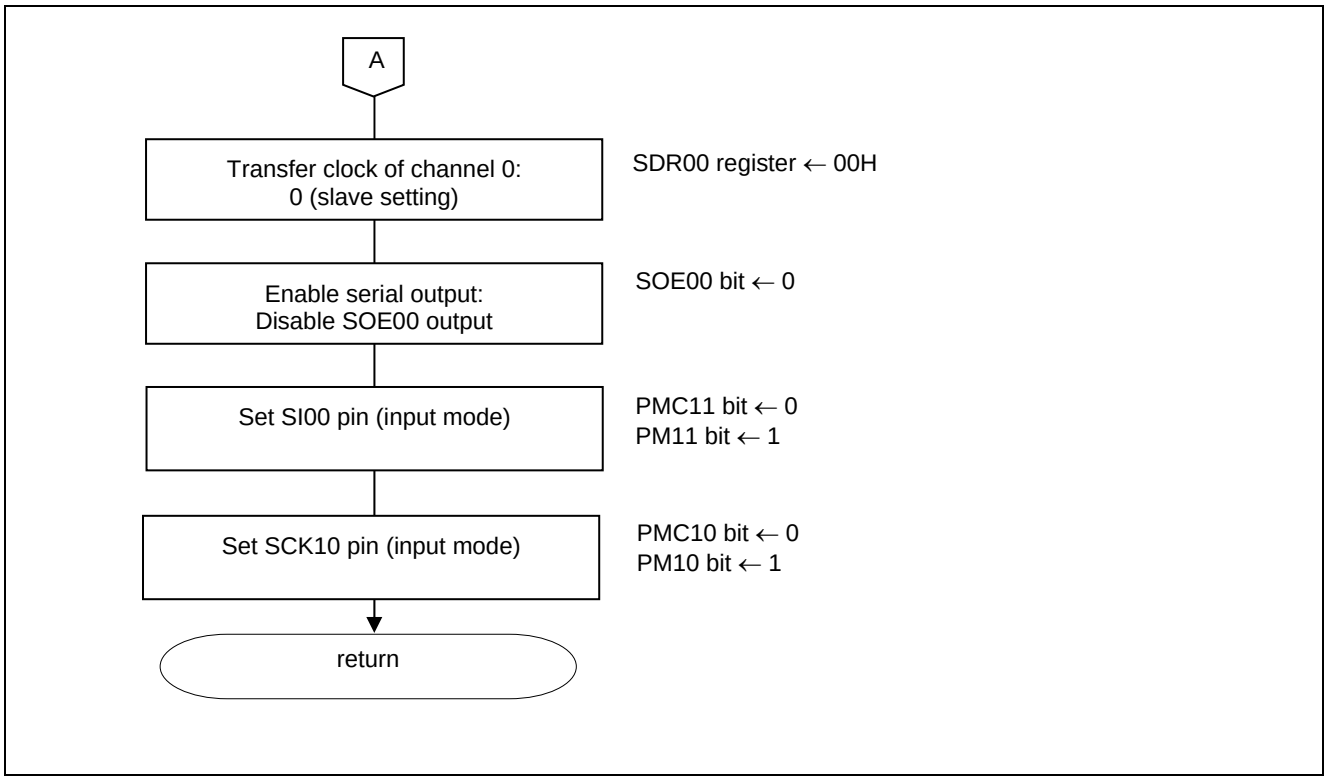

Figure 5.8 CSI00 Setup (2/2)

5.10.7 TAU0 Setup

Figure 5.9 shows the flowchart for TAU0 setup.

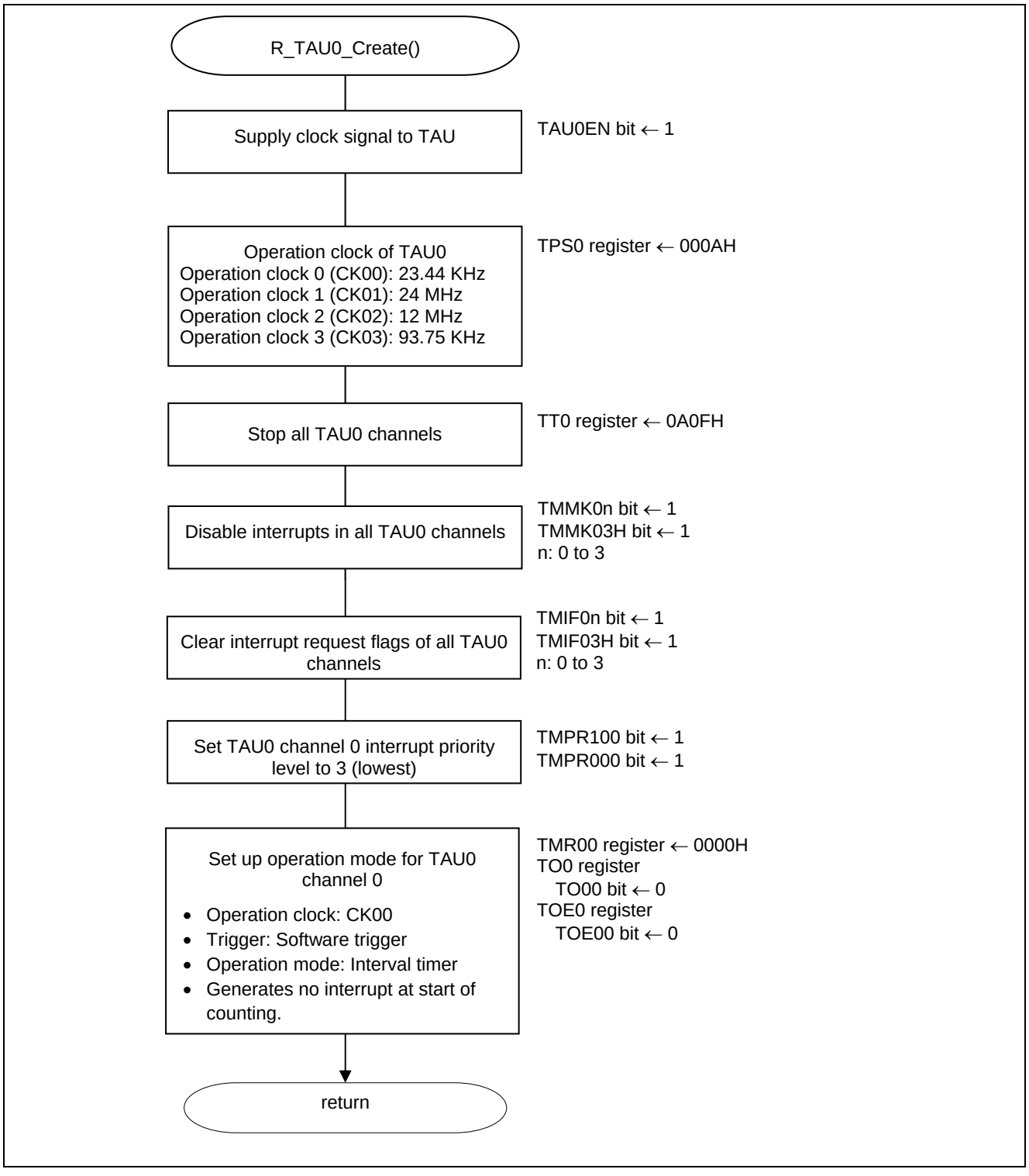

Figure 5.9 TAU0 Setup

5.10.8 Main Processing

Figure 5.10 shows the flowchart for main processing (1/2). Figure 5.11 shows the flowchart for main processing (2/2).

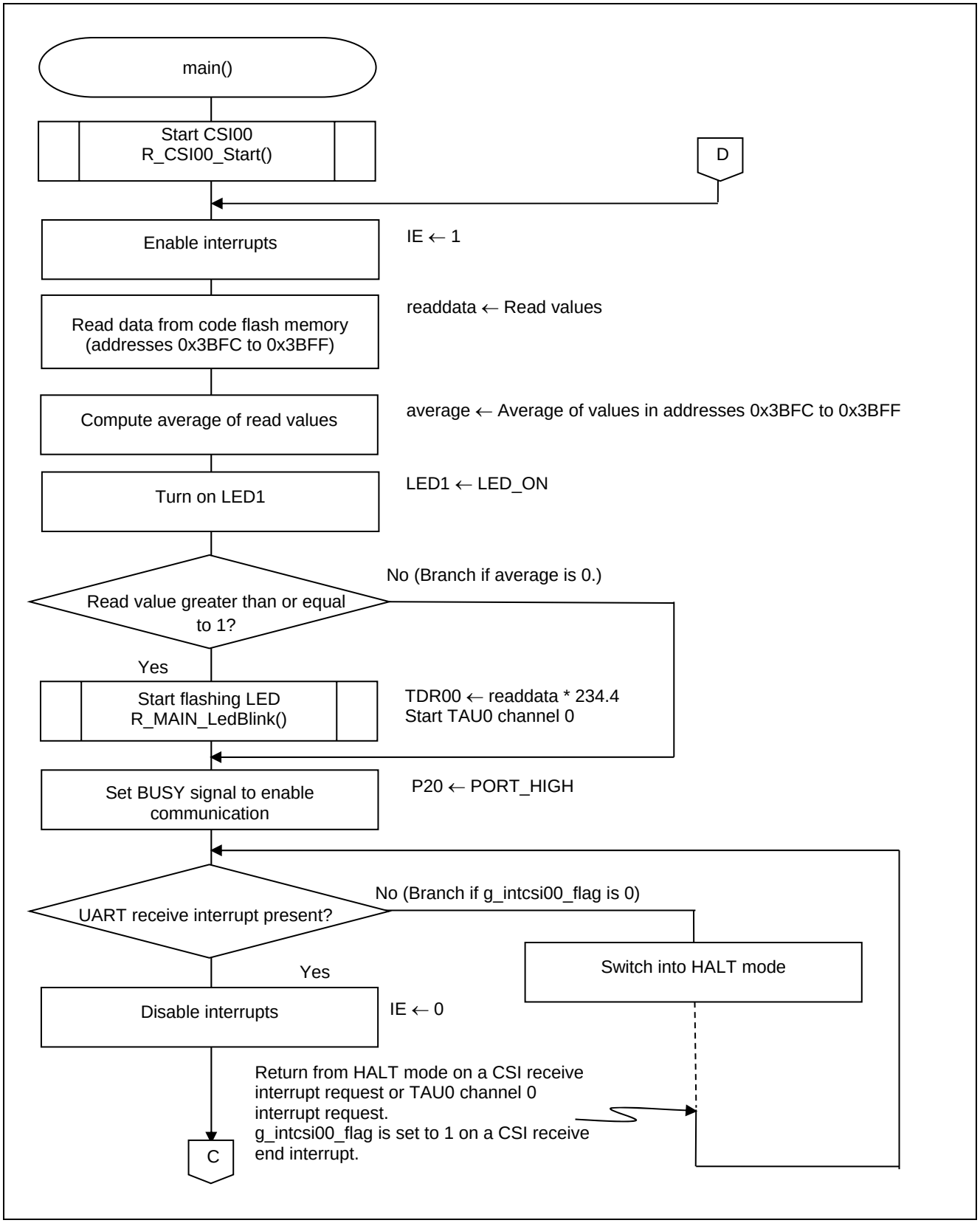

Figure 5.9 Main Processing (1/2)

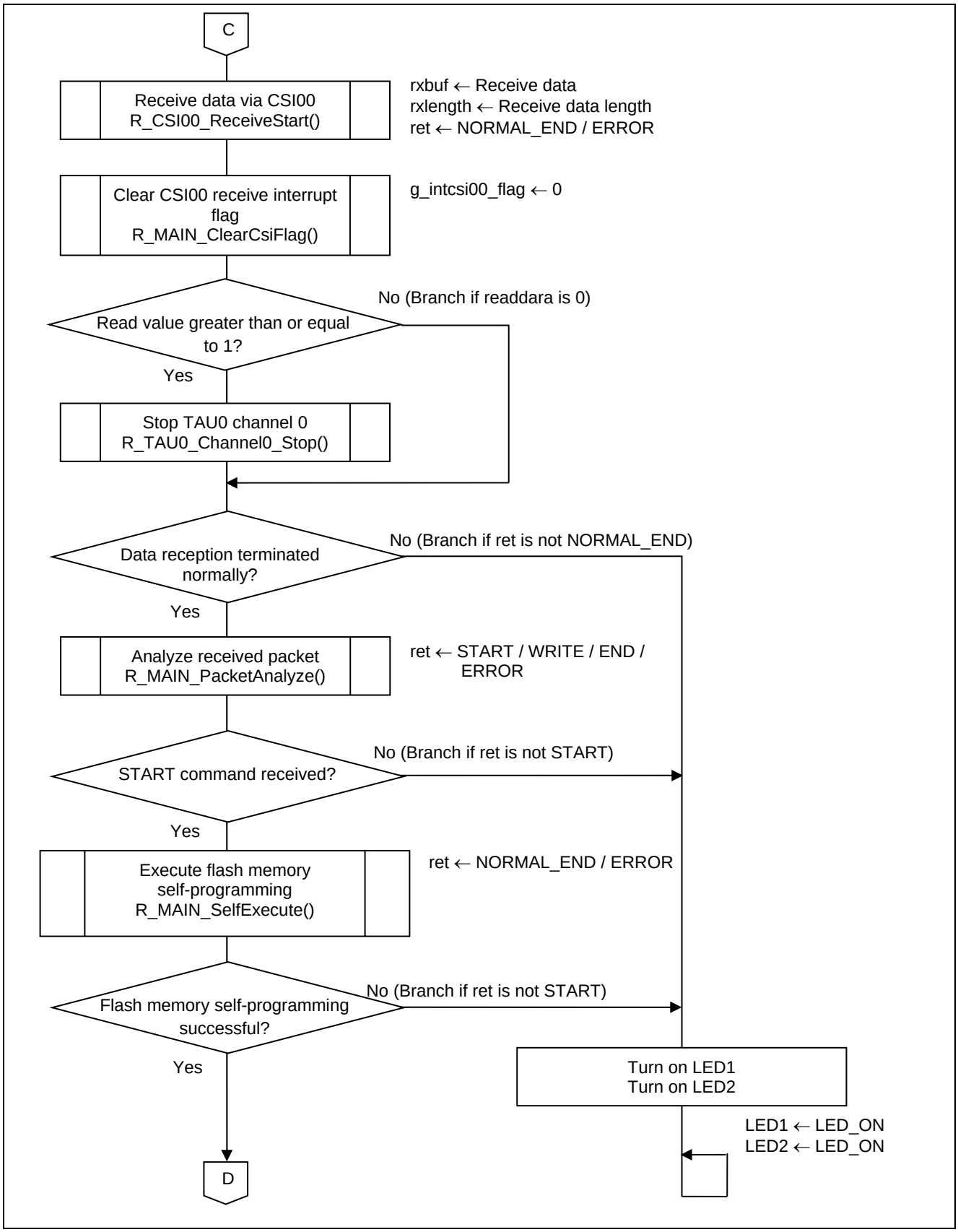

Figure 5.11 Main Processing (2/2)

5.10.9 Starting the CSI00

Figure 5.12 shows the flowchart for starting the CSI00.

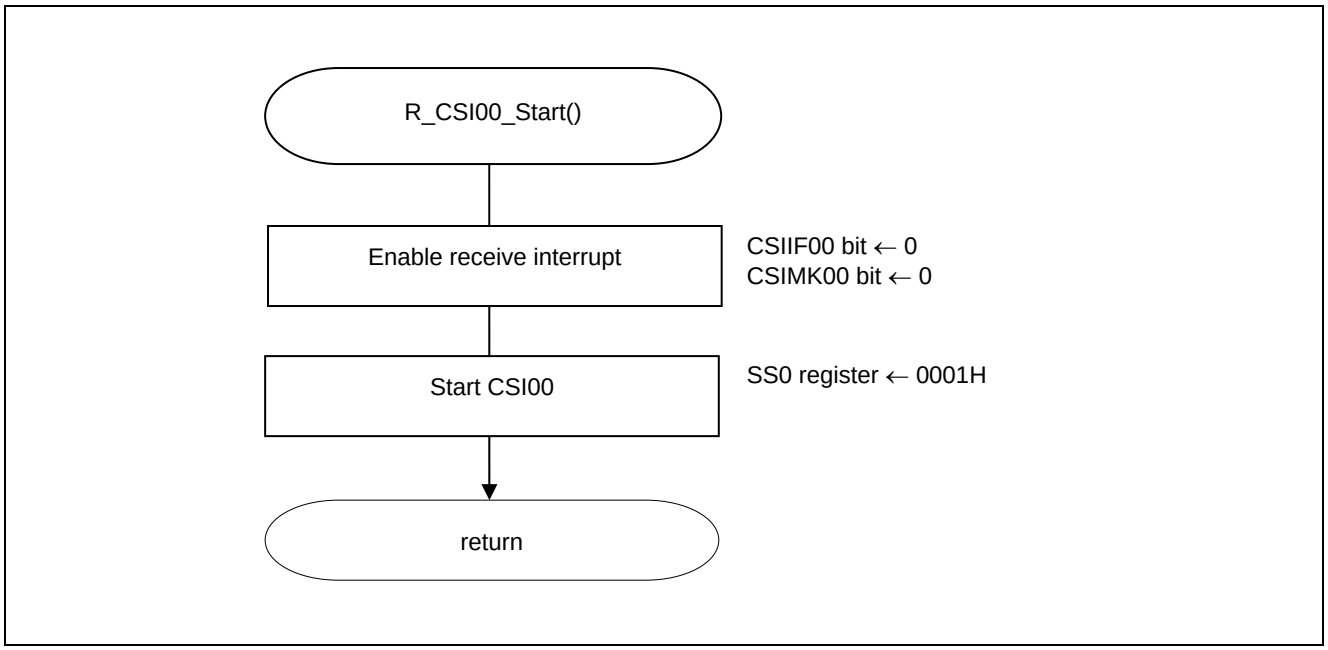

Figure 5.12 Starting the CSI00

5.10.10 CSI00 Receive End Interrupt

Figure 5.13 shows the flowchart for CSI00 receive end interrupt.

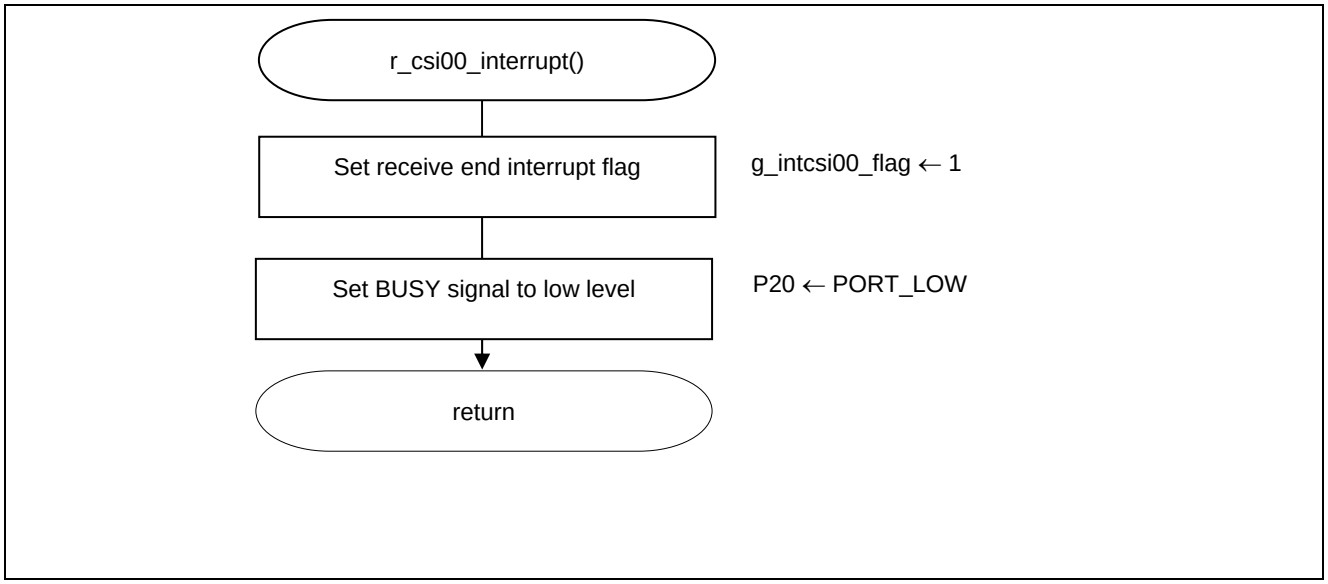

Figure 5.13 CSI00 Receive End Interrupt

5.10.11 Starting to Flash the LED

Figure 5.14 shows the flowchart for starting to flash the LED.

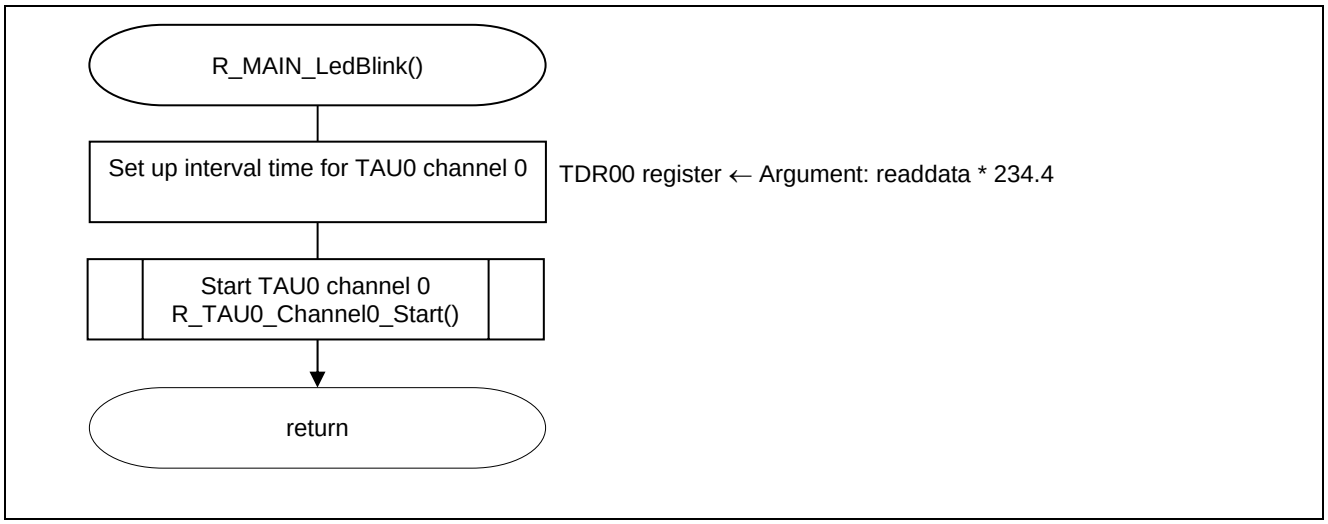

Figure 5.14 Starting to Flash the LED Flash

5.10.12 Starting the TAU0 Channel 0

Figure 5.15 shows the flowchart for starting the TAU0 channel 0.

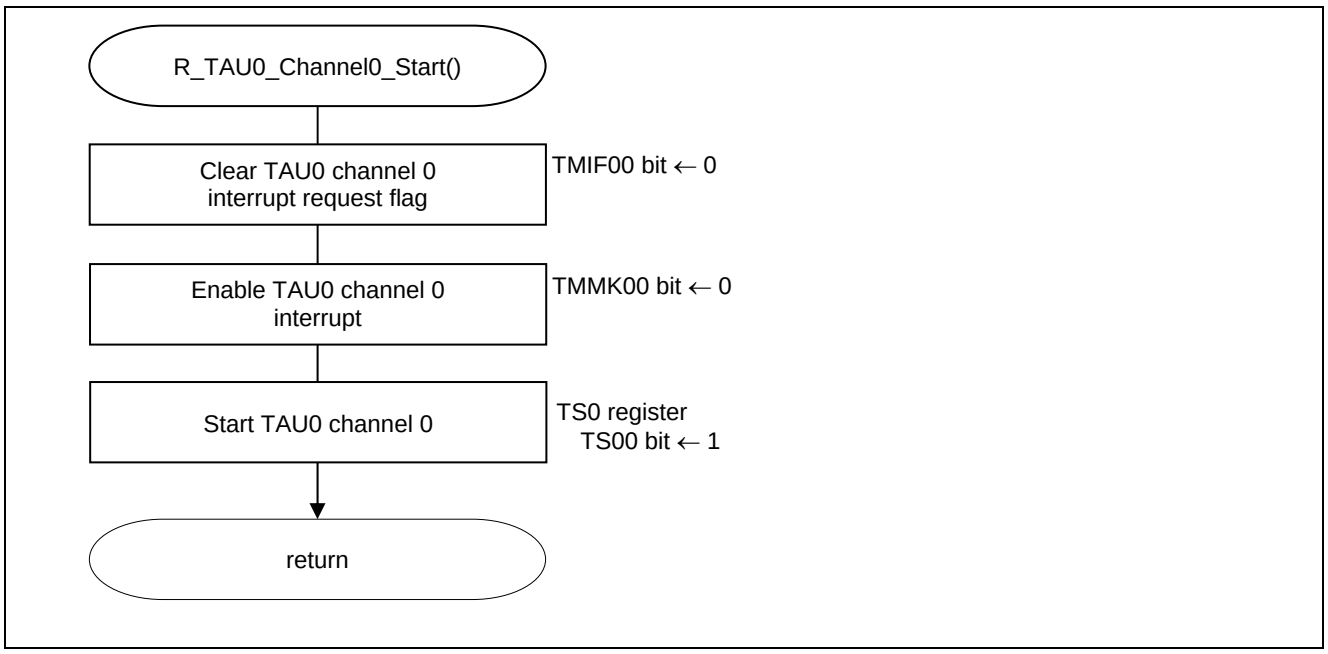

Figure 5.15 Starting the TAU0 Channel 0

5.10.13 TAU0 Channel 0 Interrupt

Figure 5.16 shows the flowchart for TAU0 channel 0 interrupt.

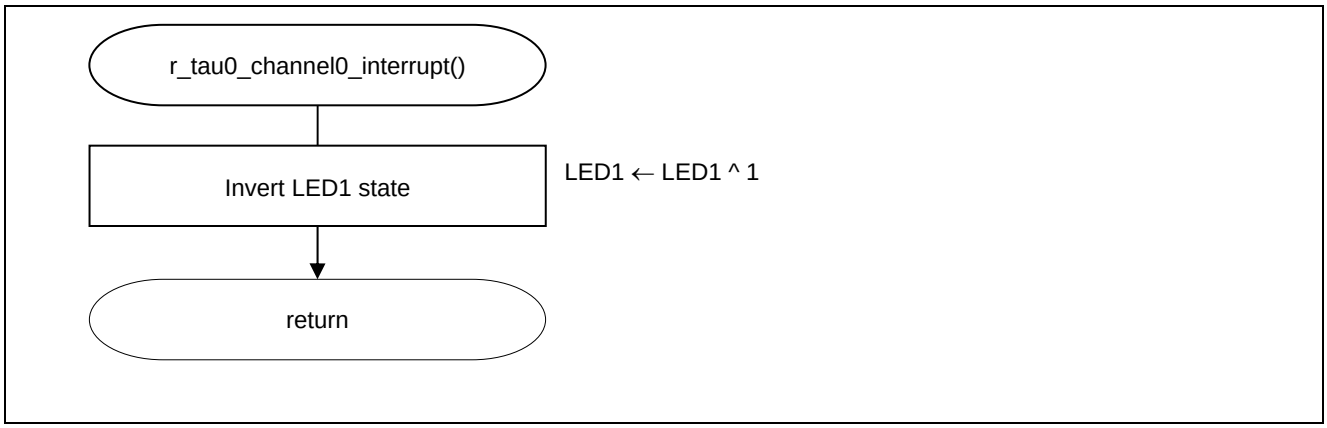

Figure 5.16 TAU0 Channel 0 Interrupt

5.10.14 Data Reception via CSI00

Figure 5.17 shows the flowchart for data reception via the CSI00 (1/2). Figure 5.18 shows the flowchart for data reception via the CSI00 (2/2).

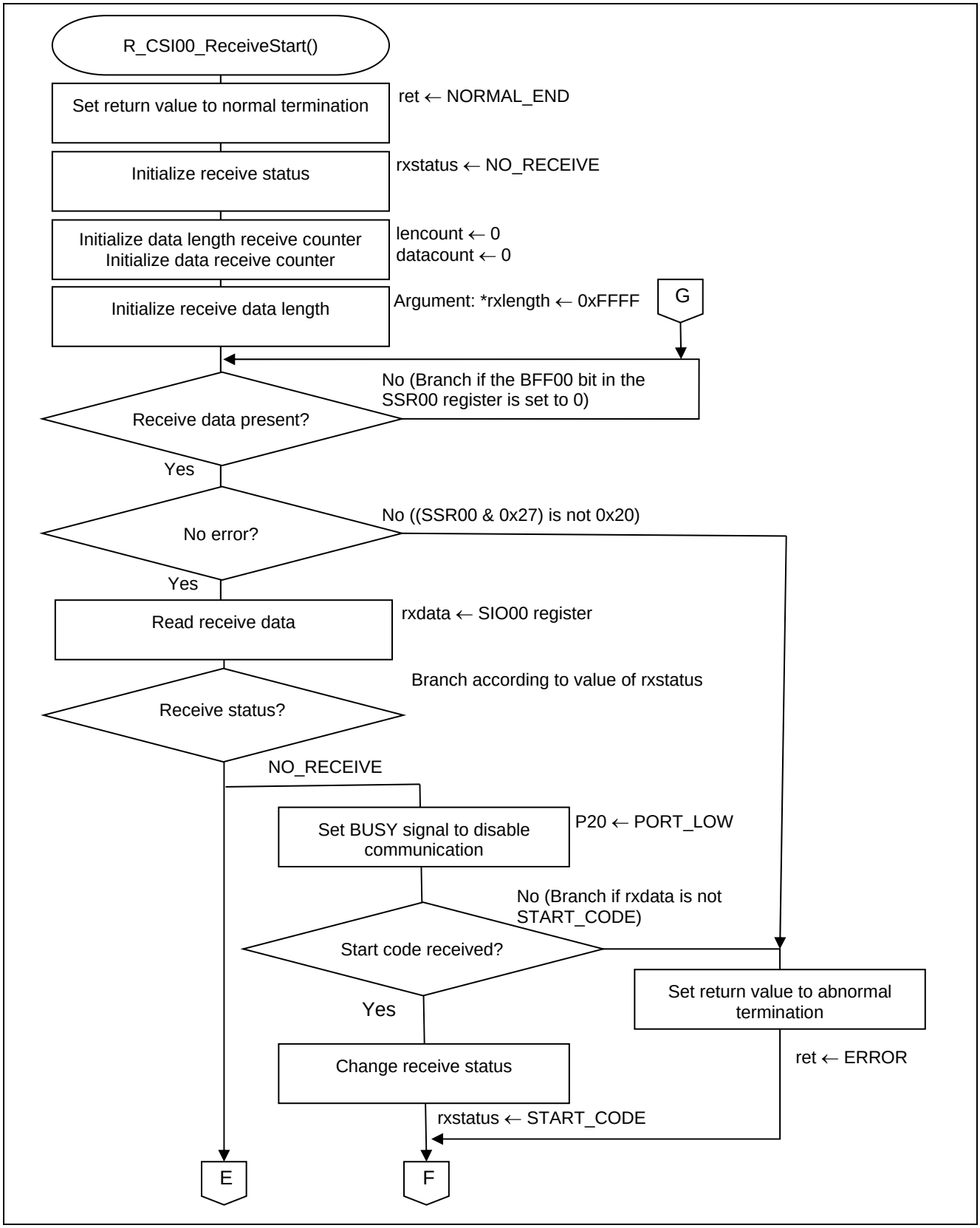

Figure 5.17 Data Reception via CSI00 (1/2)

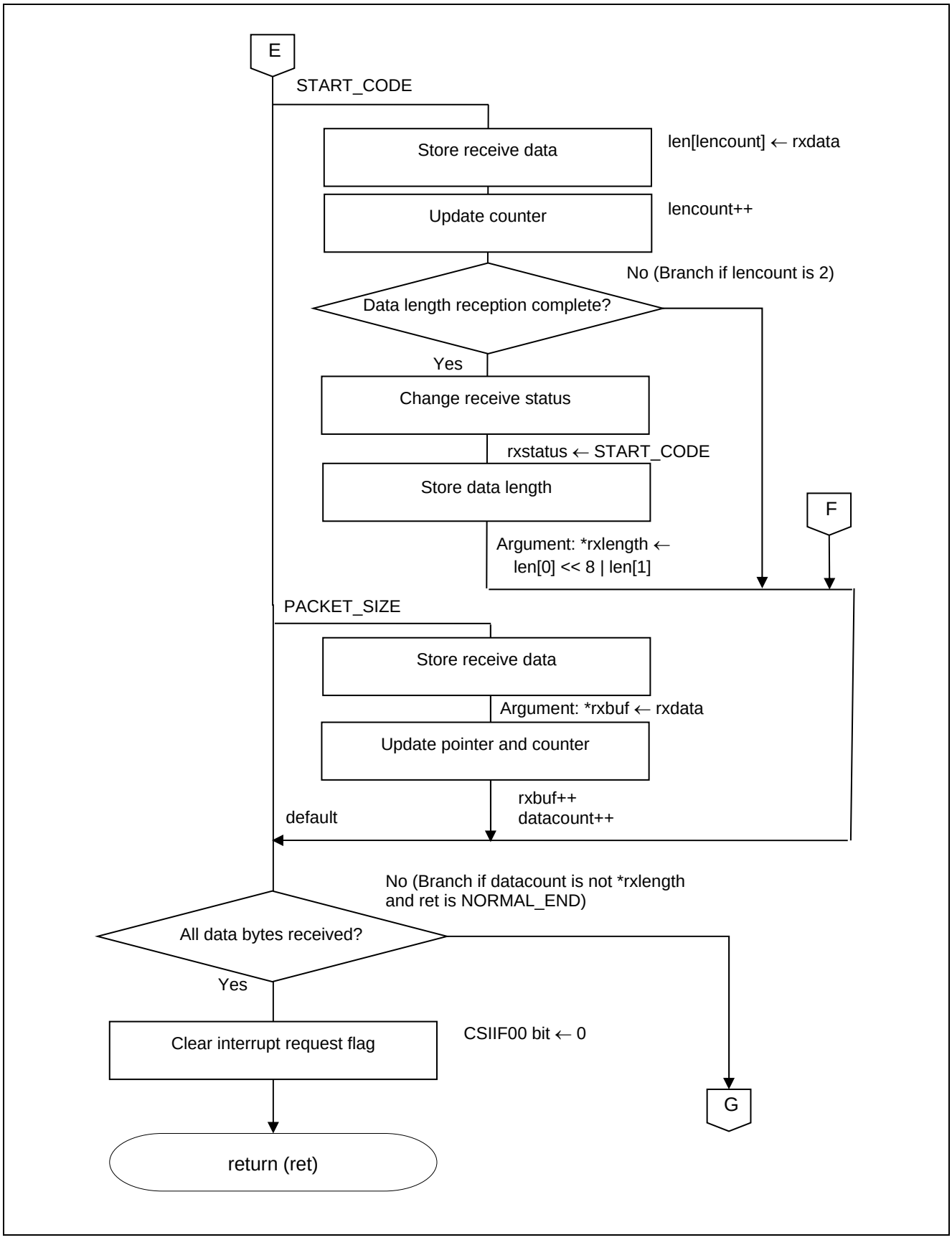

Figure 5.18 Data Reception via CSI00 (2/2)

5.10.15 Clearing the CSI00 Transfer End Interrupt Flag

Figure 5.19 shows the flowchart for clearing the CSI00 transfer end interrupt flag.

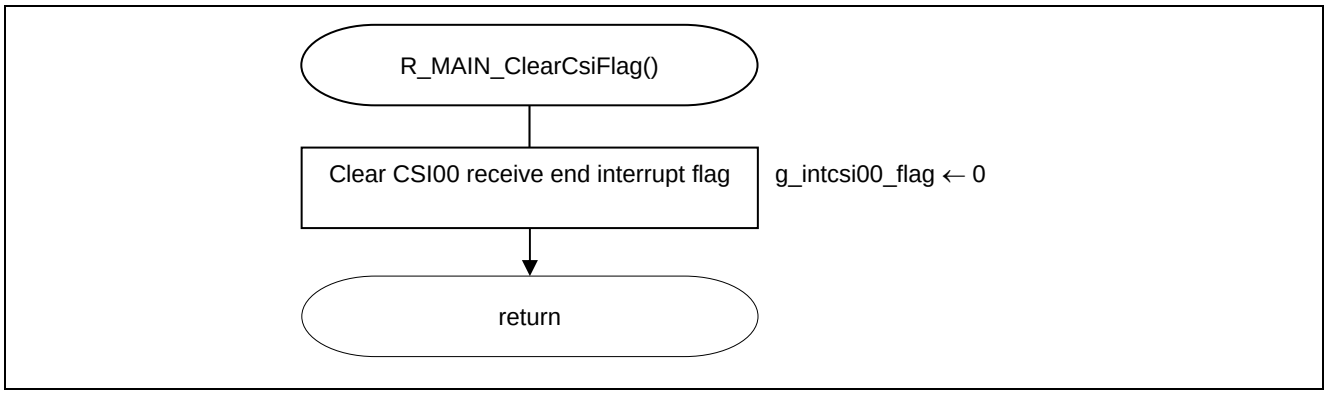

Figure 5.19 Clearing the CSI00 Transfer End Interrupt Flag

5.10.16 Stopping the TAU0 Channel 0

Figure 5.20 shows the flowchart for stopping the TAU0 channel 0.

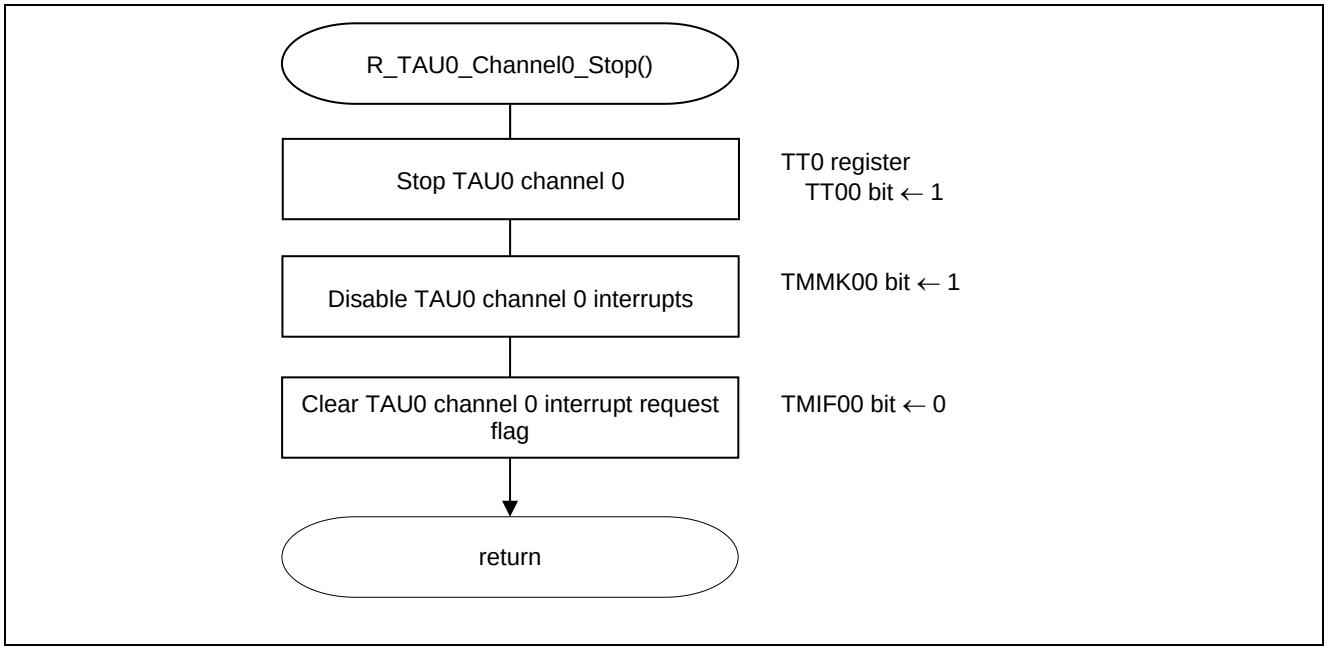

Figure 5.20 Stopping the TAU0 Channel 0

5.10.17 Receive Packet Analysis

Figure 5.21 shows the flowchart for receive packet analysis.

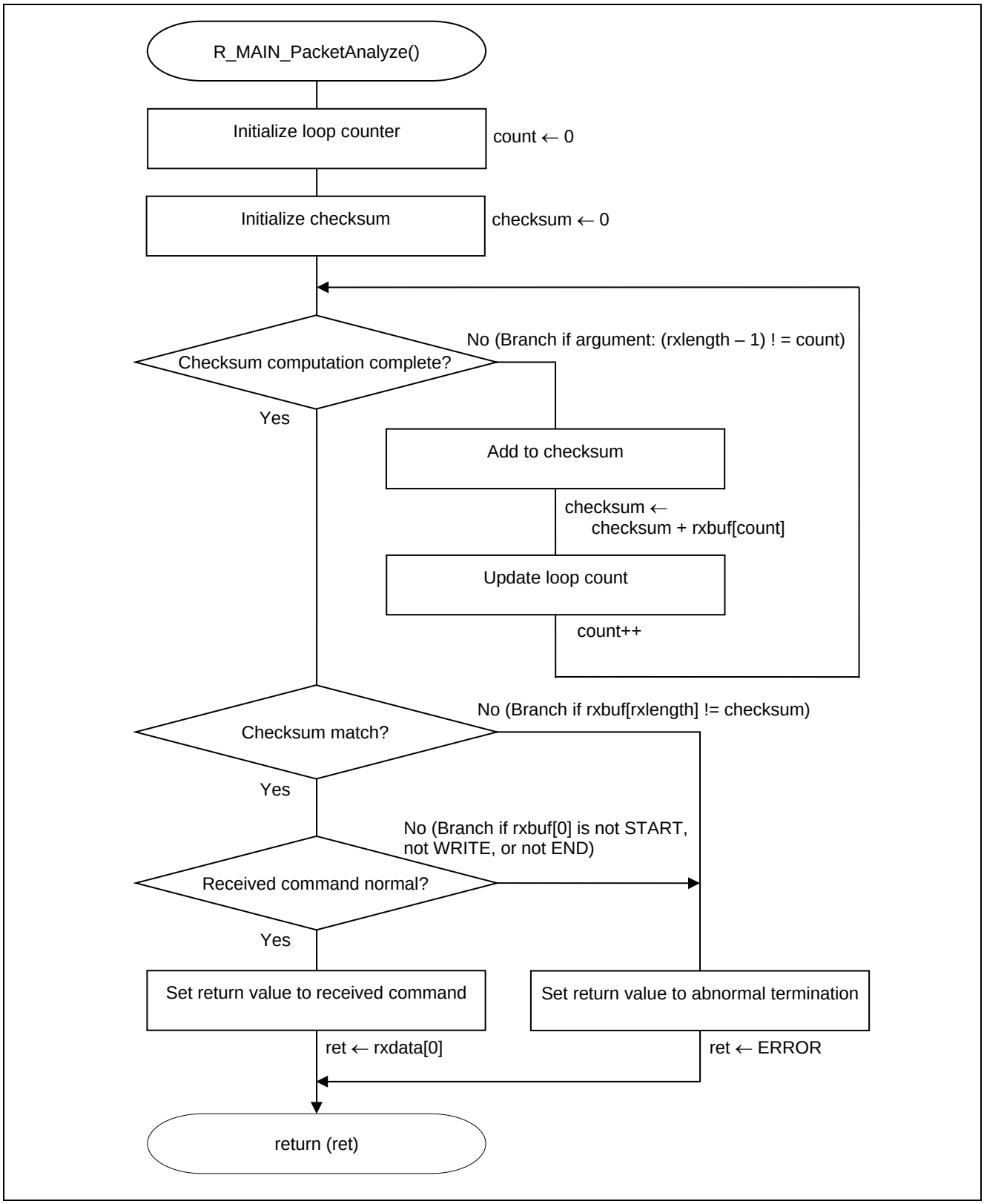

Figure 5.21 Receive Packet Analysis

5.10.18 Flash Memory Self-Programming Execution

Figure 5.22 shows the flowchart for flash memory self-programming execution.

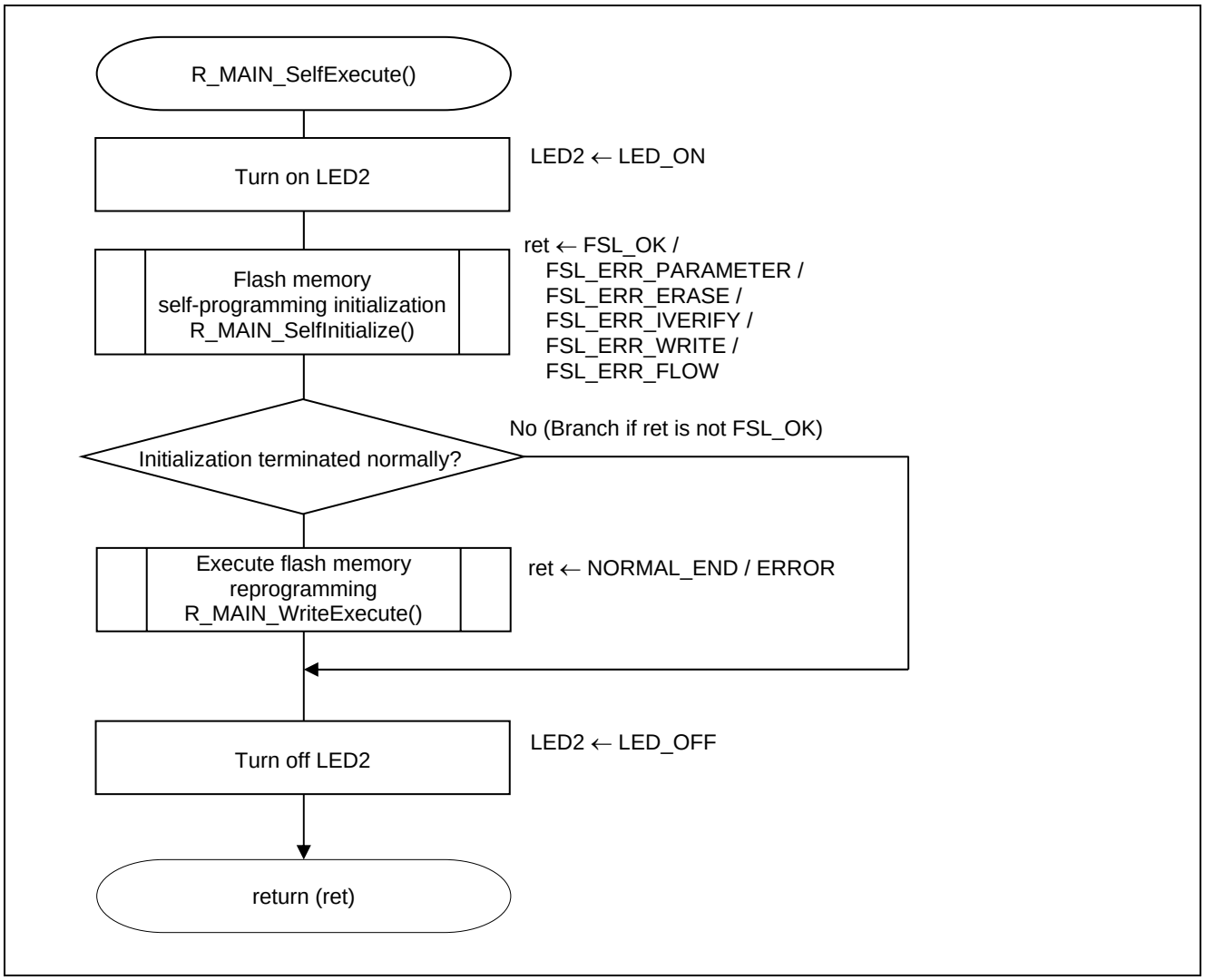

Figure 5.22 Flash Memory Self-Programming Execution

5.10.19 Flash Memory Self-Programming Initialization

Figure 5.23 shows the flowchart for flash memory self-programming initialization.

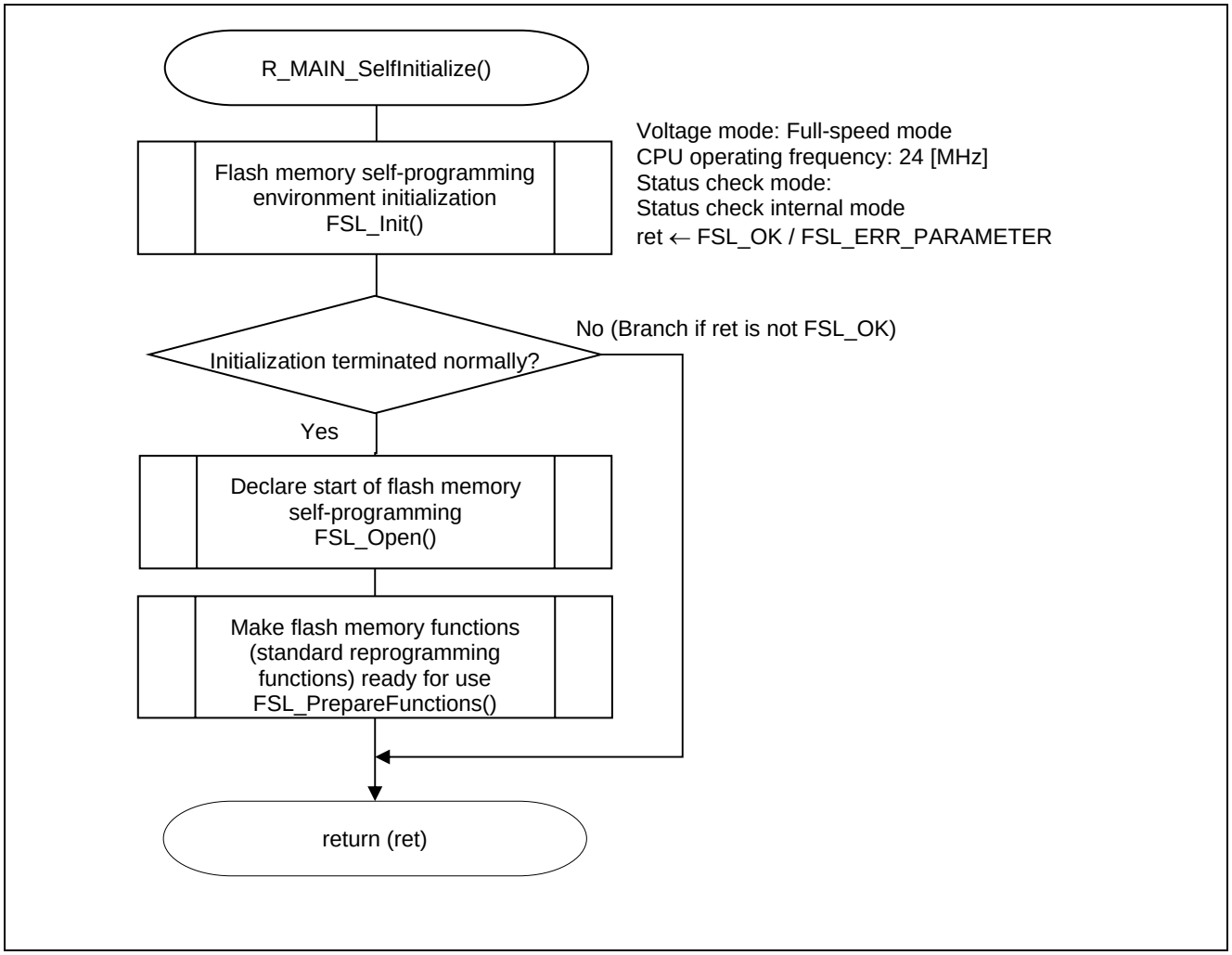

Figure 5.23 Flash Memory Self-Programming Initialization

5.10.20 Flash Memory Reprogramming Execution

Figure 5.24 shows the flowchart for flash memory reprogramming execution (1/3). Figure 5.25 shows the flowchart for flash memory reprogramming execution (2/3). Figure 5.26 shows the flowchart for flash memory reprogramming execution (3/3).

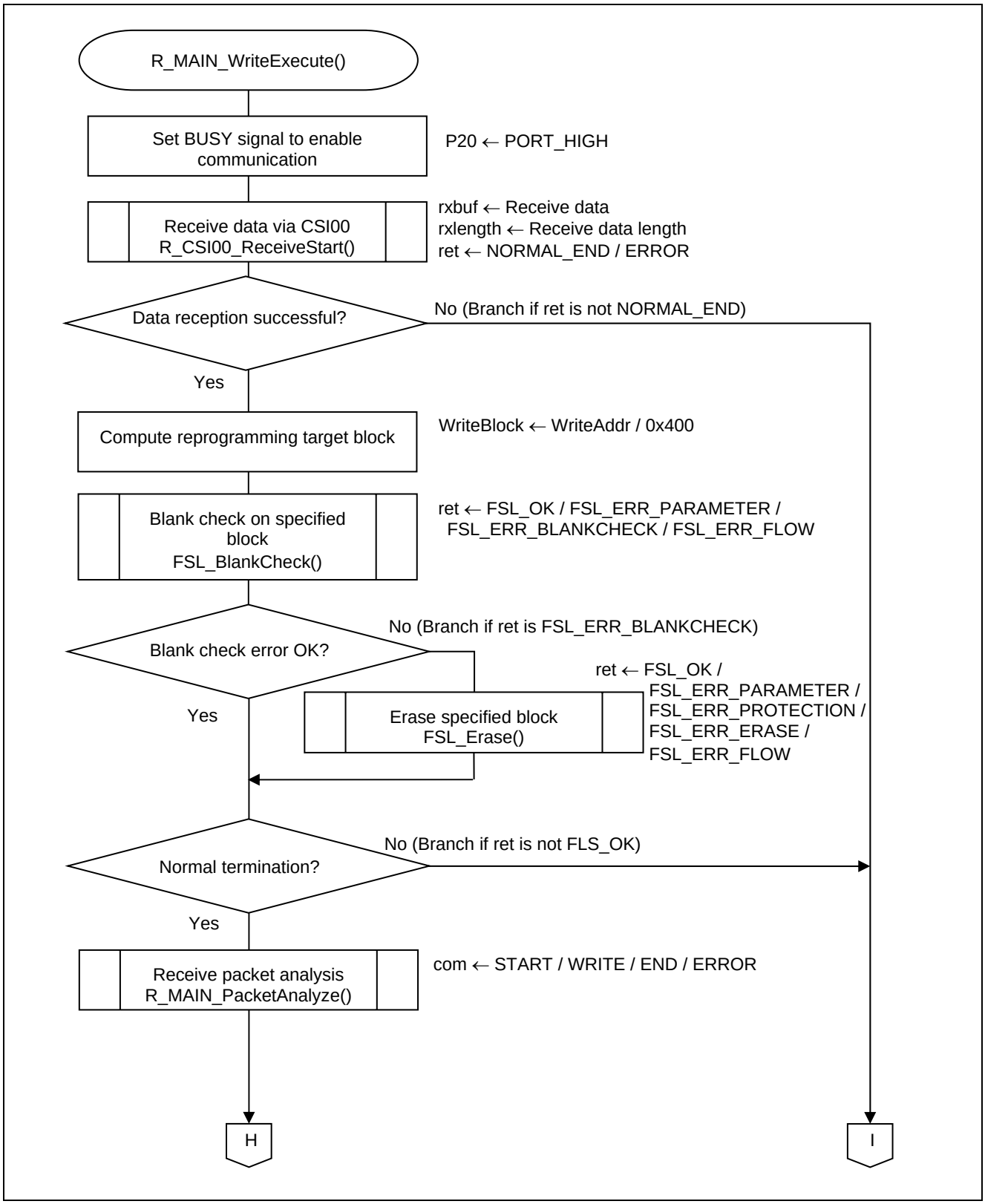

Figure 5.24 Flash Memory Reprogramming Execution (1/3)

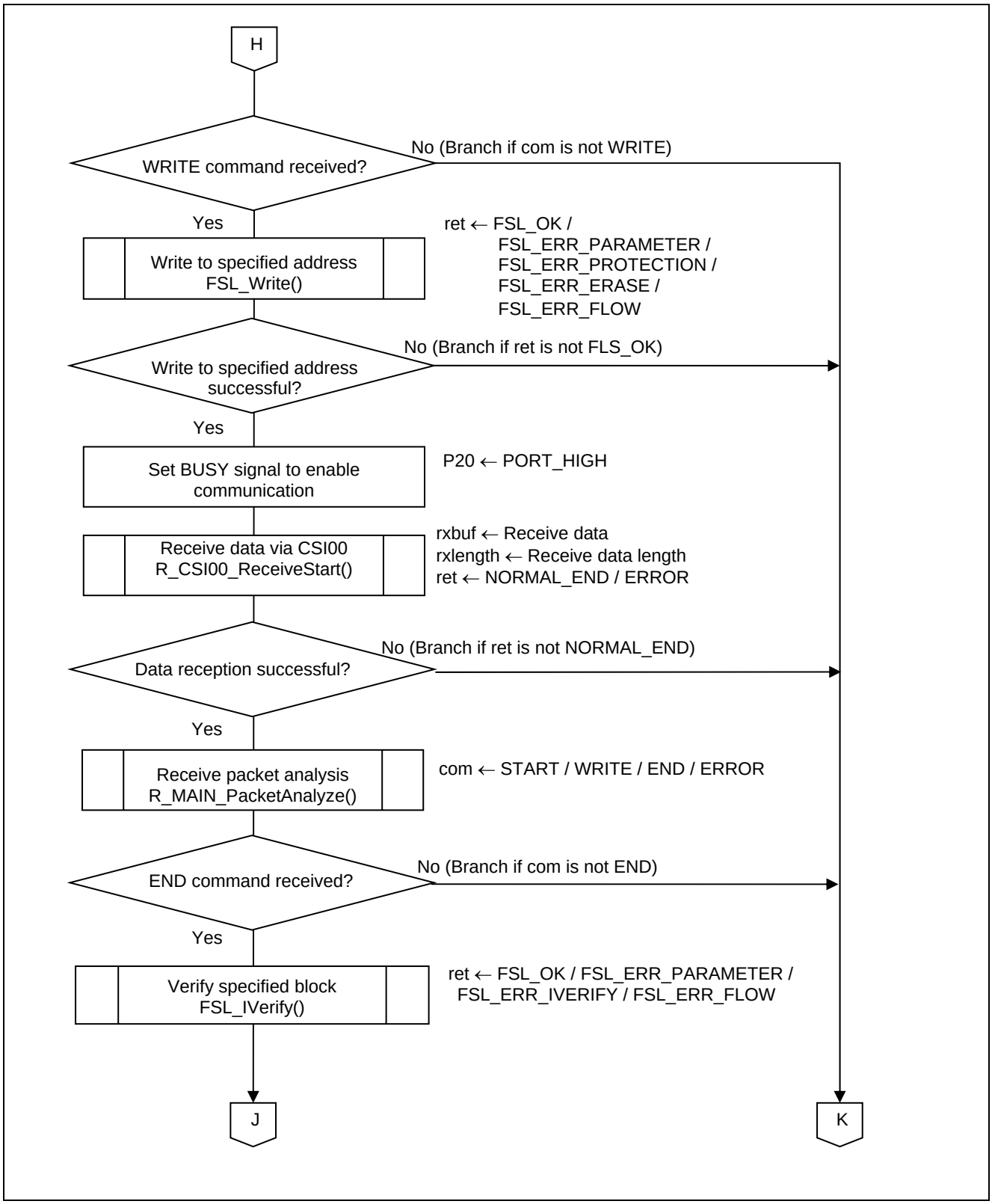

Figure 5.25 Flash Memory Reprogramming Execution (2/3)

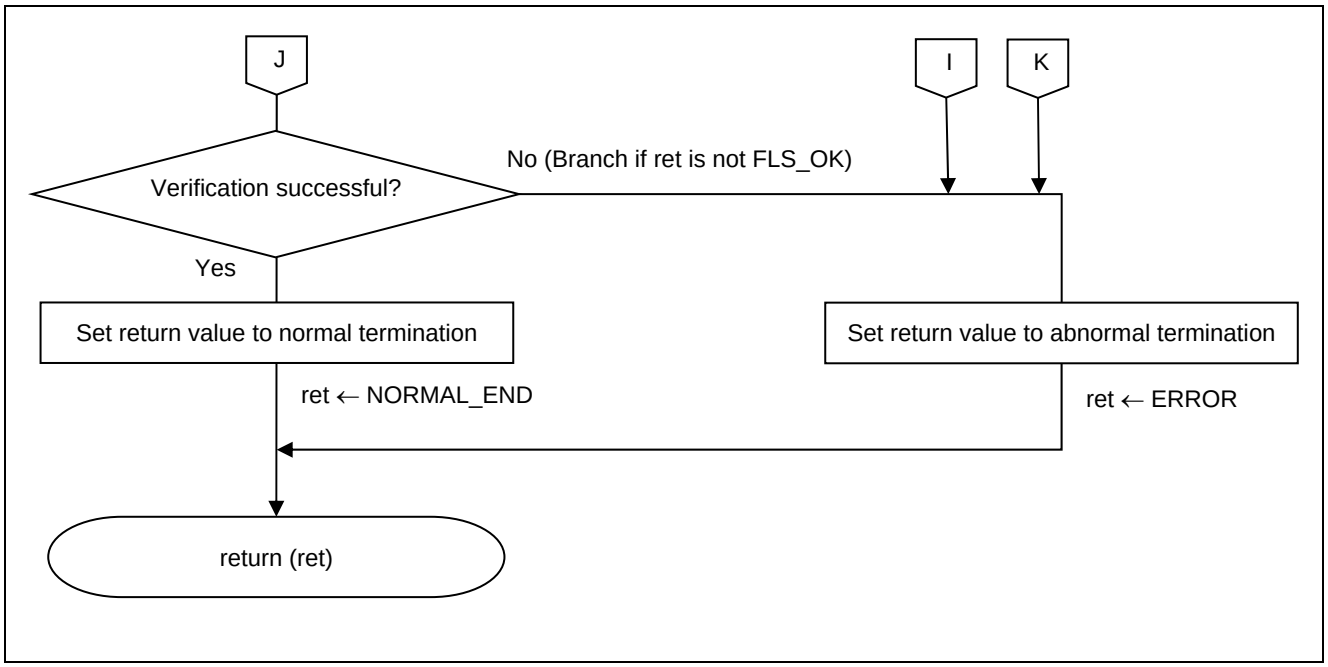

Figure 5.26 Flash Memory Reprogramming Execution (3/3)

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G12 User's Manual: Hardware (R01UH0200E)

RL78 Family User's Manual: Software (R01US0015E)

RL78 family’s Flash Self Programming Library Type01 User’s Manual (R01US0050E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

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Revision Record	RL78/G12 Self-Programming (CSI)

Rev.	Date	Description	
		Page	Summary
1.00	Mar.01, 2013	—	First edition issued
1.01	Feb.17, 2015	—	Elimination of the flash shield window function
1.10	June 01, 2016	8	Modification of 1.4 How to Get the Flash Memory Self-Programming Library.
		48	Addition of Documents for Reference.

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   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

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   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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