RL78/G10

Two-Phase Encoding Software Control CC-RL

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Introduction

This application note explains how to detect a phase difference in external input signals with RL78/G10 software using the pulse-width measurement function of the timer array unit (TAU).

Target Device

RL78/10 (R5F10Y16ASP)

When using this application note for other microcomputers, please modify it according to the corresponding specification and evaluate thoroughly before use.

Contents

1. Specifications

This application uses the pulse-width measurement function of the timer array unit (TAU) to detect a phase difference in the external input signals and count up or down

Table 1.1 shows the peripheral function and corresponding usage, and Figure 1.1 shows an operational overview of the pulse-width measurement function.

Table 1.1 Peripheral Functions and Corresponding Usage

Peripheral Function	Usage
Timer array unit	Pulse-width measurement function

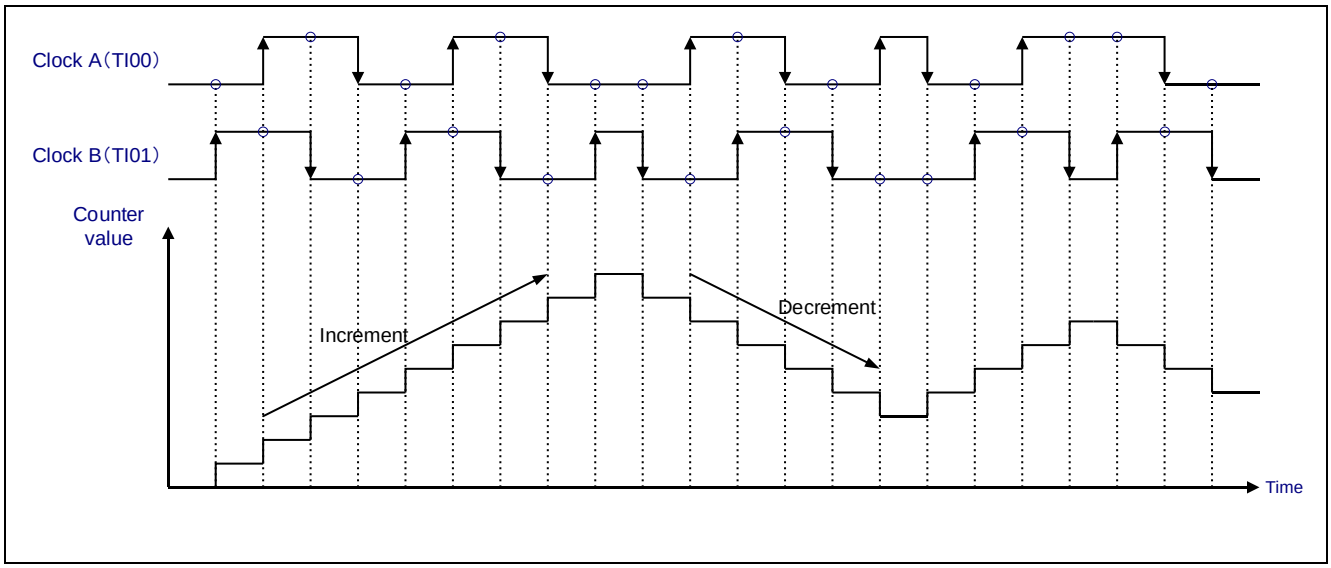

Figure 1.1 Operational Overview

2. Operating Conditions

The sample code in this application note runs under the following operating conditions.

Table 2.1 Operating Conditions

Item	Description/Specification
MCU used	RL78/G10 (R5F10Y16ASP)
Operating frequency	・High-speed on-chip oscillator clock (HOCO): 20MHz ・CPU/peripheral hardware clock: 20MHz
Operating voltage	3.0V SPOR detection voltage When power supply falls: TYP. 2.84V (2.70V to 2.96V) When power supply rises: TYP. 2.90V (2.76V to 3.02V)
Integrated development environment(CS+)	CS+ E3.01.00G (manufactured by Renesas Electronics)
Assembler(CS+)	CC-RL V1.00.00.03 (manufactured by Renesas Electronics)
Integrated development environment(e2studio)	e2studio V4.1.0.018G (manufactured by Renesas Electronics)
Assembler(e2studio)	CC-RL V4.0.0.2 (manufactured by Renesas Electronics)
Ports used	RL78/G10 target board (QB-R5F10Y16-TB)

3. Related Application Notes

Application notes related to this document are shown below. Please refer to these as needed.

RL78/G10 Initialization (R01AN0454E) Application Note

4. Hardware Explanation

4.1 Hardware Configuration Example

Figure 4.1 shows the hardware configuration example used in this application note.

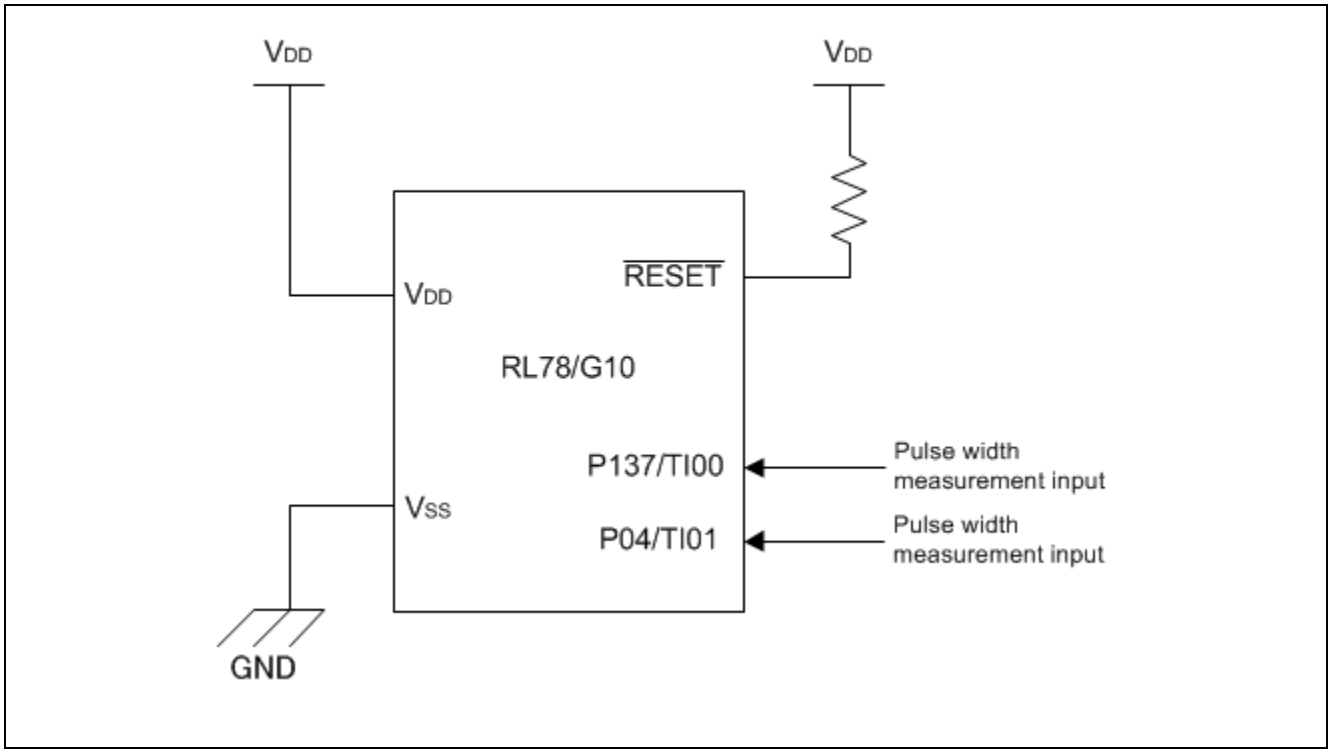

Figure 4.1 Hardware Configuration Example

Note: 1.This simplified circuit diagram was created to show an overview of connections only. When designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements. (Connect each input-only port to V_{DD} or V_{SS} through a resistor.)
2. Make V_{DD} higher than the RESET release voltage (V_{SPOR}) set in SPOR.

4.2 Pin List

Table 4.1 provides a list of the pins used in this document and their functions.

Table 4.1 List of Pins and Functions

Pin Name	Input/Output	Function
P137/TI00	Input	Clock A
P04/TI01	Input	Clock B

5. Software Explanation

5.1 Operation Outline

This application note explains how to use the TAU pulse-width measurement function to detect a phase difference between external input signals from pins T100 and T101, and then count up or down, correspondingly.

The timer array unit should be set as follows:

Setting conditions

- The TAU is used in the pulse-width measurement mode without generating an interrupt when starting up.
- Start trigger/capture trigger: valid edge of TI00/TI01 pin input
- Valid edge of external input signal: select both edges
- Operation clock and counter clock of each channel: select CK00
- Operation clock CK00: select 9.77[kHz]
- Enable the noise filter.

Table 5.1 lists the conditions for counter addition and subtraction.

Table 5.1 Counter Addition/Subtraction Conditions

TI00 (Clock A)	L	↑	H	↓	L	↑	H	↓
TI01 (Clock B)	↑	H	↓	L	↓	L	↑	H
Counter	+1	+1	+1	+1	-1	-1	-1	-1

Figure 5.1 shows an example of the phase difference detection operation.

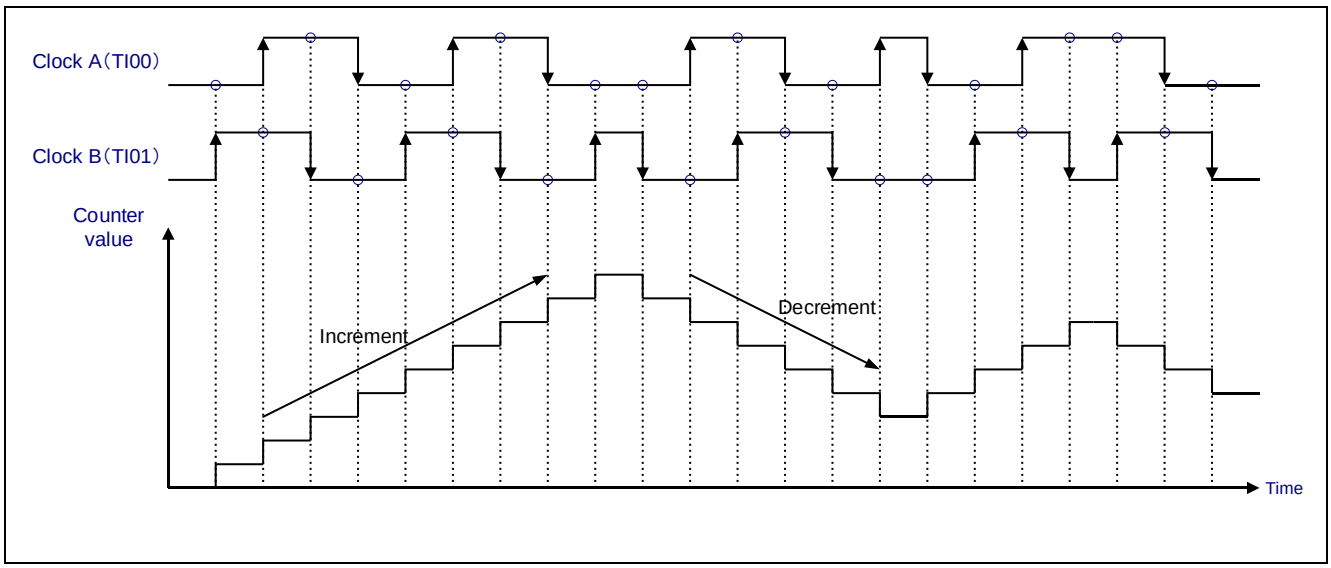

Figure 5.1 Phase Difference Detection Example

5.2 Option Byte Settings

Table 5.2 shows the option byte settings. Set the optimal value for your system as required.

Table 5.2 Option Byte Settings

Address	Setting Value	Description
000C0H	11101110B	Watchdog timer operation stops (counting stopped after reset)
000C1H	11110111B	SPOR detection voltage When power supply falls: TYP. 2.84V (2.70V to 2.96V) When power supply rises: TYP. 2.90V (2.76V to 3.02V) Uses P125 as reset pin.
000C2H	11111001B	High-speed on-chip oscillator clock (HOCO): 20MHz
000C3H	10000101B	Enables on-chip debug operation

5.3 Constants

Table 5.3 lists the constants used in the sample code.

Table 5.3 Constants

Constant Name	Setting Value	Description
RESOLUTION	60*4	Maximum counter value

5.4 Variables

Table 5.4 lists the variables used in the sample code.

Table 5.4 Variables

Variable Name	Description
PROCEADDRA	INTTI00 processing address
PROCEADDRB	INTTI01 processing address
RCOUNT	Counter
PROCTABLE	Processing address table

5.5 Functions (subroutines)

Table 5.5 lists the functions (subroutines) used in the sample code.

Table 5.5 Functions (subroutines)

Function Name	Description
main	TAU operation start processing
IINTTM00	TAU0 channel 0 interrupt processing
IINTTM01	TAU0 channel 1 interrupt processing

5.6 Function (subroutine) Specifications

The following are the specifications of functions (subroutines) used in the sample code.

Function Name: main

Outline	Main processing
Description	Starts channel 0 and 1 operations, and releases TAU0 channel 0 and 1 interrupt masks. Also sets the initial value of the processing addresses executed when INTTM00 and INTTM01 are generated to PROCEADDRA and PROCEADDRB, respectively.
Argument	None
Return Value	None
Notes	None

Function Name: IINTTM00

Outline	TAU0 channel 0 interrupt processing
Description	Executes the process of the processing address set in PROCEADDRA when the INTTM00 interrupt is generated. Also obtains the processing address to be executed when the next interrupt is generated. The address is obtained from PROCTABLE based on Clock A and Clock B signal levels, and is set in PROCEADDRA and PROCEADDRB.
Argument	None
Return Value	None
Notes	None

Function Name: IINTTM01

Outline	TAU0 channel 1 interrupt processing
Description	Executes the process of the processing address set in PROCEADDRB when the INTTM01 interrupt is generated. Also obtains the processing address to be executed when the next interrupt is generated. The address is obtained from PROCTABLE based on Clock A and Clock B signal levels, and is set in PROCEADDRA and PROCEADDRB.
Argument	None
Return Value	None
Notes	None

5.7 Flowcharts

Figure 5.2 shows the entire flow of the sample code described in this application note.

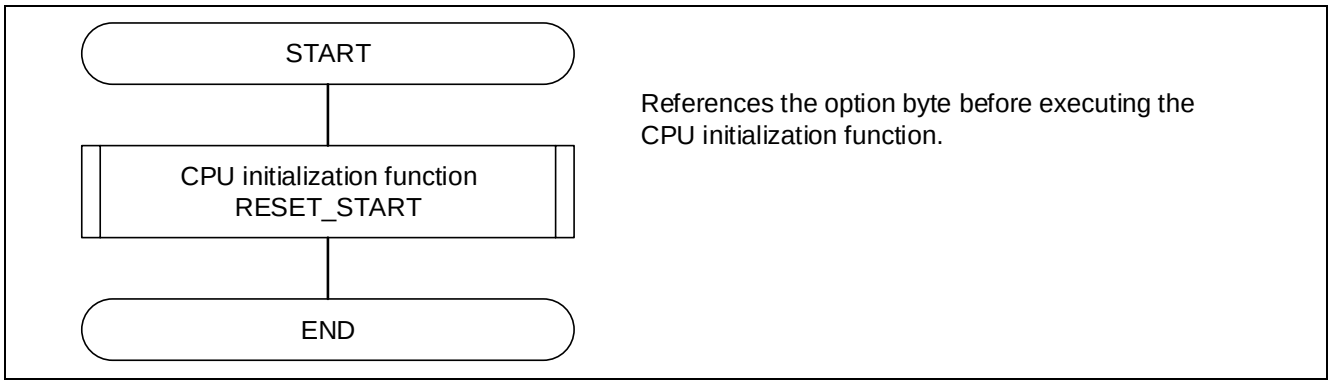

Figure 5.2 Entire Flow

5.7.1 CPU Initialization Function

Figure 5.3 shows the flowchart for the CPU initialization function.

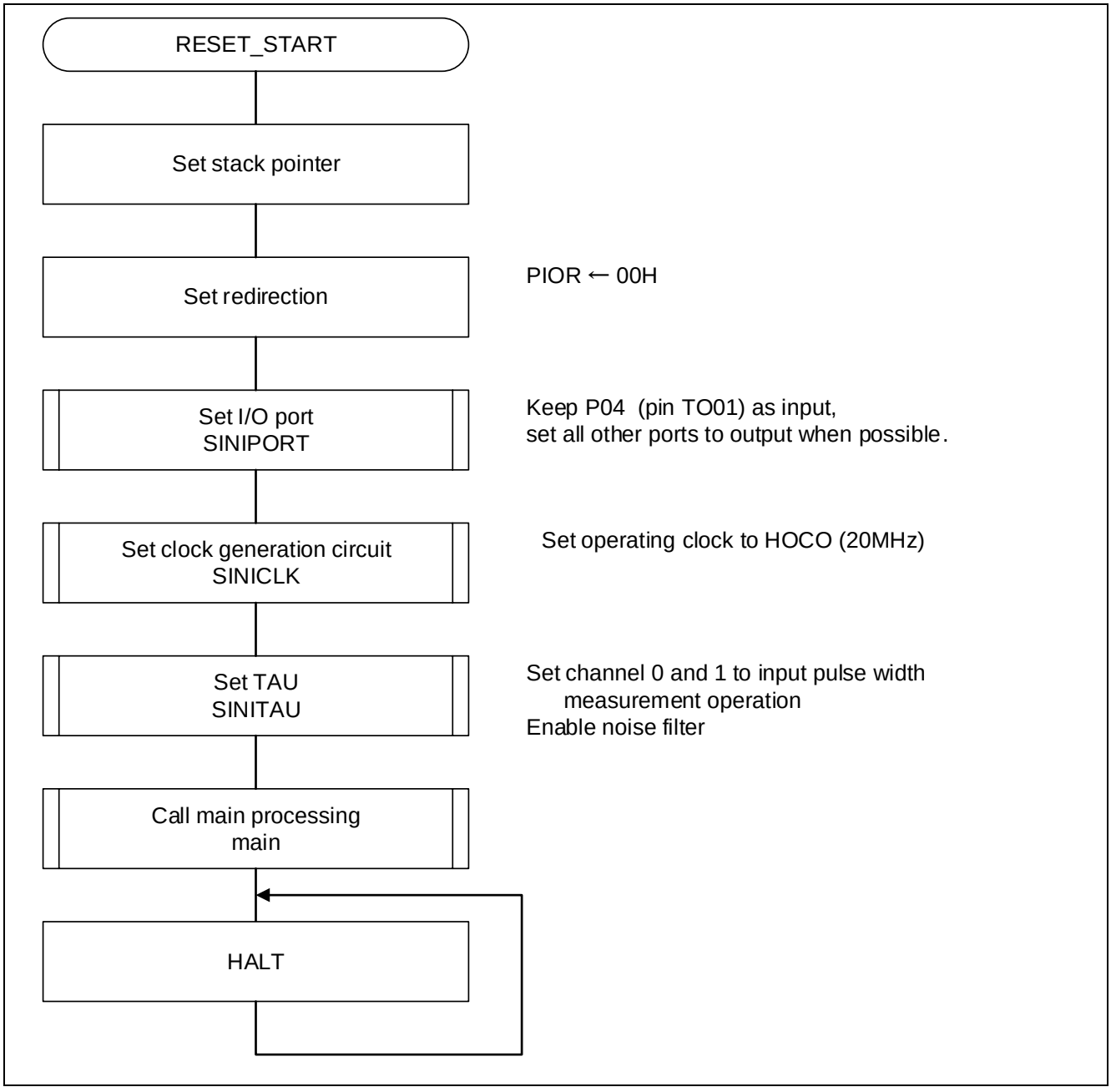

Figure 5.3 CPU Initialization Function

5.7.2 I/O Port Settings

Figure 5.4 shows the flowchart for setting the I/O ports.

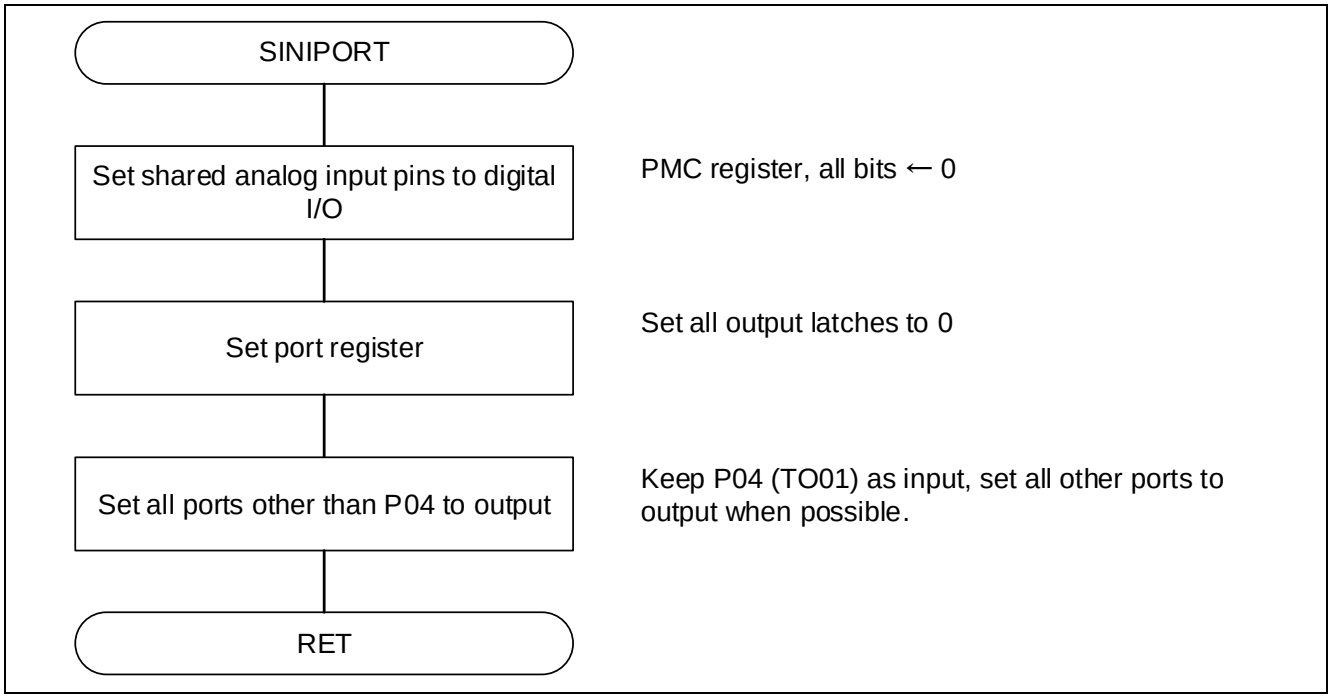

Figure 5.4 I/O Port Settings

Note: When designing circuits, always make sure unused ports are properly processed and all electrical characteristics are met. Also make sure each unused input-only port is connected to V_{DD} or V_{SS} through a resister.

Clock B pin setting

・Port Mode Register (PM0)

Select PM04 input/output.

Symbol: PM0

7	6	5	4	3	2	1	0
1	1	1	PM04	PM03	PM02	PM01	PM00
x	x	x	1	x	x	x	x

Bit 4

PM04	PM04 input/output mode select
0	Output mode (output buffer ON)
1	Input mode (output buffer OFF)

Note: For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

5.7.3 Clock Oscillation Circuit Setting

Figure 5.5 shows the flowchart for setting the clock oscillation circuit.

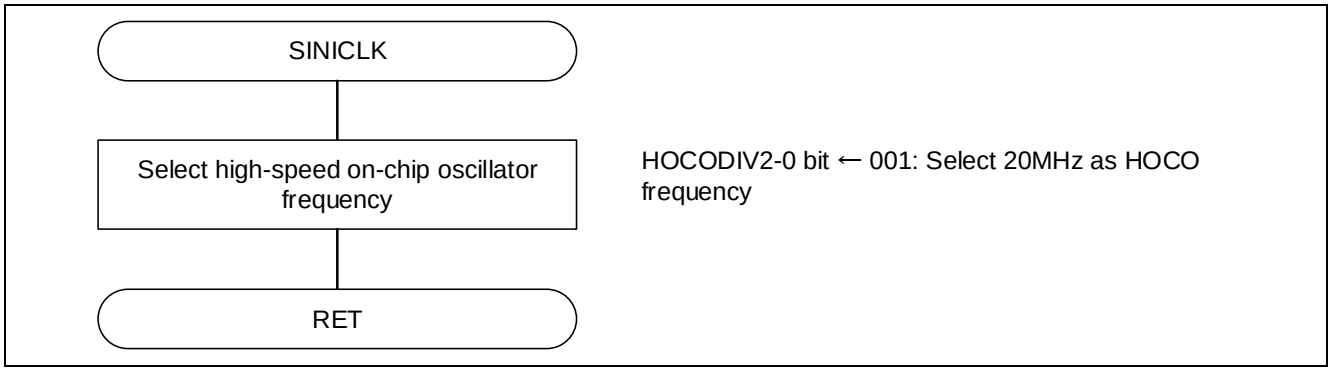

Figure 5.5 Clock Oscillation Circuit Setting

Note: For more details on the CPU clock settings (SINICLK), refer to the “Flowcharts” section in the RL78/G10 Initialization (R01AN1454J) Application Note.

5.7.4 Timer Array Unit Setting

Figure 5.6 shows the flowchart for setting the timer array unit (TAU).

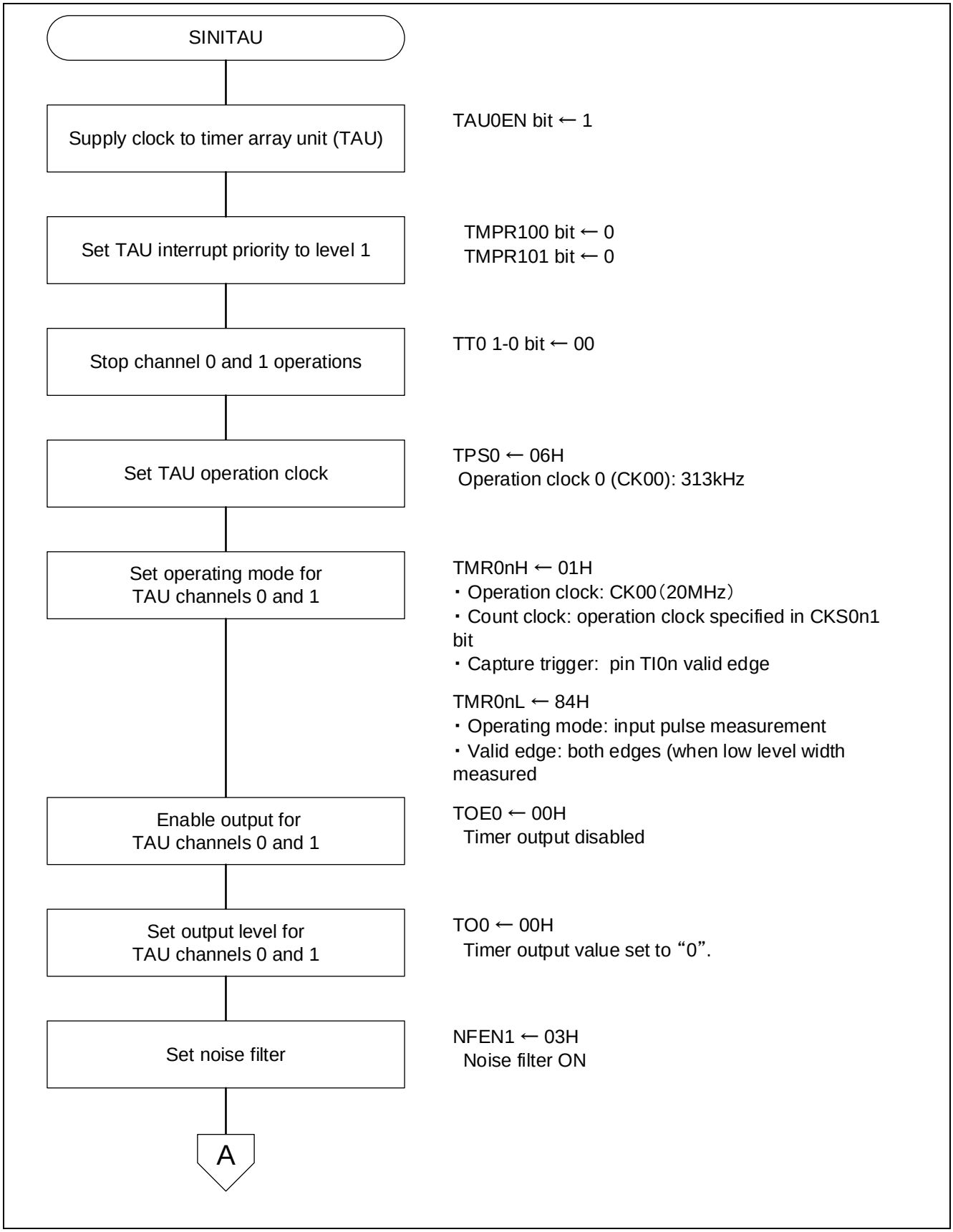

Figure 5.6 Timer Array Unit Setting (1/2)

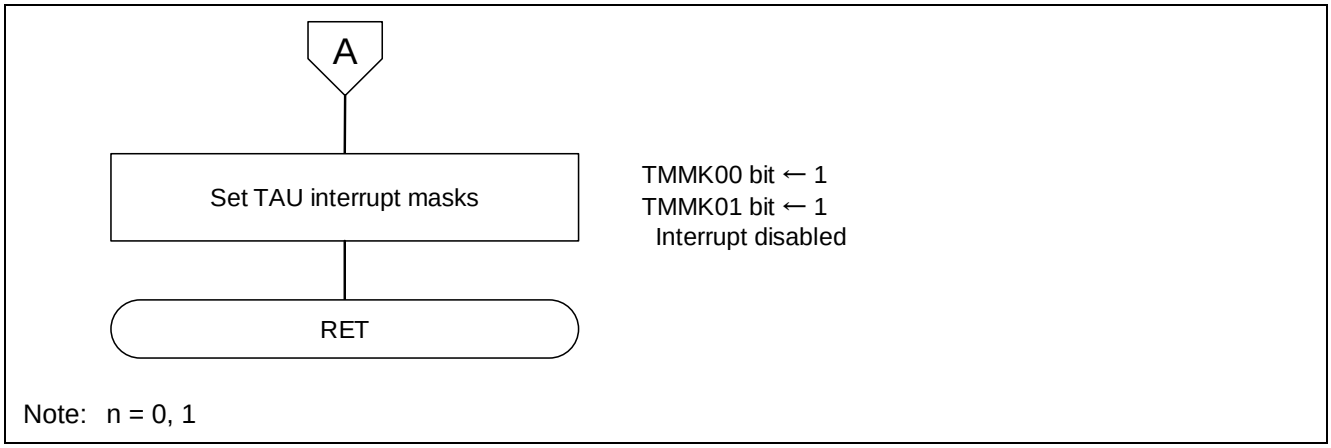

Figure 5.6 Timer Array Unit Setting (2/2)

Enable Timer Array Unit Clock Supply

・Peripheral Enable Register (PER0)

Enable clock supply to timer array unit.

Symbol: PER0

7	6	5	4	3	2	1	0
TMKAEN*	CPMEN*	ADCEN	IICA0EN*	0	SAU0EN	0	TAU0EN
x	x	x	x	0	x	0	1

*Note: 16-pin products only

Bit 0

TAU0EN	Control of timer array unit input clock supply
0	Stops input clock supply
1	Enables input clock supply

Note: For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Timer Array Unit Interrupt Level Settings

・Priority Specification Flag Registers (PR00L, PR10L, PR00H, PR10H)

Set the interrupt levels in the timer array unit.

Symbol: PR00L

7	6	5	4	3	2	1	0
TMPR000	TMPR001H	SREPR00	SRPR00	STPR00 SCIPR000 IICPR000	PPR01	PPR00	WDTIPR0
1	x	x	x	x	x	x	x

Symbol: PR10L

7	6	5	4	3	2	1	0
TMPR100	TMPR101H	SREPR10	SRPR10	STPR10 SCIPR100 IICPR100	PPR11	PPR10	WDTIPR1
0	x	x	x	x	x	x	x

Bit 7

TMPR100	TMPR000	Priority level selection
0	0	Specify level 0 (high priority)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority)

Note: For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Symbol: PR00H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRPR0	ADPR0	TMPR001
x	x	x	x	x	x	x	1

Symbol: PR10H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRPR1	ADPR1	TMPR101
x	x	x	x	x	x	x	0

Bit 0

TMPR101	TMPR001	Priority level selection
0	0	Specify level 0 (high priority)
0	1	Specify level 1
1	0	Specify level 2
1	1	Specify level 3 (low priority)

Note: For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Timer Array Unit Operation Stop Setting

・Timer Channel Stop Register (TT0)

Stops channel operation in timer array unit.

Symbol: TT0

7	6	5	4	3	2	1	0
0	0	0	0	TT03*	TT02*	TT01	TT00
1	x	x	x	x	x	0	0

*Note: 16-pin products only

Bits 0 and 1

TT01, TT00	Operation stop trigger of channel
0	No trigger operation
1	TE0n is cleared to 0, and counting operation is stopped.

Note: For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Timer Clock Frequency Setting

・Timer Clock Select Register 0 (TPS0)

Select timer array unit operation clock.

Symbol: TPS0

7	6	5	4	3	2	1	0
PRS013	PRS012	PRS011	PRS010	PRS003	PRS002	PRS001	PRS000
x	x	x	x	0	1	1	0

PRS 003	PRS 002	PRS 001	PRS 000	Selection of operation clock (CK00)					
					f_{CLK} = 1.25MHz	f_{CLK} = 2.5MHz	f_{CLK} = 5MHz	f_{CLK} = 10MHz	f_{CLK} = 20MHz
0	0	0	0	f_{CLK}	1.25MHz	2.5MHz	5MHz	10MHz	20MHz
0	0	0	1	$f_{CLK}/2$	625kHz	1.25MHz	2.5MHz	5MHz	10MHz
0	0	1	0	$f_{CLK}/2^2$	313kHz	625kHz	1.25MHz	2.5MHz	5MHz
0	0	1	1	$f_{CLK}/2^3$	156kHz	313kHz	625kHz	1.25MHz	2.5MHz
0	1	0	0	$f_{CLK}/2^4$	78.1kHz	156kHz	313kHz	625kHz	1.25MHz
0	1	0	1	$f_{CLK}/2^5$	39.1kHz	78.1kHz	156kHz	313kHz	625kHz
0	1	1	0	$f_{CLK}/2^6$	19.5kHz	39.1kHz	78.1kHz	156kHz	313kHz
0	1	1	1	$f_{CLK}/2^7$	9.77kHz	19.5kHz	39.1kHz	78.1kHz	156kHz
1	0	0	0	$f_{CLK}/2^8$	4.88kHz	9.77kHz	19.5kHz	39.1kHz	78.1kHz
1	0	0	1	$f_{CLK}/2^9$	2.44kHz	4.88kHz	9.77kHz	19.5kHz	39.1kHz
1	0	1	0	$f_{CLK}/2^{10}$	1.22kHz	2.44kHz	4.88kHz	9.77kHz	19.5kHz
1	0	1	1	$f_{CLK}/2^{11}$	610Hz	1.22kHz	2.44kHz	4.88kHz	9.77kHz
1	1	0	0	$f_{CLK}/2^{12}$	305Hz	610Hz	1.22kHz	2.44kHz	4.88kHz
1	1	0	1	$f_{CLK}/2^{13}$	153Hz	305Hz	610Hz	1.22kHz	2.44kHz
1	1	1	0	$f_{CLK}/2^{14}$	76.3Hz	153Hz	305Hz	610Hz	1.22kHz
1	1	1	1	$f_{CLK}/2^{15}$	38.1Hz	76.3Hz	153Hz	305Hz	610Hz

Note: For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Channel 0, 1 Operating Mode Settings

・Timer Mode Registers 00, 01 (TMR00H, TMR00L, TMR01H, TMR01L)

Select operation clock (f_{MCK}).

Select count clock (f_{TCLK}).

Set start trigger and capture trigger.

Select timer input valid edge.

Set operating mode.

Symbol: TMR0nH

7	6	5	4	3	2	1	0
CKS0n1	0	0	CCS0n	SPLIT01*	STS0n2	STS0n1	STS0n0
0	0	0	0	0	0	0	1

*Note: TMR01H only

Bit 7

CKS0n1	Selection of operation clock (f_{MCK}) of channel n
0	Operation clock CK00 set by timer clock select register 0 (TPS0)
1	Operation clock CK01 set by timer clock select register 0 (TPS0)

Bit 4

CCS0n	Selection of count clock (f_{TCLK}) of channel n
0	Operation clock (f_{MCK}) specified by CKS0n1 bit
1	Valid edge of input signal from TI0n pin

Bit 3

SPLIT01*	Selection of channel 1 8-bit /16-bit timer operation
0	Operates as 16-bit timer
1	Operates as 8-bit timer

*Note: TMR01H only

Bits 2-0

STS0n2	STS0n1	STS0n0	Setting of channel n start trigger/capture trigger
0	0	0	Only software trigger start valid (other trigger sources are invalid)
0	0	1	Use T10n pin input valid edge as start trigger/capture trigger.
0	1	0	Use both edges of T10n pin input as triggers, one each for start trigger/capture.
1	0	0	For one-shot pulse output, PWM output function, and multiple PWM output function slave channel: use master channel interrupt request signal (INTTM0n) as start trigger.
1	1	0	For two-channel input one-shot pulse output slave channel: use master channel interrupt request signal (INTTM0n) as start trigger. Use the slave channel's TI0 pin valid edge as end trigger.
Other than the above			Do not set

Note: 1. n = 0, 1
2. For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Symbol: TMR0nL

7	6	5	4	3	2	1	0
CIS0n1	CIS0n0	0	0	MD0n3	MD0n2	MD0n1	MD0n0
1	0	0	0	0	1	0	0

Bits 7 and 6

CIS0n1	CIS0n0	Selection of TI0n pin input valid edge
0	0	Falling edge
0	1	Rising edge
1	0	Both edges (when low-level width is measured) Start trigger: falling edge; capture trigger: rising edge
1	1	Both edges (when high level-width is measured) Start trigger: rising edge; capture trigger: falling edge

Bits 3-0

MD 0n3	MD 0n2	MD 0n1	MD 0n0	Setting of operation mode of channel n	Corresponding function	Count operation of TCR
0	0	0	1/0	Interval timer mode	Interval timer/square wave output/divider function/ PWM output (master)	Down count
0	1	0	1/0	Capture mode	Input pulse width measurement/ two-channel input one-shot pulse output (slave)	Up count
0	1	1	0	Event counter mode	External event counter	Down count
1	0	0	1/0	One-count mode	Delay counter/one-shot pulse output/tow-channel input one-shot pulse output (master)/PWM output (slave)	Down count
1	1	0	0	Capture & one-count mode	Measurement of high-/low-level width input signal	Up count
Other than the above				Setting prohibited		

The MD0n0 bit operations vary according to the operating mode, as show in the following table.

Operating Mode (set in MD0n3-MD0n1)	MD0n0	Setting of starting counting and interrupt
・Interval timer mode (0, 0, 0) ・Capture mode (0, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either)
	1	Timer interrupt is generated when counting is started (timer output also changes)
・Event counter mode (0, 1, 1)	0	Timer interrupt is not generated when counting is started (timer output does not change, either)
・One-count mode (1, 0, 0)	0	Start trigger is invalid during counting operation. At that time, a timer interrupt is not generated.
	1	Start trigger is valid during counting operation. At that time, a timer interrupt is not generated.
・Capture & one-count mode (1, 1, 0)	0	Timer interrupt is not generated when counting is started (timer output does not change, either) Start trigger is invalid during counting operation. At that time, a timer interrupt is not generated.
Other than the above		Setting prohibited

Note: 1. n = 0, 1
2. For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Timer Output Enable Setting

・Timer Output Enable Register 0 (TOE0)

Enable timer output.

Symbol: TOE0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TOE01	TOE00
0	0	0	0	0	0	0	0

Bits 1 and 0

TOE0n	Channel n timer output enable/disable
0	Timer output disabled Timer operation is not reflected in the TO0n bit, output is fixed. Write operation to bit TO0n bit is enabled, the level set in TO0n bit is output from the TO0n pin.
1	Timer output enabled Timer operation is reflected in TO0n bit, output waveform is generated. Write operation to TO0n bit is ignored.

Note: 1. n = 0, 1
2. For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Timer Output Pin Output Setting

・Timer Output Register 0 (TO0)

Set timer output.

Symbol: TO0

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TO01	TO00
0	0	0	0	0	0	0	0

Bits 1 and 0

TO0n	Channel n timer output
0	Timer output value is "0"
1	Timer output value is "1"

Note: 1. n = 0, 1
2. For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

Noise Filter Setting

・Noise Filter Enable Register 1 (NFEN1)

Turn noise filter ON/OFF.

Symbol: NFEN1

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TNFEN01	TNFEN00
0	0	0	0	0	0	1	1

Bits 1 and 0

TNFEN0n	Turn noise filter ON/OFF for TI0n pin input signal
0	Noise filter OFF
1	Noise filter ON

Note: 1. n = 0, 1
2. For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

TAU Interrupt Mask Setting

・MK0L, MK0H） Interrupt Mask Flag Registers (MK0L, MK0H)

Set interrupt masks.

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
1	x	x	x	x	x	x	x

Bit 7

TMMK00	Interrupt processing control
0	Interrupt processing enabled
1	Interrupt processing disabled

Symbol: MK0H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRMK	ADMK	TMMK01
1	1	1	1	1	x	x	1

Bit 0

TMMK01	Interrupt processing control
0	Interrupt processing enabled
1	Interrupt processing disabled

Note: For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

5.7.5 Main Processing

Figure 5.7 shows the flowchart for main processing.

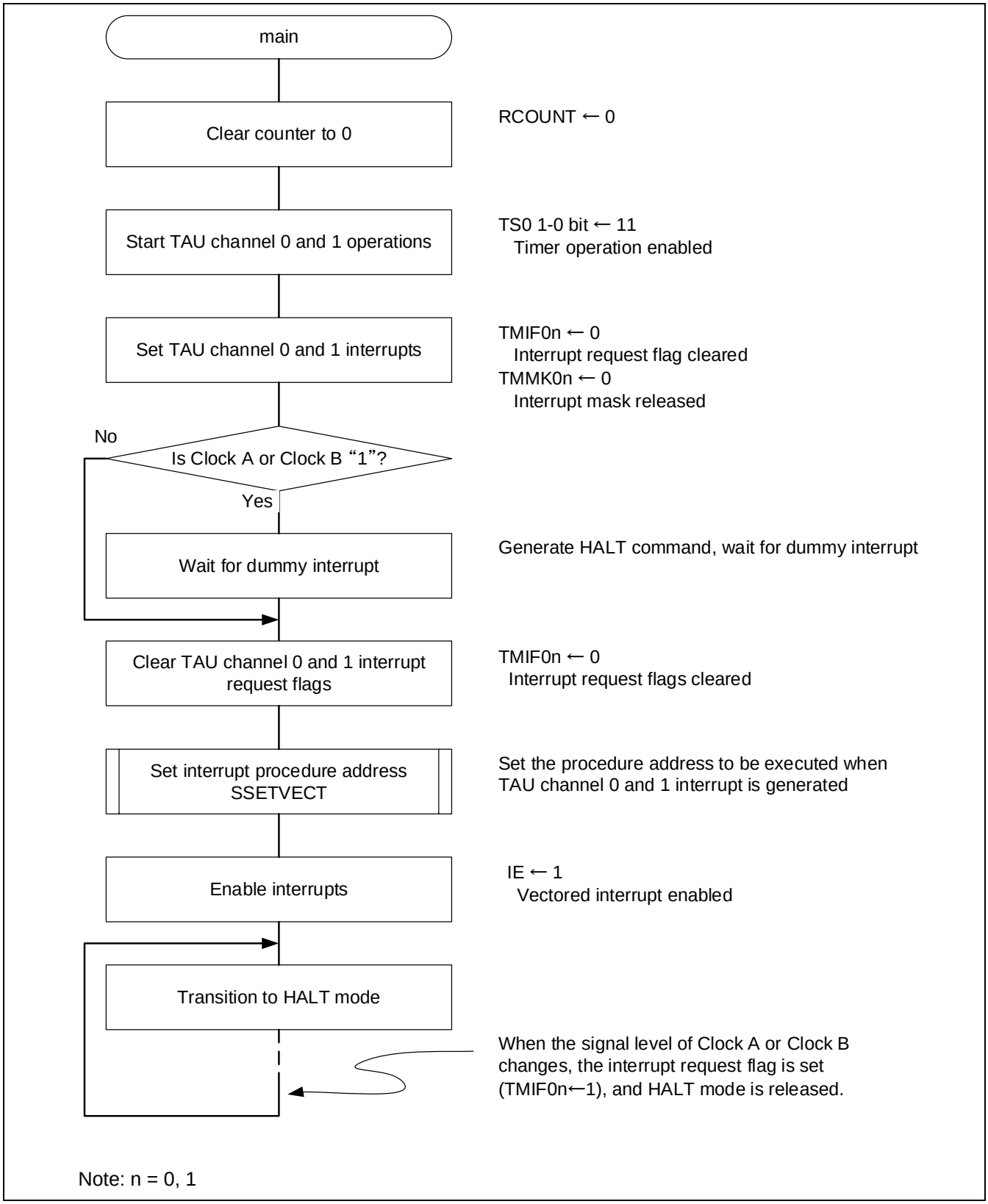

Figure 5.7 Main Processing

Timer Array Unit Operation Enable

・Timer Channel Start Register 0 (TS0)

Enable channel operation for timer array unit.

Symbol: TS0

7	6	5	4	3	2	1	0
0	0	0	0	TS03*	TS02*	TS01	TS00
1	x	x	x	x	x	1	1

*Note: 16-pin product only

Bits 0 and 1

TS01, TS00	Channel operation enable (start) trigger
0	No trigger operation
1	TE0n bit is et to 1, and the count operation becomes enabled.

Note: For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

TAU Interrupt Request Clear Flag

・Interrupt Request Flag Register (IF0L, IF0H)

Clear interrupt request flag.

Symbol: IF0L

7	6	5	4	3	2	1	0
TMIF00	TMIF01H	SREIF0	SRIF0	STIF0 CSIIF00 IICIF00	PIF1	PIF0	WDTIIF
0	x	x	x	x	x	x	x

Bit 7

TMIF00	Interrupt Request Flag
0	Interrupt request signal is not generated
1	Interrupt request signal is generated, goes to interrupt request state

Symbol: IF0H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRIF	ADIF	TMIF01
1	1	1	1	1	x	x	0

Bit 0

TMIF01	Interrupt Processing Control
0	Interrupt request signal is not generated
1	Interrupt request signal is generated, interrupt request status

Note: For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

TAU Interrupt Mask Setting

・Interrupt Mask Flag Registers (MK0L, MK0H)

Set interrupt masks.

Symbol: MK0L

7	6	5	4	3	2	1	0
TMMK00	TMMK01H	SREMK0	SRMK0	STMK0 CSIMK00 IICMK00	PMK1	PMK0	WDTIMK
0	x	x	x	x	x	x	x

Bit 7

TMMK00	Interrupt processing control
0	Interrupt processing enabled.
1	Interrupt processing disabled

Symbol: MK0H

7	6	5	4	3	2	1	0
1	1	1	1	1	KRMK	ADMK	TMMK01
1	1	1	1	1	x	x	0

Bit 0

TMMK01	Interrupt processing control
0	Interrupt processing enabled
1	Interrupt processing disabled

Note: For more details on register settings, refer to the RL78/G10 User's Manual Hardware Version.

5.7.6 Interrupt Processing Address Settings

Figure 5.8 shows the flowchart for setting the interrupt processing addresses.

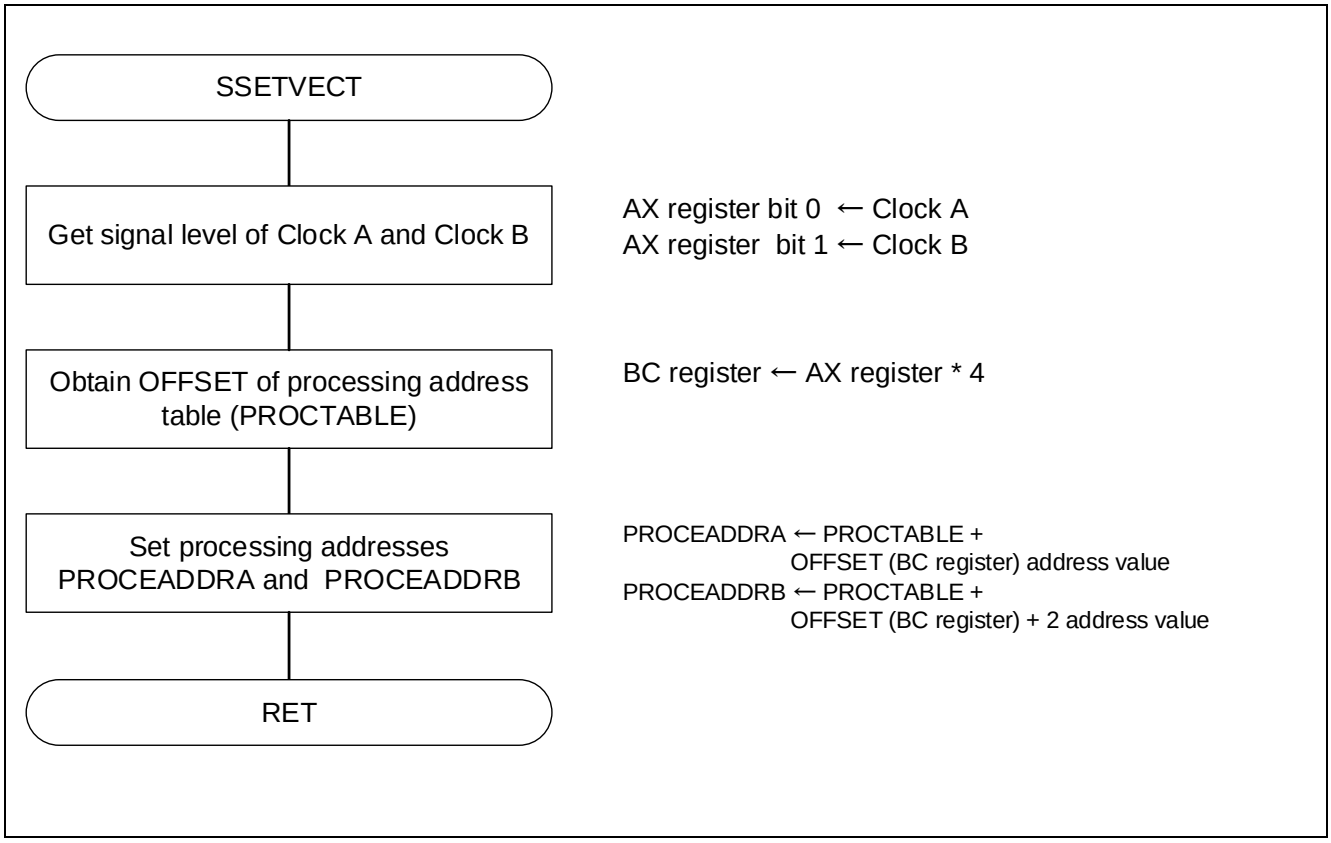

Figure 5.8 Interrupt Processing Address Setting

Processing addresses are set according to the processing address table (PROCTABLE), as shown in Figure 5.6.

Table 5.6 Processing Address Table (PROCTABLE)

OFFSET	Processing Address	Interrupt Processing Execution Conditions
+0	COUNTDOWN	Rising edge of Clock A when Clock A and B are both 0
+2	COUNTUP	Rising edge of Clock B when Clock A and B are both 0
+4	COUNTUP	Falling edge of Clock A when Clock A is 1 and Clock B is 0
+6	COUNTDOWN	Rising edge of Clock B when Clock A is 1 and Clock B is 0
+8	COUNTUP	Rising edge of Clock A when Clock A is 0 and Clock B is 1
+10	COUNTDOWN	Falling edge of Clock B when Clock A is 0 and Clock B is 1
+12	COUNTDOWN	Falling edge of Clock A when Clocks A and B are both 1.
+14	COUNTUP	Falling edge of Clock B when Clocks A and B are both 1.

5.7.7 INTTM00 Interrupt Processing

Figure 5.9 shows the flowchart for INTTM00 interrupt processing.

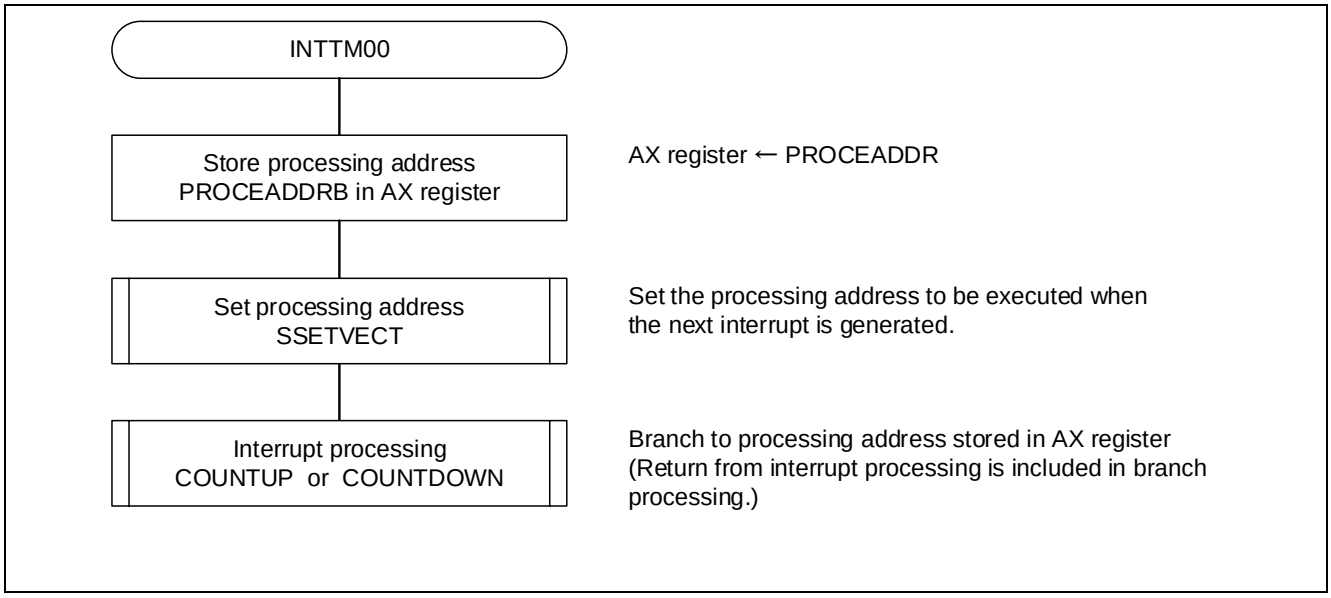

Figure 5.9 INTTM00 Interrupt Processing

5.7.8 INTTM01 Interrupt Processing

Figure 5.10 shows the flowchart for INTTM01 interrupt processing.

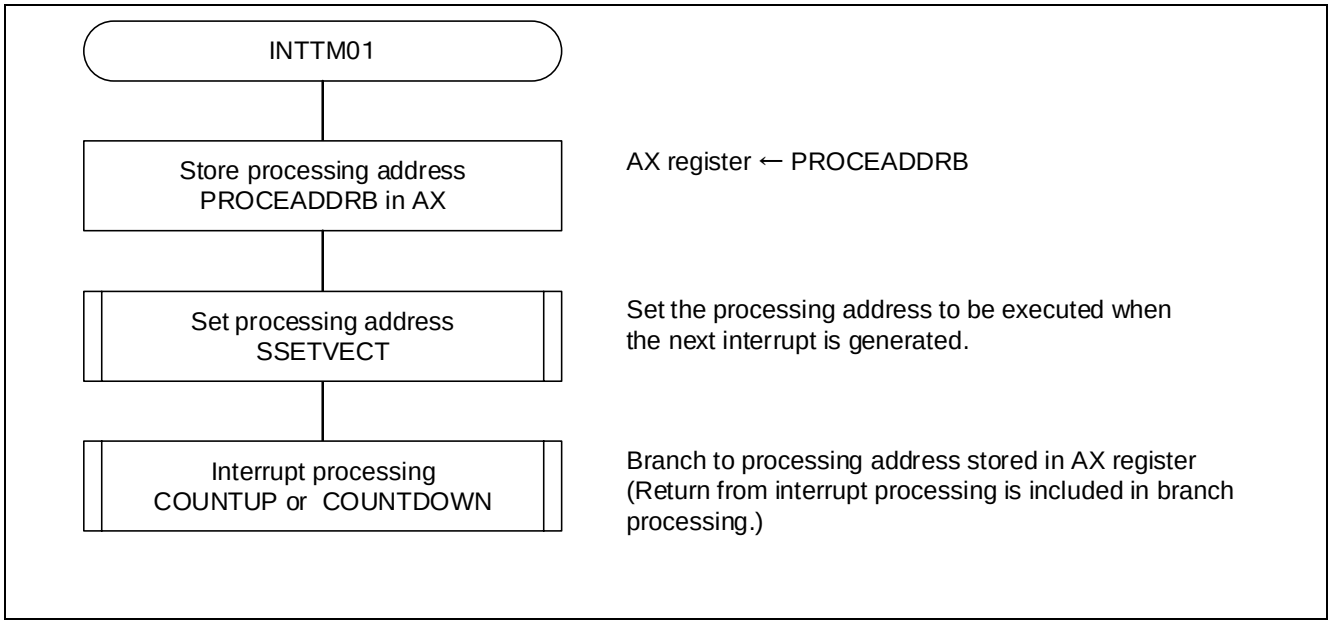

Figure 5.10 INTTM01 Interrupt Processing

5.7.9 Interrupt Processing (count-up)

Figure 5.11 shows the flowchart of count-up interrupt processing.

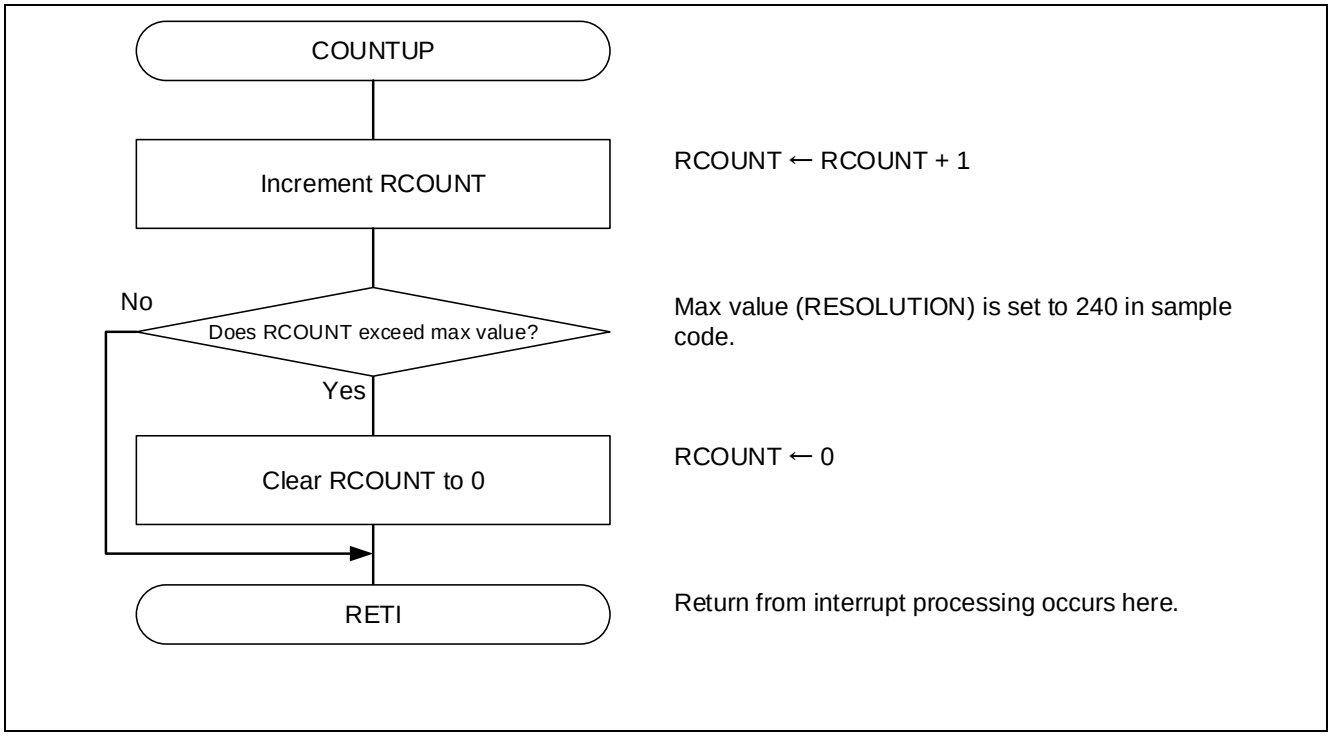

Figure 5.11 Interrupt Processing (count-up)

5.7.10 Interrupt Processing (count-down)

Figure 5.12 shows the flowchart of count-down interrupt processing.

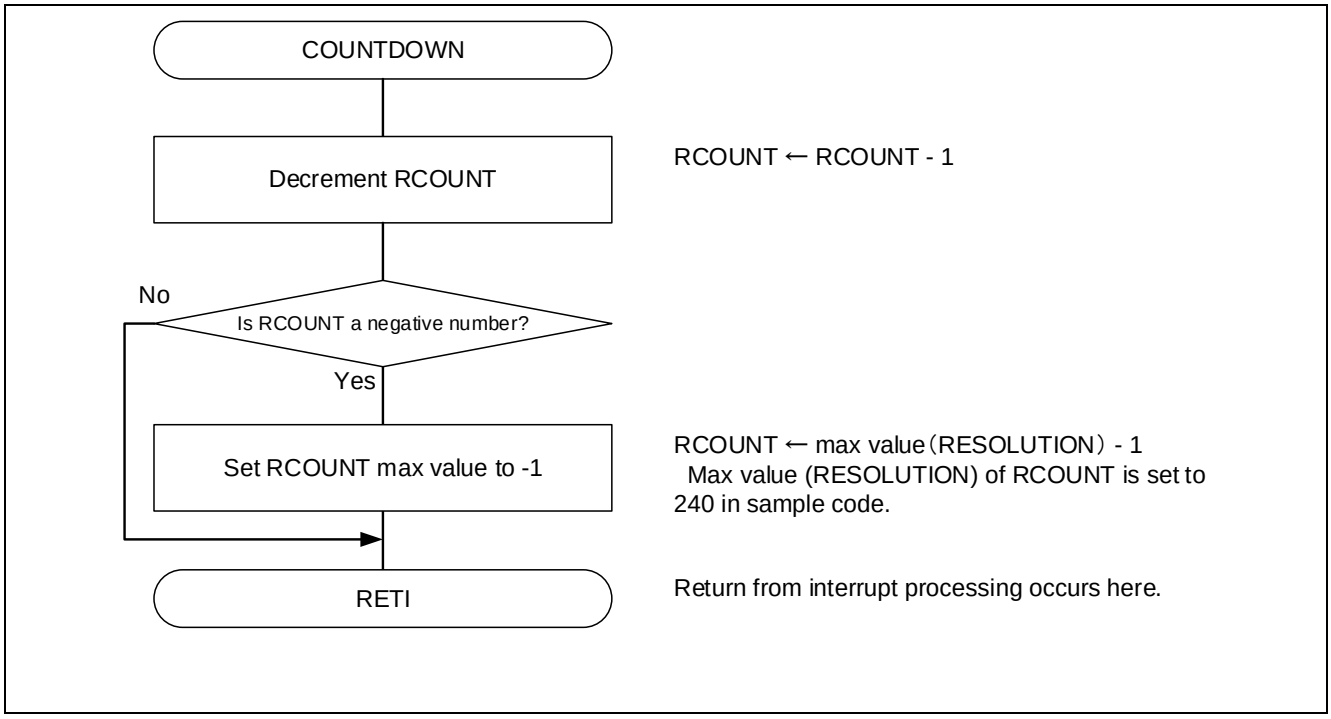

Figure 5.12 Interrupt Processing (count-down)

6. Sample Code

The sample code is available on the Renesas Electronics Website.

7. Documents for Reference

RL78/G10 User's Manual: Hardware Rev.3.00 (R01UH0384E)

RL78 Family User's Manual: Software Rev.2.20 (R01US0015E)

(The latest versions of the documents are available on the Renesas Electronics Website.)

Technical Updates/Technical Brochures

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Revision Record	RL78/G10 Two-Phase Encoding Software Control

Rev.	Date	Description	
		Page	Summary
1.00	Mar. 11. 2016	—	First edition issued

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

- Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
  - The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

- The state of the product is undefined at the moment when power is supplied.
  - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
    In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
    In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

- Access to reserved addresses is prohibited.
  - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

- After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
  - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

- Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
  - The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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