RL78/F13, F14, F15
Option Byte Setting

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Introduction

This application note describes the setting of Option Byte (User Option Byte, and On-chip Debug Option Byte) and issues to be considered when setting them for RL78/F13, F14, F15 products. For details, be sure to refer to User's Manual: Hardware

Contents

1. Option Byte for RL78/F13, F14, F15

For RL78/F13, F14, F15 Option Byte area is located on the address 000C0H to 000C3H of the flash memory. Option Byte contains of User Option Byte (000C0H to 000C2H) and On-chip Debug Option Byte (000C3H). Device automatically refers to the value of Option Byte wrote in advance at power on reset released and controls the corresponding function.

When using boot swap function, set boot cluster 0 (000C0H to 000C3H) and boot cluster 1 (020C0H to 020C3H) to the same value in order to switch boot cluster 0 (00000H to 01FFFH) and boot cluster 1 (02000H to 03FFFH).

1.1 User Option Byte (000C0H)

User Option Byte (000C0H) controls the operation of watch-dog timer. Bits of User Option Byte (000C0H) are shown in Figure 1, and the notes on setting are shown in Table 1.

b7	b6	b5	b4	b3	b2	b1	b0
WDTINT	WINDOW[1:0]		WDTON	WDCS[2:0]			WDSTBYON

Bit Symbol	Function
WDTINT	0: Interval interrupt of watchdog timer is not used 1: Interval interrupt of watchdog timer is generated when 75% ± 1/2 f_{WDT} of the overflow time is reached
WINDOW[1:0]	01B: Watchdog timer window open period: 50% 10B: Watchdog timer window open period: 75% **Note 2** 11B: Watchdog timer window open period: 100% 00B: Setting prohibited
WDTON	0: Counter operation disabled (counting stopped after reset) 1: Counter operation enabled (counting stated after reset)
WDCS[2:0]	Watchdog timer overflow time (Count source: f_{WDT} **Note 1**) 000B: $2^6/f_{WDT}$, 001B: $2^7/f_{WDT}$, 010B: $2^8/f_{WDT}$, 011B: $2^9/f_{WDT}$, 100B: $2^{11}/f_{WDT}$, 101B: $2^{13}/f_{WDT}$, 110B: $2^{14}/f_{WDT}$, 111B: $2^{16}/f_{WDT}$
WDSTBYON	0: Counter operation stopped in HALT / STOP / SNOOZE mode 1: Counter operation enabled in HALT / STOP / SNOOZE mode

Notes: 1. Oscillator characteristics of f_{WDT} (WDT dedicated lo-speed on-chip oscillator clock frequency) is (TYP.) 15 kHz. To clear the watchdog timer counter, perform within the range of the oscillator characteristics of f_{WDT}.
2. Incorrect RESET signal may occur when WDT counter is cleared (within ACH to WDTE register) at the timing when the counter value becomes exactly 50% and when window open period of watchdog timer is set to 75%. Refer to technical update “TN-RL*-A068A/E”.

Figure 1. User Option Byte (000C0H)

Table 1. Notes of User Option Byte (000C0H) Setting

Bit Symbol	Note of Setting
WDSTBYON	•If this bit is set to 0, the window open period will be 100% regardless of the setting of WINDOW[1:0] bits.
WDCS[2:0]	•Clear the counter within the window open period. (set by WINDOW [1:0] bits)
WDTON	•The invalid memory access detection function is always enabled when this bit is 1, regardless of the setting of the IAWEN bit of IAWCTL register. When not using the watchdog timer, clear this bit to 0.
WINDOW[1:0]	•Be sure to set any of 01B, 10B, and 11B •When setting 10B (window open period: 75%), clear the counter at a timing other than 50%. •If “WDSTBYON = 0” is set, the window open period will be 100% regardless of the setting of these bits.
WDTINT	•Set this bit to 1 when use interval interrupt of watchdog timer and judging the interrupt request by the WDTIIF flag of IF0L register.

Caution: Set the same value as 000C0H to 020C0H when the boot swap operation is used.

1.2 User Option Byte (000C1H)

In the User Option Byte (000C1H), set the operation mode of the voltage detector and the operation of the clock monitor function. Bits of User Option Byte (000C1H) are shown in Figure 2, and the notes on setting are shown in Table 4.

b7	b6	b5	b4	b3	b2	b1	b0
VPOC[2:0]			CLKMB	LVIS[1:0]		LVIMDS[1:0]	

Bit Symbol	Function
VPOC[2:0]	Depend on operation mode of voltage detector. Refer to Table 2 and Table 3.
CLKMB	0: Clock monitor operation is enabled 1: Clock monitor operation is stopped
LVIS[1:0]	Depend on operation mode of voltage detector. Refer to Table 2 and Table 3.
LVIMDS[1:0]	Set the operation mode of voltage detector 01B: Interrupt mode 10B: Interrupt & reset mode 11B: Reset mode 00B: Setting prohibited

Figure 2. User Option Byte (000C1H)

Table 2. Setting of VPOC[2:0] bits and LVIS[1:0] bits when Interrupt mode Note 1 and Reser mode

VPOC[2:0]	LVIS[1:0]	Function
000B	01B	Select the V_{LVD4}. Grade-L product: Rise: 3.02 V (2.95 V to 3.09 V), Fall: 2.96 V (2.89 V to 3.02 V) Grade-K product: Rise: 3.02 V (2.95 V to 3.17 V), Fall: 2.96 V (2.89 V to 3.09 V) Grade-Y product: Rise: 3.02 V (2.95 V to 3.44 V), Fall: 2.96 V (2.89 V to 3.23 V)
001B	00B	Select the V_{LVD2}. Grade-L product: Rise: 4.42 V (4.30 V to 4.51 V), Fall: 4.32 V (4.21 V to 4.41 V) Grade-K product: Rise: 4.42 V (4.30 V to 4.61 V), Fall: 4.32 V (4.21 V to 4.51 V) Grade-Y product: Rise: 4.42 V (4.30 V to 4.87 V), Fall: 4.32 V (4.21 V to 4.76 V)
010B	00B	Select the V_{LVD1}. Grade-L product: Rise: 4.62 V (4.50 V to 4.72 V), Fall: 4.52 V (4.40 V to 4.62 V) Grade-K product: Rise: 4.62 V (4.50 V to 4.82 V), Fall: 4.52 V (4.40 V to 4.71 V) Grade-Y product: Rise: 4.62 V (4.50 V to 5.09 V), Fall: 4.52 V (4.40 V to 4.98 V)
011B	00B	Select the V_{LVD0}. Grade-L product: Rise: 4.74 V (4.62 V to 4.84 V), Fall: 4.64 V (4.52 V to 4.74 V) Grade-K product: Rise: 4.74 V (4.62 V to 4.94 V), Fall: 4.64 V (4.52 V to 4.84 V) Grade-Y product: Rise: 4.74 V (4.62 V to 5.22 V), Fall: 4.64 V (4.52 V to 5.11 V)
	01B	Select the V_{LVD3}. Grade-L product: Rise: 3.22 V (3.13 V to 3.29 V), Fall: 3.15 V (3.07 V to 3.22 V) Grade-K product: Rise: 3.22 V (3.13 V to 3.39 V), Fall: 3.15 V (3.07 V to 3.31 V) Grade-Y product: Rise: 3.22 V (3.13 V to 3.66 V), Fall: 3.15 V (3.07 V to 3.47 V)
	11B	Select the V_{LVD5}. Note 2 Grade-L product: Rise: 2.81 V (2.74 V to 2.87 V), Fall: 2.75 V (2.68 V to 2.81 V) Grade-K product: Rise: 2.81 V (2.74 V to 2.95 V), Fall: 2.75 V (2.68 V to 2.88 V) Grade-Y product: Rise: 2.81 V (2.74 V to 3.22 V), Fall: 2.75 V (2.68 V to 3.00 V)
100B to 111B	-	Voltage detector not used (stopped)
Other than above		Setting prohibited

Notes are shown on the next page.

Notes: 1. If interrupt mode is used (LVIMDS [1:0] = 01B), the reset voltage (at falling voltage) is V_{PDR} (TYP. 1.55 V). In this case the V_{PDR} will be out of the specified operation voltage for this product. After the occurrence of an interrupt (INTLVI), disable other interrupt factors as long as the power supply voltage is within the valid operation range (*) and shift to STOP mode, or generate an internal reset by user software (execution of illegal instruction, reset of watchdog timer function). When supply voltage exceeds selected V_{LVD}, STOP mode or reset state is released.
(*). Use operating conditions (V_{DD} (supply voltage): 2.7 V to 5.5 V, f_{CLK} (CPU / Peripheral hardware clock frequency): 15 kHz to 32 MHz) in grade-L products. Or use operating conditions (V_{DD}: 2.7 V to 5.5 V, f_{CLK}: 15 kHz to 24 MHz) in grade-K products. Or use operating conditions (V_{DD}: 2.7 V to 5.5 V, f_{CLK}: 15 kHz to 24 MHz) in grade-Y products.
2. In this condition, reset mode can be set, but interrupt mode is prohibited.

Remark: Only RL78/F13, F14 product supports grade-Y condition.

Table 3. Setting of VPOC[2:0] bits and LVIS[1:0] bits when Interrupt and Reser mode

VPOC[2:0]	LVIS[1:0]	Function
001B	00B	Select the V_{LVD2}. Grade-L product: Reset: 2.75 V (2.68 V to 2.81 V), Reset release: 4.42 V (4.30 V to 4.51 V) Interrupt (V_{LVDH}: 4.42 V (4.30 V to 4.51 V), V_{LVDL}: 4.32 V (4.21 V to 4.41 V)) Grade-K product: Reset: 2.75 V (2.68 V to 2.88 V), Reset release: 4.42 V (4.30 V to 4.61 V) Interrupt (V_{LVDH}: 4.42 V (4.30 V to 4.61 V), V_{LVDL}: 4.32 V (4.21 V to 4.51 V)) Grade-Y product: Reset: 2.75 V (2.68 V to 3.00 V), Reset release: 4.42 V (4.30 V to 4.87 V) Interrupt (V_{LVDH}: 4.42 V (4.30 V to 4.87 V), V_{LVDL}: 4.32 V (4.21 V to 4.76 V))
010B	00B	Select the V_{LVD1}. Grade-L product: Reset: 2.75 V (2.68 V to 2.81 V), Reset release: 4.62 V (4.50 V to 4.72 V) Interrupt (V_{LVDH}: 4.62 V (4.50 V to 4.72 V), V_{LVDL}: 4.52 V (4.40 V to 4.62 V)) Grade-K product: Reset: 2.75 V (2.68 V to 2.88 V), Reset release: 4.62 V (4.50 V to 4.82 V) Interrupt (V_{LVDH}: 4.62 V (4.50 V to 4.82 V), V_{LVDL}: 4.52 V (4.40 V to 4.71 V)) Grade-Y product: Reset: 2.75 V (2.68 V to 3.00 V), Reset release: 4.62 V (4.50 V to 5.09 V) Interrupt (V_{LVDH}: 4.62 V (4.50 V to 5.09 V), V_{LVDL}: 4.52 V (4.40 V to 4.98 V))
011B	00B	Select the V_{LVD0}. Grade-L product: Reset: 2.75 V (2.68 V to 2.81 V), Reset release: 4.74 V (4.62 V to 4.84 V) Interrupt (V_{LVDH}: 4.74 V (4.62 V to 4.84 V), V_{LVDL}: 4.64 V (4.52 V to 4.74 V)) Grade-K product: Reset: 2.75 V (2.68 V to 2.88 V), Reset release: 4.74 V (4.62 V to 4.94 V) Interrupt (V_{LVDH}: 4.74 V (4.62 V to 4.94 V), V_{LVDL}: 4.64 V (4.52 V to 4.84 V)) Grade-Y product: Reset: 2.75 V (2.68 V to 3.00 V), Reset release: 4.74 V (4.62 V to 5.22 V) Interrupt (V_{LVDH}: 4.74 V (4.62 V to 5.22 V), V_{LVDL}: 4.64 V (4.52 V to 5.11 V))
	01B	Select the V_{LVD3}. Grade-L product: Reset: 2.75 V (2.68 V to 2.81 V), Reset release: 3.22 V (3.13 V to 3.29 V) Interrupt (V_{LVDH}: 3.22 V (3.13 V to 3.29 V), V_{LVDL}: 3.15 V (3.07 V to 3.22 V)) Grade-K product: Reset: 2.75 V (2.68 V to 2.88 V), Reset release: 3.22 V (3.13 V to 3.39 V) Interrupt (V_{LVDH}: 3.22 V (3.13 V to 3.39 V), V_{LVDL}: 3.15 V (3.07 V to 3.31 V)) Grade-Y product: Reset: 2.75 V (2.68 V to 3.00 V), Reset release: 3.22 V (3.13 V to 3.66 V) Interrupt (V_{LVDH}: 3.22 V (3.13 V to 3.66 V), V_{LVDL}: 3.15 V (3.07 V to 3.47 V))
Other than above		Setting prohibited

Remark: Only RL78/F13, F14 product supports grade-Y condition.

Table 4. Notes of User Option Byte (000C1H) Setting

Bit Symbol	Note of Setting
LVIMDS[1:0]	•Do not set 00B to these bits. •When setting these bits to 01B (Interrupt mode), do not select V_{LVD5}.
LVIS[1:0]	•When the voltage detector is not used, set these bits to 01B or 11B. Use the Interrupt mode or Reset mode: refer to Table 2 Use the Interrupt & Reset mode: refer to Table 3
CLKMB	•To use the clock monitor function, set this bit to 0.
VPOC[2:0]	•When the voltage detector is not used, set these bits to 1xxB (x: can be set arbitrarily). •When the voltage detector is used, not set values other than 000B, 001B, 010B, 011B for these bits.

Caution: Set the same value as 000C1H to 020C1H when the boot swap operation is used.

1.3 User Option Byte (000C2H)

User Option Byte (000C2H) sets the frequency of high-speed on-chip oscillator, and P130/RESOUT pin operation mode. Bits of User Option Byte (000C2H) are shown in Figure 3, and the notes on setting are shown in Table 5.

b7	b6	b5	b4	b3	b2	b1	b0
1	1	RESOUTB	FRQSEL[4:0]				

Bit Symbol	Function
reserved (b7, b6)	Be sure to set these bits to 11B. Setting of other values is prohibited.
RESOUTB	0: Selects P130 as the RESOUT pin 1: Selects P130 as a general port pin (output only)
FRQSEL [4:0]	Set the frequency of high-speed on-chip oscillator 00000B: 24 MHz, 00001B: 12 MHz, 01000B: 32 MHz, 01001B: 16 MHz, 01010B: 8 MHz, 01011B: 4 MHz, 01101B: 1 MHz, 10000B: 48 MHz, 11000B: 64 MHz Other than above: Setting prohibited

Figure 3. User Option Byte (000C2H)

Table 5. Notes of User Option Byte (000C2H) Setting

Bit Symbol	Note of Setting
FRQSEL[4:0]	•Be sure to set one of 00000B, 00001B, 01000B, 01001B, 01010B, 01011B, 01101B, 10000B, 11000B. When using grade-K products in condition (T_A: -40 to 125 °C) or grade-Y products in condition (T_A: -40 to 150 °C), be sure not to set 01000B (32 MHz) or 11000B (64 MHz). Device operation cannot be guaranteed, if any other value is set.
RESOUTB	•P130/RESOUT pin is not available for 32-pin product, 30-pin product and 20-pin product of RL78/F13, F14. When using these products, it is recommended that this bit be set to the initial value (“1”). •P130 pin outputs low-level during reset regardless of the setting of this bit. •When this bit is set to 0, P130/RESOUT pin automatically outputs High-level after reset release. Regardless of port latch (P130 bit), high-level is output until it is reset.
b6	•Be sure to set this bit to 1. Device operation cannot be guaranteed if 0 is set.
b7	•Be sure to set this bit to 1. Device operation cannot be guaranteed if 0 is set.

Caution: Set the same value as 000C2H to 020C2H when the boot swap operation is used.

Remark: Only RL78/F13, F14 product supports grade-Y condition.

1.4 On-chip Debug Option Byte (000C3H)

On-chip Debug Option Byte (000C3H) sets the operation when debugger is connected. Bits of On-chip Debug Option Byte (000C3H) are shown in Figure 4, and the notes on setting are shown in Table 7.

b7	b6	b5	b4	b3	b2	b1	b0
OCDENSET	0	0	0	0	1	HPIEN	OCDERSD

Bit Symbol	Function
OCDENSET	Together with the OCDERSD bit, it controls the operation when on-chip debugger is connected. Refer to Table 6 for detail.
reserved (b6 to b2)	Be sure to set these bits to 00001B. Setting of other values is strictly prohibited.
HPIEN	Controls the operation of hot plug-in function. Refer to Table 6 for detail.
OCDERSD	Together with the OCDENSET bit, it controls the operation when on-chip debugger is connected. Refer to Table 6 for detail.

Figure 4. On-chip Debug Option Byte (000C3H)

Table 6. Setting of OCDENSET, HPIEN, OCDERSD bits

OCDENSET	HPIEN	OCDERSD	Function
0	0	0	Disables on-chip debug operation Note 1
1	0	0	Enables on-chip debugging and disables hot plug-in operation. Erases data of flash memory in case of failures in authenticating on-chip debug security ID. Notes 2, 3
1	0	1	Enables on-chip debugging and disables hot plug-in operation. Does not erase data of flash memory in case of failures in authenticating on-chip debug security ID. Notes 2, 3
1	1	1	Enables on-chip debugging and hot plug-in operation. Does not erase data of flash memory in case of failures in authenticating on-chip debug security ID. Notes 2, 3
Other than above			Setting prohibited

Notes: 1. When using the flash programmer, Erase / Program of flash memory can be performed.
2. The security ID is the 10-byte ID located at 000C4H to 000CDH.
3. Both areas code flash and data flash are targeted.

Table 7. Notes of On-chip Debug Option Byte (000C3H) Setting

Bit Symbol	Note of Setting
OCDERSD	•Do not set 1 to this bit when OCDENSET bit is 0.
HPIEN Note	•When the HPIEN bit is set to 1, the f_{IL} (low-speed on-chip oscillator) operates and cannot be stopped by the user program. The f_{IL} can be stopped by register setting only in standby mode. For details, refer to User's Manual: Hardware.
b6 to b2 Note	•Be sure to set these bits to 00001B. Setting of other values is strictly prohibited.
OCDENSET	•Do not clear 0 to this bit when OCDERSD bit is set to 1.

Note: When on-chip debug function is used, the values of bits 3 to 2 and HPIEN bit will be written over and thus it will become unstable after the setting. Be sure to write 01B when writing to bits 3 to 2.

Caution: Set the same value as 000C3H to 020C3H when the boot swap operation is used. When using on-chip debugging and hot plug-in functions, some internal RAM area cannot be used depending on the product. Refer to User's Manual: Hardware.

2. Setting Range of Option Byte for RL78/F13, F14, F15

The value to be set to Option Bytes of RL78/F13, F14, F15 depends on the products to be used. The setting range of Option Bytes are shown in the Table 8.

Table 8. Setting Range of Option Byte

Option Bytes		Grade-L Products	Grade-K and Grade-Y Products
		V_{DD} = 2.7 V to 5.5 V, f_{CLK} = 15 kHz to 32 MHz, T_A = -40 °C to 105 °C	V_{DD} = 2.7 V to 5.5 V, f_{CLK} = 15 kHz to 24 MHz, T_A = -40 °C to 125 °C (Grade-K products) T_A = -40 °C to 150 °C (Grade-Y products)
000C0H	WDSTBYON	0 or 1	Same as the grade-L product
	WDCS [2:0]	000B to 111B	Same as the grade-L product
	WDTON	0 or 1	Same as the grade-L product
	WINDOW [1:0]	01B or 10B or 11B (00B setting prohibited)	Same as the grade-L product
	WDTINT	0 or 1	Same as the grade-L product
000C1H	LVIMDS [1:0]	01B or 10B or 11B (00B setting prohibited)	Same as the grade-L product
	LVIS [1:0]	・LVIMDS=01B, VPOC=000B: 01B ・LVIMDS=01B, VPOC=001B: 00B ・LVIMDS=01B, VPOC=010B: 00B ・LVIMDS=01B, VPOC=011B: 00B or 01B ・LVIMDS=10B, VPOC=001B: 00B ・LVIMDS=10B, VPOC=010B: 00B ・LVIMDS=10B, VPOC=011B: 00B or 01B ・LVIMDS=11B, VPOC=000B: 01B ・LVIMDS=11B, VPOC=001B: 00B ・LVIMDS=11B, VPOC=010B: 00B ・LVIMDS=11B, VPOC=011B: 00B, 01B or 11B (Other than the above: Setting prohibited)	Same as the grade-L product
	CLKMB	0 or 1	Same as the grade-L product
	VPOC [2:0]	・LVIMDS=01B: 000B, 001B, 010B, 011B or 1xxB ・LVIMDS=10B: 001B, 010B or 011B ・LVIMDS=11B: 000B, 001B, 010B, 011B or 1xxB (Other than the above: Setting prohibited)	Same as the grade-L product
000C2H	FRQSEL [4:0]	00000B, 00001B, 01000B, 01001B, 01010B, 01011B, 01101B, 10000B or 11000B (Other than the above: Setting prohibited)	00000B, 00001B, 01001B, 01010B, 01011B, 01101B or 10000B (Other than the above: Setting prohibited)
	RESOUTB	0 or 1	Same as the grade-L product
	bit7, bit6	11B (Setting prohibited except 11B)	Same as the grade-L product
000C3H	OCDERSD	[OCDENSET, HPIEN, OCDERSD] = 000B, 100B, 101B or 111B (Other than the above: Setting prohibited)	Same as the grade-L product
	HPIEN		
	OCDENSET		
	bit6 to bit2	00001B (Setting prohibited except 00001B)	

Caution: Set the same values as option byte of Boot cluster 0 (000C0H to 000C3H) to Boot cluster 1 (020C0H to 020C3H) when the boot swap operation is used.

Remark: Only RL78/F13, F14 product supports grade-Y condition.

3. References

Documents referenced in this application note are shown below. When referring to these documents, make sure to obtain the latest version of each document from Renesas Electronics website.

- RL78/ F13, F14 User's Manual: Hardware Rev. 2.10
- RL78/ F15 User's Manual: Hardware Rev. 1.00

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar.31, 20	-	First edition issued
1.01	Sep.30, 21	2	Correction of WDTINT in Table 1. Correct: WDTIIF flag of IF0L register
		3	Correction of description when V_{LVD0} is selected for Grade-Y product in Table 2. Fall: 4.64 V (4.52 V to ~~5.10~~ 5.11 V)
		7	Added note to HPIEN bit in Table 7. The explanation of the notes at the bottom of the Table 7 has been changed.
		9	Added “References” page.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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