# RC22504A and RC32504A: Using FemtoClock 2 for High Bandwidth Jitter Attenuation

## 1. Introduction

The RC32504A has a digital PLL (DPLL) for jitter attenuation with very low bandwidths, below 1Hz. The analog PLL (APLL) alone also can attenuate jitter but at higher bandwidths, like 500KHz. Every synthesizer essentially provides a jitter attenuation because of the loop bandwidth of its PLL. While the RC22504A synthesizer is not called out as a jitter attenuator, it will effectively attenuate jitter with relatively high loop bandwidth between 500KHz and 1MHz (compared to the RC32504).

The differential clock input can be programmed to drive the DPLL or the APLL. When operating as a high bandwidth jitter attenuator, the differential clock input will drive the APLL.

The advantage of “high bandwidth” jitter attenuation is that it does not need a crystal. This makes it an easier, smaller, and less expensive solution. The differential clock input on both the RC22504A and RC32504A is very flexible. Logic types including LVDS, HCSL, and LVCMOS can connect directly to the clock input without the need for external components. When AC coupling into the clock input, almost any signal type will work. The clock input has programmable features like termination and DC bias.

## 2. When is “High Bandwidth” Jitter Attenuation the Best Solution?

Clock generators with a lot of outputs at a variety of different frequencies often suffer from crosstalk between the outputs. Crosstalk between outputs at different frequencies causes spurious modes in the phase noise of these outputs, affecting the phase jitter of the outputs. Often these spurious modes are above 1MHz offsets; this is when “high bandwidth” jitter attenuation is most useful.

An example of a clock generator with a multitude of outputs is Renesas’ ClockMatrix product family. When the crosstalk between outputs is managed with “high bandwidth” jitter attenuation, the phase jitter in ClockMatrix outputs can be as low as 100fs. Most applications require a variety of different frequencies which can induce spurs resulting in phase jitter as high as 150 to 200fs. Inserting an RC22504A into a clock path with 150 to 200fs of phase jitter caused by > 1MHz spurs can improve the phase jitter often to below 100fs.

“High bandwidth” jitter attenuation is effective when the phase jitter of a clock would have been acceptable if it was not for spurious modes or other noise at greater than 1MHz offsets from the carrier.

# 3. Measurement Results with ClockMatrix

The following measurements show the results when using an RC22504A filters a clock output on ClockMatrix.

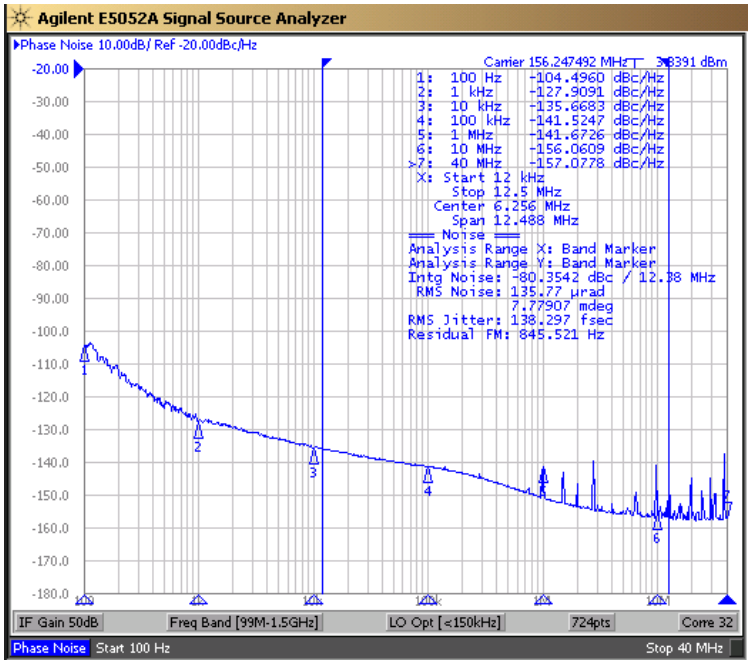


**Figure 1. Phase Noise of a 156.25MHz Clock from ClockMatrix**

There are a number of spurs above 1MHz offset. Also note the noise floor level at 40MHz offset.

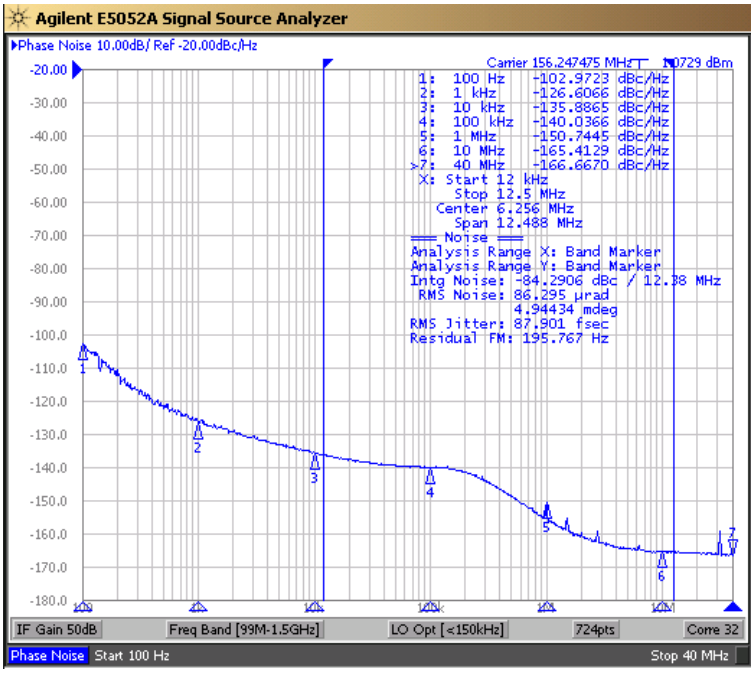


**Figure 2. Phase Noise of a 156.25MHz Clock after "Hi BW" Jitter Attenuation with an RC22504A**

Phase jitter improves from 138fs to 88fs when using an RC22504A to attenuate > 1MHz spurs. Another significant contributor to the phase jitter improvement is the lowering of the noise floor at 40MHz with 10dB.

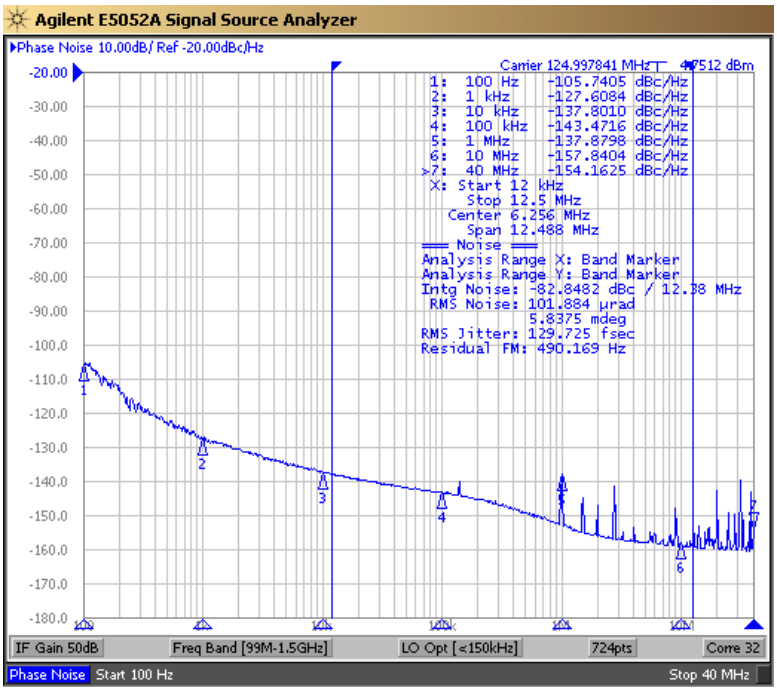


**Figure 3. Phase Noise of a 125MHz Clock from ClockMatrix**

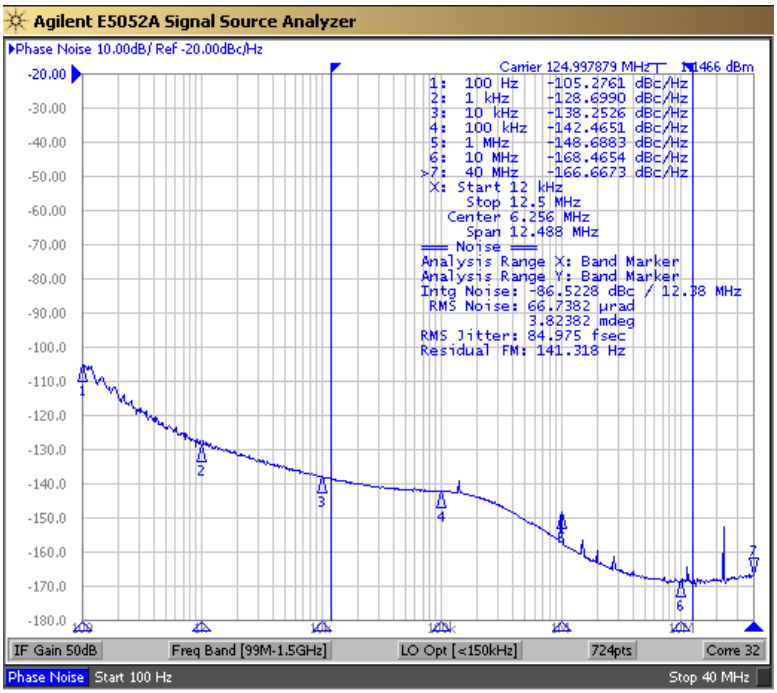


**Figure 4. Phase Noise of a 125MHz Clock after "Hi BW" Jitter Attenuation with an RC22504A**

In this case, the phase jitter improves from 130fs at the ClockMatrix output to 85fs after jitter attenuation with an RC22504A.

# 4. Additional Information

ClockMatrix has an output driver configuration called “user defined” that is the best suited for driving the RC22504A differential input, and therefore, eliminating the need for external components.

The RC22504A shows the best performance with differential input clocks in the range 100MHz to 200MHz. When, for example, a 312.5MHz or 625MHz clock is needed, it is recommended to use a 156.25MHz clock at the RC22504A input. The RC22504A is a synthesizer that can translate frequencies.

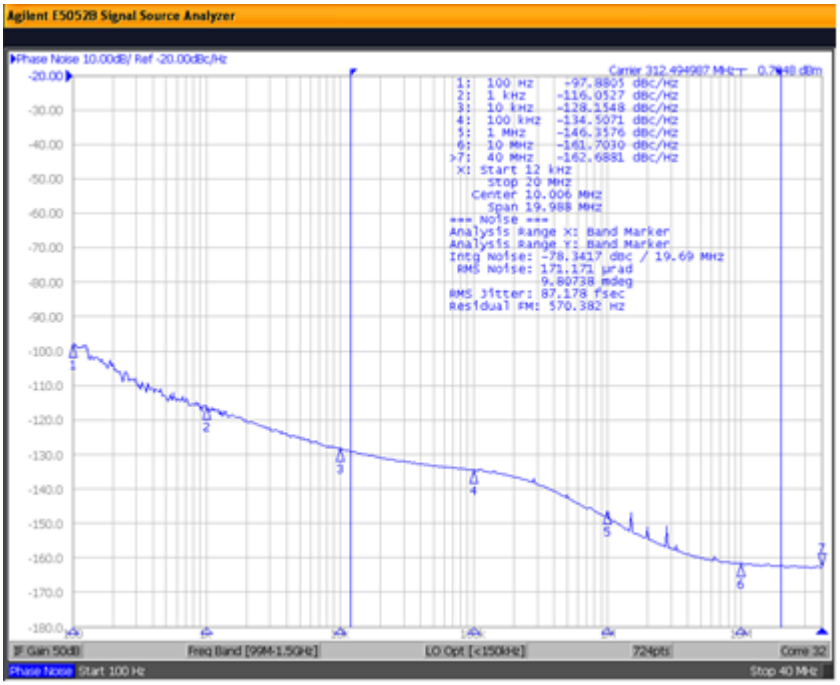


**Figure 5. Phase Noise of a 312.5MHz Clock after “Hi BW” Jitter Attenuation with an RC22504A of the 156.25MHz Clock in Figure 1**

The RC22504A APLL loop properties can be adjusted to the type of spurs that need to be filtered. When strong spurs are present at relatively low offsets (e.g., 1MHz and lower), it helps to configure the loop bandwidth of the APLL as low as possible. The overall performance of the APLL is optimized at high loop bandwidths. When the dominant spurs are at higher offsets (e.g., 5MHz and higher, it helps to configure the loop bandwidth of the APLL higher.

# 5. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | Mar 7, 2021 | Initial release. |

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